Dithering Concepts for Spur-Free Nonlinear DTC-Based Frequency Synthesizers

Christoph Preissl, *Graduate Student Member, IEEE*, Peter Preyler, *Student Member, IEEE*, Andreas Springer, *Member, IEEE*, and Mario Huemer, *Senior Member, IEEE*

***Abstract*— Digital-to-time converters (DTCs) are a promising technology for radio frequency (RF) transceivers but are prone to spur generation. A common approach to change the spurious emissions to a spur-free shape is a method called dithering. The power added due to dithering is an important aspect of this approach and gives raise to investigations on additive dither as well as methods for subtractive dithering. This work presents a mathematical model for dithering DTC-based local oscillator (LO) generators. It proposes concepts for the application of subtractive dither and it introduces a novel generalization of quantization-dither to allow for optimal dithering of nonlinear quantizers.**

***Index Terms*— Digital-to-phase converter (DPC), digital-to-time converter (DTC), spurs, local oscillator (LO), frequency synthesizer, phase shifters, dithering.**

I. Introduction

THE ever-increasing demand for higher data rates is met by mobile communication standards with more complex data transmission for each generation. Since several years, mobile devices must be able to concurrently communicate over numerous channels either for multiple radio access technologies (RATs) or due to Carrier Aggregation (CA), e.g. in the Long Term Evolution (LTE) standard [1]. The frequencies that are used range from several 100 MHz up to sub-6 GHz and include tens of GHz, if millimeter waves (mmWave) are supported, like in 5G New Radio (NR) [2]. The support of this wide frequency range needs the operation of several transceivers in parallel which is an important challenge for area and power requirements as well as demands the handling of interferences with each other. A crucial part in each RF transceiver is the generation of various required LO frequencies with sufficient spectral purity. These different LOs are typically generated by individual phase-locked loops (PLLs) which operate concurrently and - ideally - independent of each other. Normally, every PLL contains one or more oscillators which, due to the spectral purity requirements, are implemented with inductors and capacitors. Besides that, such a multiple PLL solution requires significant area, it is also prone to electromagnetic coupling between the individual blocks. An interesting alternative to PLLs is the frequency generation with phase shifters. Such phase shifters need to be able to operate in the GHz frequency range. Several works describe the construction of circuits capable of doing so, and their spectral effects [3]–[6]. These systems are using a digital input that describes a phase offset or time delay relative to a reference signal.

This work will use the term digital-to-time converter (DTC) to refer to all different phase shifter implementations. All published DTCs only allow for a finite set of delays of the input reference clock and thus, if an arbitrary frequency is to be generated, will produce periodic errors that are visible as spurs in the output spectrum. Spurs are also a problem in the current PLL-based systems, and their cancellation is the focus of ongoing research [7]–[10]. Any additional spurs which are introduced by a DTC need to be characterized. Investigations for a DTC based on delay elements have been published in [11], [12]. The results show that the resolution and linearity are major requirements for a DTC with respect to spurs. DTCs are also used to relax the requirements of a time-to-digital converter (TDC) in a PLL [13], and efforts for a predistortion to improve linearity have been published [14]. These DTCs operate synchronous to the reference clock of the PLL. Another delay-line based DTC has been used to propose an outphasing transmitter concept [15]. The effect of a DTC which is capable of generating an output in the GHz range on generating spurs in the output power spectral density (PSD) is shown in [16]. Circuit implementations of the DTCs discussed there are presented in [17] and [18]. The recent design in [18] operates with a higher frequency digital controlled oscillator (DCO) in the 8 GHz range and generates an output frequency in the range of 0.7 to 2.2 GHz which makes this DTC effectively a fractional divider. A very similar circuit has been used in recent work directly as a fractional-N frequency divider [19]. Many investigations and

Manuscript received November 19, 2020; revised February 1, 2021; accepted February 16, 2021. Date of publication March 4, 2021; date of current version April 27, 2021. The financial support by the Austrian Federal Ministry for Digital and Economic Affairs, the National Foundation for Research, Technology and Development and the Christian Doppler Research Association is gratefully acknowledged. This article was recommended by Associate Editor G. Jovanovic Dolecek. *(Christoph Preissl and Peter Preyler contributed equally to this work.) (Corresponding author: Christoph Preissl.)*

Christoph Preissl and Mario Huemer are with the Christian Doppler Laboratory for Digitally Assisted RF Transceivers for Future Mobile Communications, Johannes Kepler University Linz, 4040 Linz, Austria, and also with the Institute of Signal Processing, Johannes Kepler University Linz, 4040 Linz, Austria (e-mail: christoph.preissl@jku.at).

Peter Preyler and Andreas Springer are with the Christian Doppler Laboratory for Digitally Assisted RF Transceivers for Future Mobile Communications, Johannes Kepler University Linz, 4040 Linz, Austria, and also with the Institute for Communications Engineering and RF-Systems, Johannes Kepler University Linz, 4040 Linz, Austria.

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TCSI.2021.3060907.

Digital Object Identifier 10.1109/TCSI.2021.3060907

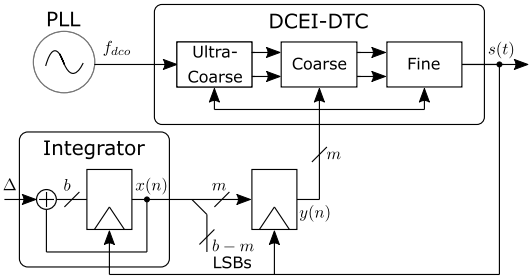

Fig. 1. Two quantization domains in a DTC-based frequency synthesizer. The integrator, having b bits, generates the required code ramp $x(n)$. The input to the DTC $y(n)$, having $m < b$ bits, results by discarding $b-m$ LSBs from $x(n)$.

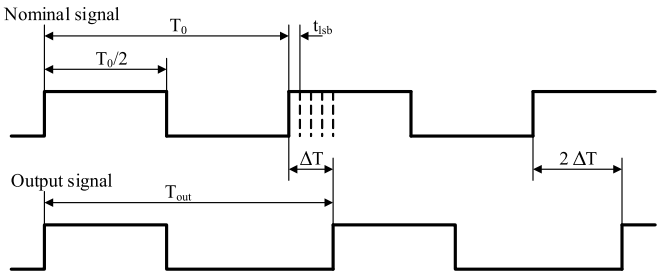

Fig. 2. Time domain signal of the DTC output signal. Rising edges can only be placed at certain time instances depending on the resolution t_{LSB}. Falling edges occur $T_0/2$ afterwards.

dithering methods discussed in this work are also applicable in that scenario. In [20], [21] dithering concepts are presented to counter the effects of the deterministic jitter due to low resolution and nonlinearities.

Dithering of quantization effects is a known solution which transforms the PSD from distinct tones or spurs into a white-like shape. Since additive dither is part of the PSD a focus of interest is in the minimum required amount of dither and the possibility to shape its PSD. Subtractive dither is an attractive method as the dither is removed from the output signal. Such a method has already been applied in [22] for a DTC in the feedback path of a PLL. The dither here is subtracted in the digital domain after sampling with a TDC. If the DTC is used to generate an LO signal, this option is not available and different ideas of subtractive dither need to be investigated. In this work we will build on the state-of-the-art and contribute the following:

- A mathematical description for dithering in DTCs.
- Generalization of additive dithering for nonlinear systems.
- Proposal of self-contained subtractive dithering variants in transceivers.
- A simplified subtractive dither method for the specific nonlinearity of phase-interpolator DTCs.

This paper begins by explaining the basic principle of a DTC-based frequency synthesizer and its problem with arising spurs in Section II. Then, the work establishes a mathematical description for the PSD when dither is applied to a DTC in Section III. The results are used to explain the known method for dithering quantization spurs, and general requirements are derived, leading to new investigations on dithering DTCs. First, a discussion on the application of subtractive dither is placed in Section IV which considers the requirements of RF transceivers to establish different methods of implementation. Then, the concept of dithering uniform quantization is taken and generalized in Section V, so that it applies to non-uniform quantization. Finally, a comparison with respect to key performance parameters in RF transceivers is discussed in Section VI, and conclusions are drawn in Section VII.

II. DTC-Based Frequency Synthesis

This section gives a short introduction to DTC-based frequency synthesis and explains the root causes for spurs in the output spectrum by summarizing results taken from [16].

A. Mathematical Definitions

Fig. 1 shows the basic principle of a DTC-based frequency synthesizer. An RF signal with frequency f_{dco} is generated by a PLL and is fed into the DTC. The DTC is controlled by a digital input $y(n)$ with m bits and generates an output signal $s(t)$ with frequency $f_{\mathrm{out}} = 1/T_{\mathrm{out}} < f_{\mathrm{dco}}$. When the digital input is kept constant, the DTC simply divides the DCO signal by an integer M, generating an output signal with the nominal frequency $f_0 = f_{\mathrm{dco}}/M$ and the nominal period $T_0 = 1/f_0$. The sequence of code words $\{y(n)\}$ determines the amount of delays added to the edges of the nominal signal. As there are 2^m possible code words that divide the nominal period into equal parts, the quantization (or time) resolution is given by

$$t_{\mathrm{LSB}} = \frac{T_0}{2^m}. \tag{1}$$

If an output frequency f_{out} that differs from the nominal frequency is generated, a code ramp needed for the successive phase shifts is applied to the DTC input. Therefore, the output sequence $\{x(n)\}$ of the integrator is generated by the recursion

$$x(n+1) = (x(n) + \Delta) \mod 2^b. \tag{2}$$

The input to the integrator, Δ, is given by

$$\Delta = \left\lfloor \frac{T_{\mathrm{out}} - T_0}{T_0}\, 2^b \right\rfloor, \tag{3}$$

and denotes the frequency difference between f_{out} and f_0 normed to the nominal frequency and quantized to b bits, i.e. $0 \le \Delta \le 2^b - 1$. As the DTC has an m bit wide input, the output of the integrator is re-quantized by discarding $b-m$ LSBs, giving

$$y(n) = \left\lfloor \frac{x(n)}{2^{b-m}} \right\rfloor. \tag{4}$$

The sequence $\{y(n)\}$ generated in this way, is the code ramp applied to the DTC input. For every single code word $y(n)$ of the code ramp it holds that

$$y(n) \in \{0, 1, \ldots, 2^m - 1\}, \quad n \in \mathbb{N}.$$

However, the re-quantization from sequence $\{x(n)\}$ to $\{y(n)\}$ leads to periodic errors in the time domain and consequently to quantization spurs in the output spectrum.

B. Nonlinearities

Any realization of a DTC by a circuit, $\mathrm{DTC_{real}}$, is expected to introduce nonidealities, which can be described in terms of the Integral Non-Linearity (INL), Differential Non-Linearity (DNL), gain and dynamic errors. The INL defines the difference between the ideal and nonideal delay for every possible code word and in this work it is given in terms of multiples of the time resolution t_{LSB}:

$$\mathrm{INL}(y) := \frac{\mathrm{DTC_{real}}(y) - y\, t_{\mathrm{LSB}}}{t_{\mathrm{LSB}}}, \quad \forall y \in \{0, 1, \ldots, 2^m - 1\}. \quad (5)$$

An important contributor to the INL is described in [17] which derives a systematic error for this phase-interpolator design. In addition to this, random changes to each possible delay due to process imperfections is expected but with smaller impact on the INL. The INL can be reduced by digital pre-distortion which re-maps a certain code to the closest actual delay. However, this requires sufficient knowledge of the actual INL. The DNL limits the quantization a DTC can accomplish. This is readily understandable as a certain gap between two delays cannot be recovered even if the DNL is perfectly known. A gain error of a DTC is an issue that is only present in certain designs, i.e. consisting of several delay-stages. Phase Interpolator (PI)-DTCs interpolate between two reference edge locations which confines all possible codes to a certain region and therefore have no gain error. Dynamic errors that impact a certain delay depending on the previously selected delays can be introduced if the circuit is not fully settled between generated edge locations. An example for this is due to the limited capacitance of the supply to the DTC. These errors are reproducible for an identical sequence of code words and consequently create the same distortion for a specific frequency offset. Now, assuming a nonlinear DTC-based frequency synthesizer, the periodic repetition of the INL results in nonlinearity spurs. A detailed derivation for the DTC output spectrum is shown in [16].

In the following, concepts are presented that can suppress both spur classes, quantization and nonlinearity spurs.

III. Mathematical Model of Dithering DTC-Based Frequency Synthesizers

The following section summarizes and applies the results from [23] more specifically to a DTC-based frequency synthesizer in a first step. Based on the detailed mathematical analysis, an expression for the PSD of the DTC output signal $s(t)$ is derived. Then, a dither that is capable of mitigating all arising quantization spurs is presented. Furthermore, general requirements for dithering a nonlinear DTC are derived.

It is assumed that a dither is applied to every rising clock edge of a DTC, the falling edges will follow a fixed time after the rising edges [17], defined here to be $T_0/2$ seconds. The DTC output $s(t)$ can be represented as a rectangular signal

$$s(t) = \sum_n p(t - nT_{\mathrm{out}} - \delta_n + \alpha), \quad (6)$$

where T_{out} is the desired output period of the DTC. The dither is modelled by a stationary discrete-time random process $\{\delta_n\}$ and $p(t)$ is a pulse of the form

$$p(t) = \begin{cases} 1 & -T_0/4 \le t < T_0/4 \\ 0 & \text{else.} \end{cases} \quad (7)$$

The random variable α, uniformly distributed in $[0, T_{\mathrm{out}}]$ and independent of $\{\delta_n\}$, models an arbitrarily chosen starting point or phase shift of the output $s(t)$.

Let

$$R_s(t, \tau) = \mathbb{E}(s(t)s(t + \tau)) \quad (8)$$

be the autocorrelation function (ACF) of the output signal which, without further assumptions, depends on both the absolute time t and the time displacement τ. Plugging (6) into (8) results to

$$R_s(t, \tau) = \mathbb{E}\Bigg(\sum_m \sum_n p\,(t - mT_{\mathrm{out}} - \delta_m + \alpha) \times p\,(t + \tau - nT_{\mathrm{out}} - \delta_n + \alpha)\Bigg).$$

Changing expectation and summation yields

$$R_s(t, \tau) = \sum_m \sum_n \mathbb{E}(p(t - mT_{\mathrm{out}} - \delta_m + \alpha) \times p(t + \tau - nT_{\mathrm{out}} - \delta_n + \alpha)). \quad (9)$$

To obtain an expression for the expectation, it is more convenient to work in the Fourier domain. To this end, $p(t)$ is expressed in terms of its Fourier Transform $P(\omega)$ as

$$p(t) = \frac{1}{2\pi} \int P(\omega) e^{j\omega t} d\omega. \quad (10)$$

Since $p(t)$ in (7) is a real valued and even signal its Fourier Transform $P(\omega)$ has the same characteristics. Therefore, the product of $p(t)$ and its time-shifted version $p(t + \tau)$ may be expressed as

$$p(t)p(t + \tau) = \frac{1}{4\pi^2} \int\int P(\omega)P(\xi) e^{j\omega t} e^{-j\xi(t+\tau)} d\omega d\xi. \quad (11)$$

Using (11) and (9) yields,

$$R_s(t, \tau) = \sum_m \sum_n \mathbb{E}\Bigg(\frac{1}{4\pi^2} \int\int P(\omega)P(\xi) \times e^{j\omega(t - mT_{\mathrm{out}} - \delta_m + \alpha)} e^{-j\xi(t + \tau - nT_{\mathrm{out}} - \delta_n + \alpha)} d\omega d\xi\Bigg). \quad (12)$$

Defining the index $n = m + k$, (12) can be written as

$$R_s(t, \tau) = \sum_m \sum_k \frac{1}{4\pi^2} \int\int P(\omega)P(\xi) e^{j\omega t} e^{-j\xi(t+\tau)} \times \mathbb{E}\left(e^{j\xi\delta_{m+k} - j\omega\delta_m}\right) \mathbb{E}\left(e^{j(\omega - \zeta)\alpha}\right) \times e^{j(\xi - \omega)mT_{\mathrm{out}}} e^{j\xi kT_{\mathrm{out}}} d\omega d\xi. \quad (13)$$

Using the Dirac comb representation

$$\sum_k e^{j\omega kT} = \frac{2\pi}{T} \sum_k \delta\left(\omega - k\frac{2\pi}{T}\right), \quad (14)$$

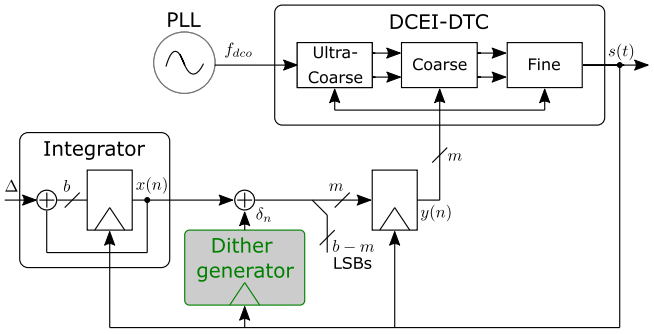

Fig. 3. Additive dither for a DTC-based frequency synthesizer. To mitigate the quantization spurs, it is necessary to add the dither δ_n at the quantization-domain crossing between integrator output (b-bit) and DTC input (m-bit).

the sum of the exponential term over all m in (13) can be expressed as

$$\sum_m e^{j(\xi-\omega)mT_{\text{out}}} = \frac{2\pi}{T_{\text{out}}} \sum_m \delta\left(\xi - \omega - m\frac{2\pi}{T_{\text{out}}}\right). \quad (15)$$

Thus it is possible to integrate with respect to ξ, leading to a sum of terms in m with ξ being replaced by $\omega + m2\pi/T_{\text{out}}$

$$R_s(t,\tau) = \sum_m \sum_k \frac{1}{4\pi^2} \int P(\omega) P\left(\omega + m\frac{2\pi}{T_{\text{out}}}\right) e^{j\omega t} \times e^{-j\left(\omega + m\frac{2\pi}{T_{\text{out}}}\right)(t+\tau)} \mathbb{E}\left(e^{j\left(\omega+m\frac{2\pi}{T_{\text{out}}}\right)\delta_{m+k} - j\omega\delta_m}\right) \times \mathbb{E}\left(e^{-jm\frac{2\pi}{T_{\text{out}}}\alpha}\right) \frac{2\pi}{T_{\text{out}}} e^{j\left(\omega+m\frac{2\pi}{T_{\text{out}}}\right)kT_{\text{out}}} d\omega. \quad (16)$$

Since the exponential term involving the random variable α is given by

$$\mathbb{E}\left(e^{-jm\frac{2\pi}{T_{\text{out}}}\alpha}\right) = \begin{cases} 1 & m = 0 \\ 0 & \text{else} \end{cases} \quad (17)$$

all but the term $m = 0$ in this sum will be zero. Taking all this into consideration, (16) can be written as

$$R_s(t,\tau) = \sum_k \frac{1}{4\pi^2} \int P(\omega) P(\omega) e^{-j\omega\tau} \times \mathbb{E}\left(e^{j\omega\delta_k - j\omega\delta_0}\right) \frac{2\pi}{T_{\text{out}}} e^{j\omega kT_{\text{out}}} d\omega. \quad (18)$$

With the definition of the joint characteristic function (CF) of the random variables δ_k and δ_0

$$C_k(\omega) = \mathbb{E}\left(e^{j\omega(\delta_k - \delta_0)}\right) \quad (19)$$

(18) can be expressed as

$$R_s(t,\tau) = \frac{1}{2\pi} \int e^{-j\omega\tau} \frac{P(\omega)^2}{T_{\text{out}}} \sum_k C_k(\omega) e^{j\omega kT_{\text{out}}} d\omega. \quad (20)$$

Since the right-hand side of (20) is independent of t, the output signal $s(t)$ is in fact wide sense stationary (WSS). Let $S(\omega)$ denote the PSD of $s(t)$, which is related to $R_s(\tau)$ by

$$R_s(\tau) = \frac{1}{2\pi} \int S(\omega) e^{j\omega\tau} d\omega = R_s(-\tau). \quad (21)$$

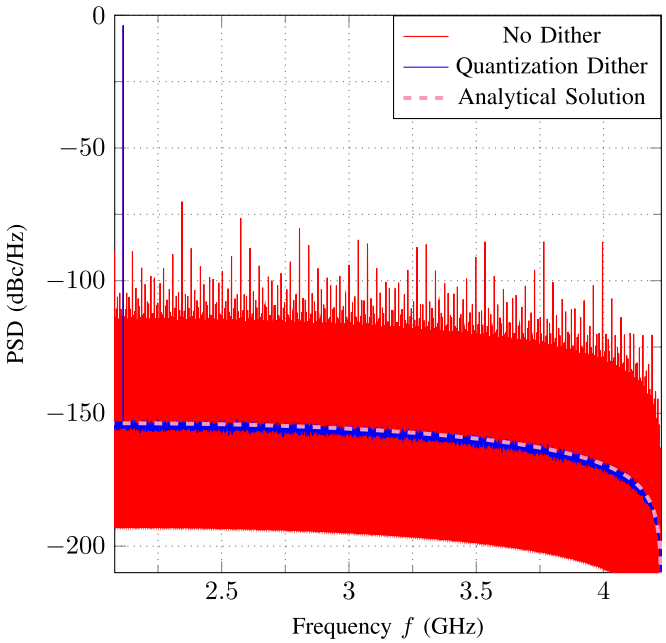

Fig. 4. PSDs of an ideal DTC-based frequency synthesizer with simulation parameters from Table I. An independent and identically uniformly distributed dither is capable to smear all quantization spurs. (27) confirms the simulation results.

TABLE I
SIMULATION PARAMETERS, [1] INL IS DISABLED FOR FIG. 4 AND FIG. 6

$f_{\text{dco}} = 8\,\text{GHz}$
$M = 4 \Rightarrow f_0 = 2\,\text{GHz}$
$b = 32$
$m = 11$
$f_{\text{out}} = 2.1134\,\text{GHz}$
INL as shown in Fig. 12 [1]

A comparison of (21) and (20) shows that

$$S(\omega) = \frac{P(\omega)^2}{T_{\text{out}}} \sum_k C_k(\omega) e^{j\omega kT_{\text{out}}}. \quad (22)$$

Equation (22) states that the PSD obviously depends on the spectrum of the pulse but as well on the CF of the applied dither. Various classes of spurs can thus be mitigated by using different statistical properties of the dither as shown in the upcoming sections.

A. Dithering Quantization Spurs

In the following, an ideal DTC-based frequency synthesizer, meaning that there are no circuit nonlinearities, is considered. In such a system the output edges can be uniformly placed at a certain number of time locations due to the finite quantization resolution of the DTC.

Assuming that the dither $\{\delta_n\}$ is independent and identically distributed (i.i.d) and let $C(\omega)$ denote its CF. In this case the joint CF in (19) reduces to

$$C_k(\omega) = \begin{cases} 1 & k = 0 \\ |C(\omega)|^2 & k \neq 0 \end{cases} \quad (23)$$

which, after substitution into (22), yields

$$\begin{aligned} S(\omega) &= \frac{P(\omega)^2}{T_{\text{out}}}\left(1+|C(\omega)|^2\left(\sum_k e^{j\omega k T_{\text{out}}}-1\right)\right) \\ &= \frac{P(\omega)^2}{T_{\text{out}}}\left(1-|C(\omega)|^2\right) \\ &\quad + \frac{P(\omega)^2}{T_{\text{out}}}|C(\omega)|^2\sum_k e^{j\omega k T_{\text{out}}} \\ &= \frac{P(\omega)^2}{T_{\text{out}}}\left(1-|C(\omega)|^2\right) \\ &\quad + \frac{2\pi}{T_{\text{out}}^2}P(\omega)^2|C(\omega)|^2\sum_k \delta\left(\omega-k\frac{2\pi}{T_{\text{out}}}\right). \end{aligned} \tag{24}$$

Expression (24) shows that in case of an i.i.d dither the PSD can be expressed as the sum of a discrete part and a continuous part:

$$S(\omega) = S_d(\omega) + S_c(\omega). \tag{25}$$

The discrete part, given by

$$S_d(\omega) = \frac{2\pi}{T_{\text{out}}^2}P(\omega)^2|C(\omega)|^2\sum_k \delta\left(\omega-k\frac{2\pi}{T_{\text{out}}}\right), \tag{26}$$

consists of spectral tones that are separated by multiples of $f_{\text{out}} = 1/T_{\text{out}}$, and its amplitudes are determined by the squared magnitude of the spectrum of the pulse and the dither CF sampled at those locations. Interestingly, by adding clock dither whose CF is zero at integer multiples of f_{out}, the harmonics could be suppressed. Similar investigations are shown in [24], where the output digital images of an all digital phase locked loop (ADPLL) can be removed by dithering the DCO clock.

In addition to the discrete part, the spectrum also contains a continuous part, which is expressed as

$$S_c(\omega) = \frac{P(\omega)^2}{T_{\text{out}}}\left(1-|C(\omega)|^2\right). \tag{27}$$

It is seen that the CF also appears as an additional spectral weighting function.

In [25]–[27] it is shown that a dither uniformly distributed between zero and one LSB satisfies all required conditions such that the total error of any quantized system becomes uniformly distributed and statistically independent. A block diagram and a simulation result of the application of such a dither are given in Fig. 3 and Fig. 4, respectively. In the simulation the parameters as shown in Table I were used. The INL was disabled to show only the effect of quantization.

The output frequency f_{out} lies within band n1 in Frequency Range 1 [28] of NR and is a worst-case scenario with respect to spur power. Using (1), the resulting DTC resolution is given by $t_{\text{LSB}} = 500\,\text{ps}/2^{11} = 244.14\,\text{fs}$ [17]. Comparing the PSDs, it can be noted that without dither many spurs across the entire frequency range arise. However, once the dither $\{\delta_n\}$ is added to the code ramp $\{x(n)\}$, before the DTC input, all quantization spurs are removed and the additive white noise model for the quantization error is applicable. Moreover, the PSD perfectly

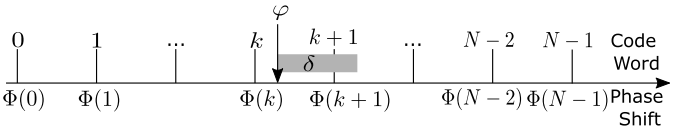

Fig. 5. Uniform grid of phase shifts for an ideal DTC. The wanted phase shift φ is in general not selectable. However, with a dither $\delta \sim \mathcal{U}[0, t_{\text{LSB}}]$ the two nearest code words k and $k+1$ are selected randomly such that on average φ is generated.

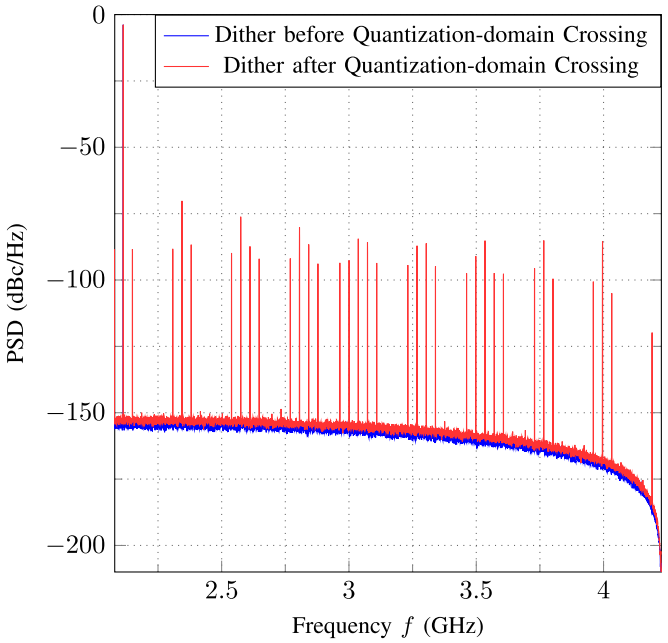

Fig. 6. PSDs of a DTC where dither is added before and after the quantization-domain crossing. Applying the dither directly at the DTC input cannot suppress all quantization spurs.

matches with the analytical expression in (27) where the CF of the applied dither $\delta_n \sim \mathcal{U}[0, t_{\text{LSB}}]$ and $P(\omega)$ are given by

$$C(\omega) = \frac{e^{j t_{\text{LSB}}\,\omega/2\pi}-1}{j t_{\text{LSB}}\,\omega/2\pi}, \tag{28}$$

and

$$P(\omega) = \frac{\sin(T_0\omega/4)}{\omega/2} \tag{29}$$

respectively.

It is necessary to add the dither before the quantization-domain crossing between integrator output and DTC input, as shown in Fig. 3. The phase shifts generated by the integrator output are placed on a finer grid than the available phase shifts of the DTC, see Fig. 5. By adding the dither before the re-quantization, the two nearest code words k and $k+1$ of the DTC are selected, such that on average the phase shifts from the integrator are generated. However, applying the dither after the quantization-domain crossing would not remove the quantization spurs. In fact, after the re-quantization the code word k is already fixed and adding a dither $\delta_n \sim \mathcal{U}[0, t_{\text{LSB}}]$, in turn, leads again to a selection of code word k. Selecting just randomly the code words k and $k+1$, cannot suppress all quantization spurs, as shown in Fig. 6.

Note, if there is no dither applied, then in (24) $C(\omega) = 1$ and the continuous part (27) of the spectrum becomes zero. The discrete part is then given by

$$S(\omega) = \frac{2\pi}{T_{\text{out}}^2} P(\omega)^2 \sum_k \delta\left(\omega - k\frac{2\pi}{T_{\text{out}}}\right), \tag{30}$$

and using (29), is seen to be an impulse train

$$S(\omega) = 2\pi \sum_k A_k \delta\left(\omega - k\frac{2\pi}{T_{\text{out}}}\right) \tag{31}$$

with magnitudes

$$A_k = \left(\frac{\sin\left(k\pi T_0/\left(2T_{\text{out}}\right)\right)}{\pi k}\right)^2, \tag{32}$$

which are the Fourier coefficients of a rectangular signal, having a period of T_{out} and a pulse width given by $T_0/2$.

B. Generic Dither Requirements for a Nonlinear DTC

The application of a dither as given in (28) changes the behavior of the output signal such that two essential requirements can be derived, see Fig. 5:

1) The code word selection needs to be random to result in smearing all quantization spurs.
2) A wanted edge location repeated over time needs to create an output which averages to the wanted delay.

If the available phase shifts or time delays are on a uniform grid as shown in Fig. 5, both requirements can be accomplished with a stationary dither like in (28). Given the more likely scenario of a non-uniform grid, i.e. the DTC shows nonlinearities, the dither must be non-stationary. However, the two mentioned requirements can be used to judge the feasibility of other dither methods as will be shown in Section IV and Section V.

IV. Subtractive Dither

An interesting way to dither unwanted nonlinearities is the possibility to remove the dither signal before the desired output. This so-called subtractive dither is well known in literature [26]. While many investigations focus on dithering the magnitude, the concept can similarly be investigated for DTCs. Subtractive dithering for a DTC within the feedback path of a PLL is discussed in [22]. Here the subtraction can be done in the digital domain only modified by the appropriate transfer functions. A popular concept in literature involves adding a digital dither before a digital-to-analog converter (DAC) and after a transmission via a channel and sampling the signal with an analog-to-digital converter (ADC) the dither is subtracted. It is thinkable to implement the very same method by replacing the ADC and DAC with a digital-to-phase and phase-to-digital converter, respectively. However, this requires the knowledge of the dither at the transmitter and at the receiver of a wireless communication system which is not practically implementable. The investigated subtractive dither here should therefore be reduced to systems where the subtractions happen without a wireless channel in between, i.e. only within the receiver (RX) or transmitter (TX) part of the transceiver. In this work it is named self-contained subtractive dithering.

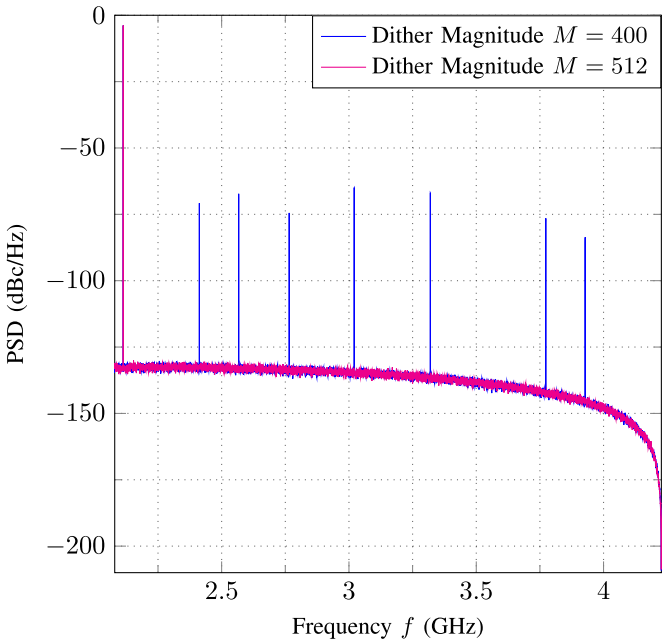

Fig. 7. PSD of a DTC-based frequency synthesizer using self-contained subtractive dither, with parameters from Table I. Two different dither magnitudes are compared.

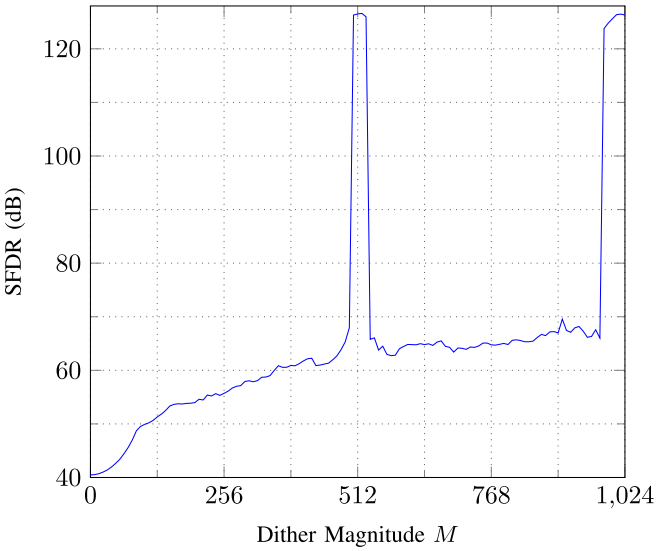

Fig. 8. SFDR simulation result over increasing dither magnitudes for self-contained subtractive dither.

In contrast to additive dither as discussed in Section V the dither presented here is not using the precise knowledge of the INL. A general concept of subtractive dither is the fact that there are multiple possibilities to generate one delay. Each of these possibilities has a different nonlinearity and the dither selects between them. Sufficient random selection results in decorrelation of the errors.

A. Self-Contained Subtractive Dithering

When the dither is not part of the transmitted signal, the magnitude of the dither is not limited by the RF emission

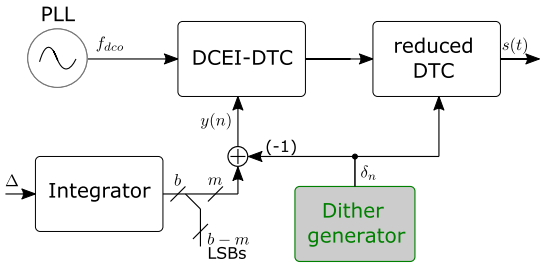

Fig. 9. Dither subtraction with a second DTC.

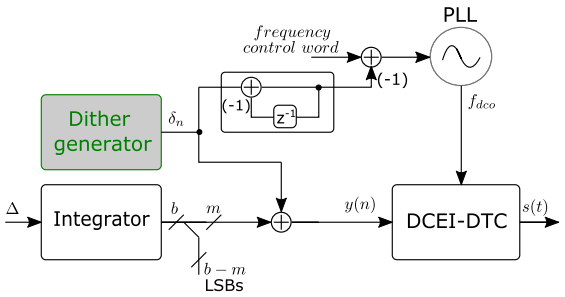

Fig. 10. Dither subtraction with a PLL.

specifications. It is possible to fulfill the requirements stated in Section III-B with only limited information about the nonlinearity. An obvious knowledge of the investigated DTC systems is, that the nonlinearity spans from the minimum to the maximum delay. Subtractive dither allows to add dither with a maximum magnitude of the full delay range and therefore resulting in a random selection of all possible INL values. A major benefit of this method is that it does not require exact knowledge of the nonlinearity and can be applied without measurements which removes significant complexity.

The resulting RX or TX system which uses subtractive dither needs two phase inputs where the dither is added and subtracted again and with the targeted nonlinearity in between those two. Obviously one of these points of addition is with the digital input data supplied to the DTC which requires the second point to subtract the same dither in the analog domain. There are several possibilities that present themself for this:

- A second DTC,
- The PLL which provides the analog reference to the DTC,
- After downconversion in the baseband processing of a receiver.

All methods randomize the selection of a DTC delay and consequently also the error associated with it. The INL of the DTC still generates unwanted spectral components. However, with sufficient random selection this energy appears as spur-free noise floor in the PSD. If the DTC is calibrated and pre-distorted this noise floor can be reduced to the level of the DNL. A challenge are dynamic errors as these change with the sequence of the applied dither and might not be sufficiently randomized. While all static errors can be dithered, dynamic errors still remain an important design challenge.

The application of uniform dither and subtraction with a DTC using simulation parameters from Table I results in a PSD as shown in Fig. 7. The applied dither is selected from the output of a discrete uniform random variable $X \sim \mathcal{U}\{0, M\}$ with M denoting the dither magnitude. It can be observed that a chosen dither magnitude of $M = 512$ results in a spur-free PSD while a magnitude of $M = 400$ still leaves nonlinearity induced spurs. The Spurious Free Dynamic Range (SFDR) for all dither magnitudes up to $M = 1024$ with the simulation parameters from Table I has been gathered and is presented in Fig. 8. The maximum SFDR of 126.47 dB is reached when all spurs are successfully dithered. This maximum is achieved at multiples of 512. This relates to the fact that the INL as shown in Fig. 12 is repetitive every 512 codewords, and a dither with the maximum of multiples of this value selects each INL value with the same probability.

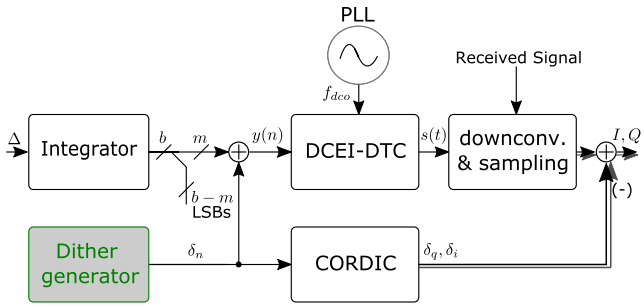

Fig. 11. Dither subtraction at baseband.

The different options of subtractive dithering come with individual drawbacks.

1) Subtractive Dither With a 2nd DTC: A second DTC, as shown in Fig. 9, introduces additional nonlinearities to the system. As a significant amount of nonlinearity is systematic [17], the nonlinearity of both DTCs would be correlated which violates an important assumption of subtractive dither. Additionally using another DTC which operates as fractional divider would limit the maximum frequency of the output. Therefore, a reduced DTC is shown in Fig. 9 which implements a reduced range of modulation. As the INL of the DTC design discussed in [17] and shown in Fig. 12 is repetitive, the subtractive dither magnitude can be confined to one range of the INL period. Consequently, the reduced DTC only needs to be able to cover the range of one INL period which simplifies its design. This dither magnitude is also supported by the simulation results of the SFDR from Fig. 8. A possible implementation of this reduced DTC is a delay-element based design that have been shown in [29], [30] and reducing the range of the delay line to the range of one repetitive INL of the DTC. The different operation principle of the reduced DTC results in an independent INL compared to the PI-DTC.

Still, this variant obviously increases the required area and current consumption and will result in tighter requirements on the existing PLL and DTC as it requires a new additional analog block within the LO path. The other methods presented here are more promising as they re-use existing blocks.

2) Subtractive Dither With a PLL: Subtracting the dither at the PLL as shown in Fig. 10, requires an extension of the PLL circuit for phase modulation. Phase modulation of a PLL is well known in literature [31]. Also, a certain frequency

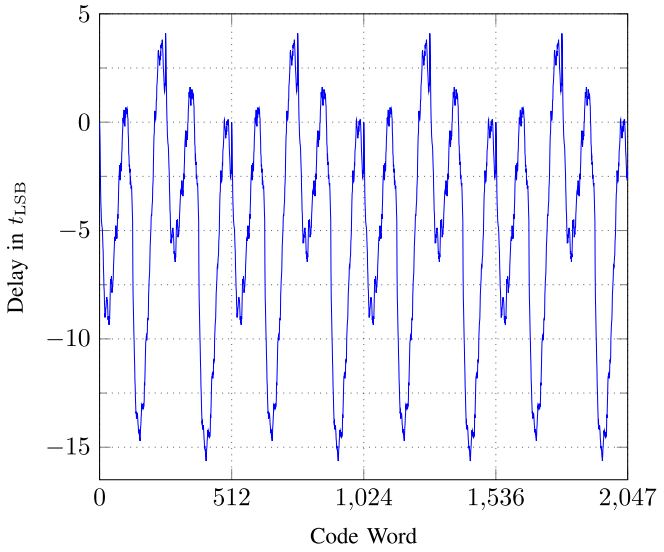

Fig. 12. INL of a DTC presented in [17]. The INL is repetitive every 512 codes due to the interpolation design.

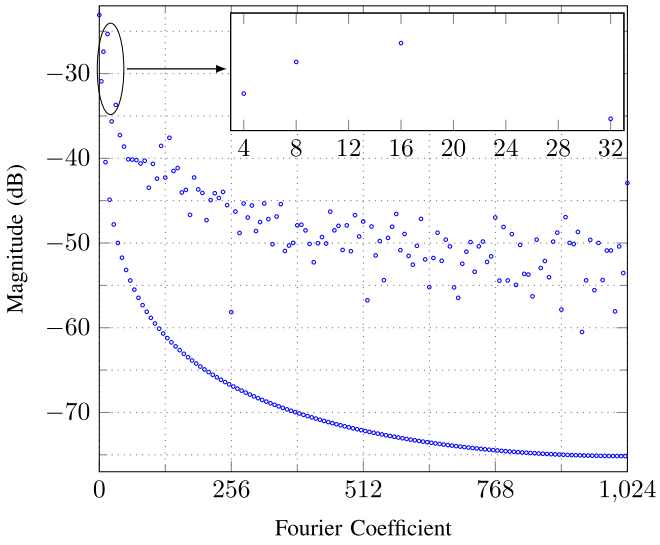

Fig. 13. Fourier decomposition from Fig. 12. The dominating Fourier coefficients 4, 8, 16 and 32 are used for subtractive dithering.

tuning range is a necessary requirement for cellular PLLs. This tuning range can be expanded to accommodate for dither. The modulation of a PLL is limited by a maximum bandwidth and frequency range which consequently limits the possible dither. In Fig. 10 a PLL with such a frequency modulation is used and the dither for the DTC is integrated to a frequency modulation for the PLL. Two additional complexities, which are omitted in the Figure for simplicity, are the different data rates for the DTC and PLL modulation input as well as the synchronization of both signal paths. The different data rates can be generated with a Fractional Sample-Rate Converter (FSRC) as published in [32]. The synchronization can be realized with buffer stages, the required delay is constant but design dependent.

One important drawback is that the generated PLL output contains the dither and any use of this RF signal for other means, like as an LO for a different transmission, might not be feasible. This severely limits the usage scenarios of such a system.

3) Subtractive Dither via Baseband: Subtraction at the digital baseband after downconversion, as shown in Fig. 11, only requires additional logic. However, this is only possible in the receive part of a transceiver. This variant uses an RF carrier with applied dither for downconversion of the received signal. The I/Q symbols contain the phase dither which can be subtracted digitally. The conversion of the dither to the I/Q domain is done via a Coordinate Rotation Digital Computer (CORDIC) in Fig. 11. A digital baseband might implement such a CORDIC for phase correction and the phase dither can be added to it's input instead. However, this schema may introduce unwanted additional components at the baseband due to folding with a modulated LO which need to be cancelled as well.

B. Fourier-Based Dithering

All self-contained subtractive dither variants allow for randomization with a much larger magnitude compared to additive variants as the dither is not part of the transmitted signal. The selection of the actual applied code word of a DTC can be chosen so, that the excited nonlinearities do not correlate with each other and therefore do not result in spurs. While this decorrelation is necessary to remove all spurs from the output PSD, the nonlinearity can also be decomposed into individual components to allow for a more granular control of the system.

Considering the actual INL shown in Fig. 12, which was observed in a phase-interpolator design [17], it becomes apparent that this INL does show a periodic characteristic. The Fourier decomposition of the INL, see Fig. 13, shows only a few dominating coefficients. This observation gives cause to the idea of dithering based on multiple independent sinusoidal shapes of the INL. As stated in Section III-B, it is necessary that the average of the output signal including all nonlinearities and the dither is equal to the intended edge location. This can be achieved by requiring the mean over all selected INL values to be zero. Each sinusoidal nonlinearity has a pair of code words which features INL values with equal magnitude and opposing sign at the distance of half a period. Random selection between these two delays decorrelates the sequence of nonlinearities which removes the according spur. The sinusoidal shapes give reason to investigate the Fourier transformation of the INL.

To evaluate the concept of Fourier-based dithering, a precise model of the DTC in [17] has been implemented in MATLAB. The periodic shape of the INL is explained and supported by a model in Section II of [17]. A circuit simulation has been used to extract the actual INL which is the basis for the simulations presented here. The INL and its Fourier decomposition are shown in Fig. 12 and Fig. 13, respectively. Based on the MATLAB model a simulation result, using the parameters from Table I, is shown in Fig. 14. It can be seen at the bottom right comparison that in the presence of nonlinearities the dither from (28) is only capable of smearing the quantization spurs while the spurs related to the nonlinearity remain.

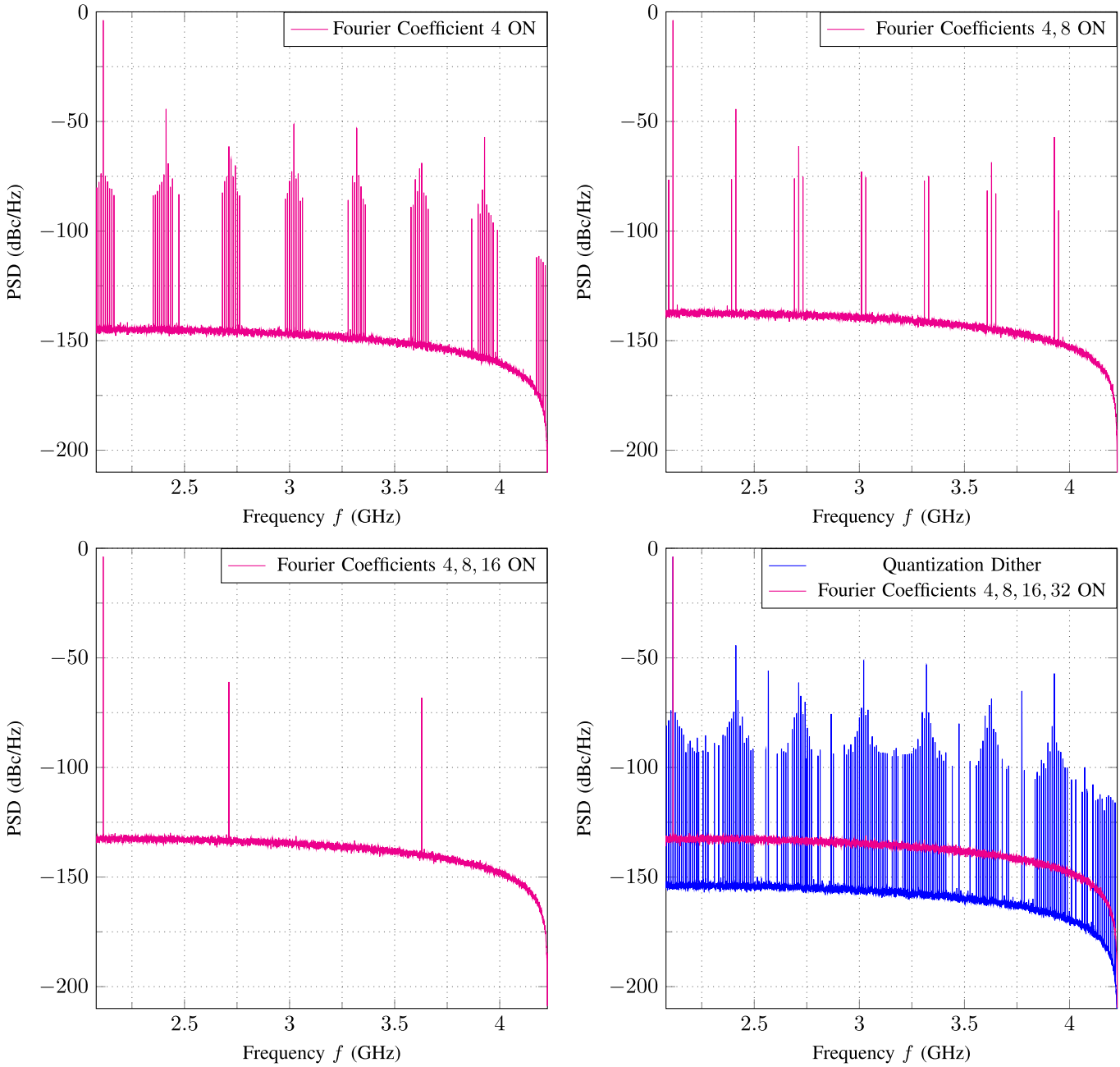

Fig. 14. Simulated PSD of a DTC-based frequency synthesizer, with parameters from Table I. Starting from top left, the first dominating Fourier coefficient is used for subtractive dither. With every additional dominating coefficient, further nonlinearity induced spurs are suppressed. Bottom right shows the comparison between the dither from (28) that is just capable of mitigating quantization spurs, and the subtractive dither including all four dominating Fourier coefficients (4, 8, 16 and 32).

With the given systematic shape of the INL, the Fourier decomposition shown in Fig. 13 is governed by a couple of dominating coefficients. The coefficients $4, 8, 16$ and 32 are several dB larger than the others. Each of these coefficients is dithered with a single value that shifts the input to half the respective period, e.g. the Fourier coefficient 4 is dithered by shifting the input for $N/8$, where N denotes the number of available DTC code words. The respective subtraction follows the same principle and requires one magnitude per Fourier coefficient. Especially for the subtraction variant with a dedicated second DTC, this proposed method reduces the required complexity significantly. Fig. 14 shows PSDs of simulation results with the same parameters from Table I, when different number of Fourier coefficients are used. It presents that with every additional dominating coefficient, further nonlinearity induced spurs are mitigated. The subtractive dither including all four dominating Fourier coefficients $(4, 8, 16$ and $32)$ results in a spur-free PSD. The ideal noise floor that can be reached with Fourier-based dithering is identical to the previously discussed subtractive variants and relates to the size of the INL. The magnitude of the first dominating Fourier coefficient 4 requires a shift of $2048/8 = 256$ code words which is half the magnitude of the required uniform dither as discussed in Section IV-A.

Since Fourier-based dithering uses dominant Fourier components to generate a reduced set of delays a predistor-

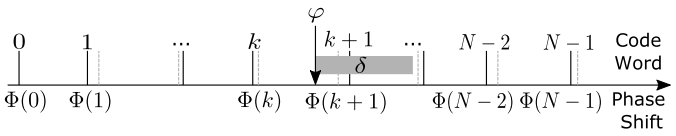

Fig. 15. Non-uniform phase grid of a DTC including nonlinearities. The uniform grid (dashed) results in selectable phase shifts on a non-uniform grid. The optimal dither δ is a non-stationary uniformly distributed random process that selects the two nearest code words k and $k+1$ such that on average φ is generated.

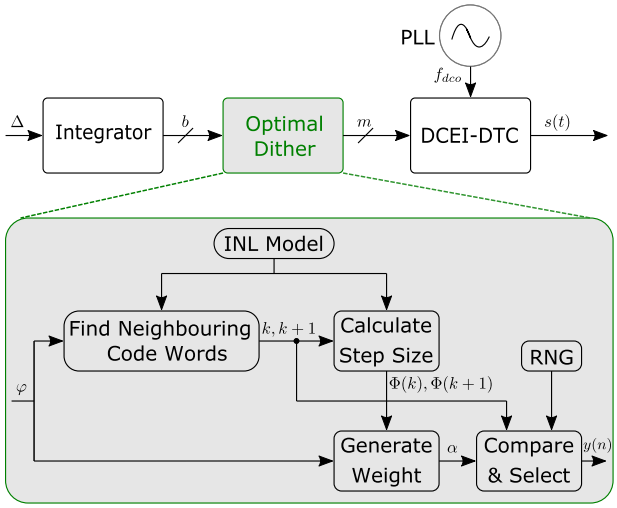

Fig. 16. Block diagram of optimal dither.

tion is counterproductive as it changes the Fourier transformation of the effective nonlinearity including predistortion. Consequently, the DNL which is interesting for a predistorted system has no equivalent interpretation for a Fourier-based subtractive dithering system. Dynamic effects are a challenge as they might introduce additional correlated errors. The maximum effect can be estimated with the largest shift of all dominant Fourier coefficients. While it is possible to apply Fourier-based dithering to all subtractive dither methods, a straightforward application is the combination with a second DTC as shown in Fig. 9. Here it enables the simplification of analog hardware. The second DTC, which realizes Fourier based subtraction of dither, only needs a few distinct binary weighted delay elements which correspond to the dominant Fourier components of the targeted nonlinearity.

V. Optimal Dither

As explained in Section III-B, certain properties are required to successfully smear spurs. The previously presented dithering of quantization spurs shown in Fig. 5 can be generalized by combining the addition of uniform additive dither and the following quantization into a weighted selection of neighbouring code words. The very same way of selection can now be extended for cases where the available phase shifts are not on a uniform grid as shown in Fig. 15.

The selection mechanism shown in Fig. 16 can be described as follows:

- Find the two nearest existing code words k and $k+1$ on the nonlinear grid, with corresponding phase shifts $\Phi(k)$ and $\Phi(k+1)$, such that φ lies in between (see Fig. 15)
- To produce on average the wanted phase shift φ, a weight α is calculated that determines the selection process of the code words k and $k+1$

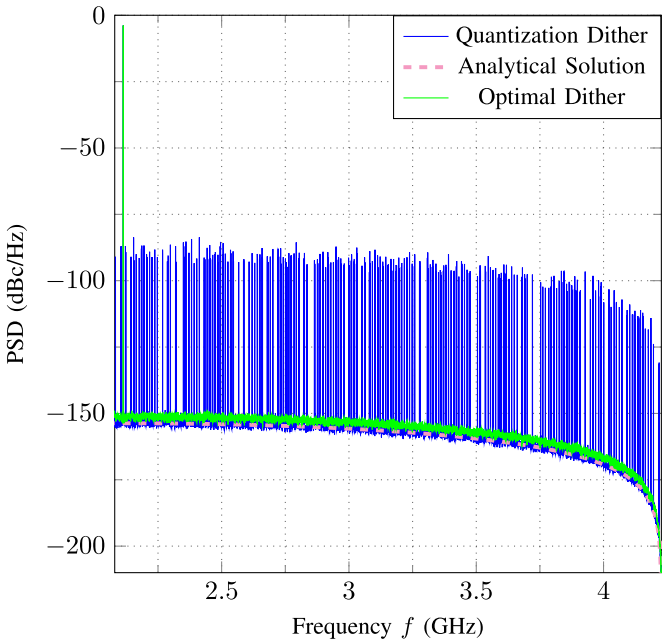

Fig. 17. Simulated PSD of a DTC-based frequency synthesizer, with parameters from Table I. The optimal dither combines a predistortion and the optimal code word selection.

- An RNG (random number generator) generates a uniformly distributed random number in the interval $[0, 1]$, which is compared to the weight α. If the random number is smaller than α select the code word k, otherwise select the code word $k+1$. The weight α is calculated with:

$$\alpha = \frac{\varphi - \Phi(k)}{\Phi(k+1) - \Phi(k)}. \tag{33}$$

The PSD in Fig. 17 shows the result of this generalized method. Here the same setup from Table I was used. The applied optimal dither itself is no longer stationary but has still the important property of not being correlated. Therefore, the derived analytical solutions from (27) can be applied to this method as well.

Optimal dithering implicitly performs a predistortion of the INL as it selects between the neighbouring code words. The error due to the remaining nonlinearity is proportional to the DNL as it increases the effective quantization of the system. This method could theoretically also account for dynamic errors if they are precisely known, but further increases the complexity. The main challenge besides the computational complexity is the required precise knowledge of the INL and dynamic effects significantly increase the challenge for optimal dither.

VI. Dither Comparison

Each of the proposed dither methods have distinct advantages and downsides. Table II compares all those variants and lists key parameters. Quantization dither and optimal dither are the only additive methods presented here. Quantization dither is the simplest method of all variants. It can successfully smear quantization spurs, but does not take any nonlinearities into account which explains the low SFDR and improvement in the last two rows of Table II. The SFDR improvement is calculated from a reference value of 40.48 dB that is achieved when no dither and the parameters from Table I

TABLE II

DITHER COMPARISON, [1] FOURIER DECOMPOSITION SHOULD BE DOMINATED BY FEW COEFFICIENTS, [2] USING PARAMETERS FROM TABLE I, [3] THE OPTIONAL CALIBRATION RESULTS IN AN INCREASED SPECTRAL PERFORMANCE, [4] W.R.T NO APPLIED DITHER AND USING PARAMETERS FROM TABLE I GIVES A REFERENCE SFDR OF 40.48 db

	Quantization Dither	Optimal Dither	Sub. at 2nd DTC	Sub. at PLL	Sub. at baseband	Fourier-based
Proposed in	[25]–[27]	This work				
Suitable for TX Suitable for RX	yes yes	yes yes	yes yes	yes yes	no yes	yes yes
Dither type For specific INL shape	additive –	additive any	subtractive any	subtractive any	subtractive any	subtractive sinusoidal[1]
Analog component required Calibration	no no	no required	yes optional	no optional	no optional	yes, small detrimental
Computational complexity	low	high	low	low	low	low
SFDR (dB)[2] SFDR Improvement[4]	79.99 39.51	145.07 104.59	126.47[3] 85.99			125.76 85.28

are used. The second additive method, optimal dither, is the extension of quantization dither. Indeed, this variant is capable of suppressing all spurious emissions and achieves the highest SFDR of 145.07. However, the disadvantage is, that it relies on the exact knowledge of the nonlinearity of the DTC. The requirement of optimal dither of knowing the INL is especially challenging when dynamic nonlinearities result in a frequency dependency of the INL. Since the algorithm for optimal dithering selects between neighbouring code words, a pre-distortion for a nonlinearity is implicitly included. This pre-distortion is optional for the three main subtractive dither variants. Here an arbitrary delay out of the full repetition period of the INL is selected randomly which removes any periodicity. The performance of these subtractive dither variants is related to the actual INL. Measuring and pre-distorting the DTC changes the effective INL to a residual INL of lower magnitude which translates to a reduced noise floor that the subtractive dither methods reach. As a consequence, a calibration is needed, depending on the out-of-band spectral requirements.

Any measurement errors or changes of the INL, e.g. due to power, voltage or temperature changes, result in a modification of the INL. If the DTC is pre-distorted, e.g. with a look-up table (LUT), it results in a change of the residual INL in the calibrated system which comprises the DTC with its digital pre-distortion [18]. This is a challenge for the additive optimal dither method and would lead to spurious emissions if the calibration is not matching the system. For subtractive dither methods any change of the nonlinearity impacts the noise floor level but does not lead to any spurious emissions as these methods do not rely on the exact knowledge of the INL.

A special case of subtractive dithering is the presented Fourier dithering. Its main advantage over the other subtractive variants is that it relies on less delay elements for the subtraction of the dither. However, it is only possible if the nonlinearity is dominated by a handful of Fourier coefficients. If a DTC is measured and pre-distorted, the magnitude of the Fourier coefficients of the residual INL will be much more equally distributed. Consequently, all Fourier components have to be dithered to successfully smear all spurs. Such a system is possible but has no advantage to the other subtractive methods.

VII. CONCLUSION

This paper extends the mathematical modelling of dithering in digital phase shifting systems. It shows how to generate an optimal dither under the influence of nonlinearity in the system. However, optimal dither relies on the exact knowledge of the nonlinearity. Subtractive dither, as known in literature for ADCs and DACs, has been successfully applied in the phase domain. Several self-contained dither concepts within a transceiver are presented. The specific requirements of wireless communication give raise to cancel only distinct spurs which is enabled by the proposed simplified subtractive dither system based on Fourier decomposition.

REFERENCES

[1] K. Pedersen, F. Frederiksen, C. Rosa, H. Nguyen, L. G. Garcia, and Y. Wang, "Carrier aggregation for LTE-advanced: Functionality and performance aspects," *IEEE Commun. Mag.*, vol. 49, no. 6, pp. 89–95, Jun. 2011.

[2] *NR; User Equipment (UE) Radio Transmission and Reception; Part 2: Range 2 Standalone*, document Technical Specification (TS) 38.101-2, 3GPP, Version 16.4.0, 2020.

[3] P. K. Hanumolu, V. Kratyuk, G.-Y. Wei, and U.-K. Moon, "A sub-picosecond resolution 0.5–1.5 GHz digital-to-phase converter," *IEEE J. Solid-State Circuits*, vol. 43, no. 2, pp. 414–424, Feb. 2008.

[4] M. S. Chen, A. A. Hafez, and C. K. K. Yang, "A 0.1–1.5 GHz 8-bit inverter-based digital-to-phase converter using harmonic rejection," *IEEE J. Solid-State Circuits*, vol. 48, no. 11, pp. 2681–2692, Nov. 2013.

[5] J. Z. Ru, C. Palattella, P. Geraedts, E. Klumperink, and B. Nauta, "A high-linearity digital-to-time converter technique: Constant-slope charging," *IEEE J. Solid-State Circuits*, vol. 50, no. 6, pp. 1412–1423, Jun. 2015.

[6] C. Preissl, P. Preyler, T. Mayer, A. Springer, and M. Huemer, "Analysis of spectral degradation and error compensation in 5G NR digital polar transmitters," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 67, no. 8, pp. 2719–2729, Aug. 2020.

[7] R. S. Kanumalli, A. Gebhard, A. Elmaghraby, A. Mayer, D. Schwartz, and M. Huemer, "Active digital cancellation of transmitter induced modulated spur interference in 4G LTE carrier aggregation transceivers," in *Proc. IEEE 83rd Veh. Technol. Conf. (VTC Spring)*, May 2016, pp. 1–5.

[8] A. Kiayani, M. Abdelaziz, L. Anttila, V. Lehtinen, and M. Valkama, "DSP-based suppression of spurious emissions at RX band in carrier aggregation FDD transceivers," in *Proc. 22nd Eur. Signal Process. Conf. (EUSIPCO)*, Sep. 2014, pp. 591–595.

[9] C. Motz, T. Paireder, and M. Huemer, "Modulated spur interference cancellation for LTE—A/5G transceivers: A system level analysis," in *Proc. IEEE 91st Veh. Technol. Conf. (VTC-Spring)*, May 2020, pp. 1–6.

[10] H.-T. Dabag, H. Gheidi, S. Farsi, P. Gudem, and P. M. Asbeck, "All-digital cancellation technique to mitigate receiver desensitization in uplink carrier aggregation in cellular handsets," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 12, pp. 4754–4765, Dec. 2013.

[11] S. A. Talwalkar, "Quantization error spectra structure of a DTC synthesizer via the DFT axis scaling property," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 59, no. 6, pp. 1242–1250, Jun. 2012.

[12] S. A. Talwalkar, "Digital-to-time synthesizers: Separating delay line error spurs and quantization error spurs," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 60, no. 10, pp. 2597–2605, Oct. 2013.

[13] N. Pavlovic and J. Bergervoet, "A 5.3 GHz digital-to-time-converter-based fractional-N all-digital PLL," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2011, pp. 54–56.

[14] S. Levantino, G. Marzin, and C. Samori, "An adaptive pre-distortion technique to mitigate the DTC nonlinearity in digital PLLs," *IEEE J. Solid-State Circuits*, vol. 49, no. 8, pp. 1762–1772, Aug. 2014.
[15] A. Ravi *et al.*, "A 2.4-GHz 20–40-MHz channel WLAN digital outphasing transmitter utilizing a delay-based wideband phase modulator in 32-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 47, no. 12, pp. 3184–3196, Dec. 2012.
[16] P. Preyler, C. Preissl, S. Tertinek, T. Buckel, and A. Springer, "LO generation with a phase interpolator digital-to-time converter," *IEEE Trans. Microw. Theory Techn.*, vol. 65, no. 11, pp. 4669–4676, Nov. 2017.
[17] S. Sievert *et al.*, "A 2 GHz 244 fs-resolution 1.2 ps-Peak-INL edge interpolator-based digital-to-time converter in 28 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 51, no. 12, pp. 2992–3004, Dec. 2016.
[18] Y. Palaskas *et al.*, "A cellular multiband DTC-based digital polar transmitter with −153 dBc/Hz noise in 14-nm FinFET," *IEEE Solid-State Circuits Lett.*, vol. 2, no. 9, pp. 179–182, Sep. 2019.
[19] T. H. Cheung *et al.*, "A 3.5-GHz digitally-controlled open-loop fractional-N frequency divider in 28-nm CMOS," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, Oct. 2020, pp. 1–5.
[20] P. P. Sotiriadis, "Spurs-free single-bit-output all-digital frequency synthesizers with forward and feedback spurs and noise cancellation," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 63, no. 5, pp. 567–576, May 2016.
[21] S. Talwalkar, T. Gradishar, B. Stengel, G. Cafaro, and G. Nagaraj, "Controlled dither in 90 nm digital to time conversion based direct digital synthesizer for spur mitigation," in *Proc. IEEE Radio Freq. Integr. Circuits Symp.*, May 2010, pp. 549–552.
[22] C.-R. Ho and M. S.-W. Chen, "A fractional-N digital PLL with background-dither-noise-cancellation loop achieving <−62.5 dBc worst-case near-carrier fractional spurs in 65 nm CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2018, pp. 394–396.
[23] B. Liu, "Timing jitter in digital filtering of analog signals," *IEEE Trans. Circuits Syst.*, vol. CS-22, no. 3, pp. 218–223, Mar. 1975.
[24] G. J. Ballantyne and J. Geng, "Effect of reference clock jitter and demonstration of near image-free operation for the ADPLL," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 57, no. 12, pp. 931–935, Dec. 2010.
[25] A. Sripad and D. Snyder, "A necessary and sufficient condition for quantization errors to be uniform and white," *IEEE Trans. Acoust., Speech, Signal Process.*, vol. ASSP-25, no. 5, pp. 442–448, Oct. 1977.
[26] L. Schuchman, "Dither signals and their effect on quantization noise," *IEEE Trans. Commun.*, vol. COM-12, no. 4, pp. 162–165, Dec. 1964.
[27] B. Widrow, "A study of rough amplitude quantization by means of Nyquist sampling theory," *IRE Trans. Circuit Theory*, vol. 3, no. 4, pp. 266–276, Dec. 1956.
[28] *NR; User Equipment (UE) Radio Transmission and Reception; Part 1: Range 1 Standalone*, document Technical Specification (TS) 38.101-1, Version 16.4.0, 3GPP, 2020.
[29] N. Markulic, K. Raczkowski, P. Wambacq, and J. Craninckx, "A 10-bit, 550-fs step digital-to-time converter in 28 nm CMOS," in *Proc. ESSCIRC-40th Eur. Solid State Circuits Conf. (ESSCIRC)*, Sep. 2014, pp. 79–82.
[30] A. Elmallah, M. G. Ahmed, A. Elkholy, W.-S. Choi, and P. K. Hanumolu, "A 1.6 ps peak-INL 5.3 ns range two-step digital-to-time converter in 65nm CMOS," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, Apr. 2018, pp. 1–4.
[31] R. B. Staszewski *et al.*, "All-digital PLL and transmitter for mobile phones," *IEEE J. Solid-State Circuits*, vol. 40, no. 12, pp. 2469–2482, Dec. 2005.
[32] A. Klinkan, E. Pfann, and M. Huemer, "A novel interpolation method for polar signals in radio frequency transmitters," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 65, no. 5, pp. 692–696, May 2018.

Christoph Preissl (Graduate Student Member, IEEE) received the bachelor's and master's degrees in technical and industrial mathematics from Johannes Kepler University Linz, Linz, Austria, in 2010 and 2013, respectively, where he is currently pursuing the Ph.D. degree with the Institute of Signal Processing. In 2014, he joined Danube Mobile Communications Engineering GmbH & Company KG (majority owned by Intel Austria GmbH), Linz, as a System Engineer. Since 2018, he has been a part of the Christian Doppler Laboratory for Digitally Assisted RF Transceivers for Future Mobile Communications, Johannes Kepler University Linz. His research interest includes the area of digital-intensive RF transceiver architectures.

Peter Preyler (Student Member, IEEE) received the M.Sc. degree in mechatronics from Johannes Kepler University Linz, Linz, Austria, in 2016, where he is currently pursuing the Ph.D. degree. In 2011, he joined Danube Mobile Communications Engineering GmbH & Company KG (majority owned by Intel Austria GmbH), Linz. Since 2018, he has been a part of the Christian Doppler Laboratory for Digitally Assisted RF Transceivers for Future Mobile Communications, Johannes Kepler University Linz. His current research interest includes the area of digital-intensive transceiver architectures.

Andreas Springer (Member, IEEE) received the Dr.Techn. (Ph.D.) and the Univ.-Doz. (Habilitation) degrees from Johannes Kepler University Linz (JKU), Austria, in 1996 and 2001, respectively. From 1991 to 1996, he was with the Microelectronics Institute, JKU. In 1997, he joined the Institute for Communications and Information Engineering, JKU, where he became a Full Professor in 2005. Since July 2002, he has been Head of the Institute for Communications Engineering and RF-Systems (formerly Institute for Communications and Information Engineering), JKU. He serves as a Research Area Coordinator for the Austrian K2 Center for Symbiotic Mechatronics. Since 2017, he has been the Co-Leader of the "Christian Doppler Laboratory for Digitally Assisted RF Transceivers for Future Mobile Communications." His current research interests include wireless communication systems, architectures and algorithms for multi-band/multi-mode transceivers, wireless sensor networks, and recently in molecular communications. In these fields, he has published more than 280 papers in journals and international conferences, one book, and two book chapters. He is a member of the IEEE Microwave Theory and Techniques, the Communications, and the Vehicular Technology societies, OVE, and VDI. In 2006, he was a co-recipient of the Science Price of the German Aerospace Center (DLR). From 2002 to 2012, he served as the Chair of the IEEE Austrian Joint COM/MTT Chapter. He was a member of the Editorial Board of the *International Journal of Electronics and Communications* (AEÜ) from 2012 to 2019, and serves as a reviewer for a number of international journals and conferences.

Mario Huemer (Senior Member, IEEE) received the Dipl.-Ing. and Dr.Techn. degrees from Johannes Kepler University (JKU) Linz, Austria, in 1996 and 1999, respectively. After holding positions in industry and academia, he was an Associate Professor with the University of Erlangen-Nuremberg, Germany, from 2004 to 2007, and a Full Professor at the University of Klagenfurt, Austria, from 2007 to 2013, where he served as the Dean of the Faculty of Technical Sciences from 2012 to 2013. In September 2013, he moved back to Linz, Austria, where he is currently heading the Institute of Signal Processing, JKU Linz, as a Full Professor. Since 2017, he is the Co-Head of the Christian Doppler Laboratory for Digitally Assisted RF Transceivers for Future Mobile Communications. His research interests include statistical and adaptive signal processing, signal processing architectures and implementations, as well as mixed signal processing with applications in information and communications engineering, radio frequency and baseband integrated circuits, sensor, and biomedical signal processing. Within these fields, he has published more than 270 scientific articles. He is a member of the IEEE Signal Processing Society, the IEEE Circuits and Systems Society, the IEEE Microwave Theory and Techniques Society, and the IEEE Communications Society, the ITG Germany, and the Austrian Electrotechnical Association (OVE). In 2000, he received the dissertation awards of the German Society of Information Technology (ITG) and the Austrian Society of Information and Communications Technology (GIT), the Austrian Cardinal Innitzer Award in natural sciences in 2010, and the German ITG Award in 2016. From 2009 to 2015, he was a member of the Editorial Board of the *International Journal of Electronics and Communications* (AEU), and he served as an Associate Editor for the IEEE Signal Processing Letters from May 2017 to April 2019.