Near-Optimal Decoding of Incremental Delta-Sigma ADC Output

Bo Wang, *Member, IEEE*, Man-Kay Law, *Senior Member, IEEE*, Samir Brahim Belhaouari, *Senior Member, IEEE*, and Amine Bermak, *Fellow, IEEE*

***Abstract*— This paper presents a nonlinear digital decoder (reconstruction filter) for incremental delta-sigma modulators. This decoder utilizes both the magnitude and pattern information of the modulator output to achieve accurate input estimation. Compared to the conventional linear filters with the same oversampling ratio (OSR), it can improve the converter's signal-to-quantization noise ratio by a few dB to a few 10's of dB with slight thermal noise performance degradation. Using the proposed decoder, the modulator's OSR can be a few times less while achieving the same resolution and data rate, thus minimizing the modulator as well as its peripheral circuits' energy consumption. In this paper, the proposed decoder is optimized for digital implementation, with its function being verified using a modulator prototype. This decoder is mainly designed for dc or near-dc signal conversions and it does not provide frequency notches.**

***Index Terms*— Reconstruction filter, incremental ADC, IDC, delta-sigma modulator, decimation filter, optimal filter, thermal noise averaging, noise penalty factor.**

I. Introduction

INCREMENTAL analog-to-digital converter (IDC), also known as charge-balancing delta-sigma ($\Delta\Sigma$) converter, has been widely used for low-bandwidth signal conversions since it was introduced in [1]. It enjoys the nature of achieving high resolution without precise analog elements matching and can be easily multiplexed between multiple input channels [2]. IDCs are particularly popular in instrumentation applications that require high conversion precision, such as high linearity, low offset, and precise gain [3]. Over the years, the energy-efficiency of IDC is continuously improving (e.g., from a Schreier FoM of 166.1 dB [4] to 185.8 dB [5]), while for emerging applications like passive sensing, IDCs with higher energy-efficiency are still being sought.

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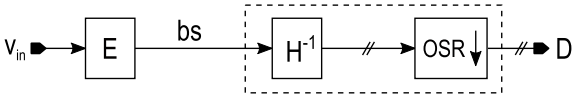

Fig. 1. Generic topology of an IDC, consisting an encoder E, and a digital decoder (a filter H^{-1} and a decimate-by-OSR operation).

As shown in Fig. 1, an IDC typically consists of an encoder ($\Delta\Sigma$ modulator or its variants) to convert the input signal into a fixed length of digital bitstream, followed by a decoder (reconstruction filter) to produce a multibit digital output. Till now, many encoder typologies were proposed, such as the classical high-order modulator [6], extended counting [7], zooming [8], loop-filter-order extension [9], linear-exponential conversion [10], etc. These encoders are nonlinear, ideally, their decoders should be nonlinear as well for best input reconstruction. Unfortunately, signal analysis tools such as impulse and frequency response cannot be applied to nonlinear filters, making them considerably difficult to be analyzed. Currently, most IDCs are using the linear cascade of integrator (CoI) filters or cascaded integrator-comb (CIC) filters (an implementation of the sinc filter [11]) for digital reconstruction because of their implementation simplicity and/or ability to reject periodic noise [12]. Noise-optimized linear filter has also been introduced [13], which is however difficult to be implemented on-chip as it requires multiply-accumulate operations using irregular filter coefficients stored in a memory.

Using linear filters, some information encoded in the modulator output is wasted. To address this issue, a nonlinear optimal decoding algorithm was developed in [14] and had been further elaborated in [15]. This algorithm can achieve the theoretically lowest mean square error (MSE) and minimum peak quantization error for a given oversampling ratio (OSR). For example, for a first-order modulator using one-bit quantizer, it requires only 98 cycles to achieve the same MSE as that of operating a digital integrator for 1024 cycles. It means one can operate the IDC with a 10.5 times slower clock. Pitifully, besides the use of area- and power-hungry digital multipliers, this algorithm cannot process the quantizer decision errors caused by circuit noise, making it more useful for theoretic estimation instead of practical implementations. In [16], a nonlinear iterative filter that can process noisy bitstream was developed for a first-order modulator. However,

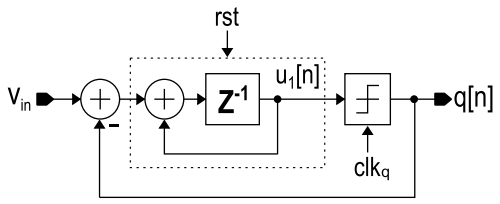

Fig. 2. Model of a first-order fully differential $\Delta\Sigma$ modulator with delaying integrator and 1-bit quantizer (signal scaling not shown).

implementing this algorithm on-chip is resource-demanding as it cannot start decoding until the whole bitstream sequence is ready. Moreover, its methodology cannot be applied in second- or higher-order modulators, not to mention it only improves the signal-to-quantization noise ratio (SQNR) of the system by 4.2 dB as compared to a sinc^2 filter.

In this paper, a nonlinear near-optimal decoder is proposed for IDCs with dc or near-dc signal conversions, such as a thermal sensor interface [17]. This decoder enjoys the benefits of quantization error reduction of optimal decoding and thermal noise averaging of linear filters. Depending on the adopted modulator topology and OSR, the proposed decoder can increase the converter's SQNR by a few dB to a few 10's of dB with slight thermal noise increase as compared to that of linear filters. Different from the other algorithmic decoders, the proposed one can be implemented on-chip efficiently. As a tradeoff, the proposed decoder occupies a larger area and has higher power consumption than most of its linear counterparts. This overhead is affordable as the area and power of the decoder is usually only a small fraction of its IDC core.

This paper is organized as follows. Section II introduces the operation of a first-order modulator and its optimal filtering. The proposed decoder is detailed in Section III. Section IV extends the analysis to a second-order modulator. Section V presents the digital implementation and verification of this decoder, followed by conclusions in Section VI.

II. Decoding of the First-Order Incremental $\Delta\Sigma$ Modulator Output

For clarity, if not specified, voltage signals in this paper are normalized to the IDC's reference signal V_{ref}, while signal powers are normalized to V_{ref}^2.

A. Modulator Operation

A typical first-order fully differential $\Delta\Sigma$ modulator with 1-bit quantizer is shown in Fig. 2. For simplicity, assuming the input $v_{\text{in}} \in [-1, 1]$ and stays constant within one A/D conversion. The comparison threshold of the quantizer is 0 and the quantizer output $q \in \{-1, 1\}$. The integrator is reset at the beginning of each conversion ($u_1[0] = 0$). Particularly, $q[0] = 0$ is used to disable the feedback during the first integration cycle. At the n^{th} quantization cycle, the integrator output $u_1[n]$ satisfies a discrete-time difference equation of

$$u_1[n] = u_1[n-1] + v_{\text{in}} - q[n-1], \quad n \geqslant 1. \tag{1}$$

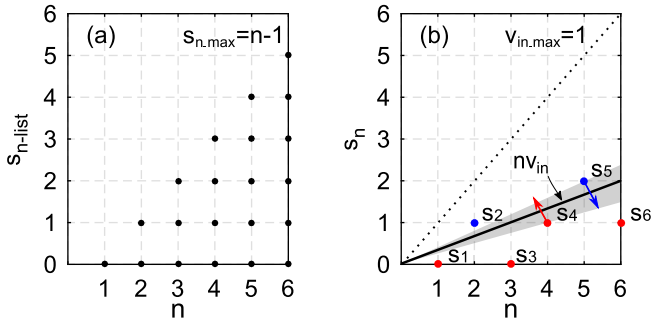

Fig. 3. (a) The upper half of a generic square lattice ($M = 6$ as an example); (b) modulated output $q = [1, -1, 1, 1, -1, 1]$ with $v_{\text{in}} = 1/3$.

After simplifying this recursive relationship, one can derive

$$u_1[n] = n \cdot v_{\text{in}} - \sum_{i=0}^{n-1} q[i] \triangleq n \cdot v_{\text{in}} - s_{\text{n}}, \quad n \geqslant 1, \tag{2}$$

where s_{n} is the running sum of $q[0]$ to $q[n-1]$. Assuming the OSR of the modulator is M (use this symbol interchangeably with OSR in this paper), $\{n \in \mathbb{Z}^+,\ 1 \leqslant n \leqslant M\}$ and $\{s_{\text{n}} \in \mathbb{Z},\ -n+1 \leqslant s_{\text{n}} \leqslant n-1\}$ will hold in (2). Since the quantizer is comparing $u_1[n]$ with 0, the digital output of the modulator is

$$q[n] = \begin{cases} 1 & v_{\text{in}} \geqslant s_{\text{n}}/n, \\ -1 & v_{\text{in}} < s_{\text{n}}/n, \end{cases} \quad n \geqslant 1. \tag{3}$$

Following (2)(3), an encoded output bitstream for any noiseless v_{in} can be derived.

The above encoding process can also be explained graphically using a square lattice [15]

$$L_{\text{n}} = \{(n, s_{\text{n-list}}) : n \in \mathbb{Z}^+, 1 \leqslant n \leqslant M\}, \tag{4}$$

where $s_{\text{n-list}}$ represents all the possible values of s_{n} at the n^{th} quantization cycle, with $s_1 = q[0] = 0$. For simplicity, Fig. 3(a) shows the upper half of such a square lattice. To encode an unknown input v_{in}, one can add a ramp of $n \cdot v_{\text{in}}$ to the lattice as in Fig. 3(b). According to (3), in each cycle, the modulator output is a result of comparing the slope of this ramp, which is v_{in}, to the slope of the line connecting dots (n, s_{n}) and $(0, 0)$, which is s_{n}/n. If the slope of the input ramp is larger or the position of the input ramp is above the lattice dot (n, s_{n}), $q[n] = 1$, and vice versa. Because $s_{\text{n+1}} = s_{\text{n}} + q[n] = s_{\text{n}} \pm 1$, the lattice dot to be compared at the $(n+1)^{\text{th}}$ cycle will be one lattice dot above or below that of the n^{th} cycle. For example, if $v_{\text{in}} = 1/3$, in the 1^{st} cycle, as $v_{\text{in}} > s_1/1 = 0$, $q[1] = 1$. In the 2^{nd} cycle, $v_{\text{in}} < s_2/2 = 1/2$, therefore $q[2] = -1$, and so on. Consequently, the sequence s_{n} forms an envelope to track the $n \cdot v_{\text{in}}$ ramp.

B. Prior Art: Optimal Decoding

Ideally, according to (3), if $q[n] = 1$, $v_{\text{in}} \geqslant lb[n]$ holds. Here $lb[n] = s_{\text{n}}/n$ can be viewed as a temporary lower bound (LB) of v_{in}. Similarly, if $q[n] = -1$, $v_{\text{in}} < ub[n]$ holds, and $ub[n] = s_{\text{n}}/n$ is a temporary upper bound (UB) of v_{in}. For $v_{\text{in}} \in [-1, 1]$, the initial bounds $lb[0] = -1$ and $ub[0] = 1$. By applying this property to the modulator

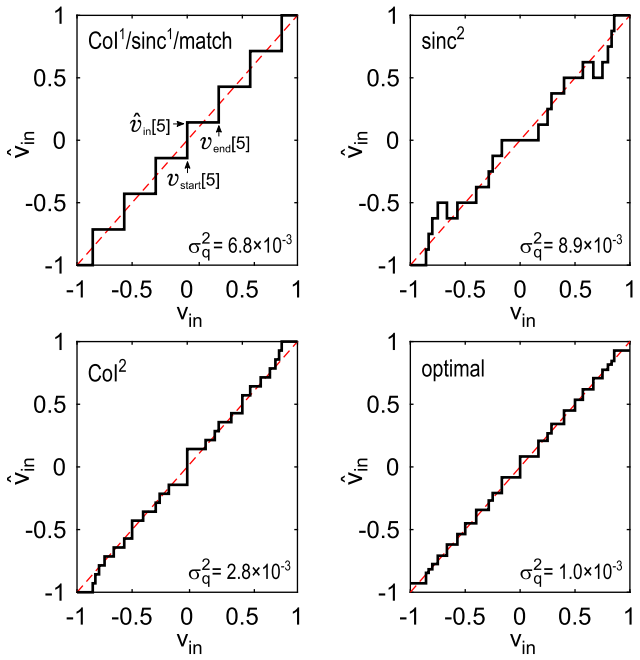

Fig. 4. First-order modulator output decoded using different filters at an OSR of 7 and a full-scale input range of ±1.

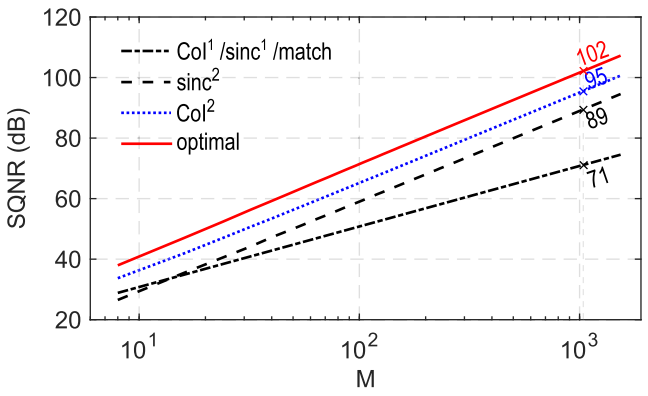

Fig. 5. SQNR of a first-order modulator decoded by different filters with a full-scale input range $V_{\rm FS} = 1$.

output, one can progressively refine the range of $v_{\rm in}$ and find out its maximum LB, $lb_{\max}$, and minimum UB, $ub_{\min}$. Graphically, this is equivalent to find the slopes of two lines connecting $(n, s_{\rm n})$ and $(0, 0)$ that can best bound the input ramp [see the grey region in Fig. 3(b)]. To obtain valid results, $\{lb[i] \leqslant ub[j],\ \forall i, j \in \mathbb{Z}_0^+\}$ must always hold. With this prerequisite, the optimal estimation of $v_{\rm in}$ is

$$\hat{v}_{\rm in} = \frac{1}{2}\left\{\min(ub[n]) + \max(lb[n])\right\}, \quad 0 \leqslant n \leqslant M. \tag{5}$$

For example, (6) shows how $\hat{v}_{\rm in}$ is obtained using this algorithm to decode the output of Fig. 3(b).

n	0	1	2	3	4	5	6
$q[n]$	0	1	−1	1	1	−1	1
$s_{\rm n}$	0	0	1	0	1	2	1
$ub[n]$	1	1	1/2	1/2	1/2	**2/5**	2/5
$lb[n]$	−1	0	0	0	**1/4**	1/4	1/6
$\hat{v}_{\rm in}$							13/40

(6)

Because this algorithm processes the modulator output with an inverse process of how it is encoded, for a given OSR, it can achieve the theoretically lowest MSE ($\sigma_{\rm q}^2$). The MSE measures the averaged quantization noise power and implies the overall accuracy of the system. As an example, Fig. 4 shows the decoded first-order modulator output at an OSR of 7. For performance benchmarking, outputs decoded by the popular linear filters, with their orders being equal or greater than the order of the modulator by one, are also added. The optimal filter achieves the lowest $\sigma_{\rm q}^2$ and does not suffer from gain or offset errors. For a uniformly distributed dc input, $\sigma_{\rm q}^2$ is calculated by

$$\begin{aligned}\sigma_{\rm q}^2 &= \frac{1}{2V_{\rm FS}}\int_{-V_{\rm FS}}^{+V_{\rm FS}} (v_{\rm in} - \hat{v}_{\rm in})^2 dv_{\rm in} \\ &= \frac{1}{6V_{\rm FS}}\sum_{i=1}^{N_{\rm step}} \left\{(v_{\rm end}[i] - \hat{v}_{\rm in}[i])^3 - (v_{\rm start}[i] - \hat{v}_{\rm in}[i])^3\right\}\end{aligned} \tag{7}$$

where $N_{\rm step}$ is the total number of quantized output steps within the input range of $\{-V_{\rm FS}, +V_{\rm FS}\}$; $v_{\rm start}[i]$, $v_{\rm end}[i]$, and $\hat{v}_{\rm in}[i]$ are the start, end, and decoded output of the $i^{\rm th}$ output, respectively. The peak SQNR of the system can be calculated by $10\cdot\log(4V_{\rm FS}^2/\sigma_{\rm q}^2)$ for dc inputs[1]. Fig. 5 shows the simulated SQNR at different OSRs. For example, at an OSR of 1024, the optimal filter achieves 31/7/13 dB higher SQNR than that of the $\text{CoI}^1/CoI^2/sinc^2$ filters, respectively.

C. Limitations of Optimal Decoding

One limitation of optimal decoding is it cannot suppress periodic noise. For many applications, this is a minor issue. More importantly, the integrator output u_1 is noisy affected by circuit thermal noise (low-frequency noise can be mitigated using the correlated double sampling technique). Therefore, the quantizer output often deviates from its ideal value. For linear filters, noisy bitstream does not hinder successful decoding. However, for optimal decoding, if noise-induced quantizer decision error happens, $\{lb[i] > ub[j],\ i, j \in \mathbb{Z}_0^+\}$ may occur, which violates its prerequisite. In this case, the output derived by (5) lost its physical meaning and becomes a poor input estimation. To apply optimal decoding in practical IDC designs, it must be improved to process noisy modulator outputs and be able to be implemented on-chip efficiently. This work utilizes the main features of optimal decoding while addressing this limitation [15].

III. Proposed Decoding Scheme

A. First-Order Modulator Output Decoding

To achieve high energy efficiency, high-resolution IDCs are mostly designed to be thermal noise limited. In this

[1]The crest-factor corrected SQNR is $10\cdot\log(V_{\rm FS}^2/2/\sigma_{\rm q}^2)$ to compare with general-purpose ADCs characterized using sinusoidal inputs [8].

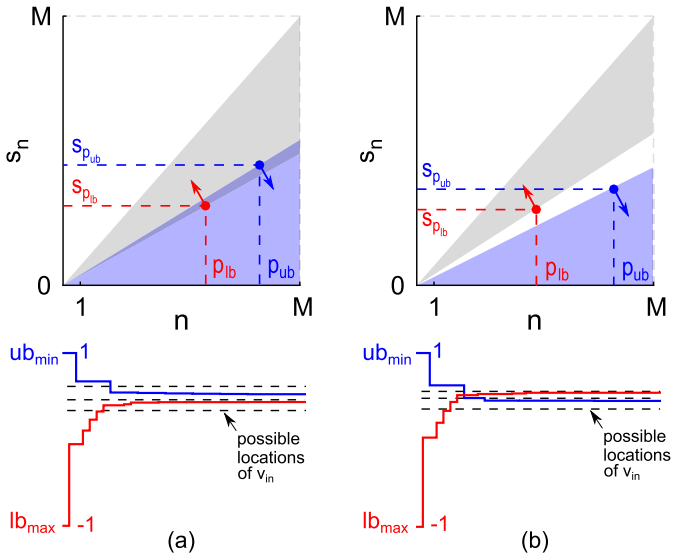

Fig. 6. Illuatration of the input bounds: (a) $lb_{\max} \leqslant ub_{\min}$; (b) $lb_{\max} > ub_{\min}$. The relative position of p_{lb} and p_{ub} is just an example.

case, assuming the input-referred thermal noise power of the modulator is $\sigma^2_{\text{t\_in}}$, $\sigma^2_{\text{t\_in}}/k_{\text{ave}} \gg \sigma^2_{\text{q}}$ must hold. Here k_{ave} is the effective thermal noise average cycle of the decoder and is the larger the better. Similar to [13], the thermal noise penalty factor is used to describe the thermal noise suppression capability of a filter compared to that of a uniform-weighted filter, which is equivalent to M/k_{ave}. Refer to Fig. 3(b), at the n^{th} integration cycle, the input ramp $n \cdot v_{\text{in}}$ follows a distribution of $\mathcal{N}(nv_{\text{in}}, n\sigma^2_{\text{t\_in}})$, whose noise content would induce erroneous quantizer outputs as compared to the ideal case. We can still follow Section II-B to calculate the input bounds $lb_{\max}$ and $ub_{\min}$. However, the actual v_{in} may not lie within the calculated bounds amid thermal noise influence. Fig. 6 shows the two possible scenarios after the bound calculation. Assuming $lb_{\max}$ and $ub_{\min}$ are derived at the conversion cycle p_{lb} and p_{ub}, respectively, the thermal noise power in $lb_{\max}$ and $ub_{\min}$ would be $\sigma^2_{\text{t\_in}}/p_{\text{lb}}$ and $\sigma^2_{\text{t\_in}}/p_{\text{ub}}$.

1) $lb_{max} \leqslant ub_{min}$: in this case, $lb_{\max}$ and $ub_{\min}$ still define a compliant region as shown in Fig. 6(a). Similar to that of optimal decoding, $(lb_{\max} + ub_{\min})/2$ is still a good input estimation. Considering the noise correlation in $lb_{\min}$ and $ub_{\max}$, thermal noise power in this estimation is

$$\sigma^2_{\text{t\_out}} = \frac{1}{4} \cdot [\frac{1}{p_{\text{lb}}} + \frac{1}{p_{\text{ub}}} + \frac{2}{\max(p_{\text{lb}}, p_{\text{ub}})}]\sigma^2_{\text{t\_in}}. \tag{8}$$

In thermal noise limited designs, the magnitude difference ($ub_{\max}$-$lb_{\min}$) is much smaller than the noise-induced magnitude shifts of $lb_{\max}$ and $ub_{\min}$ themselves. To simplify the decoder, one of the bounds, $lb_{\max}$ or $ub_{\min}$, whoever is derived at a larger quantization cycle can be used as the input estimation to allow greater thermal noise averaging. Therefore, the value of k_{ave} is $max(p_{\text{lb}}, p_{\text{ub}})$.

2) $lb_{max} > ub_{min}$: a more common scenario is shown in Fig. 6(b), in which $lb_{\max}$ and $ub_{\min}$ do not guard a meaningful region for $\hat{v}_{\text{in}}$. This happens frequently when large instantaneous noise injects into the modulator. The resulted bounds may be far from the actual input. In this case, $(lb_{\max} + ub_{\min})/2$ is not a physically meaningful nor accurate input estimation. To decode the modulator output, we also use the bound whoever experiences more quantization cycles as the input estimation, with

$$\hat{v}_{\text{in}} = \begin{cases} lb_{\max} & p_{\text{lb}} > p_{\text{ub}}, \\ ub_{\min} & p_{\text{lb}} < p_{\text{ub}}. \end{cases} \tag{9}$$

Thermal noise power in the output is

$$\sigma^2_{\text{t\_out}} = \frac{\sigma^2_{\text{t\_in}}}{\max(p_{\text{lb}}, p_{\text{ub}})}, \tag{10}$$

with k_{ave} being $max(p_{\text{lb}}, p_{\text{ub}})$. As a result, in both conditions of Fig. 6, the modulator output can be decoded successfully. It maximally maintains the low quantization noise of optimal decoding while providing good thermal noise averaging. Algorithm-1 summaries the operation of this decoder. This algorithm will not be affected by signal scalings used to limit the maximum integrator outputs in practical designs. Compared to linear filters, the overhead of this decoder is the extra digital comparison in each cycle, which will be optimized in Section V.

Algorithm 1 First-Order Modulator Output Decoding

```
input  : Output bitstream q of size 1 × M, q ∈ {−1, 1}
output : v̂in
initialize: lbmax ← −1, ubmin ←1, sn ←0, plb ←1, pub ←1
for n ← 1 to M do
    if q[n] = −1 then
        if sn/n ⩽ ubmin then  ubmin ← sn/n,  pub ← n
        else do nothing
    else
        if sn/n ⩾ lbmax then  lbmax ← sn/n,  plb ← n
        else do nothing
    end
    sn ← sn + q[n]
end
if plb > pub then v̂in ← lbmax
else v̂in ← ubmin
return : v̂in
```

B. Performance Analysis

1) Quantization Noise: as a trade-off for successful decoding, the proposed scheme cannot achieve the same performance as that of the optimal filter. However, because the bitstream is decoded by an inverse process of how it is encoded, no closer bounds than $lb_{\max}$ and $ub_{\min}$ can be derived. The proposed decoder uses one-side of the bounds as the input estimation, its output is therefore near-optimal in terms of quantization noise suppression. Fig. 7(a) shows the simulated SQNR of this scheme. At an OSR of 1024, it achieves 25/1/7 dB higher SQNR than that of using $\text{CoI}^1/CoI^2/sinc^2$ filters, respectively. Note that for a first-order modulator, the bitstream is not highly modulated thus the CoI^2 filter achieves a comparable performance to the proposed scheme. For higher-order modulators, the performance of the proposed decoder would far outweigh CoI filters as discussed in Section IV.

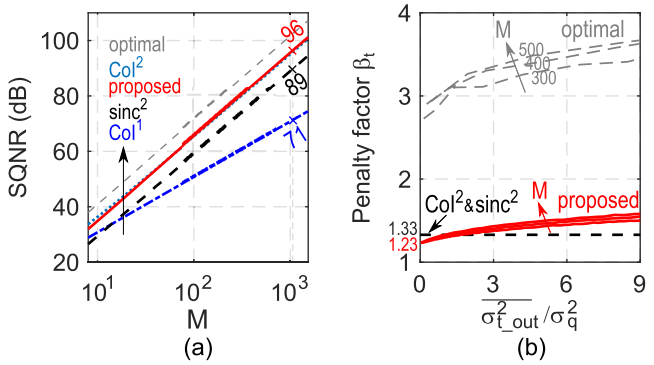

Fig. 7. (a) Simulated SQNR using different filters; (b) thermal noise penalty factor versus the averaged output thermal noise and quantization noise ratio.

2) Thermal Noise: the most important parameter to characterize the thermal noise performance of a decoder is its thermal noise penalty factor β_t. For a linear filter, assuming the filter weight of each bit is $\{w(i), i \in \mathbb{Z}^+, 1 \leqslant i \leqslant M\}$, its β_t is expressed as [10]

$$\beta_t = M \frac{\sum_{i=1}^{M} w(i)^2}{\left[\sum_{i=1}^{M} w(i)\right]^2}, \tag{11}$$

whose minimum value is 1 with uniform filter weight $w(i) \equiv 1$. Since the proposed decoder is nonlinear, statistical simulation is used to estimate its β_t. Fig. 7(b) shows the relationship between β_t and $\overline{\sigma^2_{t\_out}}/\sigma^2_q$ for different filters. Here $\overline{\sigma^2_{t\_out}}/\sigma^2_q$ is the averaged output thermal noise to quantization noise ratio of the IDC. When the IDC is quantization noise limited with $\overline{\sigma^2_{t\_out}} \ll \sigma^2_q$, the proposed decoder has a better β_t (1.23) than that of the sinc^2 and CoI^2 filters (1.33). With the increase of output thermal noise, β_t of the proposed decoder gradually degrades. This is because when thermal noise becomes large, the best p_{lb} and p_{ub} tend to be obtained at smaller quantization cycles thus less noise averaging can be achieved. For thermal noise limited modulators, $\overline{\sigma^2_{t\_out}}/\sigma^2_q$ can be designed to be 4∼9 without suppressing σ^2_q too much. In addition, β_t has a small dependency on OSR. If the required OSR exceeds 1000 using the proposed decoder, its β_t will be larger than 1.6 at $\overline{\sigma^2_{t\_out}} = 4\sigma^2_q$. In this case, the second-order modulator is a better choice as it provides the same noise penalty but a much higher SQNR. Note that for the optimal filter, its β_t is larger than 3, no net energy savings can be achieved even it has the lowest quantization noise.

An output thermal noise profile for different v_{in} (from -1 to 1 with a small simulation step of $2.7{\cdot}10^{-6}$) decoded using the proposed algorithm is shown in Fig. 8(a). In this example, the OSR used is 397, with $\sigma^2_{t\_in}$ being $1.6{\cdot}10^{-5}$ to ensure a thermal noise limited system. It shows that the output noise is uniform for the whole input range. The large spikes are simply because those inputs are at the edges of some large quantization step, which do not represent their real thermal noise contents. Fig. 8(b) shows the simulated output thermal noise for other OSR and $\sigma^2_{t\_in}$ combinations. As expected,

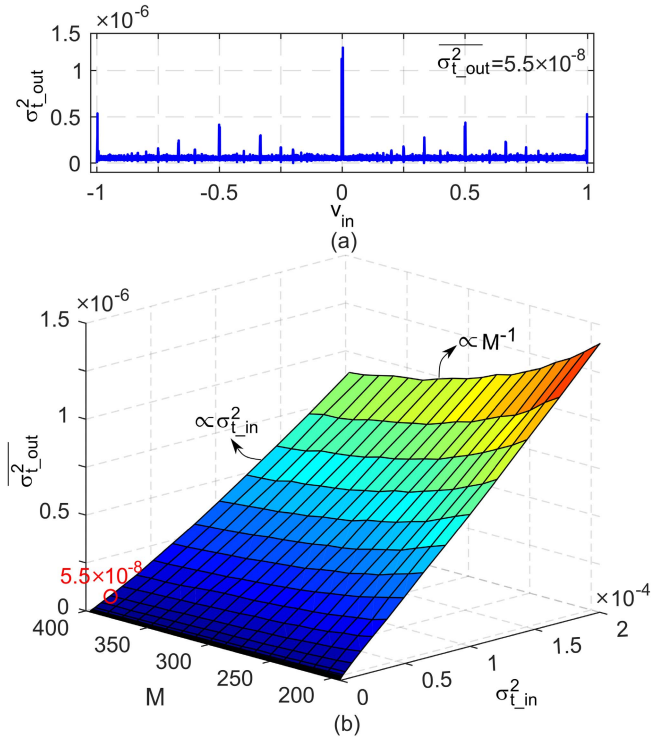

Fig. 8. (a) Output noise for different v_{in} at an OSR of 397 and $\sigma^2_{t\_in}$=1.6·10^{-5}; (b) averaged output thermal noise for different OSR and $\sigma^2_{t\_in}$ combinations using the proposed decoder.

TABLE I
REQUIRED OSR AND INPUT-REFERRED THERMAL NOISE TO ACHIEVE AN SNR OF 72 DB (1ST-ORDER MODULATOR WITH V_{FS}=1)

	sinc^1	sinc^2	CoI^2	**Proposed**
OSR	2570	467	290	**280**
$\sigma^2_{t\_in}$ †	$5.2{\cdot}10^{-4}$	$7.1{\cdot}10^{-5}$	$4.4{\cdot}10^{-5}$	**$4.0{\cdot}10^{-5}$**
Notches	Yes	Yes	No	**No**

†: Designed to be thermal-noise-limited with $\overline{\sigma^2_{t\_out}}/\sigma^2_q$ = 4.

$\overline{\sigma^2_{t\_out}} \propto \beta_t \cdot \sigma^2_{t\_in}/M$ holds when the IDC is thermal noise limited.

In practical design, for example, in order to achieve a peak signal-to-noise ratio (SNR, equals to $10{\cdot}\log[4V^2_{FS}/(\sigma^2_q+\sigma^2_{t\_out})]$ for dc inputs[2]) of 72 dB, Table I summarizes the required OSR and $\sigma^2_{t\_in}$ for different filters. The required OSR by the proposed decoder is the lowest. Since the noise penalty factor of optimal filter is too high, it is not suitable for practical design thus is not included in this table. Worthy to clarify that because the input-referred noise must decrease to meet the SNR requirement, energy consumed by the modulator cannot be reduced by using the proposed decoder. However, energy consumed by the peripheral circuits will decrease proportionally with OSR, like the digital controller, biasing, buffer, etc., which usually take more than half of the IDC's

[2]The crest-factor corrected SNR is $10{\cdot}\log[V^2_{FS}/2/(\sigma^2_q+\overline{\sigma^2_{t\_out}})]$ for general-purpose ADCs characterized using sinusoidal input.

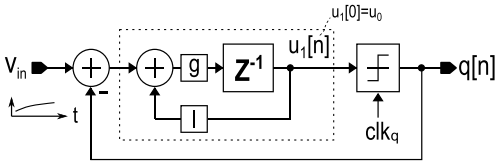

Fig. 9. Nonideal model of a first-order modulator.

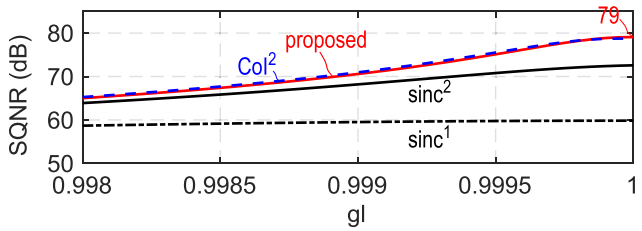

Fig. 10. Influence of integrator gain and charge leakage on the SQNR using different filters with M=280.

total energy (e.g., 52% [10]), not to mention the energy savings from the voltage reference and clock source.

C. Influence of Modulator Nonidealities

The above analysis assumes an ideal modulator model. In fact, the modulator in Fig. 2 suffers from various nonidealities (Fig. 9), including the non-zero initial condition u_0, non-unity gain $0 < g < 1$, and the integrator's slow charge leakage $0 < l < 1$ [18]. Considering these imperfections, (2) is revised to

$$u_1[n] = u_0(gl)^{\mathrm{n}} + g\frac{1-(gl)^{\mathrm{n}}}{1-gl}\cdot v_{\mathrm{in}} - g\sum_{i=1}^{n-1}(gl)^{\mathrm{n-1-i}}q[i] \triangleq \tilde{u}_0 + \tilde{r}_{\mathrm{n}}\cdot v_{\mathrm{in}} - \tilde{s}_{\mathrm{n}}, \quad 1 \leqslant n \leqslant M. \tag{12}$$

Though being computationally intensive, these imperfections can be calibrated if their values are constant. Otherwise, coefficient mismatches between the modulator and the digital filter would introduce gain and offset errors.

As in (12), the decoded output $\tilde{s}_{\mathrm{n}}/\tilde{r}_{\mathrm{n}}$ using the proposed decoder is sensitive to the product of g and l. Fig. 10 shows the simulated SQNR versus gl at an OSR of 280 (Table I). It shows that the proposed scheme has a comparable sensitivity to modulator imperfections as that of the CoI^2 filter. In modern technologies, the integrator charge leakage is almost negligible and l is close to 1. As long as a high gain op-amp is used for the integrator, SQNR drop caused by modulator imperfections is relatively small. For example, an op-amp gain of 80 dB corresponds to a g of 0.9999 and less than 1 dB SQNR drop. In (12), the decoded output also has an offset of $\tilde{u}_0/\tilde{r}_{\mathrm{n}}$. Using the same design parameters as above, an initial modulator residue signal of 0.01 introduces an offset of $35{\cdot}10^{-6}$, which can be handily calibrated out. Finally, different from the classial linear filters whose passband signal droop can be corrected, conversion error of the proposed decoder is larger for varying inputs and cannot be corrected. Therefore, it is more suitable for dc or near-dc signal conversions or converters with S&H. For varying inputs, the scheme in [19] can be explored.

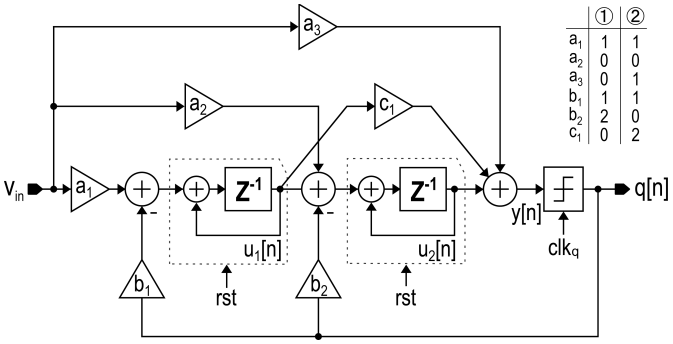

Fig. 11. Generic single-bit second-order $\Delta\Sigma$ modulator model, together with the modulator coefficients (without signal scaling) for ① the classical CIFB topology, and ② the CIFF structure.

IV. Higher-Order Incremental $\Delta\Sigma$ Modulator

The proposed decoder addressed the shortcoming of optimal filter for noisy modulator output processing, its performance is however only slightly better that of a CoI^2 filter when applied to the first-order modulator. In this section, a single-bit second-order modulator is used to further elaborate this decoder to show its superior performance for highly modulated bitstream decoding. A brief discussion on the application of this decoder on other modulator variants is also included.

A. Generic Second-Order $\Delta\Sigma$ Modulator

The generic model of a single-bit second-order $\Delta\Sigma$ modulator is shown in Fig. 11. The modulator coefficients of the classical and the cascaded integrator feed-forward structures are also listed. Using the same assumptions as in Section II-A, the discrete-time difference equations for the integrator output $u_1[n]$, $u_2[n]$, and the quantizer input $y[n]$ are

$$u_1[n] = a_1 v_{\mathrm{in}} + u_1[n-1] - b_1 q[n-1], \tag{13}$$

$$u_2[n] = a_2 v_{\mathrm{in}} + u_1[n-1] + u_2[n-1] - b_2 q[n-1], \tag{14}$$

$$y[n] = a_3 v_{\mathrm{in}} + c_1 u_1[n] + u_2[n], \quad n \geqslant 1. \tag{15}$$

Using (13)(14), (15) can be simplified to

$$y[n] = \left[a_1\frac{n(n-1)}{2} + (a_1c_1 + a_2)n + a_3\right]\cdot v_{\mathrm{in}} - \left[(b_1c_1 + b_2)\sum_{i=1}^{n-1} q[i] + b_1\sum_{k=1}^{n-1}\sum_{j=1}^{k-1} q[j]\right] \triangleq r_{\mathrm{n}}\cdot v_{\mathrm{in}} - s_{\mathrm{n}}, \quad n \geqslant 1, \tag{16}$$

where r_{n} is the effective input ramp coefficient and s_{n} is the lattice value at the n^{th} quantization cycle, with $r_0 = a_3$ and $s_0 = 0$. When $r_{\mathrm{n}} = 0$, no feedback will be applied and $q[n] = 0$. Otherwise, the operation of the quantizer follows

$$q[n] = \begin{cases} 1 & v_{\mathrm{in}} \geqslant s_{\mathrm{n}}/r_{\mathrm{n}}, \\ -1 & v_{\mathrm{in}} < s_{\mathrm{n}}/r_{\mathrm{n}}. \end{cases} \tag{17}$$

B. Digital Output Decoding

Based on (16)(17), the modulator output decoding using the proposed decoder is summarized in Algorithm-2. Similarly, both the amplitude and pattern information of the bitstream are

Algorithm 2 Second-Order Modulator Output Decoding

input : Output bitstream q of size $1 \times M$, $q \in \{-1, 0, 1\}$
output : $\hat{v}_{\text{in}}$
initialize: $lb_{\max} \leftarrow -1$, $ub_{\min} \leftarrow 1$, $r_{\text{n}} \leftarrow a_3$, $s_{\text{n}} \leftarrow 0$, inte1 $\leftarrow 0$, $p_{\text{lb}} \leftarrow 1$, $p_{\text{ub}} \leftarrow 1$
for $n \leftarrow 1$ **to** M **do**
  $r_{\text{n}} \leftarrow r_{\text{n}} + a_1(n-1) + (a_1c_1 + a_2)$
  if $q[n] = -1$ **then**
    if $s_n/r_n \leqslant ub_{\min}$ **then** $ub_{\min} \leftarrow s_{\text{n}}/r_{\text{n}}$, $p_{\text{ub}} \leftarrow n$
    else *do nothing*
  else
    if $s_n/r_n \geqslant lb_{\max}$ **then** $lb_{\max} \leftarrow s_{\text{n}}/r_{\text{n}}$, $p_{\text{lb}} \leftarrow n$
    else *do nothing*
  end
  $s_{\text{n}} \leftarrow s_{\text{n}} + (b_1c_1 + b_2) \cdot q[n] + b_1 \cdot$ inte1
  inte1 $\leftarrow$ inte1 $+ q[n]$
end
if $p_{\text{lb}} > p_{\text{ub}}$ **then** $\hat{v}_{\text{in}} \leftarrow lb_{\max}$
else $\hat{v}_{\text{in}} \leftarrow ub_{\min}$
return : $\hat{v}_{\text{in}}$

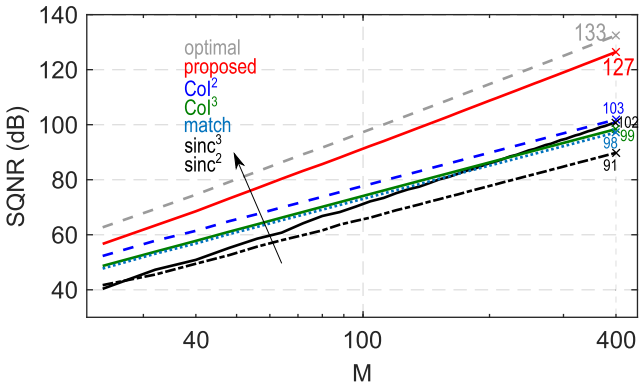

Fig. 12. Simulated SQNR of the classical single-bit second-order modulator using different filters with a full-scale input range $V_{\text{FS}} = 3/4$.

utilized to calculate the closest bounds to achieve quantization noise reduction, while the bound which experiences more quantization cycles is used as the final input estimation to allow sufficient thermal noise averaging. To characterize the proposed decoder quantitatively, the classical second-order structure is used in this paper. The simulated system SQNR using different filters is shown in Fig. 12. Because the modulator output is highly nonlinear, more information is encoded in the bitstream pattern. At an OSR of 400, the proposed decoder achieves 24/28/36/25/29 dB higher SQNR than that of the CoI^2/CoI^3/sinc^2/sinc^3/match filter, respectively. The CoI^3 filter has worse performance than that of the CoI^2 filter mainly because of its large non-linearity error when the input approaches $\pm V_{\text{FS}}$.

In terms of thermal noise suppression, Fig. 13 shows the penalty factor β_{t} of different filters versus $\sigma^2_{\text{t\_out}}/\sigma^2_{\text{q}}$. Compared to CoI filters that also do not provide signal notches, the proposed decoder achieves 14% lower β_{t} than that of CoI^3 filter, while 16% higher than that of CoI^2 filter. Considering its large quantization noise reduction, this thermal noise performance

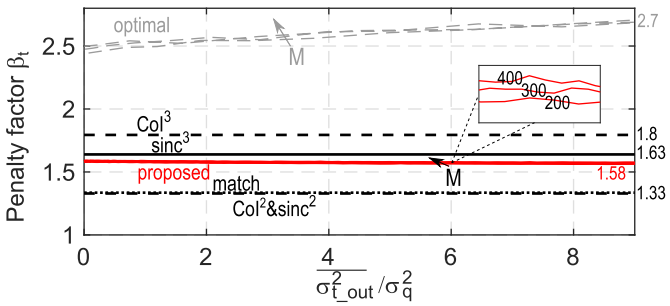

Fig. 13. Thermal noise penalty factors of different filters versus the averaged output thermal noise and quantization noise ratio.

TABLE II
REQUIRED OSR AND INPUT-REFERRED THERMAL NOISE TO ACHIEVE AN SNR OF 90 dB (2ND-ORDER MODULATOR WITH $V_{\text{FS}} = 3/4$)

	sinc^2	sinc^3	CoI^2	CoI^3	Match	**Proposed**
OSR	570	320	285	345	370	**120**
$\sigma^{2\dagger}_{\text{t\_in}}(\cdot 10^{-7})$	7.7	3.5	3.1	3.5	5.0	**1.4**
Notches	Yes	Yes	No	No	No	**No**

†: Designed to be thermal-noise-limited with $\overline{\sigma^2_{\text{t\_out}}}/\sigma^2_{\text{q}} = 4$.

degradation is very mild. Meanwhile, different from that of a first-order modulator, β_{t} has smaller dependencies on $\overline{\sigma^2_{\text{t\_out}}}/\sigma^2_{\text{q}}$ and OSR. This is because the comparison thresholds $s_{\text{n}}/r_{\text{n}}$ in (17) decrease quadratically with n, one of the best bounds, p_{lb} or p_{ub}, are mostly derived at larger quantization cycles despite of thermal noise influence. As a design example, Table II summarizes the required OSR and $\sigma^2_{\text{t\_in}}$ for different filters to achieve an SNR of 90 dB. Compared to linear filters, the required OSR of the proposed decoder is 2.4∼4.7 times less. More savings could be achieved when the target SNR is higher.

C. Other Modulator Variants

Without loss of generality, the proposed decoding scheme can also be applied to other modulator topologies, such as single-ended, multi-bit, or higher-order ones. Considering the digital complexity, it is preferred to be used for modulators with pure differential noise transfer functions (NTF). Meanwhile, as the proposed decoder performs better for heavily modulated outputs, for a multi-bit first-order modulator, its performance is still only slightly better than that of the CoI^2 filter as in Section III-B. For second- or higher-order modulators, the proposed decoder mandates an OSR $\geqslant 20$ to outweigh the performance of linear filters and the larger OSR is used, the higher SQNR improvement can be achieved.

For example, for a second-order modulator with a 5-level quantizer and an OSR of 256, the proposed decoder achieves 24/9.5/37/26/34 dB higher SQNR than that of the CoI^2/CoI^3/sinc^2/sinc^3/match filters, respectively. For a third-order CIFF modulator with a pure differential NTF and a 17-level quantizer, at a moderate OSR of 128, the proposed decoder achieves 17/7.5/43/35/30 dB higher SQNR than that of the CoI^3/CoI^4/sinc^3/sinc^4/match filters, respectively.

The noise penalty factor of this decoder is 1.95, which is also lower than that of the CoI^4 filter being 2.3. Note that the performance improvement for a third-order modulator is only 2 dB in [13].

V. Digital Implementation

In this section, the proposed digital decoder will be optimized and then implemented in a standard CMOS process, followed by its performance verification using the output bitstream of a second-order modulator prototype. Discussion on the practical applicability of this decoder is also included.

A. Optimization for CMOS Design

1) Unsigned Operations: for fully differential modulators, q is signed as in (3)(17) (in practical design, the comparator output *low* represents -1), which increases the overhead of the proposed decoder because signed addition, division, and comparison operations are needed. To avoid signed operations, a simple constant shift by adding "1" to q can be performed (except for $q = 0$) to make it unsigned. To maintain the validation of Algorithm-1 and Algorithm-2, they must be modified accordingly.

For the first-order modulator, the original decoded output is expressed in the form of s_n/n, with n being $max(p_{lb}, p_{ub})$ and s_n defined in (2). After the shift of q, it becomes $(s_n+n-1)/n$, which adds a nonlinear content to the output as n is not constant. In this case, the initial s_n (s_0) is modified to be "1" and the decoded output is $s_n/n+1$, which up shifts the real output by "1" and can be easily corrected. For example, the output derived in (6) will be 53/40 instead of 13/40.

For the classical second-order modulator, its decoded output is expressed in the form of s_n/r_n, with s_n and r_n defined in (16). After shifting q, it becomes $[s_n + (n-1)^2]/r_n$, which deviates far from the original output. Because $r_n = n(n-1)/2$, in Algorithm-2, an extra term $(n-1)$ can be added to s_n. Then, $[s_n+(n-1)+(n-1)^2]/r_n = s_n/r_n+2$, which adds a constant dc shift of "2" to the real output and can also be corrected. As a result, no signed operations are required to implement the proposed decoder.

2) Simpler Multiplications: after the above shift of q, a new lb_{max} (ub_{min}) might be produced whenever $q[n] = 2$ ($q[n] = 0$). For example, assuming lb_{max} is temporarily derived at a quantization cycle p_{lb}. For an output sequence $\{q[p_{lb}], \ldots, q[n], n > p_{lb}\}$ of $\{2, \ldots, 2\}$, we need to verify whether $q[n]$ will generate a larger lb_{max}. For the first-order modulator, we can check if

$$\frac{s'_n}{n} \geqslant \frac{s'_{plb}}{p_{lb}}, \tag{18}$$

where $s'_n = s_n + n$ after the shift of q. (18) requires digital division and comparison and is quite resource-hungry, especially when the OSR is large. Because $n, p_{lb} \geqslant 1$, the above inequality can be simplified to

$$(s'_n - s'_{plb}) \cdot p_{lb} \geqslant s'_{plb} \cdot (n - p_{lb}), \tag{19}$$

which is more hardware-friendly than that of (18) since it deals with smaller numbers [14]. For the second-order modulator (Algorithm-2), the simplified governing inequality is

$$(s'_n - s'_{plb}) \cdot r_{plb} \geqslant s'_{plb} \cdot (r_n - r_{plb}), \tag{20}$$

where $s'_n = s_n + n(n-1)$ after the shift operation of q and r_n is defined in (16). Similar analysis can be applied to check whether a smaller ub_{min} can be generated by $q[n]$ with an output sequence $\{q[p_{ub}], \ldots, q[n], n > p_{ub}\}$ of $\{0, \ldots, 0\}$.

After the above optimization, the decoder for the classical single-bit differential second-order modulator is attached in the Appendix. For single-ended modulators, its implementation is easier as the optimization in Section V-A-1 is not required.

TABLE III
Synthesized Silicon Area and Simulated Power Consumption of Different Digital Filters

	Area (mm^2)	Power† (μW)	$f_{sys}{}^\dagger$ (kHz)
sinc^2	0.015	1.2	28.5
sinc^3	0.026	0.61	16.0
CoI^2	0.007	0.21	14.3
CoI^3	0.010	0.30	17.3
Match	0.012	0.45	18.5
Proposed	**0.044**	**0.88**	**6.0**

†: At an example data rate of 50 Sa/s. The power consumption increases linearly with data rate.

B. CMOS Implementation

For performance comparison, different filters for the classical second-order modulator are implemented in a standard 0.18 μm CMOS process. Table III lists their synthesized active silicon areas. Their power consumptions to achieve an SNR of 90 dB (Table II) and a data rate of 50 Sa/s are also listed as an example. Note that to achieve the same data rate, the system clock frequencies f_{sys} used for these filters are proportional to their required OSRs (50×OSR Hz). In terms of silicon area, the proposed decoder is 2.9/1.7/6.3/3.8/4.6 times as that of the sinc^2/sinc^3/CoI^2/CoI^3/match filters, respectively. In terms of power consumption, the proposed decoder is 26% less than sinc^2 filter thanks to its reduced clock speed. Compared to the other counterparts, its power is higher due to the increased gate counts. Usually, the power (also area) of the digital decoder is only a small fraction of its IDC core, making the overhead of the proposed decoder negligible compared to the system savings resulted from a slower clock.

C. Experimental Verification

The digital output of a second-order single-bit incremental $\Delta\Sigma$ modulator prototype is used to verify the proposed decoder. This modulator is fabricated in a standard 0.18 μm CMOS process, occupying an area of 0.15 mm^2 (Fig. 14). At a sampling frequency of 20 kHz, the whole system draws 1.1 μW from a 1.8 V supply.

Because the proposed decoder is only usable for dc or near-dc signal conversion, a slow stepped ramp test driven by

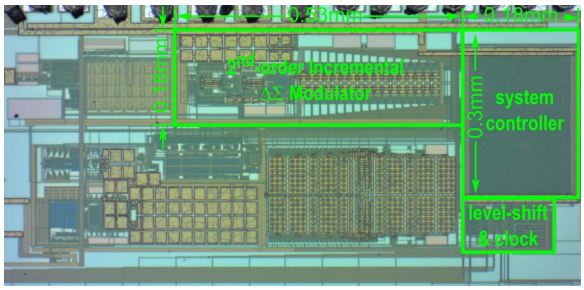

Fig. 14. Second-order modulator prototype.

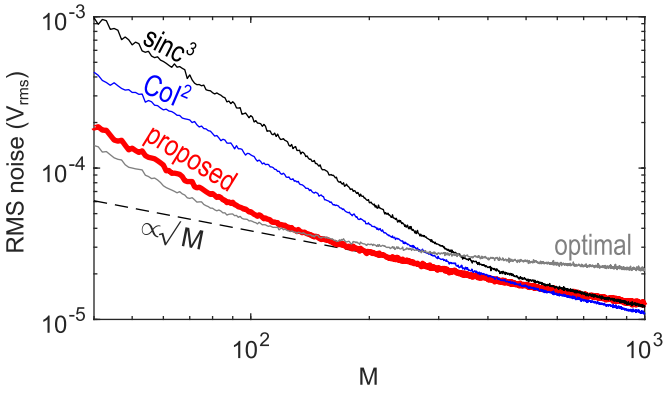

Fig. 15. Measured rms noise of the IDC at different OSRs. The conversion cycles required to reach a thermal-noise-limited state are around 350/300/150 for the sinc^3/CoI^2/proposed decoder, respectively.

a precision digital-to-analog converter is performed (8 samples per input) [20]. The input-referred rms noise using the best linear filters (CoI^2 and sinc^3 for a second-order modulator), the optimal filter, and the proposed decoder are measured as shown in Fig. 15. As expected, the proposed decoder requires at least 2× less OSR than the linear filters to suppress the quantization error and turn the converter into its thermal noise limited region. At an OSR of 150, the proposed decoder achieves a thermal-noise-limited noise of 31 μV_{rms}. Meanwhile, the 63 μV_{rms} and 102.1 μV_{rms} noise of the CoI^2 and sinc^3 filters are dominated by quantization noise. As a result, an SNR improvement of 6.1 dB and 10.3 dB can be achieved by using the proposed decoder as compared to the CoI^2 and sinc^3 filters, respectively. Although the optimal filter shows a superior performance for quantization noise suppression as in Fig. 15, its large thermal noise penalty limits its application. Using the proposed decoder, as shown in Fig. 16(a)(b), the output noise profile are quite uniform since there's no large quantization step in this second-order modulator. The end-point INL of the modulator (maximum 0.25 LSB) shown in Fig. 16(c) indicates that the proposed decoder maintains high system linearity. Unfortunately, a direct comparison with other literature is not that straightforward. As discussed in Section III-C, the main energy savings using the proposed decoder is from the IDC's peripheral circuits (reference, clock, bias, controller, buffer, etc.), whose data are seldom disclosed. Based on the analysis and testing, this saving can be a few times depending on the IDC's resolution.

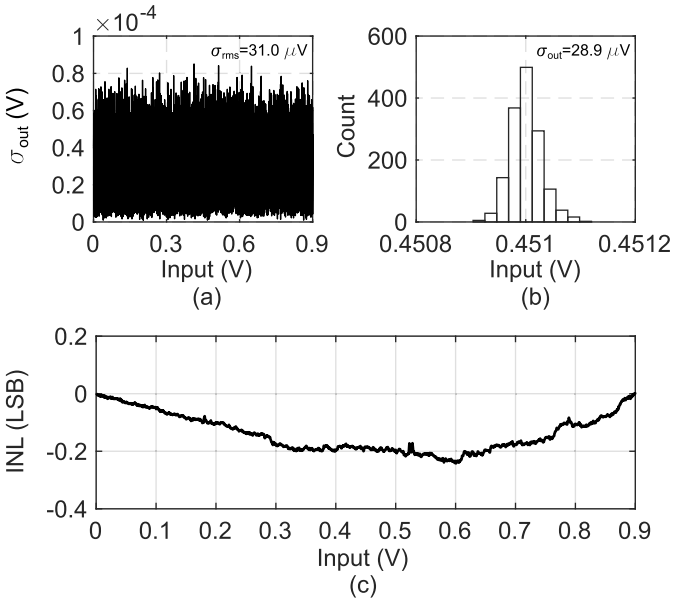

Fig. 16. Using the proposed decoder and at an OSR of 150, (a) noise profile at different inputs; (b) decoded output distribution for a constant input; (c) modulator integral nonlinearity for a 13-bit resolution.

D. Discussion

To sum up, in practical designs, if the digital filter must provide signal notches, the best option is still the CIC filters at the cost of higher OSR thus lower energy efficiency. If no periodic noise suppression is required, CoI filter and the proposed decoder are the candidates. For a first-order modulator, since its output is not highly modulated, CoI filter outweighs for its simpler implementation. For second-order, higher-order, or other modulator variants with their output bitstream being highly modulated, the proposed decoder achieves a significant SQNR improvement compared to that of CoI filters. Meanwhile, the proposed decoder can even achieve better thermal noise suppression than some CoI filters, making it a better choice for energy-efficient designs. The proposed decoder is optimized for digital design in this paper and it can be handily implemented on-chip. The main disadvantage is its nonlinear characteristics, more numerical simulations are needed to determine the OSR and noise requirements during design. Meanwhile, the proposed decoder is more suitable for dc or near-dc signal conversions or converters with S&H due to its large conversion error for varying inputs.

VI. Conclusion

A nonlinear near-optimal decoder for incremental delta-sigma modulator has been presented. By utilizing the advantages of optimal decoding as well as the conventional linear filters, both quantization noise reduction and thermal noise averaging can be achieved. For heavily modulated output (higher-order modulator), the near-optimal decoder can improve the system SQNR by a few dB to a few tens of dB with slight thermal noise performance degradation. The proposed decoder is optimized for digital implementation in this paper.

APPENDIX

The optimized decoder for the classical single-bit second-order modulator is shown in Algorithm-3, which can be easily implemented in VHDL or Verilog for digital synthesis.

Algorithm 3 Optimized 2nd-order IDC Output Decoding

input : Output bitstream q of size $1 \times M$, $q \in \{-1, 0, 1\}$
output : s_o, r_o
initialize: $s'_n \leftarrow 0$, $s'_{plb} \leftarrow 0$, $s'_{pub} \leftarrow 0$, $r_n \leftarrow 0$, $r_{plb} \leftarrow 0$, $r_{pub} \leftarrow 0$, $p_{lb} \leftarrow 1$, $p_{ub} \leftarrow 1$, inte1 $\leftarrow 0$, inte2 $\leftarrow 0$
for $n \leftarrow 1$ **to** M **do**
  $r_n \leftarrow r_n +$ inte1
  if $(q[n] + 1) = 0$ **then**
    if $(s'_n - s'_{pub}) \cdot r_{pub} \leqslant s'_{pub} \cdot (r_n - r_{pub})$ **then**
      $s'_{pub} \leftarrow s'_n$, $r_{pub} \leftarrow r_n$, $p_{ub} \leftarrow n$
    else *do nothing*
  else
    if $(s'_n - s'_{plb}) \cdot r_{plb} \geqslant s'_{plb} \cdot (r_n - r_{plb})$ **then**
      $s'_{plb} \leftarrow s'_n$, $r_{plb} \leftarrow r_n$, $p_{lb} \leftarrow n$
    else *do nothing*
  end
  $s'_n \leftarrow s'_n + 2 \cdot (q[n] + 1) +$ inte1 + inte2
  inte1 $\leftarrow$ inte1 $+ (q[n] + 1)$
  inte2 $\leftarrow$ inte2 $+ 1$
end
if $p_{lb} > p_{ub}$ **then** $s_o \leftarrow s'_{plb}, r_o \leftarrow r_{lb}$
else $s_o \leftarrow s'_{pub}, r_o \leftarrow r_{ub}$
return : s_o, r_o
$*$off-chip-calculation: $\hat{v}_{in} = s_o / r_o - 2$

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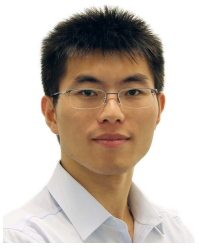

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