# A Mismatch Calibration Technique for SAR ADCs Based on Deterministic Self-Calibration and Stochastic Quantization

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***Abstract*— A capacitive DAC is an important building block of a charge-redistribution SAR ADC, for its size has a significant impact on performance. For medium- to high-resolution applications, the size of the DAC is typically determined by random mismatches. As such, an effective mismatch calibration circuit can allow the DAC to be scaled down to a much lower $kT/C$ noise limit, thereby increasing the overall ADC power efficiency. This paper reviews some of the most important reported mismatch calibration techniques and proposes a foreground calibration method based on a deterministic self-calibration and stochastic quantization. This approach is experimentally validated on a prototype 10-bit SAR ADC fabricated in TSMC 28-nm LP CMOS technology, demonstrating an INL and SFDR improvement of respectively 6.4 LSB and 14.9 dB at 85 MS/s.**

***Index Terms*— SAR analog-to-digital converter (ADC), mismatch calibration, stochastic, capacitive DAC, Gaussian process.**

## I. Introduction

THE successive-approximation register (SAR) ADC has been a particularly attractive candidate for applications where high speed and medium-to-high resolution are desired. This ADC architecture is known for its superior energy efficiency, small occupied chip area, and good compatibility with digital logic, and can be easily scaled to new CMOS technology nodes. Amongst all of the building blocks of a single-channel charge-redistribution SAR ADC, the capacitive digital-to-analog converter (CAP-DAC) deserves the most attention for two reasons. Firstly, the linearity of the SAR ADC is mainly determined by the linearity of the CAP-DAC. Secondly, the CAP-DAC not only causes a significant part of the dynamic power consumption, but also directly determines the $kT/C$ noise power, the input capacitive load of the ADC and the size of the driving and sampling switches. Although a small DAC unit capacitance is beneficial, it comes at the cost of a larger random mismatches between capacitors. If one could employ an effective mismatch calibration circuit, the size of the capacitive DAC could be kept as small as dictated by the $kT/C$ noise limit. This underlines the importance of an effective mismatch calibration for the SAR ADC.

This paper focuses on mismatch calibration techniques for the CAP-DAC in a SAR ADC by reviewing some of the most effective techniques described in literature and by proposing a hybrid mismatch calibration method based on self-calibration and stochastic quantization, which requires no prior knowledge of any of the ADC blocks and is fully automated. This foreground calibration detects the mismatch error in the analog domain and the correction is carried out in the digital domain.

Section II reviews the literature on mismatch calibration schemes. Section III proposes a stochastic mismatch calibration method and Section IV briefly explains the design details of the prototype ADC in which this calibration method is employed. Measurement results are given in Section V.

## II. Mismatch Calibration Techniques

In this section, we review some of the most important mismatch calibration techniques proposed in the literature. In particular, we concentrate on the *mismatch* resulting from the inherent random variation in capacitance values that build up in a capacitive DAC. All of the mismatch calibration methods discussed here can be used to compensate for this effect, although some may be also employed for other types of mismatch in the A/D converter.

A mismatch calibration process typically consists of two phases: a *detection* phase, where the error (i.e. capacitive mismatch) is determined in the form of an electrical quantity (e.g. voltage) in the analog domain or as a binary number in the digital domain, and a *correction* phase, where this detected error is used to correct the erroneous output.

### A. Detection

The mismatch detection process can occur in the *background* without interrupting the normal conversion of the

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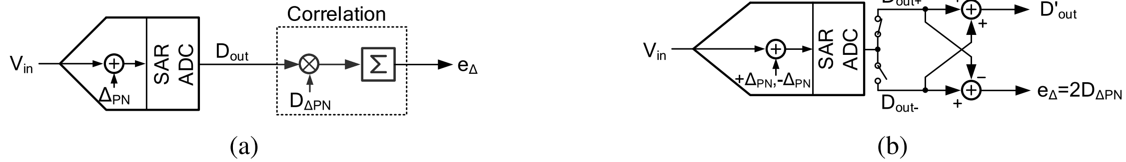


Fig. 1. Block diagram of the perturbation-based calibration with: (a) correlation, (b) dual-conversion.

ADC, or in the foreground upon the start-up of the chip and before the ADC conversion kicks off. Before we proceed and for the sake of clarification for the rest of this article, we define the term *bit weight* as the numerical weight of a particular bit of the binary output of the ADC, which is basically the (normalized) value of the capacitor(s) in the DAC that would contribute to that specific bit during the conversion process. Therefore, the output of an $N$-bit ADC can be represented by

$$y = \sum_{i=0}^{N-1} b_i w_i, \tag{1}$$

where $B = \{b_{N-1}, b_{N-2}, \ldots, b_1, b_0\}$ is the binary output and $W = \{w_{N-1}, w_{N-2}, \ldots, w_1, w_0\}$ is the bit weight vector.

*1) Background: Perturbation-based* calibration (also known as *dithering*) is a common method for error detection in an ADC. This technique is widely used to calibrate non-idealities of pipeline ADCs and can also be used with the SAR architecture to calibrate the mismatch of the CAP-DAC. This approach is based on injecting discrete-time single-bit zero-mean *pseudorandom noise* (PN) samples, $\Delta_{\text{PN}}$, into the ADC along with the analog input signal $V_{\text{in}}$, and using this as a way to estimate the actual bit weights of the capacitive DAC. In the ideal case where the ADC is perfectly *linear*, i.e. the bit weights that are used to reconstruct the output precisely match the actual bit weights in the DAC, superposition can be used to express the ADC output as

$$\begin{aligned} D_{\text{out}} &= Q(V_{\text{in}} + \Delta_{\text{PN}}) = Q(V_{\text{in}}) + Q(\Delta_{\text{PN}}) \\ &= D_{\text{in}} + D_{\Delta_{\text{PN}}}, \end{aligned} \tag{2}$$

where $D_x = Q(V_x)$ denotes the quantized representation of voltage $V_x$. The second equal sign in Eq. (2) holds if $D_{\text{in}}$ is completely independent from (uncorrelated with) $D_{\Delta_{\text{PN}}}$. On the other hand, when the bit weights of the DAC are mismatched with respect to their ideal values, the system is not linear and (2) no longer holds. In this case, the *correlation* between $D_{\text{out}}$ and $D_{\Delta_{\text{PN}}}$ can be exploited to extract the mismatched bit weights, as shown in Fig. 1(a). The PN signal $\Delta_{\text{PN}}$ is usually injected via an extra capacitor added to the capacitive DAC [1] or by using the capacitors in the DAC itself [2], [3].

Reference [1] proposed a *dual-conversion* approach where each sample is converted twice, once with a positive sign of the PN signal and once with the negative sign, as shown in Fig. 1(b). In this figure, $D_{\text{out}+}$ and $D_{\text{out}-}$ are the ADC outputs corresponding to PN signals $\Delta_{\text{PN}+}$ and $\Delta_{\text{PN}-}$, respectively. The difference between the outputs of the two conversions is then used for the bit weight extraction. This approach has an advantage in that the unknown input signal is subtracted from the calibration path, thus making it unnecessary to accumulate a large number of data. However, each conversion needs to be performed twice, hence halving the maximum achievable conversion rate of the ADC.

The bit weight extraction can be performed in various ways. One way is to use an adaptive loop. As shown in Fig. 2, a least-mean-square (LMS) weight updater can be used to adjust the reconstruction bit weights $W$, until the error term $e_\Delta = E\,[D_{\text{out}} \cdot D_{\Delta PN}]$, where $E\{\cdot\}$ is the averaging operator, becomes zero, indicating that $W$ matches the actual bit weights of the DAC. In order to work out all the $N$ bit weights $W = \{w_{N-1}, w_{N-2}, \ldots, w_0\}$, where $N$ is the resolution of the ADC, the LMS can update all of the bit weights at the same time [4] as

$$w_i(k+1) = w_i(k) - \mu e_\Delta(k), \quad (i = 0, 1, ..N-1). \tag{3}$$

In order to reduce the conversion time of the LMS procedure, [5] used $N$ different PN signals to determine the bit weights separately yet simultaneously.

Bit weight extraction can also be done directly without using an LMS approach [2], [3]. To elaborate, let us denote $C_0 \sim C_{N-1}$ as the capacitors of the DAC in the SAR ADC and $w_0 \sim w_{N-1}$ as their (normalized) corresponding weights. Let us also assume that capacitor $C_j$ is used to add the PN signal through a $\{1, -1\}$ pseudorandom sequence $K$ along with the input signal $V_{\text{in}}$. The operation of the SAR ADC is then described by

$$V_{\text{in}} + K w_j = \sum_{i=0, i\neq j}^{N-1} b_i w_i + V_q, \tag{4}$$

where $V_q$ is the quantization error. The digital representation of (4) is

$$D_{\text{in}} + K w_{Dj} = \left( \sum_{i=0, i\neq j}^{N-1} b_i w_{Di} \right) + D_q. \tag{5}$$

By correlating (5) with $K$, we have

$$\sum_{i=0, i\neq j}^{N-1} \overline{K b_i} w_{Di} = w_{Dj} + \overline{K D_{\text{in}}} - \overline{K D_q} = w_{Dj} + e_j \tag{6}$$

where $e_j = \overline{K D_{\text{in}}} - \overline{K D_q}$ is an error term. By running this procedure for the $m$ MSB capacitors, we can get $m$ equations similar to (6), which can then be written in a matrix form as

$$A \times \begin{bmatrix} w_{D(N-1)} \\ w_{D(N-2)} \\ \vdots \\ w_{D(N-m+1)} \end{bmatrix} = C - \begin{bmatrix} e_{N-1} \\ e_{N-2} \\ \vdots \\ e_{N-m+1} \end{bmatrix}, \tag{7}$$

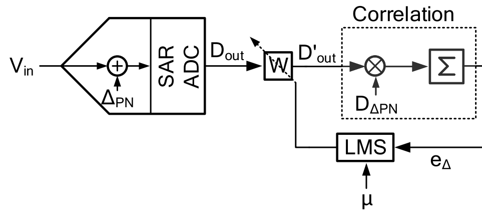


Fig. 2. Bit-weight extraction of the perturbation-based calibration through an LMS algorithm.

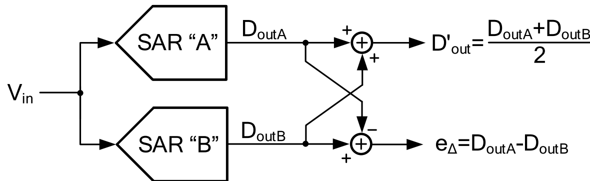


Fig. 3. Split ADC calibration method.

where $A$ and $C$ are matrices which depend on the correlation between $K$'s, $b_i$s and the bit weights of the LSB capacitors. With a sufficiently long PN sequence, the error terms $e_j$'s converge to zero. Therefore, (7) can be solved to determine the mismatched bit weights $\{w_{D(N-1)}, w_{D(N-2)}, \ldots, w_{D(N-m+1)}\}$.

Ref. [6] proposed a *split ADC* approach where the capacitor array of the SAR ADC was split into two identical banks and performed two SAR conversions at the same time, as shown in Fig. 3. The average of the outputs of the two conversions is taken as the final output, while the difference could be used to calibrate the bit weights, e.g. via an adaptive loop similar to that in Fig. 2. It is worth noting that the difference between the outputs of the two conversions in Fig. 3 could be zero even when the two paths still exhibit a mismatch. To circumvent this, [6] also employed a "shuffling" technique for the capacitive array where different unit capacitors were used for different bits in every conversion in a randomized manner. This guarantees the independence of the two conversions and can force $e_\Delta$ to zero only if the mismatch is zero. Nonetheless, this approach leads to a very complex connection web between the capacitors in the layout, thereby jeopardizing the conversion speed of the ADC.

In another method, [7] took advantage of *redundancy* for mismatch calibration and made use of the fact that in a SAR ADC with redundancy, multiple codes can result in the same final output. We make this clear by considering an 8-bit SAR ADC as an example, whose (normalized) bit weights are $W = \{128, 64, 32, 32, 16, 8, 4, 2, 1\}$. Note that the 4$^{\text{th}}$ bit is *redundant*, and its weight is the same as the 3$^{\text{rd}}$ bit. Therefore, the two 9-bit codes $B_1 = \{1, 0, 0, 0, x, x, x, x, x\}$ and $B_2 = \{0, 1, 1, 1, x, x, x, x, x\}$ both represent the same digital output if the ADC is linear, i.e. there is no mismatch in the MSB capacitor. This allows the mismatch of the MSB capacitors before the redundant capacitor to be detected as follows. Whenever code $B_1$ appears at the output of the ADC during a normal conversion, the ADC undergoes an extra 10-th cycle, where the switching of the CAP-DAC is updated to one corresponding to code $B_2$, followed by an extra comparison. Similarly, when the code $B_2$ is observed, the CAP-DAC switching is updated to one corresponding to $B_1$ during the extra comparison cycle. The result of the extra comparison can thus be used to detect the sign of the MSB capacitor mismatch for an appropriate correction method. Similar procedure can be followed to detect the mismatch of the MSB−1 and MSB−2 capacitors. For instance, to detect the mismatch of the MSB−2 capacitor, the extra calibration cycle is activated when the codes $B_3 = \{0, 1, 0, 1, x, x, x, x, x\}$ or $B_4 = \{0, 1, 1, 0, x, x, x, x, x\}$ are observed at the ADC output.

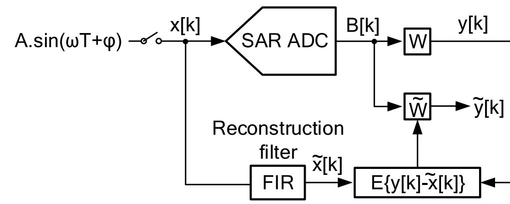


Fig. 4. A foreground mismatch calibration based on estimation of the DNL error.

*2) Foreground:* Foreground mismatch calibration can be performed by estimating the DNL error of all possible output codes using a known input, e.g. a sinusoidal signal. The DNL estimation can be done in the same way as it is done for the DNL measurement of an ADC, e.g. using a histogram-based method in the time domain or using frequency-based methods [8]–[11]. Ref. [12] used an averaging method to estimate the DNL as follows. Let us denote $x[k]$ as the ideal analog sampled signal at the quantizer (ADC) input, with $k$ being the sample index. We denote the quantized number associated with $x[k]$ by $B[k] = Q_N\{x[k]\}$, where the operator $Q_N\{\cdot\}$ is the $N$-bit quantization performed by the ADC. The output of the ADC, $y[k]$, can then be worked out by using (1). Thus, the error associated with $B[k]$ is

$$e[k] = y[k] - x[k]. \tag{8}$$

This error includes both the ADC quantization error and nonlinearity errors. The goal is to minimize $e[k]$ through updated bit weights $\widetilde{W}$ that would result in a corrected output $\widetilde{y}[k]$, as shown in Fig. 4. It was proved in [13] that this error is minimized when for a specific output code $B$, $\widetilde{y}[k]$ is set to the average of all sampled inputs $x[k]$ that are mapped to code $\widetilde{B}$. The reconstruction filter in Fig. 4 estimates the sampled input voltage and a sinusoidal waveform is employed as input signal during calibration. One problem associated with this approach is that the computed DNL includes all types of static and potentially frequency-dependent non-linearities of the ADC, with the CAP-DAC mismatch being only one of them. As a consequence, this error detection mechanism only proves to be accurate for a particular frequency. *Dynamic detection* has been proposed to overcome this limitation [12] where the estimated DNL is not only a function of the current output code, but also depends on the previous output code(s) or some other additional information, such as the slope of the input signal, as proposed in [14]. In [15], apart from the current

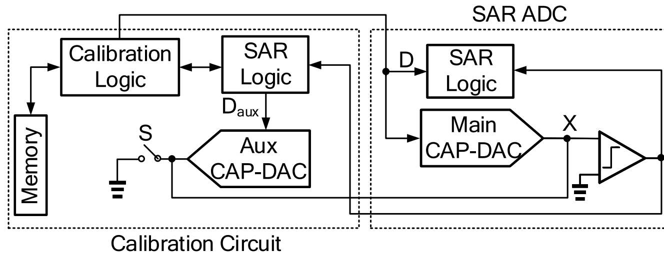


Fig. 5. Block diagram of self-calibration using an auxiliary CAP-DAC.

output of the ADC, $k$ previous outputs were also used to estimate the DNL.

*Self-calibration* is another method of foreground mismatch calibration of SAR ADCs, and is based on the DNL error estimation of the individual capacitors using a DAC and can only be applied to binary-weighted capacitive DACs. This technique can be realized in two ways: either by utilizing an *auxiliary* CAP-DAC, as shown in Fig. 5, or by using the same DAC of the ADC itself (*main CAP-DAC*). The former can be exploited following a *bottom-up* or a *top-down* approach.

In a bottom-up approach [16], the direction of the calibration is from the LSB towards the MSB. Specifically, in the case of the $N$-bit capacitor array shown in Fig. 6, binary-scaling implies

$$C_j = 2 \cdot C_{j-1} \quad (j = 1, 2, ..N-1). \tag{9}$$

Capacitor $C_{00} = C_0$ is added to make the total capacitance a power of two multiples of the LSB capacitor (unit capacitor) $C_0$, i.e.

$$C_{00} + \sum_{i=0}^{N-1} C_i = 2^N C_0. \tag{10}$$

The self-calibration method makes use of the fact that for an ideal binary-weighted capacitor array with no mismatch, the value of any individual capacitor in the array is equal to the sum of all of the lower significant bit capacitors, i.e.

$$C_j = C_{00} + \sum_{i=0}^{j-1} C_i \quad (j = 1, 2, ..N-1) \tag{11}$$

Equivalently, if capacitor $C_j$ in the array of Fig. 6 is mismatched with its ideal value and assuming that the LSB capacitors are ideal, then (11) is not exact. In other words, if $\Delta C_j$ is the deviation of capacitor $C_j$ from its ideal value, then the term

$$C_j - \left(C_{00} + \sum_{i=0}^{j-1} C_i\right) = \Delta C_j \tag{12}$$

is its corresponding mismatch. Now assume it is desired to estimate the mismatch of capacitors $C_j$ to $C_{(N-1)}$, assuming that capacitors $C_0$ to $C_{(j-1)}$ are all mismatch-free.[1] The self-calibration procedure occurs in a multi-phase process as follows:

[1]This assumption does not pose any restrictions as the calibration can start from the LSB capacitor.

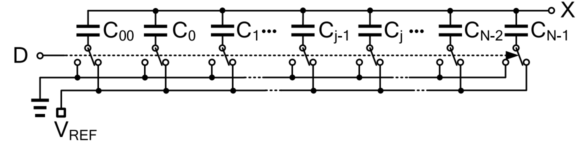


Fig. 6. Circuit schematic of an $N$-bit CAP-DAC.

*Phase I:* The reset switch $S$ in Fig. 5 closes to bring node $X$ to ground. At the same time, the calibration logic sets $D$ to

$$\begin{aligned} D &= \left\{d_{00}, d_0, d_1, \ldots, d_{(j-1)}, d_j, \ldots, d_{(N-2)}, d_{(N-1)}\right\} \\ &= \{1, 1, 1, \ldots, 1, 0, \ldots, 0, 0\} \end{aligned} \tag{13}$$

It also sets the binary input signal driving the auxiliary CAP-DAC, $D_{\text{aux}}$, to the mid-code $\{0, 0, \ldots, 0, 1\}$.

*Phase II:* The reset switch opens and the calibration logic changes $D$ to

$$\begin{aligned} D &= \left\{d_{00}, d_0, d_1, \ldots, d_{(j-1)}, d_j, \ldots, d_{(N-2)}, d_{(N-1)}\right\} \\ &= \{0, 0, 0, \ldots, 0, 1, \ldots, 0, 0\}. \end{aligned} \tag{14}$$

$Q_X$, the charge on node $X$, thus becomes

$$\begin{aligned} Q_X &= \alpha V_{\text{REF}} \cdot \left[C_j - \left(C_{00} + \sum_{i=0}^{j-1} C_i\right)\right] \\ &= \alpha V_{\text{REF}} \cdot \Delta C_j, \end{aligned} \tag{15}$$

where $\alpha$ is a constant factor that represents the charge sharing between the total capacitance of the main CAP-DAC and that of the auxiliary CAP-DAC, that is $\alpha = C_{\text{DAC,main}}/(C_{\text{DAC,main}} + C_{\text{DAC,aux}})$, where $C_{\text{DAC,main}}$ and $C_{\text{DAC,aux}}$ are the total capacitance of the main DAC and the auxiliary DAC, respectively. This gives rise to a voltage on node $X$ equal to

$$V_X = \frac{\alpha V_{\text{REF}} \cdot \Delta C_j}{C_X}, \tag{16}$$

where $C_X$ is the total capacitance at node $X$.

*Phase III:* The calibration logic processes the output of the comparator. A negative output implies that $\Delta C_j < 0$. The SAR logic of the calibration circuit then progressively increments $D_{\text{aux}}$ in a successive-approximation manner, making the auxiliary CAP-DAC to inject a charge into node $X$ that is proportional to $D_{\text{aux}}$. This sequence continues until the output of the comparator becomes positive. The binary number $D_{\text{aux}}$ is then registered as the mismatch of $C_j$ (normalized to the unit capacitor $C_0$) and is stored in the memory. If the comparator output is positive at the start of this sequence, then $\Delta C_j > 0$. The calibration logic then decrements $D_{\text{aux}}$ until the comparator output becomes negative, and again $D_{\text{aux}}$ is stored as the mismatch of $C_j$. It is worth noting that, in order to mitigate the detrimental impact of the thermal noise (e.g. $kT/C$ noise), averaging should be performed by repeating the procedure from phase I to III a sufficient number of times, and averaging the obtained results. The next capacitor to be calibrated is $C_{(j+1)}$. Phases I to III are repeated in the same

way. At the end of phase II, $V_X$ will be equal to

$$V_X = \alpha V_{\mathrm{REF}} \cdot \frac{C_{(j+1)} - \left(C_{00} + \sum_{i=0}^{j} C_i\right)}{C_X} = \alpha V_{\mathrm{REF}} \cdot \frac{\Delta C_{(j+1)} + \Delta C_j}{C_X}. \tag{17}$$

As can be seen, this time $V_X$ contains the mismatch error for both $C_{(j+1)}$ and $C_j$. Therefore, at the end of phase III, $D_{\mathrm{aux}}$ represents the sum of the mismatches of $C_j$ and $C_{(j+1)}$. By denoting by $e_j$ the estimated mismatch error of capacitor $C_j$, the mismatch error of $C_{(j+1)}$, which is stored in the memory, can be expressed as

$$e_{(j+1)} = D_{\mathrm{aux}} - e_j. \tag{18}$$

Similarly, for all of the subsequent capacitors, the mismatch error would be equal to the value of $D_{\mathrm{aux}}$ at the end of phase III minus the sum of the mismatch errors of all of the previously calibrated capacitors. In other words, the binary number representing the mismatch of capacitor $C_L$ is

$$e_L = D_{\mathrm{aux}} - \sum_{i=j}^{L-1} e_i. \tag{19}$$

One problem associated with the bottom-up self-calibration approach is the residual voltage at node $X$ at the end of phase III, due to the limited resolution of the calibration DAC (i.e. a quantization error). This quantization error occurs during the mismatch estimation of a particular capacitor and gets doubled for every subsequent capacitor under calibration, resulting in an exponential growth of the error. The accumulated error contributed by all of the capacitors that undergo calibration could then be large, unless a high resolution auxiliary DAC is used. This constraints the number of capacitors whose mismatch is estimated by this approach, using a finite resolution auxiliary DAC.

The *top-down* approach [17]–[21] is similar to the bottom-up approach. The main difference is the direction of calibration, that is from the MSB capacitor to the LSB one. Moreover, it assumes that the sum of the mismatch errors of all of the capacitors is zero, i.e.

$$\Delta C_{00} + \sum_{i=0}^{N-1} \Delta C_i = 0. \tag{20}$$

In general, though, the assumption of (20) is not necessarily correct. In other words

$$\Delta C_{00} + \sum_{i=0}^{N-1} \Delta C_i = \Delta S, \tag{21}$$

where $\Delta S$ is non-zero. This is however not problematic. To explain why, note that the estimated mismatches of the capacitors based on the self-calibration method are all in units of the LSB capacitor $C_{00}$ (i.e. they are normalized to the value of $C_{00}$). Now, if we define a new value for the LSB capacitor as

$$C'_{00} = C_{00} + \frac{\Delta S}{2^N}, \tag{22}$$

then we can write

$$C_j = 2^j \cdot C'_{00} - \frac{\Delta S}{2^{N-j}} + \Delta C_j. \tag{23}$$

As can be seen in (23), this new definition of the LSB capacitance adds an extra term of $-\Delta S/2^{N-j}$ to the capacitor mismatch. We now define a new value for the mismatch of the capacitor based on this redefinition of the unit capacitance as

$$\Delta C'_j = -\frac{\Delta S}{2^{N-j}} + \Delta C_j, \tag{24}$$

which satisfies the assumption of (20), i.e.

$$\Delta C'_{00} + \sum_{i=0}^{N-1} \Delta C'_i \tag{25}$$

$$= \left(\Delta C_{00} + \sum_{i=0}^{N-1} \Delta C_i\right) + \left(\sum_{i=0}^{N-1} -\frac{\Delta S}{2^{N-i}}\right) \tag{26}$$

$$= \Delta S - \Delta S = 0. \tag{27}$$

In practice, this essentially means that the estimated capacitor mismatches will eventually be expressed in units of the new LSB capacitance $C'_{00}$.

Similarly to the bottom-up approach, the detection process occurs in a three-phase procedure which starts from the MSB capacitor ($C_{N-1}$) and proceeds as follows:

*Phase I:* With reference to Fig. 5, the reset switch $S$ sets node $V_X$ to ground and the calibration logic sets $D$ to

$$D = \left\{d_{00}, d_0, d_1, \ldots, d_{(N-2)}, d_{(N-1)}\right\} = \{1, 1, 1, \ldots, 1, 0\}, \tag{28}$$

and $D_{\mathrm{aux}}$ to $\{0, 0, \ldots, 0, 1\}$.

*Phase II:* $S$ opens and the calibration logic sets $D$ to

$$D = \left\{d_{00}, d_0, d_1, \ldots, d_{(N-2)}, d_{(N-1)}\right\} = \{0, 0, 0, \ldots, 0, 1\}. \tag{29}$$

Charge redistribution occurs, and charge $Q_X$ becomes

$$Q_X = \alpha V_{\mathrm{REF}} \cdot \left[C_{(N-1)} - \left(C_{00} + \sum_{i=0}^{N-2} C_i\right)\right]. \tag{30}$$

From (20), it follows that

$$Q_X = \alpha V_{\mathrm{REF}} \cdot 2\Delta C_{(N-1)}, \tag{31}$$

which gives rise to

$$V_X = \frac{\alpha V_{\mathrm{REF}} \cdot 2\Delta C_{(N-1)}}{C_X}. \tag{32}$$

*Phase III:* Depending on the output of the comparator, the calibration logic increments or decrements $D_{\mathrm{aux}}$ until the comparator output changes. According to (32), $D_{\mathrm{aux}}$ is therefore equivalent to twice the mismatch error of $C_{(N-1)}$, and it is stored in memory as $e_{(N-1)}$. The mismatch of the next capacitor (the MSB$-$1 capacitor) is detected in the same way. Following phase I and II and the charge distribution at the end of phase II, $Q_X$ becomes

$$Q_X = \alpha V_{\mathrm{REF}} \cdot \left[C_{(N-2)} - \left(C_{00} + \sum_{i=0}^{N-3} C_i\right)\right] \tag{33}$$

$$= \alpha V_{\mathrm{REF}} \cdot \left(2\Delta C_{(N-1)} + \Delta C_{(N-2)}\right). \tag{34}$$

This follows

$$V_X = \alpha V_{\mathrm{REF}} \cdot \frac{2\Delta C_{(N-2)} + \Delta C_{(N-1)}}{C_X}, \tag{35}$$

resulting in

$$e_{(N-2)} = \frac{1}{2}\left(D_{\mathrm{aux}} - e_{(N-1)}\right). \tag{36}$$

Following the same methodology, it can be shown that the mismatch error $e_L$ of the $L$-th capacitor is equal to

$$e_L = \frac{1}{2}\left(D_{\mathrm{aux}} - \sum_{i=L+1}^{N-1} e_i\right), \tag{37}$$

where $D_{\mathrm{aux}}$ is the output of the SAR logic of the calibration circuit at the end of phase III. As evident from (37), the accumulated error of all previous capacitors *halves* every time when it appears in the estimated mismatch error equation of the capacitor under calibration. Therefore, the *top-down* approach does not present the issue of the exponentially growing quantization error as severe as in the *bottom-up* approach.

As previously mentioned, self-calibration method can also be realized by using the main CAP-DAC of the SAR ADC as the calibration DAC [22], [23]. This is a more hardware-efficient solution. However, the accuracy of the mismatch detection is limited by the resolution of the SAR ADC itself, i.e. one LSB. Therefore, the problem of accumulation of the quantization error is even more severe here. For this reason, this approach is only used to detect the mismatch of a few MSB capacitors, and it is only effective when this mismatch is larger than 1 LSB. This type of deterministic self-calibration, which uses the main CAP-DAC, is indeed what is employed in this work, and it operates jointly with the proposed stochastic quantization.

### B. Correction

*1) Analog:* One of the most straightforward approaches of correcting a capacitor value is trimming [24]. This is performed by progressively adding or removing smaller capacitors to the capacitor which is being calibrated, until the total capacitance matches the desired value. Determining when the desired value has been reached, and thus when trimming should be ended can be accomplished in different ways. In [25], a *reference capacitor* ($C_{\mathrm{REF}}$) is used and the first calibrated capacitor $C_0$ is trimmed until its value becomes equal to $C_{\mathrm{REF}}$. Next, $C_{\mathrm{REF}}$ plus the calibrated $C_0$ are used as the new reference capacitor for the second capacitor to be calibrated. This approach continues until all of the capacitors within the binary-weighted capacitor array are calibrated.

When a self-calibration method is used, the calibration DAC itself is normally used to correct the detected mismatches, and this is performed during the normal conversion of the ADC as follows. Let us denote the estimated mismatch error associated to capacitor $C_i$ with $e_i$ ($L \le i \le N-1$, with $L$ being the number of LSB capacitors assumed to be ideal, and whose errors are not estimated during the detection process), where $e_i$ is a binary number stored in the memory. If, at some point during the normal operation of the ADC, the binary code driving the main CAP-DAC is the code $D = \{d_0, d_1, \ldots, d_{(N-2)}, d_{(N-1)}\}$, the calibration logic outputs the code

$$D_{\mathrm{aux}} = \sum_{i=L}^{N-1} d_i e_i \tag{38}$$

to the auxiliary CAP-DAC. This causes a charge redistribution to occur, correcting the mismatch of the capacitors which have contributed charge to the output of the CAP-DAC up to this point of the conversion. The arithmetic operation of (38) can be implemented in various ways [16], one of which is to store the individual capacitor errors ($e_L$ to $e_{(N-1)}$) along with the permutation of the summations of these errors (e.g. $e_L + e_{L+2} + e_{(N-1)}$). This would require a memory of length $2^{N-L}$. However, no adder is needed to perform the sum operation in (38). Another way is to only store the individual capacitor errors $e_L$ to $e_{(N-1)}$ in the memory, and perform the summation of (38) during the conversion. This, however, requires an adder which needs to operate at least $N$ times faster than the sampling rate of the SAR ADC, which appears rather unpractical for high-speed ADCs. The third method is to employ $N-L$ different auxiliary CAP-DACs, one for the error correction (detection) of each capacitor. In such way, neither a memory nor an adder is required. However, the power consumption of the calibration CAP-DAC increases by a factor $N$–$L$. Moreover, the realization of the detection process should also be modified accordingly.

*2) Digital:* When no extra DAC is used to inject a residue charge during the conversion (and in the analog domain), the correction must be performed in the digital domain. This is basically done by using the updated bit weights $\widetilde{W} = \{\widetilde{w}_0, \widetilde{w}_1, \ldots, \widetilde{w}_{N-1}\}$ containing the mismatch errors of the capacitors and perform the arithmetic sum of

$$\widetilde{D}_{\mathrm{out}} = \sum_{i=0}^{N-1} D_{\mathrm{out},i}\,\widetilde{w}_i, \tag{39}$$

where $D_{\mathrm{out}}$ and $\widetilde{D}_{\mathrm{out}}$ are the output of the ADC before and after correction, respectively. Since the precision of the correction bit weights $\widetilde{w}_0 \sim \widetilde{w}_{N-1}$ can be higher than that of the ADC, the output of (39) needs to be *truncated* to the resolution of the ADC. This truncation limits the accuracy of the DNL improvement of the digital correction to 1 LSB. In other words, after the digital correction, the DNL values smaller than 1 LSB will remain unchanged.

## III. Proposed Calibration Method

The mismatch calibration method proposed in this work is a combination of the self-calibration approach and a stochastic approach that makes use of a noisy comparator to estimate a residue voltage [26]. The idea of stochastic quantization to estimate the mismatch of the CAP-DAC and/or to reduce the quatization noise has been already used in the literature [27], [28]. Our proposed method, however, differs from those in the following ways:

1. The stochastic approach is only employed when the residue voltage is lower than 1 LSB. Otherwise, the calibration

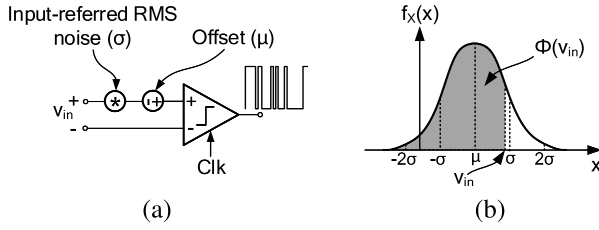


Fig. 7. (a) Model of a comparator with its input-referred noise and offset. (b) Illustration of the input distribution function on the Gaussian curve.

starts with a deterministic self-calibration until the residue voltage narrows to below 1 LSB, at which point the stochastic quantization is commenced. The combination of these two calibration approaches substantially decreases the calibration time when the mismatch is (much) larger than the LSB, compared to when only the stochastic approach is adopted.

2. As explained later, in order to estimate the residue voltage using a noisy comparator, the knowledge of the input-referred comparator noise power is required. In the previous publications, this value was either measured off-chip post-fabrication, or assumed equal to the simulated value. Here, we propose a new technique to compute this entirely on-chip.

Thanks to the stochastic nature of the proposed technique, a mismatch estimation with a precision of better than 1 LSB can be achieved. Numerical simulations show that a combination of the deterministic self-calibration and stochastic quantization allows to theoretically improve the average ENOB of a 10-bit SAR ADC with 5% mismatch of the unit capacitor by almost 0.7-bit compared to when only the deterministic calibration is adopted.[2]

### A. Theoretical Background of Stochastic Quantization

What follows is the concept underlying the proposed stochastic calibration, whereas its interaction with the deterministic self-calibration, which operates jointly on it, is discussed later in this section.

Fig. 7(a) illustrates a dynamic comparator with an input-referred rms noise and offset $\sigma$ and $\mu$ (expressed in volts), respectively, and an input voltage $v_{\text{in}}$. At the rising edge of the clock (*Clk*), a logic one is asserted at the comparator output if $v_{\text{in}} + \sigma + \mu > 0$, while a logic zero is asserted otherwise. Assuming the noise of the comparator follows a normal distribution, then the input-referred noise and offset can be described by a random variable $X_{\text{comp}}$ with (Gaussian) normal distribution of mean $\mu$ and standard deviation $\sigma$, $X_{\text{comp}} \sim \mathcal{N}(\mu, \sigma^2)$. As such, for the sample space of output ones and zeros, the ratio between the count of ones and the size of the sample space (i.e. the total number of runs, $\Phi$) corresponds to the probability that the comparator input signal is greater than $X_{\text{comp}}$, i.e.

$$\Phi(v_{\text{in}}) = P_r\left(v_{\text{in}} - X_{\text{comp}} \geq 0\right) \tag{40}$$

Knowing that the *cumulative distribution function* (CDF) of a random variable $X$ is defined as $F_X(x) = P(X \leq x)$, (40) corresponds to the CDF of a normal random variable $X_{\text{comp}}$ for an input of $v_{\text{in}}$. Therefore, $\Phi(v_{\text{in}})$ is given by

$$\Phi(v_{\text{in}}) = \frac{1}{2}\left[1 + \operatorname{erf}\left(\frac{v_{\text{in}} + \mu}{\sigma}\right)\right], \tag{41}$$

where $\operatorname{erf}(x)$ is the *error function* of variable $x$. Therefore, if $\Phi(v_{\text{in}})$ is known, $v_{\text{in}}$ can be expressed as

$$v_{\text{in}} = \sigma \cdot \operatorname{erf}^{-1}[2\Phi(v_{\text{in}}) - 1] - \mu, \tag{42}$$

where $\operatorname{erf}^{-1}(x)$ is the *inverse error function* of variable $x$. Of course, the accuracy of this estimation depends on the size of the sample space, i.e. the total number of comparisons. It also depends on the magnitude of the input voltage compared to the input-referred noise of the comparator, i.e. $v_{\text{in}}/\sigma$. Following (41), and for a sample space of limited size, the smaller the value of input $v_{\text{in}}$, the higher the accuracy of (42). For instance, for a sample space size of 1000, if $v_{\text{in}} = 3\sigma$ and $\mu = 0$ then $\Phi(v_{\text{in}}) = 0.9999$. This means that, on average, out of 10000 samples, only one of them indicates that the input of the comparator is greater than $v_{\text{in}}$. Therefore, for such an unlikely event, 1000 samples would not be enough to obtain a meaningful statistical output. Since $\operatorname{erf}(1) \simeq 0.85$, as a rule of thumb and for a reasonably large sample space, the outcome of (42) can be assumed to be accurate when

$$-1 < \frac{v_{\text{in}} + \mu}{\sigma} < 1, \tag{43}$$

which is equivalent to

$$0.1 < \Phi(v_{\text{in}}) < 0.9. \tag{44}$$

MATLAB simulations have been performed to assess the estimation error of $v_{\text{in}}$ by (42), referred to as $e_{est}$, versus various parameters. For instance, for $-\sigma < v_{\text{in}} < +\sigma$, the relationship between $e_{est}$ and the number of comparisons ($N_{\text{comp}}$) is a straight line in a log-log scale with a slope of $\approx -3.6\sigma$ dB/dec. Also, for (normalized values of) $v_{\text{in}} = 1.5$, $\mu = 0.5$ and $N_{\text{comp}} = 2^{14}$, $e_{est}$ is minimum at $\sigma \approx 1$.[3]

What is also evident from (42) is that, in order to estimate $v_{\text{in}}$, the values $\mu$ and $\sigma$ must be known beforehand. Prior works have aimed at accomplishing this through post-fabrication measurements [26]. This is, however, quite inefficient because, firstly, they cannot be fully automated and, secondly, since $\mu$ and $\sigma$ differ among devices, they demand that each IC be separately calibrated, which is both time-consuming and costly from a large-scale production perspective. Here, we propose a novel method to perform this completely on-chip as follows. Eq. (42) can be seen as a formula with two unknowns: $\mu$ and $\sigma$. Therefore, $\mu$ and $\sigma$ can be found by using two different values of $v_{\text{in}}$ ($v_{\text{in1}}$ and $v_{\text{in2}}$) and solving a system of two equations:

$$\begin{cases} \mu + \sigma \cdot \left[\operatorname{erf}^{-1}(2\Phi(v_{\text{in1}}) - 1)\right] = v_{\text{in1}} \\ \mu + \sigma \cdot \left[\operatorname{erf}^{-1}(2\Phi(v_{\text{in2}}) - 1)\right] = v_{\text{in2}}. \end{cases} \tag{45}$$

[2]Assuming the mismatch of capacitors is the only nonideality of the system (e.g. ideal reference voltages and noiseless devices).

[3]Simulations show that the ADC SNDR starts degrading for $N_{\text{comp}} < 2^{14}$, and that there is a marginal improvement for $N_{\text{comp}} > 2^{14}$.

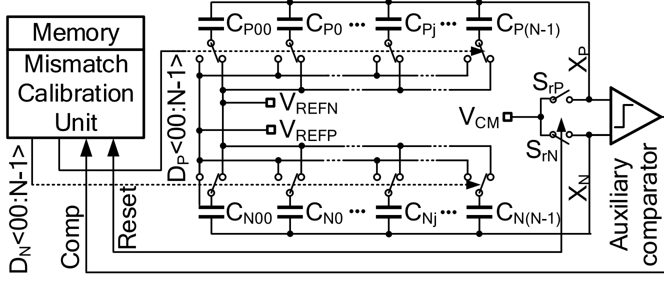


Fig. 8. A differential capacitor array to demonstrate the process of stochastic mismatch calibration.

Solving for $\mu$ and $\sigma$ results in

$$\begin{cases} \sigma = \dfrac{v_{\text{in}1} - v_{\text{in}2}}{\text{erf}^{-1}(2\Phi(v_{\text{in}1}) - 1) - \text{erf}^{-1}(2\Phi(v_{\text{in}2}) - 1)} \\ \mu = \dfrac{v_{\text{in}2}\text{erf}^{-1}(2\Phi_1(v_{\text{in}2}) - 1) - v_{\text{in}1}\text{erf}^{-1}(2\Phi_2(v_{\text{in}1}) - 1)}{\text{erf}^{-1}(2\Phi(v_{\text{in}1}) - 1) - \text{erf}^{-1}(2\Phi(v_{\text{in}2}) - 1)}. \end{cases} \quad (46)$$

### *B. Calibration Process*

According to (43), if an input voltage smaller than 1 LSB is to be estimated using a noisy comparator, then $\sigma$ should be larger than 1 LSB, provided that $\mu$ is negligible. Since comparators in SAR ADCs are usually designed so as to exhibit an input-referred noise and offset lower than 1 LSB, they do not satisfy such requirement. However, a possibility is to use a second *noisier* comparator (hereinafter referred to as *auxiliary comparator*), specifically designed for the mismatch calibration process with the proper characteristics. This auxiliary comparator's bandwidth can be more relaxed compared to that of the main comparator as the calibration process can run at a lower speed.

The calibration process is split into two phases: the computation of $\mu$ and $\sigma$ (which is the necessary information for stochastic quantization) and the actual mismatch calibration (inclusive of both the deterministic and stochastic methods).

*1) Computation of $\mu$ and $\sigma$:* In order to satisfy the requirement of (43), the auxiliary comparator is designed to have an input-referred noise of ~1.5 LSB and offset of <0.5 LSB. The offset is lowered down by means of a dedicated offset calibration circuit which operates before the mismatch calibration process begins. The aim of this initial phase of the complete calibration process is to form the two equations in (46), where $v_{\text{in}1}$ and $v_{\text{in}2}$ are two comparator inputs, and are set to +LSB and 0, respectively.[4] These equations are then solved in the digital domain in order to estimate the values of $\sigma$ and $\mu$ and the results are subsequently stored in a memory. The inverse error function $\text{erf}^{-1}(x)$ of (46) is also stored as a look-up table.

*2) Mismatch Calibration:* Let us consider the binary-scaled differential capacitor array shown in Fig. 8 as an example so as to explain the flow of the proposed calibration process. Here, for both $P$ and $N$ sides, the value of $C_{00}$ is equal to that of

[4]These voltages can simply be generated by an appropriate control of the CAP-DAC through the SAR logic.

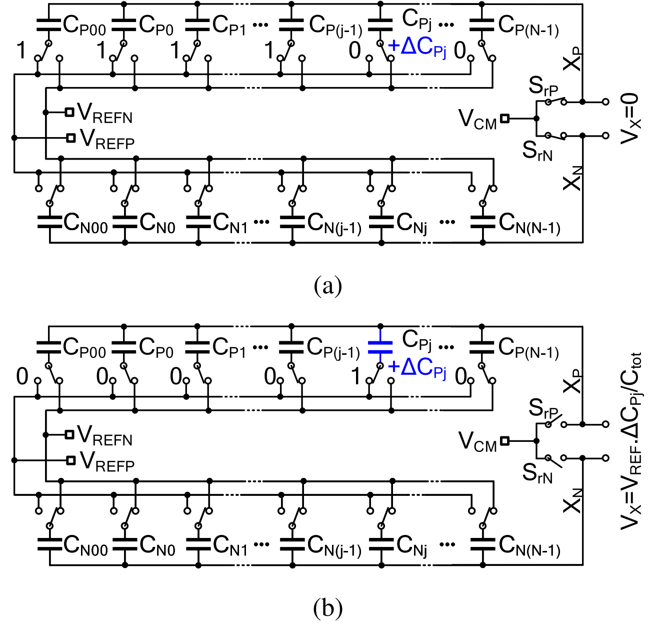


Fig. 9. CAP-DAC during the calibration process: (a) phase I, (b) phase II.

$C_0$, and $C_j = 2C_{j-1}$, where $1 \le j \le N - 1$. Let us assume that the mismatch of capacitor $C_{Pj}$ is to be computed, and that the mismatch of all smaller capacitors (also referred to as LSB *capacitors*), which consist of $C_{P0} \sim C_{P(j-1)}$ and $C_{N0} \sim C_{N(j-1)}$, is known (i.e. previously computed). The process evolves in a three-phase procedure that combines a bottom-up deterministic self-calibration by using the main CAP-DAC and a stochastic-based quantization as follows:

*Phase I:* The reset switches $S_{\text{rP}}$ and $S_{\text{rN}}$ close, thus precharging nodes $X_P$ and $X_N$ to a common-mode voltage $V_{\text{CM}}$. At the same time, the calibration logic sets $D_P$ to

$$\begin{aligned} D_P &= \{d_{P00}, d_{P0}, d_{P1}, \ldots, d_{P(j-1)}, d_{Pj}, \ldots, d_{P(N-1)}\} \\ &= \{1, 1, 1, \ldots, 1, 0, \ldots, 0\} \end{aligned} \quad (47)$$

and $D_N$ to all zeros (Fig. 9(a)).

*Phase II:* The reset switches open and the calibration logic changes $D_P$ to

$$\begin{aligned} D_P &= \{d_{P00}, d_{P0}, d_{P1}, \ldots, d_{P(j-1)}, d_{Pj}, \ldots, d_{P(N-1)}\} \\ &= \{0, 0, 0, \ldots, 0, 1, \ldots, 0\}. \end{aligned} \quad (48)$$

whereas $D_N$ remains unchanged (Fig. 9(b)). This causes voltage $V_{XP}$ to become

$$\begin{aligned} V_{XP} &= V_{\text{CM}} + V_{\text{REF}} \cdot \frac{C_{Pj} - \left(C_{P00} + \sum_{i=0}^{j-1} C_{Pi}\right)}{C_{\text{tot}}} \quad (49) \\ &= V_{\text{CM}} + V_{\text{REF}} \cdot \Delta C_{Pj}/C_{\text{tot}}, \quad (50) \end{aligned}$$

where $C_{\text{tot}}$ is the total capacitance of the capacitive array and $V_{\text{REF}}$ is equal to $V_{\text{REFP}} - V_{\text{REFN}}$. The voltage at node $V_{\text{XN}}$ remains at $V_{\text{CM}}$. Therefore, the differential voltage at the input of the comparator becomes

$$V_X = V_{\text{XP}} - V_{\text{XN}} = V_{\text{REF}} \cdot \Delta C_{Pj}/C_{\text{tot}}. \quad (51)$$

*Phase III:* With (51) being the input, the auxiliary comparator is activated to make a large number of comparisons,

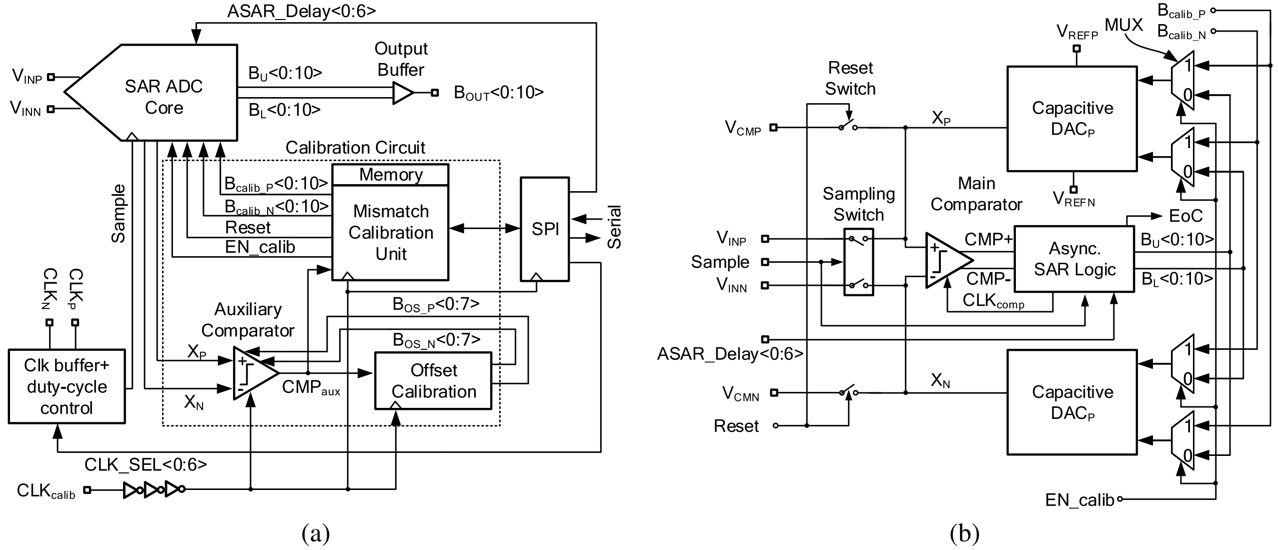


Fig. 10. (a) Overall architecture of the ADC with mismatch calibration. (b) Block diagram of the SAR ADC core.

and the output 1's and 0's are recorded by the calibration unit in order to form the cumulative distribution function $\Phi(V_X)$. According to (43) and (44), if $0.1 < \Phi(V_X) < 0.9$, then $V_X$ is smaller than 1 LSB, meaning that a *deterministic* self-calibration method would not be able to estimate it. The calibration unit then, by skipping the deterministic approach and employing the stochastic one, uses the value of $\Phi(V_X)$ and arithmetically solves (42) using the values of $\sigma$ and $\mu$ that were previously computed and stored in memory to find $V_X$.

On the other hand, if $\Phi(V_X) > 0.9$, the input of the comparator is positive, and thus $\Delta C_{Pj} > 0$. The calibration then progressively increments $D_N$ (by skipping the first LSB bit associated to $C_{N00}$, i.e. $D_{N00}$) using a successive approximation search along with a counter $E$ (an integer number referred to as the *error counter*) until $\Phi(V_X)$ becomes less than 0.9 (deterministic self-calibration). At this point, the calibration uses the stochastic method previously discussed to estimate $V_X$. Let us denote the quantified binary number associated with this residual voltage with $x_a$. The binary number

$$E_{Pj} = E + x_a - \sum_{i=0}^{j-1} e_{Pi} \tag{52}$$

would be thus the mismatch of $C_{Pj}$ (normalized to the unit capacitance $C_0$) and stored in the memory. Here, $\sum_{i=0}^{j-1} e_{Pi}$ is the sum of the mismatch errors of all of the LSB capacitors.

Similarly, if $\Phi(V_X) < 0.1$, then $V_X$ would be negative, implying $\Delta C_{Pj} < 0$. The calibration logic then increments $D_P$, along with $E$, until $\Phi(V_X) > 0.1$ (deterministic self-calibration). Once again, the calibration solves (42) to compute $V_X$. This time, the value

$$E_{Pj} = -E + x_a - \sum_{i=0}^{j-1} e_{Pi} \tag{53}$$

is stored in the memory as the mismatch of $C_{Pj}$. It is worth mentioning that the presence of any parasitic capacitance on the top-plate of CAP-DAC only changes the value of $C_{\text{tot}}$ in the above equations and does not affect the validity of the calibration algorithm.

The mismatch correction is done as follows. Let us assume that $B_{\text{OUT}} = \{b_0, b_1, \ldots, b_{N-1}\}$ is a raw digital output of the ADC. Two error terms $\Delta E_P$ and $\Delta E_N$ are calculated as

$$\Delta E_P = \sum_{i=1}^{N-1} b_i E_{Pi}, \quad \Delta E_N = \sum_{i=1}^{N-1} \overline{b_i} E_{Ni}, \tag{54}$$

where $\overline{b_i}$ is the binary inversion of bit $b_i$, and $E_{Pi}$ and $E_{Ni}$ are the estimated mismatches corresponding to $C_{Pi}$ and $C_{Ni}$, respectively [see (52) and (53)]. The final error is then calculated as a sum of $\Delta E_P$ and $\Delta E_N$ that is added to the raw output of the ADC to produce the calibrated output as

$$\widetilde{B}_{\text{OUT}} = B_{\text{OUT}} + \Delta E_P + \Delta E_N. \tag{55}$$

which is then rounded off to the nearest integer.[5]

## IV. Circuit Implementation

The ADC architecture is shown in Fig. 10. It consists of a 10-bit SAR ADC core, the calibration circuitry, the clock duty-cycle control and the SPI interface. The calibration circuitry comprises the mismatch calibration digital unit and the *auxiliary* comparator along with its offset calibration circuit. The block diagram of the SAR ADC core is shown in Fig. 10(b). The differential input signal $V_{\text{INP/INN}}$ is sampled by two bootstrapped switches on the top plate of the binary-weighted capacitive DAC, which is controlled by an asynchronous SAR logic. The *reset* switches are only used during the calibration phase. Fig. 11 also illustrates the timing diagram of the ADC during the three different operational phases. During the offset calibration phase, where the auxiliary comparator's offset is corrected, the Reset signal is asserted, connecting the inputs of the comparator to the common-mode voltage ($V_{\text{CMP}} = V_{\text{CMN}}$, as seen in the figure).

[5]Note that retaining the fractional bits of (56) would result in a marginally better ENOB, but at the expense of more output bits than the nominal resolution of the ADC, which may add unnecessary hardware overhead.

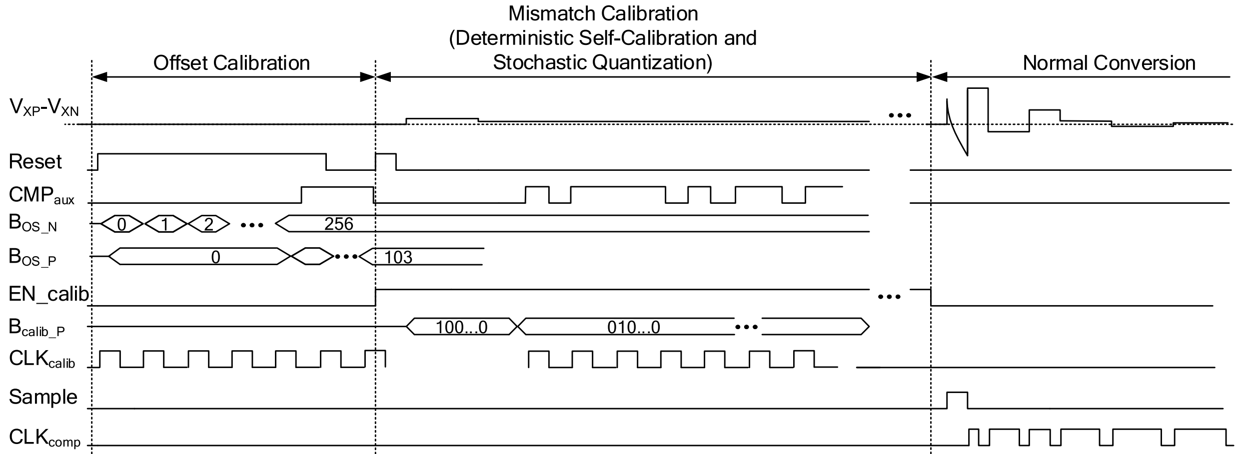


Fig. 11. Operational timing diagram of the ADC signals along the three operational phases.

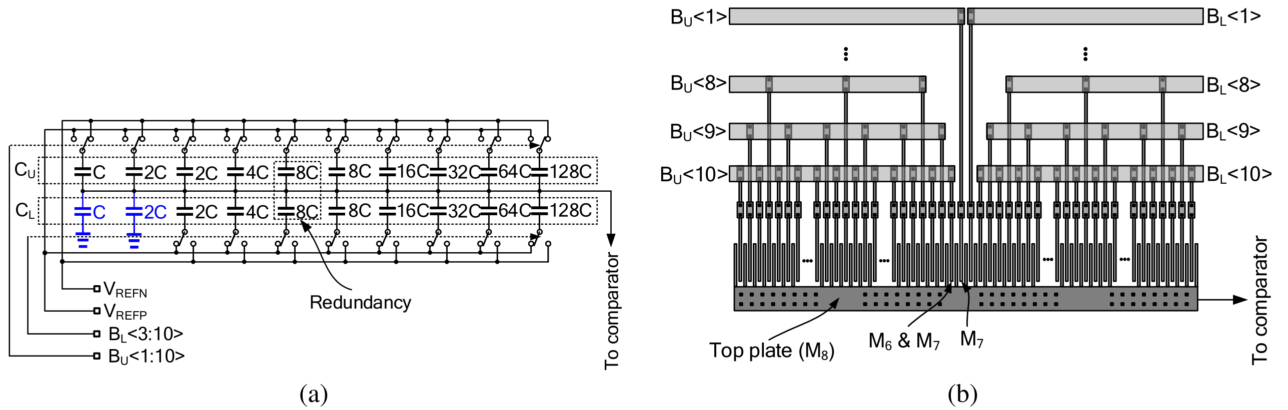


Fig. 12. (a) 9-bit binary-weighted split-capacitor array with redundancy at $8C$. (b) Inter-digitized layout structure of the split-capacitor array.

The comparator's offset is then canceled using two arrays of binary-weighted MOS capacitors connected to its output nodes and controlled by signals $B_{\mathrm{OS_N}}$ and $B_{\mathrm{OS_N}}$. Afterwards, the mismatch calibration phase starts in a stochastic process which was explained earlier. The ADC then enters the normal binary search conversion phase, where the *Sample* signal is asserted and the input voltage is quantized.

### A. Capacitive DAC

Thanks to the proposed mismatch calibration, the total size of the capacitive DAC has managed to go as low as 148 fF,[6] resulting in a unit capacitance $C$ of only 280 aF. Eight LSBs of intentional systematic mismatch were also introduced on purpose to the DAC (+4 LSBs to the MSB capacitor and −2 LSBs to the MSB-1 and MSB-2 capacitors) in order to demonstrate the effectiveness of the proposed calibration approach. Split-capacitor topology is used to implement the CAP-DAC, as shown in Fig. 12(a).[7] Redundancy is introduced by adding an additional capacitor of size $8C$, which can compensate for variation in $V_{\mathrm{REF}}$ and/or settling errors with magnitude up to 32 LSB (≈ 60 mV). The CAP-DAC is laid-out using custom fringe capacitors in an inter-digitized manner, as shown in Fig. 12(b). These capacitors are formed between the vertical metal structures. In order to reduce parasitics due to coupling with the substrate, only metal layers 6 and 7 are used. As can be seen in the figure, the unit capacitors are distributed along the structure. This reduces the effect of process gradients in the horizontal direction. To reduce the length of the top-plate connection (metal 8), thereby reducing its parasitic resistance and capacitance, both circuit and layout techniques are adopted. At the circuit level, two LSB capacitors ($C$ and $2C$) are connected to ground on one side of the split-capacitor array [29], as indicated in Fig. 12(a) by blue color, resulting in an MSB capacitance of $128C$ rather than $256C$. In the layout, as shown in Fig. 12(b), the LSB capacitor is made by the same number of fingers as the LSB + 1 capacitor (1 finger) by using only one layer of metal (M6) rather than two (M6 + M7). This effectively halves the total number of fingers, hence reducing the length of the top metal connection.

[6]The $kT/C$ limit is lower than 148 fF for the resolution of the ADC. This value is chosen based on how much dynamic range loss could have been tolerated. This loss is mainly due to the unwanted parasitic capacitance at the top-plate of the CAP-DAC (e.g. metal routing parasitics, input capacitance of the compactor and top-plate parasitic of the DAC itself).

[7]For the sake of simplicity, capacitor $C_{00}$ is not shown in this figure.

### B. SAR Logic

The configuration of the SAR logic along with the asynchronous clock generator is shown in Fig. 13. The SAR logic of Fig. 13(a) is implemented using transmission-gate-based D-flip-flops (DFFs). A programmable delay block (chain

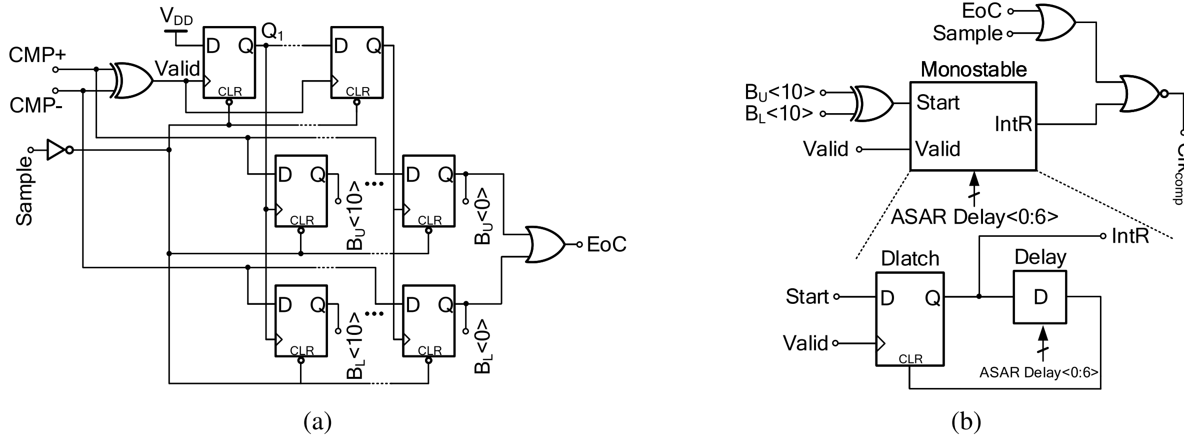


Fig. 13. (a) SAR logic. (b) Asynchronous clock generator of the SAR control logic.

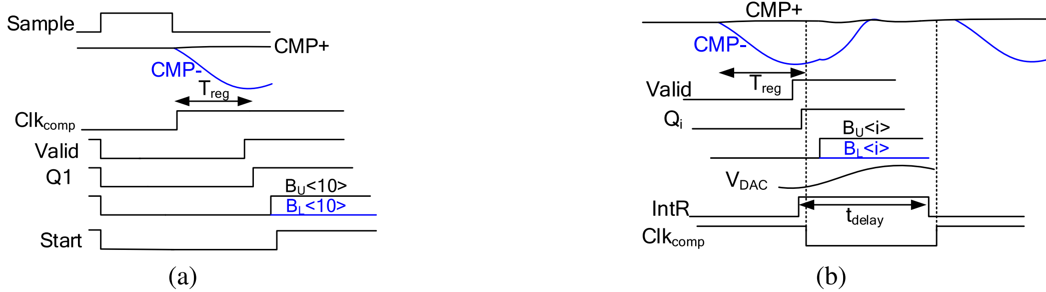


Fig. 14. Operational timing diagram of the SAR logic during the +MSB-bit decision (a), and for the following bits (b).

of inverters controlled by SPI) is used in the monostable pulse generator of Fig. 13(b), which introduces a delay, $t_{\text{delay}}$, that needs to be large enough to accommodate the digital logic propagation delays, $t_{\text{logic}}$, and the CAP-DAC capacitors settling time, $t_{\text{DAC}}$, i.e $t_{\text{delay}} > t_{\text{logic}} + t_{\text{DAC}}$.

Timing operation of the asynchronous clock generator is depicted in Fig. 14. When *Sample* (sampling signal of the ADC) goes high, the differential input analog signal is sampled on the capacitive DAC, and when it goes low, the comparator makes the first comparison. After a regeneration time, $T_{\text{reg}}$, the outputs of the comparator CMP+ and CMP− diverge. This would generate a *Valid* signal that triggers the top row of DFFs of the SAR logic. The MSB bits $B_U < 10 >$ and $B_L < 10 >$ are determined (depending on the sign of comparator output) causing *Start* to go high. From then onward and throughout 10 more cycles, the next bits (from MSB − 1 to the LSB) are determined as follows (Fig. 14(b)). When the comparator makes a successful comparison after its regeneration time, *Valid* goes high. This would clock the first row of DFFs, thus resulting in a bit decision followed by the settling of CAP-DAC top-plate voltage to a new value. *Valid* also triggers the monostable. This leads to generation of a pulse with on-time equal to $t_{\text{delay}}$ which resets the comparator for the next bit-decision.

### C. Comparator and Sampling Network

The double-tail comparator proposed in [30] is employed in this work as the main comparator. Neutralization cross-coupled capacitors are used to mitigate the effect of kick-back noise. The comparator achieves input-referred noise of $\sim 300\,\mu V_{\text{rms}}$ while consuming $\sim 120\,\mu$W at the full clock rate of 85 MS/s. The input capacitance of the main comparator is 23 fF. The auxiliary comparator, on the other hand, has an input capacitance of only 3 fF, hence exerting minimal impact on the total top-plate parasitic capacitance of the DAC. The average current consumption of the auxiliary comparator is $\sim 200\,\mu$A, which can be neglected for it is turned off during the normal operation. The measurement results also reveal input-referred noise of $\sim 1.75\,\text{mV}_{\text{rms}}$, which is consistent with the simulation results.

A pair of bootstrapped switches samples the analog input. Cross-coupled neutralization capacitors are employed here as well so as to mitigate the signal feed-through via the drain-source capacitance of the sampling switches.

### D. Mismatch Calibration

The proposed stochastic mismatch calibration algorithm as well as the offset calibration of the auxiliary comparator have been implemented using a standard digital synthesis flow in the targeted 28-nm CMOS. The inverse error function $\text{erf}^{-1}(x)$ (see Sec.III) is digitally approximated by a $1024 \times 16$ LUT. The entire mismatch calibration circuit is fully implemented on-chip. The mismatch calibration process starts by computing the mismatch from the LSB + 1 capacitor all the way up to the MSB capacitor for both the positive and the negative CAP-DACs, resulting in two sets of fractional binary numbers $E_P = \{e_{P,1}, e_{P,2}, \ldots, e_{P,N-1}\}$ and $E_N = \{e_{N,1}, e_{N,2}, \ldots, e_{N,N-1}\}$. To estimate the input voltage of the comparator using the discussed CDF method, a total of $2^{14}$ comparisons are carried out by the comparator.

It is worth mentioning that, since nodes $X_P$ and $X_N$ (i.e. the top-plates of positive and negative CAP-DACs) are left floating

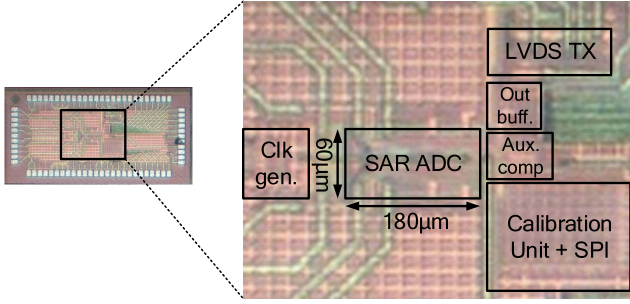


Fig. 15. Chip micrograph.

during phase III of the calibration process (Section III-B2), any leakage current at these nodes may result in an unwanted charge loss. Given the long duration of phase III ($2^{14}$ comparisons), even a small leakage current may result in a considerable discharge of $X_P$ and $X_N$, thus corrupting the voltage stored on these nodes. A viable solution is to break phase III into multiple shorter sub-phases, each followed by a reset, as explained in the following. Let us assume that the number of times the comparator is clocked during phase III is $k$ ($k = 2^{14}$ here). Hence, the cumulative distribution function $\Phi(V_X)$ would be equal to the total number of logic 1's produced by the comparator divided by $k$. Similarly, the comparator can be clocked $l$ times, where $l = k/c$ and $c$ is an integer, followed by a reset of nodes $X_P$ and $X_N$, and this can be repeated $c$ times. This would result in $c$ cumulative distribution functions $\Phi_1(V_X), \Phi_2(V_X), \ldots, \Phi_c(V_X)$. Due to the *stationary* nature of the comparator random noise, $\Phi(V_X)$ can therefore be expressed as

$$\Phi(V_X) = \frac{\Phi_1(V_X) + \ldots + \Phi_c(V_X)}{c}. \qquad (56)$$

This way, the time during which nodes $X_P$ and $X_N$ are left floating is shortened by a factor $c$. This *averaging* operation is also beneficial in eliminating detrimental effects of other noise sources, such as the $kT/C$ sampled thermal noise of switches $S_{rP}$ and $S_{rN}$ (see Fig. 8). Here, $l = 128$ is chosen. This produces 128 CDF functions, which are averaged out according to (56) to obtain the final CDF.

The whole calibration process takes about 5 ms using a 50 MHz clock. Once the calibration is completed, the calibration data ($E_P$ and $E_N$) are sent by SPI for storage. The mismatch is corrected off-chip numerically (as it would be using a downstream DSP) the way it was discussed in Section III-B2.

## V. Measurement Results

The proposed SAR ADC with the stochastic mismatch calibration has been fabricated in TSMC 28-nm LP CMOS and occupies a core area of 0.011 mm$^2$, as shown in Fig. 15. Figure 16 shows the DNL and INL plots of the ADC before and after calibration. Before the calibration, the maximum values of DNL and INL were +1.1/−1.0 LSB and +4.2/−3.6 LSB, respectively, whereas, after the calibration, these values improved to +0.7/−0.8 LSB and +0.7/−0.7 LSB.

Fig. 17 shows the ADC Nyquist output spectrum of an input 39.9 MHz sinewave sampled at 85 MS/s. After the foreground mismatch calibration, the ADC achieves SFDR and SNDR of 60.5 dB and 56.8 dB SNDR, respectively, which is an improvement of 14.9 dB and 11.5 dB compared to the no calibration case (approximately 2 bit ENOB), demonstrating the effectiveness of the proposed mismatch calibration technique. The residual SFDR is mainly limited by the nonlinearity of the input sampling switch while the residual SNDR is limited by the thermal noise of the circuit, including the $kT/C$ noise and the comparator noise.

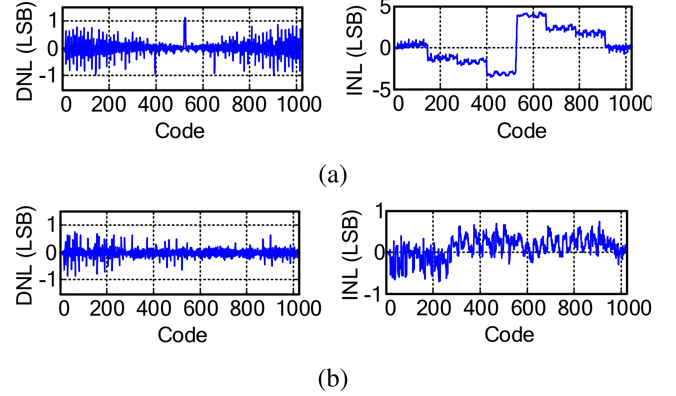


Fig. 16. Static performance of the ADC (a) before and (b) after the calibration.

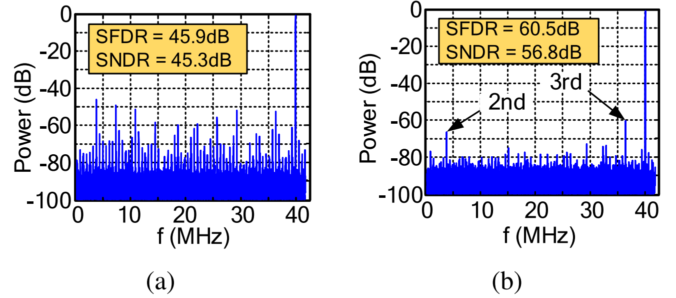


Fig. 17. ADC output spectrum at a sampling frequency of 85 MS/s and Nyquist-rate input (a) before calibration, (b) after calibration. The number of points for the FFT calculation are $2^{14}$.

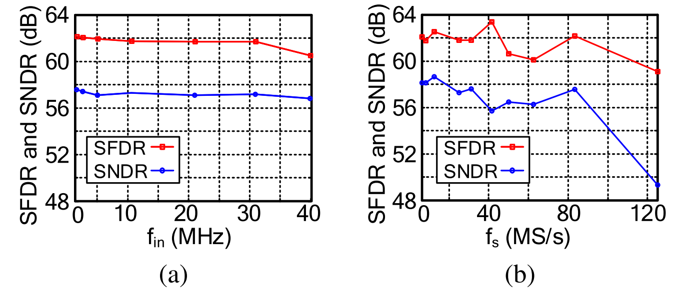


Fig. 18. Calibrated SFDR and SNDR vs. (a) input frequency at a sampling rate of 85 MS/s, (b) sampling frequency for a 1.5 MHz input.

Fig. 18(a) shows the dynamic performance of the ADC versus the input sinewave frequency at a sampling rate of 85 MS/s, showing a SFDR and SNDR deterioration, from low- to high-frequency, of 1.8 dB and 0.7 dB, respectively. The dynamic performance of the ADC is also presented versus the sampling frequency, using a 1.5 MHz sinewave input. As shown in Fig. 18(b), SFDR and SNDR are above 60 dB and 55.8 dB, respectively, up to a sampling frequency of 85 MS/s.

TABLE I
PERFORMANCE COMPARISON

| | [31] | [32] | [33] | This work |
|---|---|---|---|---|
| Technology (nm) | 90 | 65 | 28 | 28 |
| Calibration | Off-chip | Off-chip | On-chip | On-chip |
| Calibration Time | 11 $\mu$s | 20 ms | - | 5 ms |
| Supply voltage ($V$) | 1.2 | 1.2 | 1.1 | 0.9 |
| Input swing ($V_{pp,d}$) | 2 | 2.4 | 1.7 | 1.75 |
| Resolution (bits) | 12 | 12 | 12 | 10 |
| Sampling rate (MS/s) | 120 | 50 | 104 | 85 |
| DNL/INL (LSB) | 0.8/2.3 | 1.2/1/9 | 0.5/1.1 | 1.5/1.4 |
| SFDR (@Nyq.) | 68 | 67 | 52 | 61 |
| ENOB (bits) | 10.39 | 10.9 | 10.2 | 9.14 |
| Power (mW) | 3.2 | 2.1 | 0.88 | 0.52 |
| FoM (fJ/conv-step) | 28 | 21.9 | 7.3 | 10.9 |

Running at 85 MS/s under a 0.9 V supply, the ADC consumes 582 $\mu$W, comprising 267 $\mu$W (46%) consumed by the SAR logic, 219 $\mu$W (33%) by the CAP-DACs, and 121 $\mu$W (21%) by the comparator. The measured Walden and Schreier figure-of-merit (FoM) at Nyquist rate are 10.9 fJ/conv-step and 165.9 dB, respectively. Table I compares the performance of this ADC with other state-of-the-art mismatch-calibrated SAR ADCs.

## CONCLUSION

This paper reviews some of the most relevant techniques for mismatch detection and correction of capacitive-DAC capacitors in SAR ADCs. It proposes a fully-automated method which combines self-calibration with a stochastic estimation of the input of a noisy comparator to effectively detect the mismatch error of the capacitive DAC in a 10-bit SAR ADC. It also proposes a new fully integrated method to compute the input-referred noise and offset of a comparator, which are the primary information needed to exploit the proposed stochastic mismatch calibration technique. Experimental results of the prototype 10-bit SAR ADC, operated at a sampling frequency of 85 MS/s, demonstrate calibration improvements in SNDR and SFDR of 11.5 dB and 14.6 dB, respectively, resulting in a Walden FoM of 10.9 fJ/conv-step.

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