Distortion Contribution Analysis for Identifying EM Immunity Failures

Lammert Duipmans, Dusan Milosevic, *Member, IEEE*, Arnoud van der Wel, *Member, IEEE*, and Peter Baltus, *Senior Member, IEEE*

***Abstract*— One of the main causes of expensive IC redesigns is a failure to meet electromagnetic compatibility (EMC) requirements. For this reason, there is a huge demand for verification methods to identify and prevent immunity failures on chip. Strongly nonlinear effects, in particular DC operating point shifts, are a major cause of such immunity failures. Conventional analysis techniques, used to simulate these strongly nonlinear effects, suffer from a few drawbacks. They can be time-consuming and suffer from convergence issues. Moreover, they do not provide insight into the root causes of the nonlinear behavior. In this paper, an automated method is proposed that overcomes the mentioned drawbacks and identifies causes of immunity failures by listing critical distortion contributions. The method is applicable to very large, strongly nonlinear integrated circuits. It uses a simple model that determines the nonlinear contribution of one device in its linearized environment. Because the computation time is negligible, the analysis can be repeated for many devices and interference frequencies. Additionally, the method gives insight into the drivers responsible for the distortion effects, such that the designer can efficiently solve the problem. The method is demonstrated by applying it to a practical test case.**

***Index Terms*— Distortion contribution analysis, electromagnetic compatibility, harmonic balance, nonlinear distortion, polynomial device model, strongly nonlinear behavior, verification.**

I. Introduction

ELECTROMAGNETIC compatibility (EMC) requirements are getting stricter due to a more widespread use of electronics and a trend towards more connectivity. This is especially noticeable in the automotive industry where an increased use of electronic systems brings about a challenging electromagnetic environment [1]. In such an environment, systems must be immune to high levels of interference. Failure to meet these requirements is one of the main causes of expensive IC redesigns [2]. Therefore, it is important to identify immunity problems in an early stage of the design process.

If an interferer is injected into a circuit, some devices can operate nonlinearly and cause distortion effects that disrupt the functional behavior of the circuit. For example, the interferer can drive a transistor out of its operating region, consequently producing a DC operating point shift that causes a functional failure. Such strongly nonlinear effects are a major cause of EMC failures on chip [3], [4]. The conventional analysis techniques that are used to simulate these nonlinearities suffer from a few drawbacks. First, they can be time-consuming. This is especially the case when methods based on direct numerical integration (i.e. a transient analysis) are used to simulate circuits with a combination of high frequency content and large time constants or large frequency differences. Secondly, they can suffer from convergence problems, which is quite common for a harmonic balance (HB) analysis when applied to large-scale, strongly nonlinear circuits [5], [6]. The third drawback is that these analysis techniques do not provide insight into the root causes of the nonlinear effects. They tell the designer what will happen, not how and why it is happening, such that redesigning often remains a matter of trial-and-error.

The problem addressed in this paper is to develop an automated method that points to causes of immunity failures by identifying critical contributions to distortion effects. It needs to be applicable to very large ICs with strong nonlinearities and should not suffer from the above-mentioned drawbacks. The focus will be on time-invariant circuits with a discrete frequency spectrum. Only few methods have been published that focus on the combination of computational efficiency and gaining insight specifically for EM immunity verification. In [7]–[9], individual devices are pinpointed that are potential contributors to immunity failures. However, the method in [7], [8] does not result in a quantified prediction of distortion components and the method in [9] still requires carrying out many DC analyses of the full circuit and focuses only on DC shifts. There remains a need for a proper distortion contribution analysis (DCA) for immunity verification. A DCA serves for splitting the total distortion into different contributions and identifying the dominant contributions. Several different implementations of a DCA have been published [10]–[21]. However, these DCAs are not suitable candidates for solving the given problem for a few reasons. First, several analyses demand an initial step in which a transient or HB simulation is carried out at least

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Lammert Duipmans, Dusan Milosevic, and Peter Baltus are with the Department of Electrical Engineering, Eindhoven University of Technology, 5600 MB Eindhoven, The Netherlands (e-mail: l.j.duipmans@tue.nl; d.milosevic@tue.nl; p.g.m.baltus@tue.nl).

Arnoud van der Wel is with NXP Semiconductors, 5656 AE Eindhoven, The Netherlands (email: arnoud.van.der.wel@nxp.com).

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once. This is done to either determine the full nonlinear response upfront [10]–[14], or to simulate the response of the full circuit when test signals are applied for inspecting certain nonlinearities [15], [16]. For large circuits containing thousands of transistors, such a step suffers from the first and second drawbacks mentioned previously. The second reason is that many of these analyses are only applicable to weakly nonlinear circuits [10], [11], [17], [18], while the aim is to gain insight into strongly nonlinear effects. They are commonly based on Volterra series theory [22] and are valid only when the nonlinear response can be seen as a slight variation of the dominant first-order response. Some methods in the field of power amplifiers have been presented that are able to analyze strongly nonlinear effects [19]–[21]. However, they assume low feedback conditions, such that higher-order effects will not affect the input signal much. This assumption is very limiting for many types of real-life circuits.

In this paper, we propose a method that overcomes the mentioned limitations. It provides a highly computationally efficient model for determining the influence of the nonlinearity of any one device in its linearized environment, whereby full account is taken of feedback behavior and strongly nonlinear effects. An HB analysis is carried out to analyze the equivalent model. Because the analysis time of the model is negligible, it is easy to repeat the analysis for multiple devices and interference frequencies. For providing the inputs to the model, the method needs to perform a) one DC simulation to determine the operating point of the full circuit, b) one AC simulation of the whole circuit in the presence of the interferer and c) one AC simulation per device that needs to be investigated. Next to pointing to the most critical devices, we show which design parameters are playing a role in generation of the distortion. The proposed method identifies four different drivers for distortion generation: 1) the transfer from the interference input to the nonlinear device, 2) the feedback from the nonlinear device output back to its input, 3) the nonlinear device characteristic itself, and 4) the transfer from the distortion source to the output. These drivers can be controlled by the designer to improve immunity of the circuit.

It is worth mentioning that although the method can analyze strongly nonlinear effects, it only determines the responses when the nonlinearity of one device at a time is included; we neglect nonlinear interaction between devices. Therefore, the method should not be used to obtain an accurate representation of the complete circuit, but rather it serves for pointing to the causes of strongly nonlinear effects, i.e. accuracy is exchanged for insight and speed.

In Section II-A and II-B, we introduce the model that is used to separate the total distortion into contributions per device. To gain insight into the role the four mentioned drivers play in distortion generation, we need to analyze the model in more detail. For this purpose, a polynomial approximation of the nonlinear function is made, which is demonstrated in Section II-C. Using this polynomial model, Volterra theory is applied to obtain closed-form expressions of the model in Section II-D. Though these expressions only guarantee accurate results for weakly nonlinear systems, they do provide insight into the triggers of strongly nonlinear effects. To also identify the dominant nonlinearities for strongly nonlinear systems, a simple extension to the method is proposed in Section II-E. In Section III, the complete method is described step by step and its computational efficiency is proven. Subsequently, the method is applied to a level shifter circuit in Section IV. In Section V, conclusions are drawn.

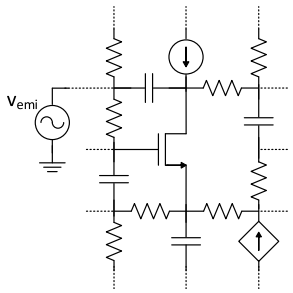

Fig. 1. Circuit to inspect influence of nonlinearity of one device in its linear environment.

II. Model for Device-Wise Nonlinear Analysis

In this section, we introduce the model that is used to calculate the effect of the nonlinearity of a certain device on the signal waveforms. This is useful to identify the sources of strongly nonlinear effects that are often the cause of immunity failures.

Suppose a continuous-wave (CW) electromagnetic interference (EMI) source is applied to one of the pins of a complex nonlinear circuit that has a fixed DC operating point. The circuit is assumed to be implemented in a CMOS technology, with transistors being the dominant sources of nonlinearity. As a starting point, we perform a DC and AC analysis to obtain a first-order representation of the performance of the circuit and the propagation of the interferer. We want to investigate the deviation from this linear behavior when we include the nonlinearity of one specific transistor while retaining all other small-signal models, as depicted in Fig. 1. For this, we replace the small-signal model of the transistor by a nonlinear model that models the behavior around its DC bias point. We want to exploit the fact that the largest part of the circuit is linear and that this part can efficiently be characterized in the frequency domain. For this purpose, a computationally efficient equivalent circuit diagram of the circuit in Fig. 1 has been developed. In the next section, we treat the equivalent diagram, assuming that i_{DS} is a function of only v_{GS}. In Section II-B, we extend the model for a two-dimensional transistor current dependent on both v_{GS} and v_{DS}.

A. Model for One-Dimensional Transistor Current

The equivalent diagram of the circuit in Fig. 1 is shown in Fig. 2. The circuit models the nonlinear behavior around the DC bias point. The transistor model consists of an independent current source and a voltage-controlled current source that represent the linear (i_{lin}) and nonlinear (i_{nonl}) part of the output current, respectively. i_{lin} is equal to $g_m \cdot v_{gs,lin}$, where g_m is the transconductance. Both i_{lin} and $v_{gs,lin}$ can be

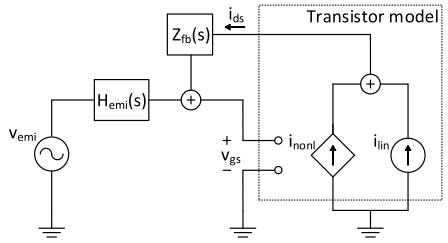

Fig. 2. Equivalent diagram of circuit in Fig. 1, assuming one-dimensional transistor current.

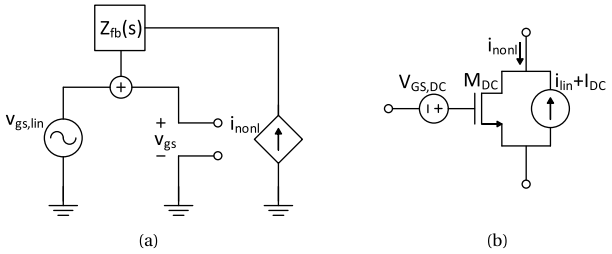

Fig. 3. (a) Equivalent diagram for simulating nonlinearity contributions per device. (b) Implementation of nonlinear current function.

found by the AC analysis. The Laplace transform of $v_{gs,lin}$ is given by:

$$V_{gs,lin}(s) = V_{emi}(s)\frac{H_{emi}(s)}{1 - g_m Z_{fb}(s)} \tag{1}$$

i_{nonl} is defined as $\mathrm{f}(v_{gs}) - g_m \cdot v_{gs,lin}$, in which $\mathrm{f}(\ldots)$ is the nonlinear function of the DC transistor characteristic around the bias point. If i_{nonl} is left out, the steady-state circuit response is exactly equal to that found by the AC analysis. Adding i_{nonl} is equivalent to adding the nonlinearity of one transistor. It will be shown that by separating the transistor current into a linear part and a nonlinear part, we can further simplify the equivalent diagram in Fig. 2 and efficiently re-use the AC simulation results for every transistor of which we want to inspect the nonlinearity contribution.

The surrounding linear components in Fig. 1 are characterized by two linear transfer functions. One that represents the gain from the EMI source to the input port of the transistor with the output current replaced by an open circuit:

$$H_{emi}(s) = \left.\frac{V_{gs}(s)}{V_{emi}(s)}\right|_{i_{ds}=0} \tag{2}$$

and a transimpedance that represents the feedback from the output current to the input port of the transistor with the interference source replaced by a short circuit:

$$Z_{fb}(s) = \left.\frac{V_{gs}(s)}{I_{ds}(s)}\right|_{v_{emi}=0} \tag{3}$$

where $V_{gs}(s)$, $V_{emi}(s)$ and $I_{ds}(s)$ are the Laplace transform of the gate-source voltage, the interference voltage and the output current, respectively. The linear transfer functions include the influence of the equivalent capacitances of the transistor. This way, the linear dynamic behavior of the transistor is separated from the nonlinear static behavior. In other words, we assume the frequency-dependent behavior can be modeled by only linear components and the nonlinear behavior can be modeled by a static source. Though the equivalent capacitances of the transistor can be nonlinear as well, the most dominant sources of nonlinearity in a MOSFET are the transconductance and output conductance [23], so this is a fair approximation.

For the Laplace transform of the gate-source voltage, we can say the following:

$$\begin{aligned} V_{gs}(s) &= V_{emi}(s)H_{emi}(s) + I_{ds}(s)Z_{fb}(s) + V_{GS,DC}\,\delta(s) \\ &= V_{emi}(s)H_{emi}(s) + \mathcal{L}\left(\mathrm{f}\left(v_{gs}(t)\right)\right)Z_{fb}(s) \\ &\quad + V_{GS,DC}\,\delta(s) \end{aligned} \tag{4}$$

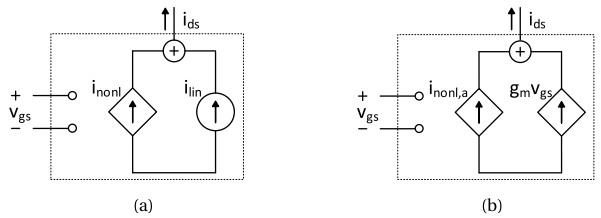

Fig. 4. (a) Proposed transistor model. (b) Alternative transistor model.

where $V_{GS,DC}$ is the DC voltage of the gate-source voltage as calculated by the DC analysis, i.e. when the interferer is not connected, and $\mathcal{L}(\ldots)$ is the Laplace transform. Because the network excluding the nonlinear model of the transistor is purely linear, we can use superposition. Due to the nonlinear function inside the equation, it is not straightforward to solve this equation analytically. It is possible to approximate the nonlinear function with a polynomial and use Volterra series to come to a solution, as we will demonstrate in Section II-D.

Since we separated the output current into a linear and nonlinear part, we can rewrite (4):

$$\begin{aligned} V_{gs}(s) &= V_{emi}(s)H_{emi}(s) + I_{lin}(s)Z_{fb}(s) + I_{nonl}(s)Z_{fb}(s) \\ &\quad + V_{GS,DC}\,\delta(s) \\ &= V_{gs,lin}(s) + I_{nonl}(s)Z_{fb}(s) + V_{GS,DC}\,\delta(s) \\ &= V_{gs,lin}(s) + V_{gs,nonl}(s) + V_{GS,DC}\,\delta(s) \end{aligned} \tag{5}$$

Hence, $V_{gs}(s)$ consists of a linear, nonlinear and DC part. The linear part and DC part are already known from the previously carried out DC and AC analyses, whereas the nonlinear part is still unknown. Using this information, we can further reduce the equivalent diagram, resulting in the new diagram depicted in Fig. 3a. It is also possible to use a similar transistor model as in Fig. 2 in which i_{ds} is separated in such a way that i_{lin} is a dependent current source equal to $g_m \cdot v_{gs}$, instead of an independent current source, see Fig. 4. In the end, this gives the same results. However, the current approach avoids the need for including the influence of g_m in the feedback transimpedance in the simplified diagram in Fig. 3a. Moreover, when working with an independent current source, the AC analysis results serve as a convenient reference. We will see later that for low feedback conditions, v_{gs} approximates $v_{gs,lin}$, while for high feedback conditions, i_{ds} tends to follow i_{lin}. The model provides a more intuitive understanding of this mechanism.

The input that excites the nonlinear function of the model in Fig. 3a is $V_{gs,lin}(s)$. In case there are more inputs to the system than just the one interference source, $v_{gs,lin}$ becomes a sum of sinusoids with different frequencies. The diagram in Fig. 3a can be generated for every transistor in the circuit. The AC analysis that we carried out to estimate the propagation of the interferer now also gives us $V_{gs,lin}(s)$ of all transistors in the circuit. The nonlinear part of the output current can be implemented as shown in Fig. 3b. In this figure, M_{DC} is the full static model of the transistor that is valid at DC. A DC voltage source $V_{GS,DC}$ is added to make sure the transistor is operating at its DC bias point. By subtracting the linear and DC part from the total current, the nonlinear part remains.

To find the nonlinear waveforms, the diagram in Fig. 3a can be simulated using an HB analysis. This analysis is applicable, because we are mainly interested in the steady-state response of the circuit and we consider the problem with a limited number of known input frequencies.

B. Model for Two-Dimensional Transistor Current

The analysis of the previous section can be extended for a multivariate nonlinear function. The equivalent diagrams including a transistor with both v_{GS} and v_{DS} dependency can be seen in Fig. 5. In this circuit, the nonlinear output current is now a two-input function and an extra branch is added for determining $V_{ds,nonl}(s)$. The associated equations for the signals are as follows:

$$V_{gs}(s) = V_{gs,lin}(s) + I_{nonl}(s)Z_{gs}(s) + V_{GS,DC}\,\delta(s) \quad (6)$$

$$V_{ds}(s) = V_{ds,lin}(s) + I_{nonl}(s)Z_{ds}(s) + V_{DS,DC}\,\delta(s) \quad (7)$$

$$I_{lin}(s) = g_m V_{gs,lin}(s) + g_{ds} V_{ds,lin}(s) \quad (8)$$

$$V_{gs,lin}(s) = V_{emi}(s)H_{lin,gs}(s) = V_{emi}(s) \times \frac{H_{gs}(s)\,(1 - g_{ds}Z_{ds}(s)) + H_{ds}(s)g_{ds}Z_{gs}(s)}{1 - g_m Z_{gs}(s) - g_{ds}Z_{ds}(s)} \quad (9)$$

$$V_{ds,lin}(s) = V_{emi}(s)H_{lin,ds}(s) = V_{emi}(s) \times \frac{H_{ds}(s)\left(1 - g_m Z_{gs}(s)\right) + H_{gs}(s)g_m Z_{ds}(s)}{1 - g_m Z_{gs}(s) - g_{ds}Z_{ds}(s)} \quad (10)$$

In the remainder of this paper, we will work with a two-input function for the transistor current. The diagram in Fig. 5b needs a couple of inputs: the DC and AC values of the device output current and input voltages and the feedback transimpedances $Z_{gs}(s)$ and $Z_{ds}(s)$. The idea of splitting the current of the transistor into a part that is calculated from the AC simulation and a nonlinear part is to efficiently re-use the results of the AC simulation that is carried out to estimate the propagation of the interferer. To obtain the inputs for the model, we need to perform:

- One DC simulation to determine the DC excitation of all transistors.
- One AC simulation to determine the AC excitation of all transistors.
- One AC simulation per transistor to determine $Z_{gs}(s)$ and $Z_{ds}(s)$.

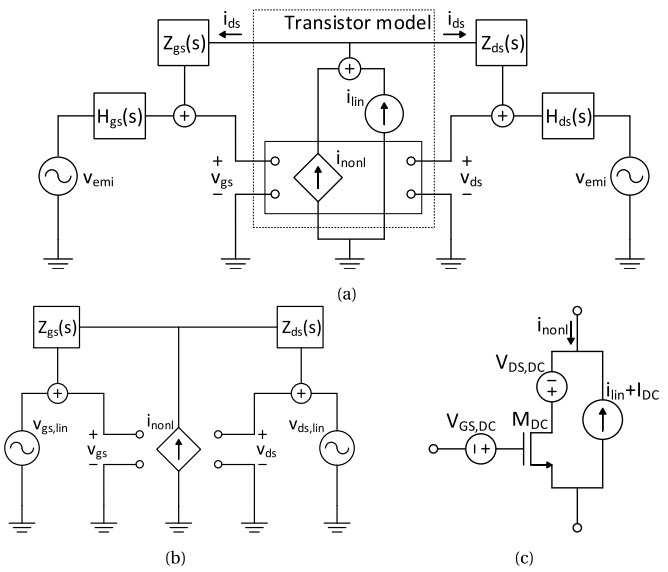

Fig. 5. (a) Equivalent diagram for nonlinearity contributions per device for two-dimensional transistor current. (b) Simplified diagram for simulation. (c) Implementation of nonlinear current function.

When the inputs are obtained, $m \cdot n$ HB analyses are carried out to find the nonlinear waveforms, with m being the number of devices and n the number of interference frequencies. Because the model is described by only two nonlinear equations with two unknowns, computation time is negligible, no matter how large the original circuit is. Moreover, many devices will most likely not contribute much to the distortion. To limit the number of simulations, we can include only those devices and interference frequencies for which the interference level at the input ports is significant. In [7], [8], devices are preselected based on the occurrence of operating region transitions. The AC simulation used for finding the feedback impedances also serves for determining all node voltages in the surrounding linear part of the circuit as soon as i_{DS} is known. This is because the AC simulation gives us the transfer functions from the nonlinear output current to all node voltages. How to use the model to find distortion contributions is described in more detail in Section III.

C. Polynomial Modeling

When running an HB analysis on the diagram in Fig. 5b, we get an accurate representation of the waveform. However, the HB analysis solves a set of nonlinear equations numerically and therefore does not provide closed-form expressions showing the relation between design parameters and the circuit response. Instead, it is possible to use a recursive method, such as Volterra series theory [22] or perturbation analysis [24]. A polynomial description of the nonlinear devices in the circuit is needed in this case. Commonly this is done by generating a Taylor polynomial of the nonlinear functions. A problem with this approach is the difficulty of determining the higher-order derivatives [10]. Additionally, the Taylor series suffers from a limited convergence radius, especially for transistors biased close to operating region boundaries [20].

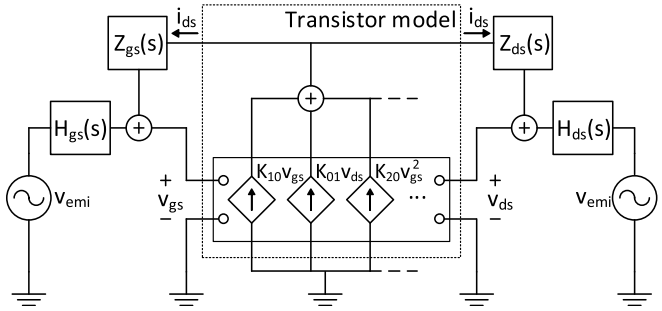

Fig. 6. Equivalent diagram for analyzing nonlinear contributions per device with polynomial transistor current.

To solve these issues, we fit the polynomial models from simulated I-V data using a least squares approximation [25]. The fitting procedure needs to be done over a representative range of inputs, for example the calculated linear excitation. We choose to use the actual amplitude range of the inputs, found using the HB analysis. A two-dimensional transistor current is assumed and the characteristic is approximated with a third-order polynomial:

$$\begin{aligned} i_{DS} = \mathrm{f}(v_{gs}, v_{ds}) = {} & K_{00} + K_{10}v_{gs} + K_{20}v_{gs}^2 + K_{30}v_{gs}^3 \\ & + K_{01}v_{ds} + K_{02}v_{ds}^2 + K_{03}v_{ds}^3 + K_{11}v_{gs}v_{ds} \\ & + K_{21}v_{gs}^2 v_{ds} + K_{12}v_{gs}v_{ds}^2 \end{aligned} \tag{11}$$

The fitting can be done either in the time domain or frequency domain. In the method proposed in this paper we perform the fitting in the time domain. To sample all combinations of i_{ds}-v_{gs}-v_{ds} values within the signal range, the inputs v_{gs} and v_{ds} need to be uncorrelated and they are thus chosen orthogonally. This is achieved by applying a sine wave with frequency f_l for input v_{gs} and another sine wave with frequency f_h for input v_{ds}, with f_l and f_h taken as incommensurate frequencies. The amplitudes of these tones are set to $v_{gs,max} - v_{gs,min}$ and $v_{ds,max} - v_{ds,min}$ respectively, while their DC values are set right in between the max and min voltages. These values are determined from the previously carried out HB analysis. After simulating the transistor with the fixed input voltages using a transient analysis for several periods, the corresponding i_{ds} samples can be determined. Subsequently, the sampled data is interpolated and curve fitting is applied, leading to a fitted set of nonlinearity coefficients. We can repeat this process for every interference frequency. This way, we end up with an optimum set of fitted nonlinearity coefficients that suits the signal range for that interference frequency.

D. Volterra Series Theory

Now that the fitted nonlinearity coefficients have been determined, we can analyze the circuit diagram in Fig. 6 using Volterra series theory, as described in [22]. The aim is to obtain closed-form expressions, showing the relation between model inputs and generated distortion. The transistor current is now built up of parallel current sources, corresponding to the different terms in (11). The first-order transfer functions can be determined by replacing g_m and g_{ds} by the fitted coefficients K_{10} and K_{01} in (9) and (10):

$$\begin{aligned} & H_{1,vgs,lin}(s) \\ & \quad = H_{fb}(s)\left(H_{gs}(s)\left(1 - K_{01}Z_{ds}(s)\right) + H_{ds}(s)K_{01}Z_{gs}(s)\right) \end{aligned} \tag{12}$$

$$\begin{aligned} & H_{1,vds,lin}(s) \\ & \quad = H_{fb}(s)\left(H_{ds}(s)\left(1 - K_{10}Z_{gs}(s)\right) + H_{gs}(s)K_{10}Z_{ds}(s)\right) \end{aligned} \tag{13}$$

with:

$$H_{fb}(s) = \frac{1}{1 - K_{10}Z_{gs}(s) - K_{01}Z_{ds}(s)} \tag{14}$$

Equations (12) and (13) reduce to $H_{lin,gs}$ (9) and $H_{lin,ds}$ (10) when V_{emi} goes to zero and K_{10} and K_{01} become equal to g_m and g_{ds}, respectively. H_{fb} is the transfer function caused by the feedback path through Z_{gs} and Z_{ds}. The equivalent circuit diagram can be interpreted as an amplifier circuit with feedback, in which the loop gain is:

$$LG(s) = K_{10}Z_{gs}(s) + K_{01}Z_{ds}(s) \tag{15}$$

For the second-order nonlinear transfer functions, we have:

$$H_{2,ids}(s_1, s_2) = H_{fb}(s_1 + s_2)H_{2,inonl}(s_1, s_2) \tag{16}$$

$$\begin{aligned} H_{2,inonl}(s_1, s_2) = {} & K_{20}H_{1,vgs}(s_1)H_{1,vgs}(s_2) \\ & + K_{02}H_{1,vds}(s_1)H_{1,vds}(s_2) \\ & + \frac{1}{2}K_{11}\left(H_{1,vgs}(s_1)H_{1,vds}(s_2)\right. \\ & \left. + H_{1,vgs}(s_2)H_{1,vds}(s_1)\right) \end{aligned} \tag{17}$$

The expression for the nonlinear current source of order two is derived in [26]. For full expressions of the third-order nonlinear transfer functions, the reader is referred to [26].

It appears there is a common term for all nonlinear transfer functions, being the feedback transfer function H_{fb}. From the nonlinear current method [22], it follows that all higher-order nonlinear current sources appear in parallel to the linear part $K_{10}v_{gs}$ and $K_{01}v_{ds}$. Then, similar to the second-order transfer function of the nonlinear current in (16), all higher-order nonlinear current transfer functions are multiplied by H_{fb} to come to the total current. Because the higher-order current sources are calculated recursively from lower-order transfers, they are dependent on the same transfer function H_{fb}, evaluated at different frequencies. This means that H_{fb} can be adjusted to minimize certain distortion components. For example, we can increase the loop gain $K_{10}Z_{gs} + K_{01}Z_{ds}$ at a frequency where we want to reduce distortion. Ideally we want to minimize $V_{gs,lin}$ and $V_{ds,lin}$, or even better: H_{gs} and H_{ds}. They lie at the root of all distortion behavior; if the interferer would not arrive at the nonlinear device inputs, the signal would not get distorted in the first place. However, it is not always possible to block the path from interferer to nonlinear device without affecting the desired operation of the circuit. Adjusting H_{fb} is an extra means for the designer to minimize distortion.

It is important to note that even though the fitted polynomial approximation of the nonlinear function converges, this is not a guarantee that the Volterra series itself converges. For

higher input amplitudes, the higher-order terms may relatively increase more than the lower-order terms, resulting in a diverging series. The convergence radius of the Volterra series representation is dependent on the nonlinear function characteristic and the amount of feedback. There are no general criteria or methods available for determining this convergence radius [26], [27]. It is therefore hard to predict for which systems a Volterra series can still be used to approximate a given nonlinear system. For this reason, often only weakly nonlinear systems are used. However, if we exclude unstable systems, Volterra series do give an accurate representation of the response for lower input amplitudes to most systems and can provide insight into the triggers of strongly nonlinear effects that arise when the input amplitude grows.

E. Impact of Nonlinearity Coefficients

Using the HB analyses of the developed model, we can separate distortion into contributions per device. Using Volterra theory, we can see these distortion components as a sum of mixing products as a function of the nonlinearity coefficients and the input. The problem with Volterra theory is that it only guarantees accurate results for weakly nonlinear systems. Since most immunity problems are caused by strongly nonlinear behavior, it is useful to also gain insight into contributions per nonlinearity coefficient for strongly nonlinear systems. However, there are no general methods available yet to obtain closed-form expressions of strongly nonlinear systems [26]. This means it is in most cases not possible to find a causal relation between the distortion components and the input amplitude and phase.

Instead, it is possible to simply check how the nonlinear function is excited and see which nonlinearity coefficients play the largest role in the formation of the nonlinear output current. Since we approximated the output current of the transistor with a third-order polynomial, we can characterize the total current as a sum of parallel current sources as in Fig. 6. By checking the value of each of the parallel current sources at a given frequency, we get an indication of the dominant nonlinearity coefficients for a certain distortion component. The value of the parallel current sources can be calculated by substituting the v_{gs} and v_{ds} signals that are determined with the HB analysis in (11). This way, a distortion component can be viewed as a sum of phasors, each attributable to different coefficients corresponding to the different parallel current sources:

$$I_{ds,\omega_x} = I_{ds,\omega_x,K_{10}} + I_{ds,\omega_x,K_{20}} + I_{ds,\omega_x,K_{30}} + \ldots \quad (18)$$

in which I_{ds,ω_x} is the phasor of the total output current at frequency ω_x, and $I_{ds,\omega_x,K_{mn}}$ the phasor of the parallel current source corresponding to coefficient K_{mn} at frequency ω_x, with m and n being an integer.

To sum up the considerations presented in Section II, an intuitive, computationally efficient model for analyzing nonlinearity contributions per device is proposed. By characterizing its nonlinear function as a polynomial, closed-form expressions are determined for weakly nonlinear systems. For strongly nonlinear systems, insight into nonlinear behavior is gained by identifying the dominant nonlinearity coefficients of the polynomial.

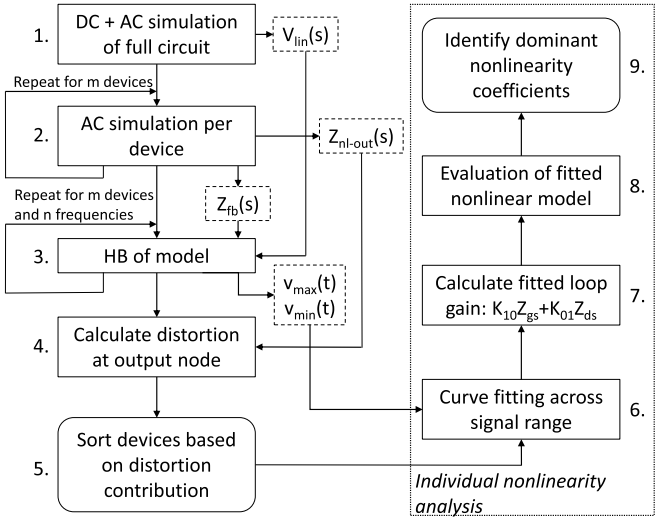

Fig. 7. Flowchart of the method.

III. METHOD

A. Implementation of the Method

In this section, we will briefly describe the different steps of the proposed distortion contribution analysis. The flowchart is shown in Fig. 7.

1. The first step is to perform a DC operating point analysis and an AC analysis on the full circuit with the interference source connected. From the simulation results, we acquire the linear signals associated with the transistors, i.e. $v_{gs,lin}$, $v_{ds,lin}$, $V_{GS,DC}$, $V_{DS,DC}$, i_{lin} and I_{DC}. These signals serve as input to the model. A preselection can be carried out [7], [8] to include only those devices in the analysis that see a significant part of the interferer at their input ports.
2. After determining the transistors to be included in the analysis, we perform one extra AC analysis per transistor for obtaining the feedback transimpedances $Z_{gs}(s)$ and $Z_{ds}(s)$. In this step, the transistor is effectively replaced by an AC current source with unit magnitude that is connected between the drain and the source while the interference source is set to zero. For this purpose, several components are added to a transistor under investigation, as shown in Fig. 8. Both the capacitance and inductance are ideal components that have an infinite value. The capacitance ensures that the current sources are not disturbing the DC operating point. The inductance prevents the bottom node of the capacitance from becoming a floating node for DC. The sum of the AC currents $g_m v_{gs}$ and $g_{ds} v_{ds}$ has the same magnitude as the small-signal i_{ds}, but opposite sign, such that i_{ds} is effectively replaced by i_{ac} and the parasitic capacitances of the transistor are included in the AC analysis. In the AC simulation results, the value of $V_{gs}(s)$ and $V_{ds}(s)$ is equal to $Z_{gs}(s)$ and $Z_{ds}(s)$, respectively. From the same simulation, also the

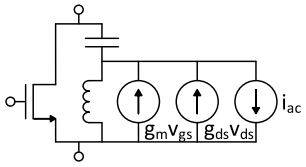

Fig. 8. Circuit for effectively replacing the transistor with an AC current source, which is used for determining $Z_{gs}(s)$ and $Z_{ds}(s)$.

transfer function from $I_{ds}(s)$ to any node in the circuit becomes apparent.

3. The next step is to carry out an HB analysis of the circuit diagram in Fig. 5b for all relevant devices and interference frequencies. Using the model, the nonlinear spectra of the transistor signals are determined for the situation where the nonlinearity of one transistor at a time is included.
4. Since the spectrum of the nonlinear output current is known, it can be multiplied by the transimpedance $Z_{nl-out}(s)$ to obtain the distortion at any given output node due to a specific device.
5. Now that the distortion components caused by all selected devices can be calculated, we can sort the different devices in terms of their generated distortion. We can, for example, identify the main contributors to a DC shift at a given output node. Another possibility is to use a more general criterion, in which the devices are arranged in terms of the sum of the power at all harmonic frequencies.
6. So far, the distortion components are separated into contributions per device. To identify the drivers for the individual nonlinearity contributions, four extra steps are carried out. First, curve fitting across the input signal range is applied to the transistor under investigation. The i_{DS} samples are obtained by running a transient analysis with fixed, orthogonal inputs, as described in Section II-C. The fitting results in a set of nonlinearity coefficients that describes the transistor current with a third-order polynomial approximation. Because the input signal range can vary for different interference frequencies, the curve fitting is carried out for all interference frequencies.
7. Using the generated first-order coefficients, it is possible to determine the fitted loop gain. The loop gain tells how much the generated distortion of a certain transistor is counteracted by the feedback loop and is one of the means for the designer to minimize distortion.
8. Next, the nonlinear signals v_{gs} and v_{ds} are substituted in the fitted polynomial approximation of the nonlinear current function. v_{gs} and v_{ds} are known for all selected devices, because they have been calculated in step 3.
9. By separating the total current into portions attributable to the different nonlinearity coefficients (see (18)), the most dominant coefficients for a given distortion component can be identified.

With this method, we can efficiently calculate the influence of the nonlinearity of a device in its linearized environment. By doing this for all (critical) devices, we get an indication of which share of a certain distortion component can be attributed to which device. It is important to keep in mind that this approach does not give an exact response to the complete nonlinear circuit, because we are neglecting nonlinear interaction between devices. Nevertheless, to improve the design, it is useful to find the origin of the problem and attribute the distortion components to these devices that are at the root of the problem. A device-wise nonlinear approach as presented in this paper aims to fulfill this purpose.

TABLE I
THE FOUR DRIVERS THAT PLAY A ROLE IN DISTORTION GENERATION

	Driver	Main relevant parameters
1	Transfer from interferer to nonlinear device	$V_{gs,lin}$, $V_{ds,lin}$, H_{gs}, H_{ds}
2	Feedback path	H_{fb}, LG
3	Nonlinear function	$V_{GS,DC}$, $V_{DS,DC}$, $\frac{W}{L}$, K_{mn}
4	Transfer from distortion source to output	Z_{nl-out}

We identify four different drivers that play a role in distortion generation. They are shown in Table I. The method addresses each driver. When trying to minimize distortion, the most obvious choice is to minimize $V_{gs,lin}$ and $V_{ds,lin}$. This is most effectively achieved by limiting H_{gs} and H_{ds}, such that the interferer does not arrive at the nonlinear device. When this is not possible due to design constraints, one can make sure the distortion that is generated is counteracted by the feedback loop, achieved by maximizing the loop gain for a certain frequency. Another possibility is to adjust the nonlinear function characteristic, for example by adjusting the bias point or changing the sizing of the transistor. To support the designer in taking the right measures, the method shows which nonlinearity coefficients are dominant for a certain distortion component. Finally, the path from the nonlinear device current to the output can be suppressed by minimizing Z_{nl-out}. In Section IV, we will show how the method points to the different drivers of distortion for a practical test case.

B. Computational Complexity

In this section we compare the computational complexity of the device-wise nonlinear method with that of a normal HB analysis. We consider only steps 1 to 5 in Fig. 7. The remaining steps are seen as an extra post-processing step to analyze the nonlinearity for the most critical devices into more detail. The heaviest computational step in an HB analysis is constructing and factoring the Jacobian matrix, which is a square matrix of dimension $2N(K+1)$, with N being the number of nodes and K the number of frequencies [28].

In the device-wise nonlinear method, the nonlinearity of one device at a time is accounted for while the rest of the circuit is linearized. The linear part is then characterized more efficiently in the frequency domain. This approach of partitioning the circuit into a linear and nonlinear subcircuit is also seen in all early versions of the HB analysis [28]. Using this approach, the circuit is reduced to an N-port network, with N being the number of nodes with a nonlinear device attached. For hybrid microwave circuits, in which the

number of nonlinear devices is commonly much lower than the total number of nodes, this is still the preferred method. For monolithic integrated circuits, on the other hand, the number of nonlinear devices is often in the same order as the total number of nodes and a method is commonly followed in which all node voltages are seen as the independent variables. This greatly increases the size of the Jacobian. Nevertheless, when the number of nonlinear devices is large, sparse matrix techniques can be more efficient when including all nodes in the Jacobian [29]. When analyzing only one nonlinear device in its linear environment, however, partitioning the circuit is far more efficient than using this nodal formulation.

The number of nodes in the proposed model is equal to 2 and thus its Jacobian is very small. The linear transfer functions that provide the inputs to the model can be found by lower-upper (LU) factoring [30] the (sparse) admittance matrix of the full circuit only once and subsequently re-using the matrix factorization for every device. In the method, this process is carried out by the DC and AC simulations. Because the HB simulation is run for every nonlinear device separately, the computation time is $\mathcal{O}(n)$, with n the dimension of the Jacobian of the full circuit. This is much faster than using a direct solver, in which the computation time is theoretically $\mathcal{O}(n^3)$ (although for sparse matrices, it can go down to $\mathcal{O}(n^{1.5})$ [30]). A Krylov solver, which uses an iterative method for solving sparse linear systems, in theory comes close to the time complexity of the method in case a partition between a linear and nonlinear subcircuit is used. However, the method converges much more easily than a Krylov solver, because it treats only one nonlinearity at a time. It typically needs only very few iterations, saving a lot of processing time. Moreover, Krylov solvers need an extra preconditioning step that introduces an extra tradeoff between computational efficiency and robustness [6].

The method can be used together with a preselection step, like in [7], [8]. Using this step, only those devices are selected that show strongly nonlinear behavior. This selection is done based on the already found solution of the linear network with the interferer attached and therefore takes no extra processing time. Now, only a fraction of the total number of devices is simulated using an HB simulation, hereby reducing the computation time significantly. Another advantage is that the HB simulations per device and frequency can be carried out completely independently, which means it is easy to exploit parallel computing to reduce the computation time even further.

IV. Results

The utility of the method is demonstrated by applying it to a representative level shifter circuit that suffers from an immunity failure. The circuit, shown in Fig. 9, is implemented in a 0.14 μm high-voltage silicon-on-insulator (SOI) CMOS technology. The circuit shifts the level of the binary signal from 1.8 V at the input to V_{DD} at the output. V_{DD} is equal to 3.3 V. Transistor M_1 serves to enable or disable the level-shifting operation. This function can be controlled with the signal $V_{DISABLE}$. When the disable signal becomes high,

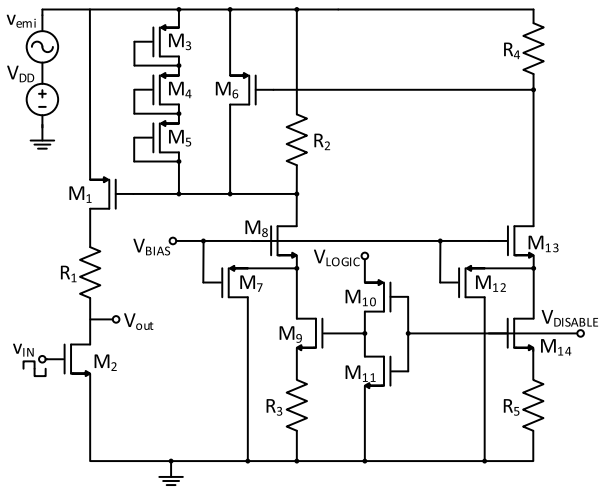

Fig. 9. Level shifter circuit with interference injected at V_{DD}.

transistor M_9 will turn off and current will flow through the branch of M_{14}, which results in M_6 turning on. As a result, the gate voltage of M_1 goes up and the output does not react to the input anymore. Transistors M_7 and M_{12} serve as overvoltage protection for M_8 and M_{13}, respectively.

The interferer is injected on V_{DD}. When the interferer peak amplitude is set to 1 V and the circuit is simulated using an HB analysis for different interference frequencies, it appears that there is an upward DC shift at the gate node of M_1, turning M_1 off and making the output insensitive to the input. This occurs only for higher frequencies. To investigate this effect in more detail and point to the cause and critical contributions, we apply the method to the given circuit.

A fully automated tool based on the method has been implemented in Matlab. The DC, AC, and HB simulations are run in Cadence Spectre(RF). At first, a DC and AC simulation are carried out to determine the propagation of the interferer to the nonlinear device terminals. Based on these results, it is convenient to preselect the devices that see a significant part of the interferer at their input ports and include those devices for the device-wise nonlinear method. In [7], this selection is based on the occurrence of operating region transitions. From this preselection, the critical transistors are identified to be M_6, M_8 and M_9, the remaining transistors do not appear to cause significant distortion. It should be noted that the level shifter has several operating states due to the binary input signals v_{IN} and $V_{DISABLE}$. The method assumes a fixed DC operating point, so to prevent multiple runs of the tool, it is helpful to identify the critical operating states beforehand. Using the preselection, critical devices are found only when $V_{DISABLE}$ is set to a low value, i.e. a logic '0'. The value of v_{IN} does not influence the results much. Hence, it is sufficient to run the tool for only one operating point out of the theoretical four.

After the preselection, steps 2 and 3 in Fig. 7 are carried out. For step 4, we choose to investigate the distortion at the gate node of M_1. The summed distortion at the first 50 harmonics (excluding the DC component) as well as the DC shift are calculated per critical device. The simulated contributions can be seen in Fig. 10. They are plotted as a function of the

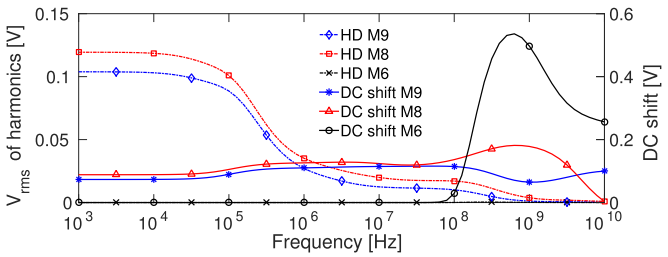

Fig. 10. Distortion at first 50 harmonics and DC shift per critical device as a function of the interference frequency. Distortion is evaluated at gate node M_1.

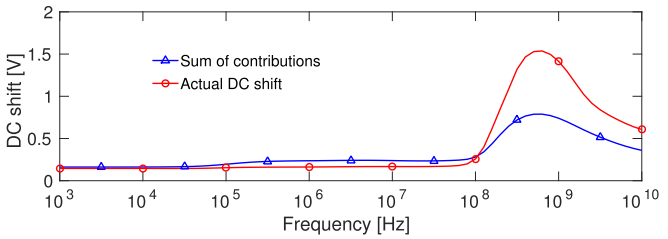

Fig. 11. Sum of DC shift contributions vs. actual DC shift at gate node M_1.

interference frequency. For lower frequencies, M_8 and M_9 generate a significant amount of harmonic distortion, while the harmonic distortion caused by M_6 is zero. Looking at the DC shift contributions per device, we see that the main contribution is due to M_6. For low frequencies, only M_8 and M_9 contribute. To see how the sum of the contributions compares to the total DC shift, both curves are plotted in Fig. 11. There is a clear correlation noticeable between the sum of contributions and the actual DC shift in the original circuit. It becomes clear now that the increased DC shift for higher frequencies, which gives rise to the immunity failure, is caused by M_6. The difference in the peak value of both curves can be explained as follows. By looking only at the influence of one nonlinearity at the time, we ignore the effect the distortion generated by M_6 has on the distortion generated by the other transistors. This effect will be stronger for larger DC shifts, explaining the largest difference at the peak. However, it is evident that this is by no means affecting the ability to point to the source of the problem. Suppose that the DC shift induced by a certain transistor is causing another initially linearly operating transistor to increase the DC shift even further, leading to the failure. Then it is still the first device that lies at the root of the problem. When a nonlinear response becomes a complex clutter of contributions of many different devices, it is difficult to separate cause from effect. The method comes to aid here and points to those devices that initiate critical distortion effects.

Both the model and the full circuit are simulated using an HB analysis. The computation times are compared and the results are shown in Table II. Also a comparison with the linearized circuit with one nonlinear model (which has the same number of nodes as the original circuit) is made, since the response to this circuit is the same as the response to the proposed model. Note that the values in Table II are CPU

TABLE II
SIMULATION TIME OF MODEL VS CIRCUIT

Type of circuit	Average CPU time per HB simulation
Full nonlinear circuit	0.7 s
Linearized circuit with one nonlinear model	0.4 s
Proposed model	33 ms

times, which means that time for parsing is excluded. The average CPU time of the HB simulation of the model is seen to be much smaller, compared to both other circuits. To obtain the nonlinear contributions for the level shifter, the model was simulated for three critical devices and 71 frequency samples, leading to 213 HB analyses. The CPU times of the DC and AC simulations, needed to provide the inputs to the model, sum up to approximately 70 ms. Hence, the total CPU time for finding the nonlinear contributions is 7.1 s. Calculating the response of the full circuit for all 71 frequency samples takes roughly 50 seconds. However, this number quickly increases for larger interference amplitudes. For example, for an amplitude of 3 V, the simulator fails to converge at a frequency of 1 kHz, while the computation time of the proposed model remains unchanged. Moreover, it can be expected that the computational advantage becomes much greater for larger circuits, as explained in Section III-B.

It is worth mentioning that the proposed method shows similarities with the compression distortion summary, developed by Cadence [17]. This method also calculates contributions of individual devices while linearizing the environment. Nonlinear contributions to the first three harmonics of a given frequency are calculated per device, similar to the proposed method. In contrast to the proposed method, Cadence's method is valid only for weakly nonlinear systems. As an example, in Fig. 12a the contributions of M_8 to the second and third harmonic at the gate node of M_1 are compared to the contributions calculated by the method for an interference frequency of 1 kHz. The values are plotted as a function of the interference amplitude, together with the actual contributions where a full nonlinear model including nonlinear capacitances is used in a further linearized environment. The contributions calculated by the method show perfect agreement with the reference. This is as expected, since all nonlinear effects are accounted for, except for the dynamic nonlinear effects, which can be neglected at 1 kHz. The contributions predicted by the compression distortion method, however, strongly diverge from the reference when the amplitude grows. In Fig. 12b, the real HD2 and HD3 components, calculated by an HB analysis of the full circuit, are plotted. They are compared to the sum of contributions calculated by the method and the value predicted by Cadence's method when all nonlinear devices are included. Although the method still shows good agreement with the reference for the HD2 component, the limitation of ignoring nonlinear interaction becomes more noticeable for the HD3 component. This is due to the fact that HD3 can originate from an odd-order nonlinearity of individual devices, but also from the combination of two even-order nonlinearities

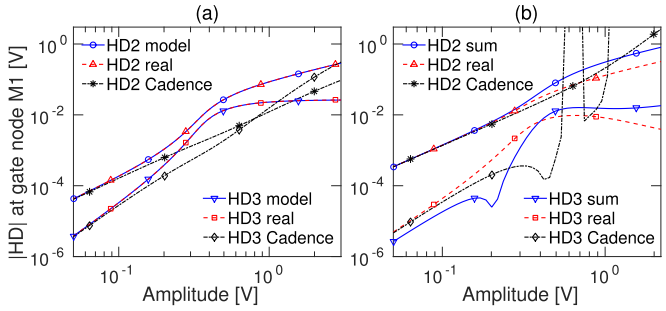

Fig. 12. Comparison between the method, full HB analysis, and Cadence's compression distortion method for calculation of HD2 and HD3 at gate node of M_1, assuming 1 kHz interference frequency and (a) only the nonlinear contribution of M_8 and (b) all nonlinear devices included.

of separate devices (where the latter can commonly reach the same order of magnitude as the former). HD2, on the other hand, is mainly caused by the even-order nonlinearity coefficients of individual devices. The values predicted by the compression distortion method match well for low amplitudes. For higher amplitudes, the HD2 value starts to diverge strongly, whereas the HD3 value clearly becomes unreasonable. This is because Cadence's method uses perturbation analysis, which can lead to highly inaccurate results under strongly nonlinear conditions.

Now that we know what the contributions per device are, we can proceed to the individual nonlinearity analysis to identify the drivers for the nonlinear behavior. Steps 6 to 9 in Fig. 7 are carried out for the three critical devices, resulting in values for the fitted loop gain and an overview of the dominant nonlinearities. The loop gain, given by (15), is dependent on the interference frequency, because the fitted coefficients K_{10} and K_{01} are calculated for an amplitude range that varies for different interference frequencies. Since our target is to minimize DC shift, we evaluate the loop gain at DC. The plots are shown in Fig. 13a-c. The dominant coefficients are shown as contributions to the DC output current of the associated transistor and can be seen in Fig. 13d-f. Additionally, $|V_{gs,lin}|$, $|V_{ds,lin}|$, $|H_{gs}|$ and $|H_{ds}|$, associated with the model in Fig. 5, are plotted in Fig. 13a-c.

We now have enough information to get insight into the different drivers of nonlinear behavior that we identified in the previous chapter. First focusing on the first driver, which is the transfer from interferer to nonlinear device, we see that $|V_{gs,lin}|$ and $|V_{ds,lin}|$ of all transistors are significant. For M_8 and M_9, interference arrives mostly through the path to v_{ds}; in other words, H_{ds} is large. For M_6, we see that H_{gs} and H_{ds} are equal to $V_{gs,lin}$ and $V_{ds,lin}$, respectively, meaning that the transfer is fully determined by the forward path; there is no small signal feedback, see (9), (10). Furthermore, the fitted loop gain of M_6 is practically zero, while the loop gain of M_8 and M_9 is large across the whole frequency range. This means that, in contrast to the situation of M_8 and M_9, the DC distortion component generated by M_6 is not counteracted. To clarify the situation, the 3rd order fitted nonlinear current characteristics are plotted for an interference frequency of 600 MHz, as shown in Fig. 14. The fitting is done based on the samples found using the transient simulations, depicted in the same graphs. The red lines represent the nonlinear trajectory of the i_{DS}, v_{GS} and v_{DS} waveforms. It becomes clear that M_6 switches from the cutoff region to inversion due to the interference at v_{GS}. Since the characteristic is practically flat as a function of v_{DS}, the DC current consists mainly of the component caused by K_{20}, i.e. the even order i_{ds}-v_{gs} nonlinearity. This is clearly visible in Fig. 13d. The DC current shift shows up for higher frequencies, when $v_{gs,lin}$ increases and turns on the device.

From Fig. 14, we see that the amplitude range of i_{ds} of M_8 and M_9 is much higher than that of M_6. However, the DC current of M_6 is higher than that of M_8 and M_9. For example, the DC current at 600 MHz is -480 nA for M_6. For M_8 and M_9, it is -90 nA and -40 nA, respectively. In this, we see the influence of the higher loop gain at DC for M_8 and M_9. When the DC current of M_8 and M_9 tends to increase, it is immediately counteracted by a decreased v_{GS} and v_{DS}. An increased DC current in M_6 also reduces v_{DS}, but this has only a minor effect because M_6 is operating in saturation and thus the v_{DS} dependency of the current is only small. This can also be understood by looking at (15). For M_6, the loop gain is small, because a change in i_{DS} does not affect v_{GS} and the linear dependency of i_{DS} on v_{DS} is very small. In other words, both K_{01} and Z_{gs} are practically zero. This means that the DC current shift of M_6 is unconstrained and therefore detrimental. To see how this DC current shift contributes to the DC voltage shift at the gate node of M_1, we need to consider the fourth driver defined in Section III-A: the transfer from distortion source to a given output node. In this case, we see the gate node of M_1 as our output node. This means that the transfer function $Z_{nl-out}(s)$ is equal to $Z_{ds}(s)$ for M_6. Due to resistances R_2 and R_3, $Z_{ds,dc}$ is large and thus the DC current of M_6 is directly contributing to the DC shift at the gate of M_1.

The steady-state nonlinear waveforms from the HB analysis of the model of M_6 as well as the linear waveforms from the AC analysis are shown in Fig. 15a. The generated DC shift is visible as the difference between v_{DS} and $v_{ds,lin}$. We see that v_{GS} is equal to $v_{gs,lin}$, because of the lack of feedback. Therefore, the nonlinear function is fully excited, leading to a large value for i_{DS}. The linear signal $i_{ds,lin}$ is zero, because the transistor is biased in cutoff, in which the transconductance is zero. When the interference amplitude increases, the DC shift generated by M_6 quickly builds up. This continues until the moment M_6 is driven into the triode region. When this occurs, the transistor current drops as a function of v_{DS}. In other words, feedback takes place through v_{DS}, which brings a hold to the rising DC shift. This can be seen in an increased fitted loop gain due to a higher K_{01}.

Compared to the nonlinearity coefficient contributions plot of M_6, the coefficient plots of M_8 and M_9 are much more complex. Due to the large feedback, there are many higher-order components coupled back to the input, leading to more distinct distortion products. It is apparent, however, that the i_{ds}-v_{ds} nonlinearities play the largest role, of which K_{02} seems the most dominant. The dominance of these nonlinearities can be understood by looking at Fig. 14b and c and taking into consideration that both M_8 and M_9 are biased far into the

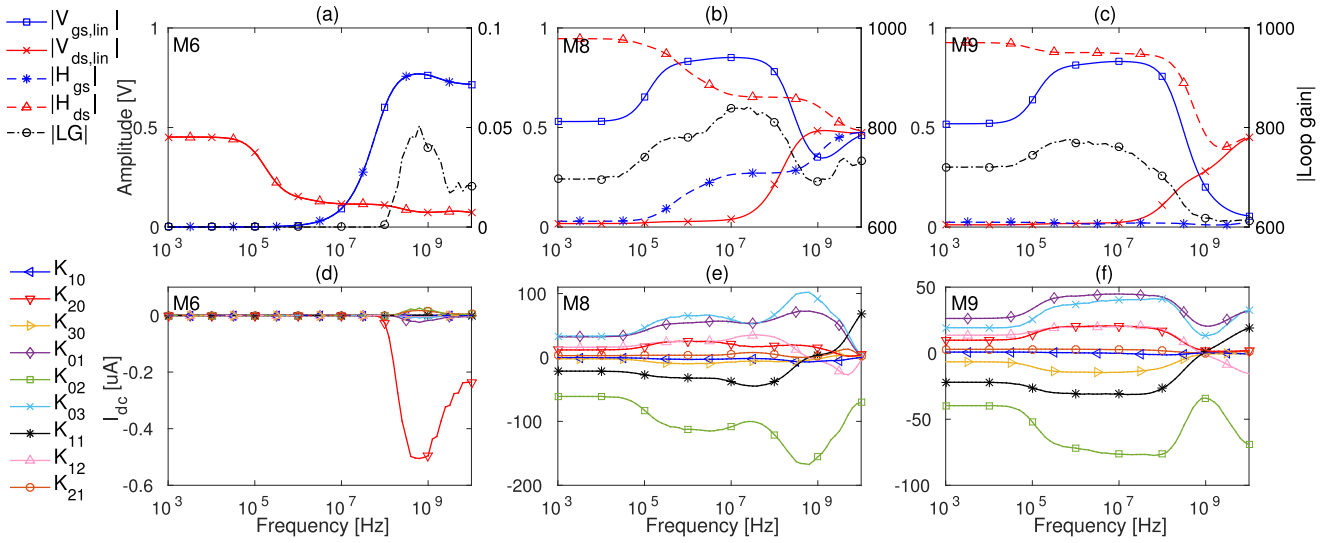

Fig. 13. Loop gain at DC and amplitude of linear input voltages in (a)-(c). Value of parallel current sources associated to nonlinearity coefficients (see (11)) at DC in (d)-(f). All plots are a function of the interference frequency.

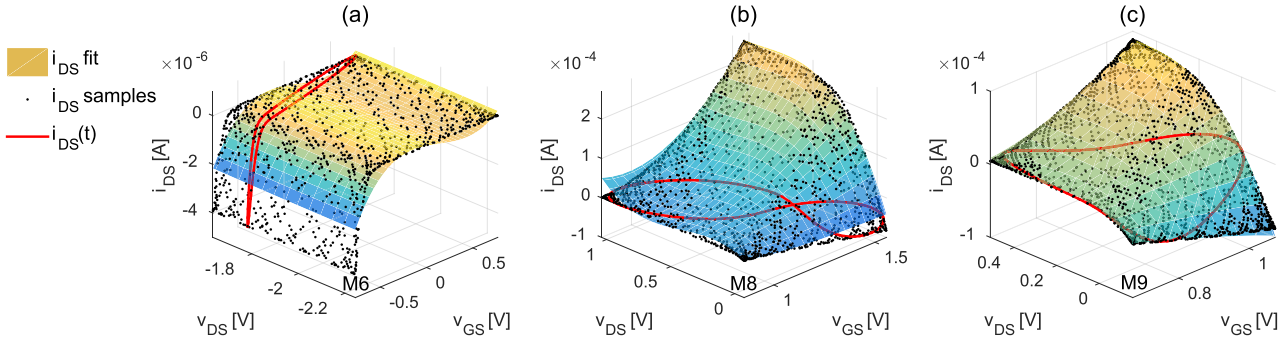

Fig. 14. Fitted 3rd order characteristics of i_{DS}, together with transient samples used for fitting and nonlinear waveform for an interference frequency of 600 MHz. Goodness of fit parameters: M6: $R^2 = 0.7190$, RMSE $= 0.30\ \mu A$, M8: $R^2 = 0.9880$, RMSE $= 7.51\ \mu A$, M9: $R^2 = 0.9987$, RMSE $= 1.19\ \mu A$.

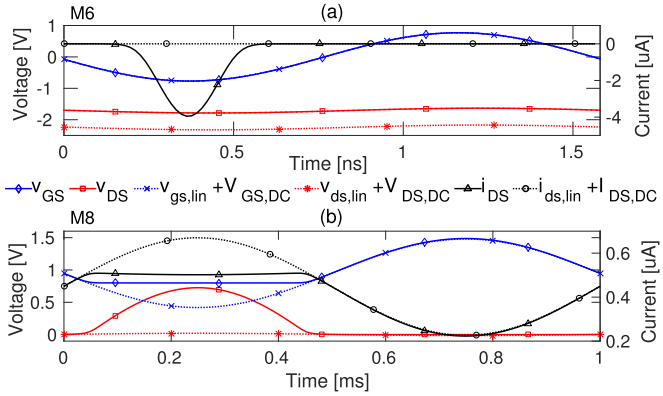

Fig. 15. Nonlinear waveforms from HB analysis of model and linear waveforms from AC analysis for (a) M_6 with interference frequency of 600 MHz and (b) M_8 with interference frequency of 1 kHz.

triode region. The plots of the nonlinear currents at 600 MHz show that v_{DS} extends over a large range from the triode to saturation region, hereby experiencing strong nonlinearities. From Fig. 10, we noticed that M_8 and M_9 are generating a significant amount of distortion, especially for lower frequencies. This distortion can cause transistor M_1 to intermittently conduct and therefore propagate to the output. To illustrate how the distortion is generated, we can analyze the circuit in Fig. 5b for the case of M_8. The distortion mechanism of M_9 is similar to that of M_8. The linear and nonlinear waveforms of M_8 for an interference frequency of 1 kHz are shown in Fig. 15b. There is significant feedback from the current of M_8 back to its v_{GS} and v_{DS}. This means that any deviation away from the linear current $i_{ds,lin}$ is immediately counteracted, in contrast to the situation of M_6 where i_{DS} can vary freely. Because the time constants in the feedback network are small compared to the period of 1 ms, the effects of the feedback happen almost instantly. As can be seen from Fig. 14b, the characteristic is very steep for v_{DS} values close to zero, which is around the bias point for M_8. Hence, the output conductance g_{ds} is high and the linear current of M_8 is mainly dependent on $v_{ds,lin}$, even though the $v_{ds,lin}$ amplitude is only in the range of millivolts. In the first half of the period in Fig. 15b, $v_{ds,lin}$ goes up, causing the i_{DS} characteristic to flatten somewhat. In other words, i_{nonl} in Fig. 5b becomes

negative. This effect is counteracted by the feedback to v_{GS} and v_{DS}. As a result, the v_{GS} decrease is resisted and v_{DS} goes from the triode to the saturation region. Consequently, the characteristic flattens even further and i_{DS} cannot keep up with $i_{ds,lin}$ anymore. This is causing the clipping effect, leading to a lot of high frequency distortion. In the second half of the waveform, the signals stay within the steep part of the characteristic and thus i_{DS} is able to follow $i_{ds,lin}$.

V. Conclusion

A device-wise nonlinear method has been presented that can serve as an EMC verification tool for large-scale ICs, due to its computational efficiency and applicability to strongly nonlinear systems. It points to causes of immunity failures by identifying critical devices that contribute to strongly nonlinear distortion. Distortion contributions are sorted per device as a function of the interference frequency. The method models the circuit by including the nonlinearity of one device at a time. We have analyzed the used model by approximating its nonlinear transistor function by a fitted polynomial. Based on this analysis, we have identified four different drivers that play a role in distortion generation: the transfer from interferer to nonlinear device, the feedback path, the nonlinear transistor function and the transfer from distortion source to output. The method provides insight into each of these drivers and therefore helps the designer to take measures in different ways. The method has been demonstrated on a level shifter circuit to show its utility and efficiency. Additionally, the influence of the different drivers on the distortion mechanisms has been explained.

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Lammert Duipmans received the M.Sc. degree from the University of Twente, The Netherlands, in 2013, and the Ph.D. degree from the Eindhoven University of Technology, The Netherlands, in 2019. His research interests include nonlinear circuit analysis and immunity verification of analog circuits.

Dusan Milosevic (Member, IEEE) received the M.Sc. (Dipl.Ing.) degree in electronics and telecommunications engineering from the University of Nis, Serbia, in 2001, and the Ph.D. degree in electrical engineering from the Eindhoven University of Technology (TU/e), The Netherlands, in 2009. During his Ph.D. research, he was focusing on switched-mode RF power amplifiers and techniques for high-efficiency linear amplification. Since 2010, he has been an Assistant Professor with the Integrated Circuits Group, TU/e. His research interests include RF and microwave power amplifiers, ultra-low power RF front ends, and RF energy harvesting systems.

Arnoud van der Wel (Member, IEEE) studied at the University of Twente, Enschede, The Netherlands, where he received the master's degree *(cum laude)* in electrical engineering in 1997, a qualification to teach physics in 2000, and the Ph.D. degree *(cum laude)* for his thesis "MOSFET LF noise under large signal excitation" in 2004. He is currently a Team Lead for a group of power conversion specialists at NXP in Eindhoven, The Netherlands. His current research interests include integrated power conversion, LF noise in CMOS technology, clock and data recovery for high speed serial links, and digitally assisted analog circuit design.

Peter Baltus (Senior Member, IEEE) was born in Sittard in July 1960. He received the master's degree in electrical engineering and the Ph.D. degree from the Eindhoven University of Technology in 1985 and 2004, respectively. He worked at Philips for 22 years, and later at NXP in Eindhoven, Nijmegen, Tokyo, and Sunnyvale in various functions, as a Research Scientist, a Program Manager, an Architect, a Domain Manager, a Group Leader, and a Fellow in the areas of data converters, microcontroller architecture, digital design, software, and RF circuits and systems. In 2007, he started his current job at the Eindhoven University of Technology as Professor in high-frequency electronics. From 2007 to 2016, he was the Director of the Centre for Wireless Technology, and as of 2017, he is the Chair of the Integrated Circuits Group. He coauthored more than 200 articles and holds 16 U.S. patents.