A 0.36-V 5-MS/s Time-Mode Flash ADC With Dickson-Charge-Pump-Based Comparators in 28-nm CMOS

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***Abstract*— Dickson charge-pump (CP) is proposed here to realize a voltage-to-time converter (VTC) within an array of time-domain comparators of a 54-level time-mode subthreshold flash ADC operating at 0.36 V. Two identical CPs in each of the 54 ADC slices convert the input and reference voltages into variable-slope ramp signals fed into comparators for 'flash' quantization. Considering the fact that the comparator's evaluation time gets severely degraded at subthreshold input voltages, the proposed ADC delivers the maximum bandwidth by means of the inherent input voltage boosting by the Dickson CPs. The proposed architecture quantizes the analog input signal into time with CPs and then into digital domain with latches and simple logic, without using any analog-intensive circuits such as amplifiers and current sources, thus yielding a digitally friendly implementation. Measurement results show peak ENOB of 5.04-bit, SNDR of 32.1 dB at the peak, power consumption of 88 μW. The conversion rate of 5 MS/s is the highest among near- and subthreshold ADCs.**

***Index Terms*— Flash analog-to-digital converter (ADC), time-based ADC, subthreshold ADC, Dickson charge pump (CP), time quantization, voltage-to-time converter (VTC), wideband subthreshold ADC.**

I. Introduction

RECENTLY, subthreshold (sub-V_t) and near-threshold ADCs have been proposed [1]–[3]. Low supply voltage ADCs find increasing applications from wireless sensor networks to biomedical monitoring devices and wearable autonomous sensors for Internet-of-Things (IoT). For IoT applications, wireless networks are being widely used to improve the device portability while energy harvesters aim to lower the reliance on batteries [4]. Energy harvesters are able to convert thermal energy [5], [6], solar energy [7], or vibrational energy [8] into electricity. However, these harvesters might only be able to deliver as high as a few hundred mV. On the other hand, self-sustainable wireless systems consist of different sub-systems, including ADCs. In order to increase the simplicity of IoT systems and relieve them from very complex and bulky power management schemes, ADCs should work directly with the low supply voltage provided by the energy harvesters. The advancement of CMOS technology also results in a continual reduction of the available voltage headroom for analog and mixed-signal circuits, unavoidably deteriorating the signal-to-noise ratio of analog front-end circuits and ADCs. Time-domain analog signal processing is an effective way to partly overcome such issues.

A category of time-mode ADCs performs an intermediate conversion of the analog input voltage into time information by means of a voltage-to-time converter (VTC) prior to digitization with a time-do-digital converter (TDC) [9]–[13]. Most of the existing topologies are however hardly amenable to the subthreshold operation, given their analog-intensive implementation (e.g. the use of operational amplifiers and current sources) [9] and whose performance depends on the VTC linearity, which severely deteriorates at low supplies. In [13], the compact nature of the current-starved inverter (CSI)-based VTC presents a potential for high-speed operation of time-based ADCs. In [14]–[18], "hybrid" converters that make use of time-mode quantizers show promising performance due to their use of fine and coarse digital quantization of different topologies. In [18], a current source was used to amplify the time residue, which highlights the need there of a highly linear current source. In order to increase the resolution in time-domain ADCs, a time amplifier was employed in [19]; however, that approach needs complex calibration to correct the time amplifier's nonlinearity. Other approaches, using a linear current source for the time amplification have been reported in [20], [21]. Although these designs show power-efficient data conversion, utilizing the time-domain signal processing without a complex residue amplifier, they are restricted in performance, offering low bandwidth (i.e. 15.6 kHz) [20]. In [40], a time-interleaved time-based ADC was introduced that uses a multi channel, low bandwidth comparator to cover the required sampling rate but at a cost of higher sensitivity to the jitter of reference clock. In [39] and [34], the resolution of the presented ADC was increased by using a time and voltage amplifier but that increases the system's dependency on the linearity of the analog amplifiers. In [38], a time-based ADC was combined with a voltage-domain ADC, i.e. flash ADC. In [33], a SAR ADC was used as a coarse ADC and the introduced VTC was used for the fine ADC. However, that limits the bandwidth

Manuscript received October 9, 2019; revised December 11, 2019 and January 1, 2020; accepted January 19, 2020. Date of publication February 6, 2020; date of current version June 3, 2020. This work was supported in part by the Science Foundation Ireland under Grant 14/RP/I2921 and in part by Marie Sklodowska-Curie Actions under Grant 747585. This article was recommended by Associate Editor A. M. A. Ali. *(Corresponding author: Ali Esmailiyan.)*

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Digital Object Identifier 10.1109/TCSI.2020.2969804

and also requires an extra calibration to align the coarse and fine bits.

Successive-approximation register (SAR) ADCs in near- and subthreshold regimes [22]–[28] have demonstrated excellent power efficiency with more than 8 bits of resolution by introducing efficient techniques for the reduction of digital-to-analog converter (DAC)'s switching energy and comparator noise. However, such SAR ADCs typically require complex calibrations for the sought resolution higher than 10 bits. On the other side, state-of-the-art subthreshold ADCs [1]–[3], despite their ultra-high energy efficiency, feature low signal bandwidths in weak inversion. In [23], the use of a bidirectional comparator relieves the circuit from the trade-off of power and noise level but the comparator's threshold comparison level is dependent on the input signal which can affect the bandwidth and linearity. In [24], by using the voltage-controlled delay line (VCDL), the authors propose an adaptive time-domain (ATD) comparator that adjusts the noise performance; however, the performance is still restricted to the linearity of the VCDL.

$\Sigma\Delta$ ADCs are also good candidates for low supply voltage applications since they can provide noise shaping and high resolution alongside with less sensitivity to the circuit non-idealizes. In [42], a low supply voltage, continuous-time, inverter-based $\Delta\Sigma$ ADC relieves from difficulties in designing high gain and bandwidth OTAs. However, it still suffers from low bandwidth performance of the system.

In this paper, we introduce a 54-level time-mode subthreshold flash ADC operating at a nominal 0.36 V single supply. It integrates Dickson charge-pumps (CPs), proposed here as a variable-slope VTC, thus enabling fast voltage-to-time conversion thanks to their inherent voltage boosting operation, followed by simple latches and digital logic. The ADC achieves a sample rate of 5 MS/s, the highest among state-of-the-art near and subthreshold ADCs, ENOB of 5 bits, SNDR of 32.1 dB at the peak, power consumption of 88 μW, in a highly digital implementation (no current sources nor op-amp).

The proposed approach needs to be contrasted with a rather straightforward combination of a conventional ADC, operating at *above* V_t and powered by a step-up Dickson CP-based DC-DC converter. In contrast to our case, the sub-V_t DC-DC converter there would need to deliver significant power, likely suffering from long charging times and excessive size of its holding capacitors [35], [36].

Figure 1 shows the comparison table between the proposed time-based ADC with the conventional ramp based ADC. The proposed system has different advantages such as tunability in the bandwidth and wide bandwidth in sub-threshold operating point. Due to the use of the Dickson CP ramp generator as the VTC, the input common mode voltage of the comparator is maximum, resulting in fast data conversion and also time-based data processing in the proposed ADC. Using two identical Dickson CP for reference and analog input signal results in insensitivity of the proposed system to the non-linearity of the generated ramp and complex calibration circuits.

This paper is organized as follows: Section II presents the structure of the Dickson CP as the VTC and the topology of the sub-ADC slice (array of which is used inside the ADC for sub-system quantization). Section III presents the equivalent model of the proposed sub-ADC slice with timing and delay analysis of the Dickson CP and the used latch. Simulation results pertaining to the effects of nonlinearities on the performance as well as the design process of the ADC are further disclosed in this section. In Section IV, more details of the proposed ADC regarding the implementation aspects are shown. Section V provides measurement results of the fabricated chip and finally the conclusion is presented in Section VI.

Proposed Dickson-CP-based ADC	Conventional ramp-based ADC [9]
No need for analog-intensive circuits, such as amplifiers, current sources, etc.	Requires analog-intensive circuits.
High conversion rate in sub-threshold operation due to maximum input common-mode voltage of comparators.	Slow conversion rate at low supply voltages due to varied input common-mode voltage of comparators.
High achievable bandwidth with power/bandwidth scalability.	Difficulty with bandwidth tunability due to limitations of the following TDC of fixed resolution.
Amendable to very low supply voltages, resulting in no need for bulky DC-DC converters for sub-threshold applications.	Not usable at sub-threshold voltage.
Independent of the non-linearity of the Dickson-CP-based VTC.	Heavily dependent on linearity of the generated ramp signal in the VTC, requires intensive calibration.
No calibration needed.	
Time-based processing system.	Voltage-based processing system.

Fig. 1. Comparison table of the proposed ADC vs. conventional ramp based ADC.

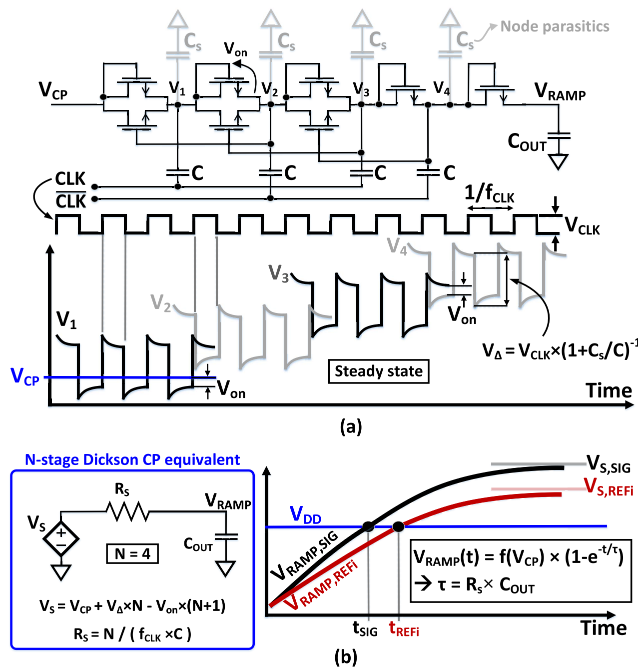

Fig. 2. Dickson charge-pump: (a) schematic diagram, (b) signals and equivalent model.

II. Dickson Charge-Pump as an Integrator for Time Comparison

A. Dickson Charge-Pump Working Principle

Figure 2(a) shows a schematic diagram and signal waveforms of a modified version of well-known Dickson charge-pump [41] (in this example, of four cascaded stages). Each stage is made of capacitor C and the parallel of a diode-connected MOS and a MOS switch. During the initial

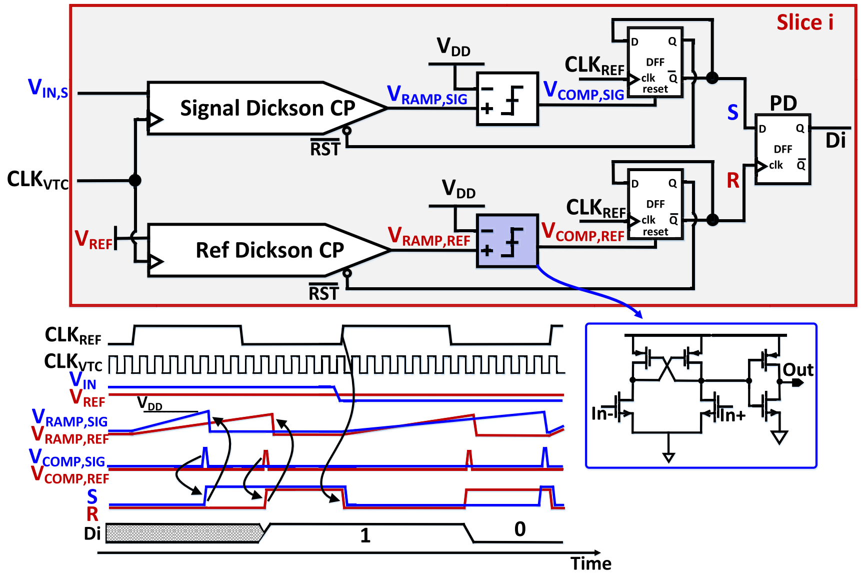

Fig. 3. Schematic diagram and signal patterns of a sub-ADC slice operating as time-domain latch.

exponential transient, the charge is transferred along the chain towards the output V_{ramp}. The voltages across the capacitors increase until reaching their steady-state values of $V_{\mathrm{CP}} - V_{\mathrm{on}}$, $V_{\Delta} + V_{\mathrm{CP}} - 2V_{\mathrm{on}}$, $2V_{\Delta} + V_{\mathrm{CP}} - 3V_{\mathrm{on}}$, and $3V_{\Delta} + V_{\mathrm{CP}} - 4V_{\mathrm{on}}$, respectively, where V_{CP} is the input voltage, V_{on} is the drop voltage of the switch when it turns on, and V_{Δ} is the voltage shift at nodes $\mathrm{V}_{1,2,3,4}$ equal to the the clock amplitude V_{CLK} (i.e. 360 mV in this design) attenuated by the effect of parasitic capacitances C_{S}. The last diode-connected MOS and the load capacitor C_{out} act as a rectifier, producing an output V_{ramp} which monotonically tends to the asymptote $4V_{\Delta} + V_{\mathrm{CP}} - 5V_{\mathrm{on}}$ (i.e. V_{S} equivalent generator shown in the model in Fig. 2(b)). Conventionally, the use of Dickson CPs has been limited to power management applications, in which a DC voltage is multiplied by a factor N equal to the number of cascaded stages. Due to the charge-transfer operation of a Dickson multiplier, the output steady-state voltage V_{S} is a proportional function of the input, and its time behavior is well approximated by an RC exponential transient, increasing asymptotically towards V_{S} and with a time constant that depends on the CLK frequency, number of stages N and the value C of internal capacitors. This arrangement allows using the Dickson CP as a controllable voltage-slope generator (indeed, a VTC) within a time-domain comparator, suitable for a low-supply operation.

The last diode-connected FET in Fig. 2, along with the output capacitor C_{OUT}, also form a low-pass RC filter to suppress the high frequency response of the Dickson CP's clocking activities during the generation of the ramp signal. This helps the system to filter out the generated ripples on the output ramp signal.

B. Dickson Charge-Pump-Based Subthreshold Time-Domain Comparator

Fig. 3 illustrates the use of a Dickson CP as a voltage integrator within a time-domain comparator, representing one of the 54 slices of the proposed time-mode flash ADC. The *Signal* and *Ref* Dickson CPs are two identical voltage multipliers, one for the sampled input voltage $V_{\mathrm{in,S}}$ and the other for the reference V_{ref}, followed by a pair of comparator latches, two D flip-flops (DFFs) and a 1-bit phase detector (PD). The two Dickson CPs are clocked at 200 MHz by $\mathrm{CLK}_{\mathrm{VTC}}$, boosting their inputs ($V_{\mathrm{in,S}}$ and V_{ref}) until the outputs $V_{\mathrm{ramp,sig}}$ and $V_{\mathrm{ramp,ref}}$ reach the V_{DD} comparison level. The timestamp of the output voltage crossing the V_{DD} threshold (t_{sig}, see Fig. 2(b)) is modulated by the applied input voltage (i.e. shorter for higher input signal). The threshold crossings are detected by the pair of latches, acting as pseudo-differential comparators, whose outputs $V_{\mathrm{comp,sig}}$ and $V_{\mathrm{comp,ref}}$ eventually become logic 1s, causing the reset of the following DFFs. This will, in turn, assert signals S and R and reset the *Signal* and *Ref* Dickson CPs by shorting their V_{1-4} internal nodes to ground (not shown) until the next $\mathrm{CLK}_{\mathrm{ref}}$ rising edge. The 1-bit PD is implemented as a DFF whose input and clock are S and R, respectively. The Dickson CP's inherent voltage boosting allows the comparison threshold of the latches (comparators) to be conveniently set to V_{DD}, which is crossed by V_{ref} with a time derivative almost close to its maximum (i.e. the waveform is still not in the settling region), thus ensuring fast comparison time (as shown in waveforms of Fig. 3 and Fig. 2(b) and also in the analysis of Section III). Making use of two identical Dickson CP in each slice helps reducing the effects of nonlinearity and mismatch, as well as the effects of different capacitive and resistive loading on the output of the Dickson CPs and, finally, different time constants in the equivalent model of Fig. 2(b), which can lead to an increased error in the quantization process. The proposed circuit for sub-ADC slice benefits from fast reset time period (see $V_{\mathrm{comp,sig}}$ and $V_{\mathrm{comp,ref}}$ in Fig. 3), thanks to the used digital topology of reset section. Short reset time has a relatively less impact on the conversion period, thus slightly improving the ADC bandwidth.

III. Modeling

In this section, we first analyze the effects of mismatches and non-idealities on the performance of the proposed ADC. Different scenarios are then compared. We then evaluate the

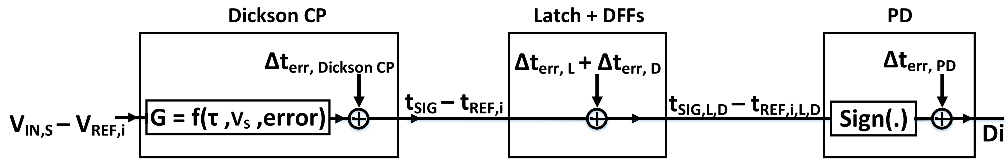

Fig. 4. Equivalent differential model of the sub-ADC slice.

timing of the utilized latch and Dickson CP inside each sub-ADC slice. Then, top-level modeling simulations with respects to the effects of non-idealities are presented. Finally, Monte Carlo simulations for the Dickson CP and also input refereed offset voltage of the proposed VTC are studied.

A. Sub-ADC Slice Mismatch/Nonlinearity Modeling

Fig. 4 illustrates an equivalent model of the proposed sub-ADC slice of index i. Dickson CP is modeled as a voltage-to-time converter (VTC) block that uses the equivalent equation of Fig. 2(b) to convert the input voltage differential signal (i.e. $V_{\text{in,S}} - V_{\text{ref}}$, see Fig. 3) to $t_{\text{sig}} - t_{\text{ref}}$, see Fig. 2(b). Mismatches between PDs, latches and DFFs in each branch of the sub-ADC slice (i.e. reference and signal paths) are added as error signals into the proposed model in Fig. 4. Timestamps S and R, which are the physical input signals to the PD, were subtracted to represent the equivalent model of the PD in Fig. 3 and the equivalent *sign* of the result of that subtraction is modeled as the ADC's digital output bit D_i.

Clock skew between the two Dickson CPs branches in the sub-ADC slice can cause an error in the ADC's digital quantization process. The effect of clock skew can be modeled by an initial voltage V_0 at t_0' in the output capacitors, as shown in Figs. 5 and 2(b): the initial voltage is directly proportional to the time-skew via the voltage-to-time gain of the Dickson CP at the beginning of the ramp, with the assumption of absence of mismatch between reference and signal path. Leading or lagging the input clock signal for either of the Dickson CPs (with reference to Fig. 3) can change the initial voltage V_0 that is stored in C_{out} of the equivalent model. By replacing the starting time t_0 of the output ramp with the new reference time (i.e. t_0') and initializing V_0 for the leading branch in the sub-ADC (either reference or signal), the generated sub-ADC digitization error can be modeled as shown at the right hand side of Fig. 5. The generated V_0 due to the clock skew error is a function of the modeling parameters of the Dickson CP (i.e. V_{S}, R_{S}, and C_{out} in Fig. 2(b)). Higher voltage gain in Dickson VTC as well as longer clock skew result in higher V_0 and larger amount of generated error. This is due to a stronger time amplification of the Dickson CP or larger $\Delta t_{\text{err,skew}}$, resulting in higher V_0.

Based on the equivalent Dickson CP model shown in Fig. 2(b) and 5, V_{ramp} signal in Fig. 3 can be expressed as:

$$V(t) = V_{\text{S,sig,ref}} + \left(V_{0,\text{sig,ref}} - V_{\text{S,sig,ref}}\right) e^{-\frac{t}{\tau}} \quad (1)$$

where $V_{0,\text{sig,ref}}$ represents the initial voltage of the Dickson CP in the reference or signal path, accounting for clock skew $\Delta t_{\text{err,skew}}$, whose effect is proportional to the voltage gain of

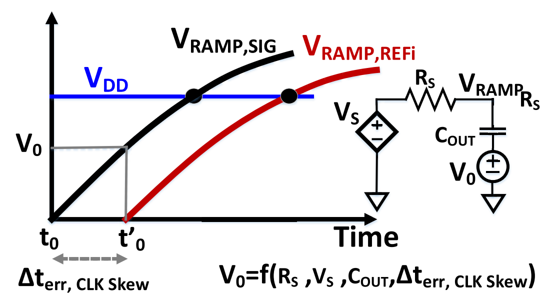

Fig. 5. Equivalent model of Dickson CP for the effect of clock skew.

the Dickson VTC, as previously discussed, while $V_{\text{S,sig,ref}}$ is the asymptotic output voltage of the respective Dickson CP. $t = t_{\text{sig,ref}}$ is the timestamp of the threshold crossing (i.e. V_{DD} here) at the respective latch of Fig. 3, and it can be written as:

$$t_{\text{sig,ref,i}} = -\tau_{\text{sig,ref}} \cdot \ln\left(\frac{V_{\text{DD}} - V_{\text{S,sig,ref}}}{V_{0,\text{sig,ref}} - V_{\text{S,sig,ref}}}\right) \quad (2)$$

where $\tau_{\text{sig,ref}}$ is the time constant of the equivalent model of Dickson CP and is equal to $R_{\text{S}} \cdot C_{\text{out}}$.

If the noise and mismatch in DFFs, latches and PD of the equivalent model in Fig. 4 are considered to be negligible (i.e., $\Delta t_{\text{err,DicksonCP}}$, $\Delta t_{\text{err,L}}$, $\Delta t_{\text{err,D}}$ and $\Delta t_{\text{err,PD}} \approx 0$), the input signal to the digital quantizer (Δt) can be written as:

$$\begin{aligned}\Delta t &= t_{\text{sig}} - t_{\text{ref,i}} \\ &= \tau_{\text{ref}} \cdot \ln\left(\frac{V_{\text{DD}} - V_{\text{S,ref}}}{V_{0,\text{ref}} - V_{\text{S,ref}}}\right) - \tau_{\text{sig}} \cdot \ln\left(\frac{V_{\text{DD}} - V_{\text{S,sig}}}{V_{0,\text{sig}} - V_{\text{S,sig}}}\right) \quad (3)\end{aligned}$$

In the next sub-sections, three representative scenarios of nonidealities are outlined, and their impact on the resulting VTC timing error is analyzed.

1) Source of Error: Time Constant of Dickson CP Model: In the first scenario, the source of error in $t_{\text{sig}} - t_{\text{ref,i}}$ is considered to be embedded within the time constants τ_{ref} and τ_{sig} due to the mismatch between C_{out}'s or C's and the two branches of signal/reference in each sub-ADC slice. The time constant in the Dickson CP model in Fig. 2(b) can be expressed as

$$\tau = \tau_{\text{ref}} = \tau_{\text{sig}} + \Delta\tau_0 \quad (4)$$

where $\Delta\tau_0$ represents the time constant mismatch between the reference and signal paths in the sub-ADC slice. The final voltage of the Dickson CP (i.e. V_{S} in Fig. 2(b)), considering the same voltage value applied to the reference and signal Dickson CPs and also considering a negligible initial voltage on capacitors C_{out}, can be written as:

$$V_s = V_{\text{S,ref}} = V_{\text{S,sig}} \quad (5)$$

In (5), it is considered that a dependency of V_S on τ of the CP equivalent model, and also V_Δ dependency on the parasitic CP capacitors, as well as the initial voltage in the output capacitor of the equivalent model (i.e. $V_{0,\mathrm{sig,ref}}$ in Fig. 5) are negligible. Inserting (5) into (3) results in:

$$\Delta t = \Delta\tau_0 \cdot \ln\left(1 - \frac{V_{DD}}{V_S}\right) \tag{6}$$

From (6), it can be concluded that for a specific mismatch value, the larger the input signal the larger V_S, resulting in a lower error in the quantization process in each sub-ADC slice. Thus, (6) captures the effect of the input signal on the mismatch on the digital quantization process.

2) Source of Error: Threshold Voltages of the Turned-On Switches in the Dickson CP Model: In the second scenario, it is assumed that the effect of clock skew is negligible [i.e. $\Delta\tau_0 \approx 0$ in (4)] and so the mismatch among capacitors C_{out} or among R_S's in Fig. 2(b). The sole source of error in this condition is represented by the mismatch in the drop voltages of the switches in the Dickson CPs (i.e. V_{on} in Fig. 2(b)), yielding:

$$V_{S,\mathrm{sig}} = V_{S,\mathrm{ref}} + \Delta V_S \tag{7}$$

Inserting (7) into (3) results in:

$$\Delta t = \tau \cdot \ln\left(\left(1 - \frac{V_{DD}}{V_{S,\mathrm{ref}}}\right)\frac{V_{S,\mathrm{ref}} + \Delta V_S}{V_{S,\mathrm{ref}} + \Delta V_S - V_{DD}}\right) \tag{8}$$

from which it can be concluded that for the same input voltage to both the reference and signal paths in each sub-ADC slice, and for a specific mismatch error in ΔV_S, a lower input signal results in lower V_S, thus significantly deteriorating Δt or, in other words, the mismatch of V_{on} of the Dickson CP switches will have a larger effect, ultimately causing a higher harmonic distortion in the ADC output spectrum.

3) Source of Error: Clock Skew in the Dickson CP Model: In the third scenario, the mismatches among switches and capacitors in the two branches are considered to be negligible, resulting in $\Delta V_S \approx 0$ and $\Delta\tau_0 \approx 0$ in (7) and (4), respectively. Hence, the sole source of error now is represented by the clock skew in the Dickson CP. This results in different initial voltages for the equivalent Dickson model due to the different initial clock timing in each branch, which depends on the clock skew error and the voltage gain of the Dickson VTC (as discussed in the previous section). Consequently,

$$V_{0,\mathrm{sig}} = V_{0,\mathrm{ref}} + \Delta V_0 \tag{9}$$

Inserting (9) into (3) yields:

$$\Delta t = \tau \cdot \ln\left(1 - \frac{\Delta V_0}{V_S - V_{0,\mathrm{ref}}}\right) \tag{10}$$

Similarly to (6) and (8), (10) also shows the dependency of the error of the clock skew on the input signal voltage.

Based on the mentioned three scenarios for the effect of mismatch between the reference and signal Dickson CP comparators, it can be concluded that to reduce the sensitivity of the system to the comparator mismatch and also to the time gap error between $V_{\mathrm{RAMP,SIG}}$ and $V_{\mathrm{RAMP,REF}}$ (with reference to Fig. 3), the ratio of V_{DD} over V_S should be minimized. This can reduce Δt in (6), (8) and (10). Increasing V_S can be facilitated by increasing the number of stages (i.e. N) in the Dickson CP. Increasing V_S can reduce the effect of mismatch of the reference and signal paths but at a cost of higher power consumption and occupied area.

The equivalent model of the proposed ADC in Fig. 4 was simulated in MATLAB to evaluate the effects of mismatches between the reference and signal paths in the Dickson CPs. The results are presented in Section III-C.

SPICE Monte Carlo Simulations are also presented in Section III-D to study the effects of the mismatch on the input-refered offset voltage of the Dickson CP VTC.

B. Delay Modeling of Sub-ADC Slice

In this subsection, we derive equations pertaining to the delay timing of the implemented latch and Dickson CP and also provide support with SPICE simulations.

Based on [29]–[31], the subthreshold drain current of MOS transistors can be expressed as:

$$I_D = I_{D0}\,(1 - \lambda V_{DS})\,e^{\frac{V_{GS}}{nV_{\mathrm{th}}}}\left(1 - e^{\frac{-V_{DS}}{V_{\mathrm{th}}}}\right) \tag{11}$$

For small λ or V_{DS}, (11) can be rewritten as:

$$I_D = I_{D0}e^{\frac{V_{GS}}{nV_{\mathrm{th}}}} \tag{12}$$

Fig. 6 shows a more detailed schematic of the implemented latch of Fig. 3. The input signal to M_1 is V_{DD} while M_2 receives the respective Dickson CP output, labeled as $V_{\mathrm{ramp}}(t)$. V_n is the negated output of the latch that is buffered through the output inverter. Fig. 7 plots the SPICE simulation results. While the $V_{\mathrm{ramp}}(t)$ signal at the gate node approaches V_{DD}, the voltage at node V_n starts to decrease and results in an increase in V_p, which further leads to the decrease of V_n. This positive feedback cycle continues until V_n is low enough to trigger the next-stage inverter output V_{out} going from logic 0 to logic 1. The difference between the time at which $V_{\mathrm{ramp}}(t)$ crosses V_{DD} and that at which the decreasing voltage V_n crosses $V_{DD}/2$ is defined as t_{delay}.

Based on Fig. 6, the current through the load capacitor C_L (connected to node V_n), during the comparator evaluation time, can be written as:

$$I_{C_L} = I_{D4} - I_{D2} \tag{13}$$

Plugging (12) into (13) results in:

$$I_{C_L} = I_{D0}e^{\frac{V_{SG_{M4}}}{nV_{\mathrm{th}}}} - I_{D0}e^{\frac{V_{GS_{M2}}}{nV_{\mathrm{th}}}} \tag{14}$$

which can be expanded as:

$$I_{C_L} = I_{D0}e^{\frac{V_{DD}-V_p}{nV_{\mathrm{th}}}} - I_{D0}e^{\frac{V_{DD}+k\cdot\tan(\alpha)\cdot t}{nV_{\mathrm{th}}}} \tag{15}$$

where, $k \cdot \tan(\alpha)$ represents the slope of $V_{\mathrm{ramp}}(t)$. In Fig. 7, V_P is lower than V_{DD} during the comparator evaluation time. As a result, (15) can be simplified to:

$$I_{C_L} = I_{D0}e^{\frac{V_{DD}}{nV_{\mathrm{th}}}} - I_{D0}e^{\frac{V_{DD}+k\cdot\tan(\alpha)\cdot t}{nV_{\mathrm{th}}}} \tag{16}$$

The voltage variation at node V_n which would cause the output inverter to commutate is at half the supply ($V_{DD}/2$)

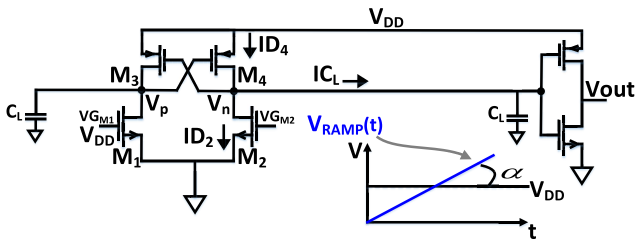

Fig. 6. Schematic of the subthreshold latch.

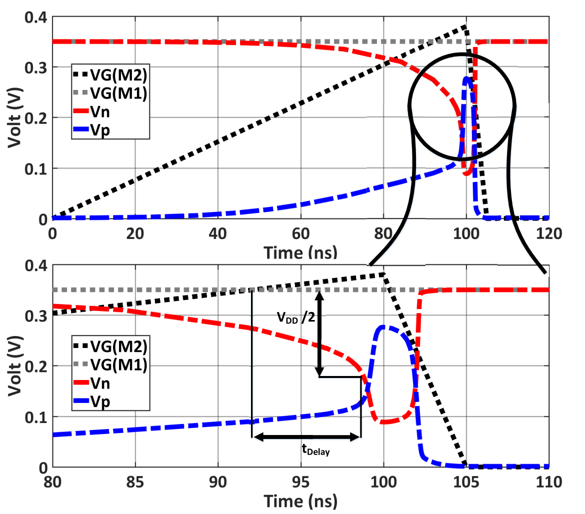

Fig. 7. Voltage waveforms of the internal latch signals.

and corresponds to the voltage shift caused by the current I_{C_L} integrated on capacitor C_L:

$$\int_0^{t_{\text{delay}}} \frac{I_{C_L}}{C_L} \mathrm{d}t = \frac{V_{\text{DD}}}{2} \tag{17}$$

Solving (17) for I_{C_L} (16) yields:

$$e^{\frac{V_{\text{DD}}}{nV_{\text{th}}}} t_{\text{delay}} - \frac{nV_{\text{th}}}{k \cdot \tan(\alpha)} e^{\frac{V_{\text{DD}} + k \cdot \tan(\alpha) \cdot t_{\text{delay}}}{nV_{\text{th}}}} = \frac{C_L V_{\text{DD}}}{2I_{D0}} \tag{18}$$

By using the Taylor series expansion of the exponential terms, (18) can be developed as:

$$e^{\frac{V_{\text{DD}}}{nV_{\text{th}}}} t_{\text{delay}} - \frac{nV_{th}}{k \cdot \tan(\alpha)} \cdot \left(1 + \frac{V_{\text{DD}}}{nV_{\text{th}}} + \frac{k \cdot \tan(\alpha) \cdot t_{\text{delay}}}{nV_{\text{th}}}\right) \approx \frac{C_L V_{\text{DD}}}{2I_{D0}} \tag{19}$$

Solving for t_{delay} results in:

$$t_{\text{delay}} \approx \frac{1}{e^{\frac{V_{\text{DD}}}{nV_{\text{th}}}} - 1} \left[\frac{nV_{th} + V_{\text{DD}}}{k \cdot \tan(\alpha)} + \frac{C_L \cdot V_{\text{DD}}}{2I_{D0}}\right] \tag{20}$$

It is evident from (20) that increasing the supply voltage (V_{DD}) or the gain of the Dickson CP VTC ($k \cdot \tan(\alpha)$) decreases the propagation time of the latch (t_{delay}), thus resulting in a faster A/D conversion.

Fig. 8(a) shows SPICE and the proposed MATLAB model of the simulated latch propagation delay for different input slopes of $V_{\text{ramp}}(t)$. In agreement with (20), steeper V_{ramp} ensures a shorter propagation delay. Similarly, a higher V_{DD} also results in a shorter propagation delay as suggested by (20) and shown by the simulated curve in Fig. 8(b).

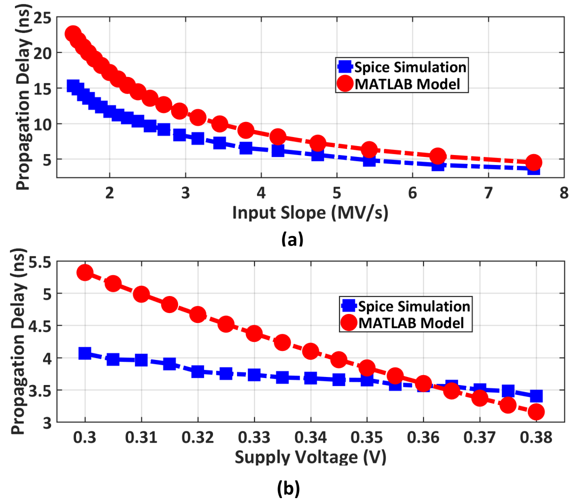

Fig. 8. SPICE and MATLAB model simulations of the latch propagation delay, t_{delay}: (a) vs. slope of V_{ramp} (i.e., $k \cdot \tan(\alpha)$), and (b) vs. supply voltage.

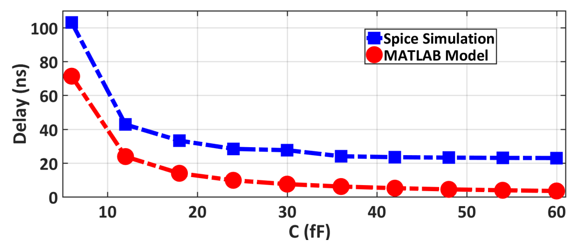

Fig. 9. Simulated rise-time of the Dickson CP output voltage vs. parasitic capacitance C, when C_{out} is set to 12 fF and f_{CLK} is set to 200MHz.

In the above analysis of the latch operating in subthreshold, we conclude that its propagation time is minimized thanks to the high input common-mode voltage at which the comparison occurs (i.e. V_{DD}).

In the next section, we will study the effect of the Dickson CP evaluation time on the proposed sub-ADC slice conversion. In that section, we assume that the ADC propagation delay is limited to the Dickson CP slope generation process.

The time for the generated Dickson CP output voltage ramp to cross V_{DD} (i.e. 360 mV) was simulated with SPICE, versus the node capacitance C, for an input voltage of 150 mV, and shown in Fig. 9. MATLAB model simulation of (2), in the absence of mismatch and clock skew is also added to Fig. 9. We conclude that higher C results in a faster generated slope due to the higher gain of the VTC. From the design point of view, if the proposed ADC's conversion delay is limited by the Dickson CP slope generation and, in order to limit the delay time of the generated slope to 60 ns, C of the Dickson VTC should be larger than 10 fF, based on the SPICE simulations.

Figures 10 and 11 show the Dickson CP propagation delay for different values of C_{out} and clock frequencies (which were shown in Fig. 2(a)). We conclude that to ensure this ADC to be

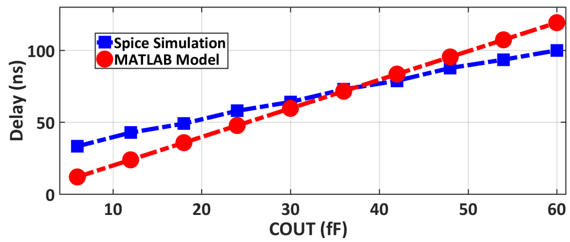

Fig. 10. Simulated rise-time of the Dickson CP output voltage vs. output capacitance C_{out}, when f_{CLK} is set to 200 MHz and C is set to 12 fF.

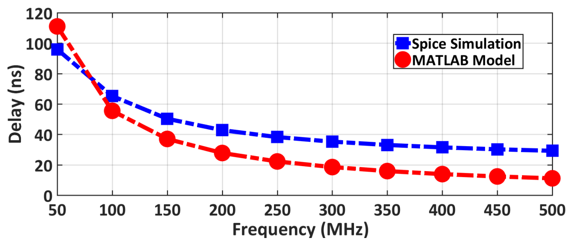

Fig. 11. Simulated rise-time of the Dickson CP output voltage vs. clock frequency, when C_{out} and C are set to 12 fF.

faster than 60 ns, the Dickson CP needs the output capacitor (i.e. C_{out}) lower than 28 fF and the clock frequency higher than 120 MHz.

In this design, the delay time allocated to the Dickson CP is 50 ns, which is due to the selection of 12 fF for C and C_{out} and 200 MHz for CLK_{VTC}. The delay timing for Dickson CP can be derived from Figs. 9–11. Based on the modeling equations and Spice simulation results in Fig. 8, the comparator delay time was allocated to 20 ns. In general, the delay time for the Dickson CP comparator was designed to be <70 ns. However, due to parasitics, the total measured delay time increased a bit.

The presented analysis and behavioral simulations suggest that the employed latches exhibit lower propagation time thanks to the high input common-mode voltage (i.e. the comparison occurs when the input terminals are around the supply voltage). We consider this the most significant reason as to why the proposed ADC is faster than the conventional ADCs in near-threshold or subthreshold region. Meanwhile, if the delay is mainly limited by the delay of the Dickson CP, which is the time interval that the generated slope in the output of the Dickson CP passes V_{DD} (shown in Fig. 3), SPICE and MATLAB modeling simulations confirm that choosing higher f_{CLK} and C and smaller C_{out} can make the proposed ADC faster than the conventional subthreshold ADCs.

The source of error for the divergence between MATLAB and Spice simulations stems from various factors including the body effect, rising/falling edge effects of the high-frequency clock on the performance of Dickson CP comparator, gate leakage current of the switches, and dependency of the voltages of the conducting switches on the input voltage.

C. Behavioral Modeling of Linearity Impairments

The voltage-to-time conversion delay comprises the exponential ramp of V_{ramp} waveform crossing the V_{DD} level and the nonlinear propagation time of the following latches. Remarkably, the nonlinear relationship between the CP differential input ($V_{in,S} - V_{ref,i}$) and the difference between the threshold crossing timestamps ($t_{sig} - t_{ref,i}$) does not impair the overall converter linearity as long as the respective Dickson CPs are matched (i.e. identical and with the same output load) within each sub-ADC slice. The actual top-level impairments include the time skew between the signal and reference CLK_{VTC} paths within a slice, which adds a systematic offset to the time difference $t_{sig} - t_{ref,i}$ to be detected (although reasonably suppressed by a symmetric layout), and the statistical mismatch of transistors and capacitors between the signal and reference Dickson CPs, which impacts both the R_S and V_S terms in the model of Fig. 2(b), and thus ultimately the threshold-crossing timestamps.

It is also worth mentioning the source of trade-off between bandwidth and accuracy in this ADC topology. A high CLK_{VTC} frequency results in a steeper slope of the Dickson CPs' output voltage (i.e. smaller equivalent time constant τ), which helps reducing the comparison time of the slices. Faster signals at the charge-pump outputs, however, decrease the time gap between t_{sig} and $t_{ref,i}$ (i.e. higher VTC gain), thus deteriorating the signal-to-noise ratio of the comparison latches, whose input-referred time-offset and noise are unchanged. Similarly, a high number N of Dickson CP stages would also result in a smaller t_{sig} to $t_{ref,i}$ difference, since the sensitivity of $V_{ramp,sig}$ and $V_{ramp,ref}$ to the CPs' input would be lower, as visible from the expression of V_S in Fig. 2(b).

The ADC is modeled numerically, describing each of the 54 slices, as depicted in Fig. 4. The proposed model is differential and the gain error between the Dickson CP voltage-to-time conversion of reference and signal paths is included. Delay mismatch $\Delta t_{err,DicksonCP}$ between these two paths is also added. At first, a 1% mismatch in the CP capacitance and in the conduction voltage threshold of CMOS switches is assumed, together with a clock skew of 20 ps between the reference and signal CPs, randomly distributed among ADC slices, further superimposed by 10 ps rms jitter. As per Fig. 2(b), all these nonidealities result in random deviations from the nominal time constant τ as well as V_S in the reference and signal Dickson CPs. The mismatch in the propagational delay between DFFs and latches in Fig. 4 is modeled with a random 1% standard deviation (std), with an additional 10 ps rms jitter added at the PD. MATLAB simulation results of the ADC quantization spectrum, for low and high input frequencies, are illustrated in Figs. 12(a)–(b), show 32 dB SNDR and ~52 dB SFDR. The visible harmonic distortion in the ADC output spectrum is caused by the mismatch between the reference and signal paths in each sub-ADC slice and also the dependency of the effect of this mismatch on the input analog signal, as was discussed in Section A.

Fig. 13 shows the numerically modeled SNDR of the proposed ADC versus the clock frequency of the Dickson CPs. Here, the only source of error is the thermal jitter of the PD, set to 10 ps rms input-referred. As mentioned earlier, increasing the clock frequency causes the Dickson charge-pumps to be more sensitive to the PD noise, as evident from the 6 dB drop in SNDR from 50 to 500 MHz. High clocking frequency

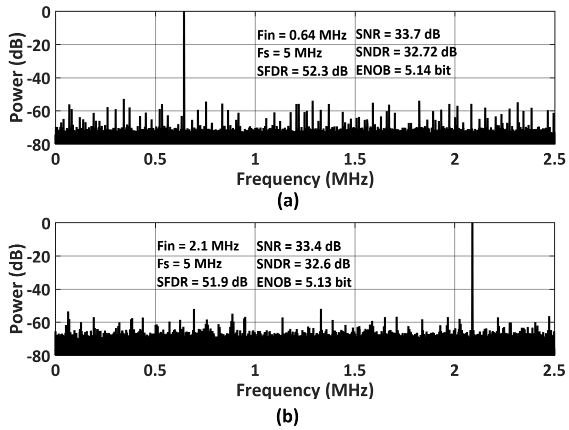

Fig. 12. Simulation results of MATLAB dynamic modeling when each of the 54 sub-ADC slices is subject to 1% standard deviation (std) mismatch, 20 ps clock skew error, and 10 ps rms jitter, for (a) 0.64 MHz and (b) 2.1 MHz input sine-wave signal.

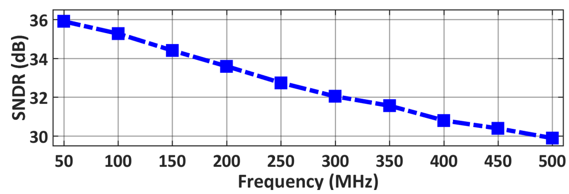

Fig. 13. Simulated SNDR vs. Dickson CP clock frequency.

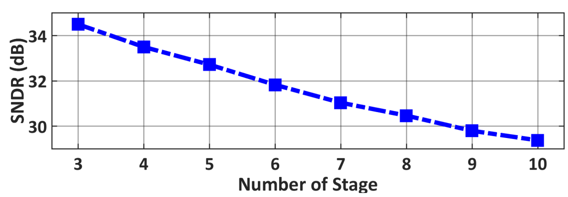

Fig. 14. Simulated SNDR vs. number of stages of the Dickson CP.

increases the bandwidth of the proposed ADC but results in high sensitivity to the jitter of the PD, which degrades the SNDR of the system.

The number of stages N within the charge-pumps also affects the noise-speed trade-off since higher N results in a steeper slope and can increase the bandwidth of the ADC thus boosting the effect of PD noise on the overall SNDR, as shown in Fig. 14 of the MATLAB modeling simulations.

Figure 15 shows the effects of various mismatches between the reference and signal Dickson CP paths in each sub-ADC slice on the total SNDR. We include the input-referred PD jitter of 10 ps rms. Subfigure (a) deals with the time-constant mismatch (i.e. τ in Fig. 2(b)) caused by the mismatch between C's and C_{out}'s. A 10 dB drop in the ADC SNDR is revealed. Subfigure (b) deals with the mismatch in the drop voltage V_{on} of the CMOS switches. The results show an 8 dB SNDR degradation when the error std changes from 0 to 6%.

As previously described, the clock skew between the reference and signal Dickson CPs can be modeled as an initial voltage mismatch ($V_{0,\text{sig,ref}}$) between the output capacitors C_{out} of the charge pumps. Fig. 16 presents behavioral modeling

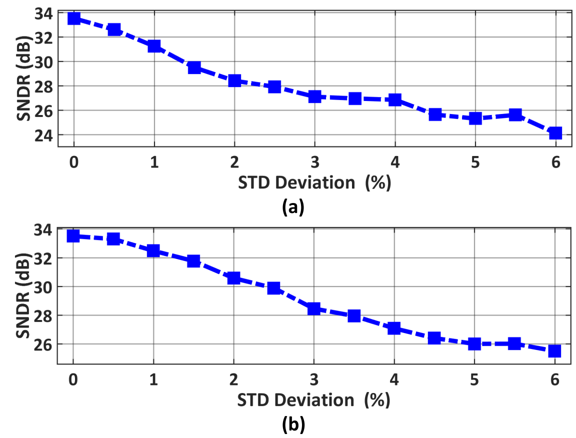

Fig. 15. (a) Effect of std variation mismatch in the Dickson CP's equivalent exponential time constant on the ADC SNDR, (b) and effect of SNDR vs. std variation of the conducting threshold voltage (V_{on} with reference to Fig. 2) in Dickson CP.

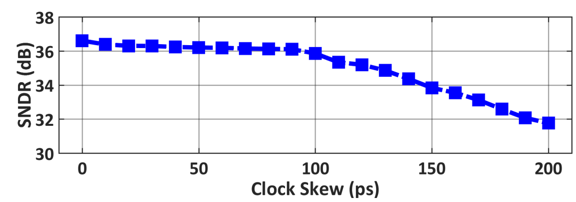

Fig. 16. SNDR vs. clock skew error between signal and reference paths of sub-ADC slice.

simulation results of the complete ADC with a sole imperfection source of the clock timing skew, which is modeled as a randomly distributed error among the ADC slices, ultimately resulting in an offset $\Delta t_{e,skew} = t_{\text{sig}} - t_{\text{ref,i}}$ of the ith sub-slice. Simulation results reveal a 5 dB SNDR degradation from 0 to 200 ps in the clock skew error. If the slope of the Dickson CP output voltage were steeper, the sensitivity of the sub-ADCs to the clock skew error would be higher due to the smaller timing signal $t_{\text{sig}} - t_{\text{ref,i}}$.

The presented behavioral modeling simulation results serve the purpose of outlining circuit specifications and providing directions to the design of the proposed time-mode flash ADC. Increasing the clock frequency broadens the ADC bandwidth, albeit resulting in a higher sensitivity to noise, thus degrading the system's SNDR and power efficiency (with reference to Figs. 11 and 13). Furthermore, designing the Dickson CP with a higher number of stages N, as shown in Fig. 2(a) has the same effect as increasing the clock frequency.

D. Monte Carlo Simulations and Input Referred Offset Voltage

In this section, Monte Carlo simulations of the designed Dickson CP are presented. Fig. 17 shows the test setup. Two identical Dickson CP ramp generators, representing reference and signal circuit paths, are fed with the identical input DC voltage and high frequency clock (i.e. 200 MHz) to quantize the generated ramp signal based on the input DC voltage. In the absence of mismatch between the two Dickson CPs,

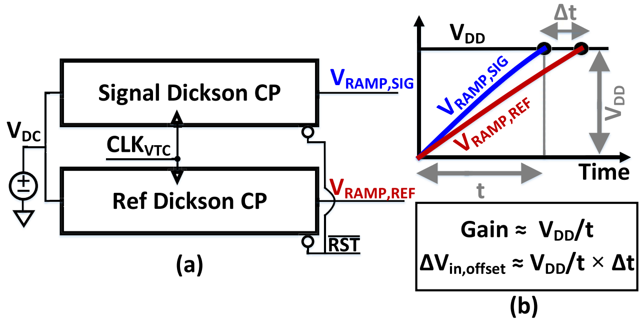

Fig. 17. (a) Test setup for the SPICE Monte Carlo simulation of the proposed Dickson CP ramp generator to calculate the input referred offset voltage. (b) Timing generated error of the Dickson CP due to the mismatch and the used approach to calculate the input referred voltage of the Dickson CP time compartor.

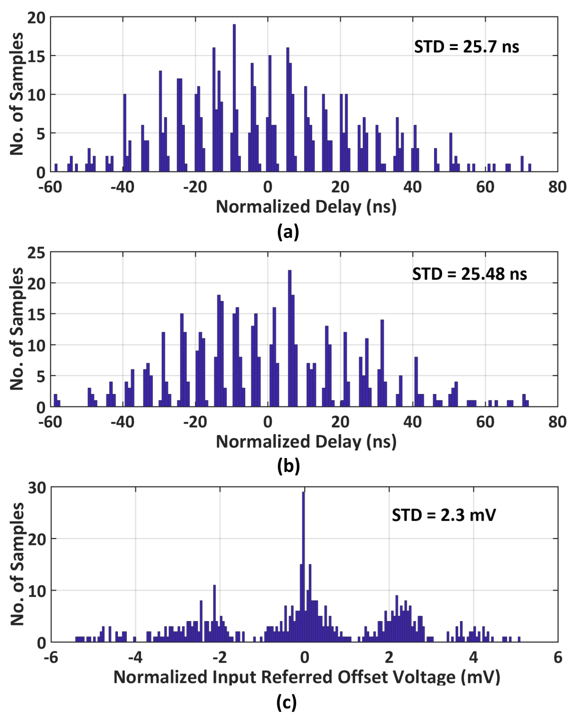

Fig. 18. (a) Monte Carlo simulation results of the reference Dickson CP. (b) Monte Carlo simulation results of the signal Dickson CP. (C) Normalized input-referred offset voltage of the Dickson CP ramp generator.

the times at which the generated ramp passes the V_{DD} are identical. Due to the mismatch between the two reference and signal paths, small timing error will be generated as shown in Fig. 17(b). The generated timing error (i.e. Δt), can be mapped as the input offset voltage, which is defined as the input offset voltage that should be added or subtracted from the input DC voltage to the Dickson CP to compensate the timing error due to the mismatch effect. To calculate the input-referred offset voltage of the Dickson CP, gain of the generated ramp should be calculated based on the mentioned equations in Fig. 17(b).

Figs. 18(a) and (b) show the normalized SPICE Monte Carlo simulation results of the reference and signal Dickson CP circuits around the time at which the generated ramp signals pass V_{DD}. It was executed for 500 points. Fig. 18(c) shows the input-refereed offset voltage of the Dickson CPs simulated in Figs. 18(a) and (b). The offset voltage was calculated based on the mentioned approach in Fig. 17(b). The calculated std from Fig. 18(c) is 2.3 mV, which is less than one LSB of the proposed ADC. The input voltage to the ADC goes from 150 mV to 360 mV, resulting in a 210 mV voltage swing amplitude. The LSB of this ADC can be calculated by dividing the voltage swing amplitude by 54 voltage levels, resulting in 3.8 mV LSB. In the proposed structure, there is a trade off between the ADC's bandwidth and the input-referred offset voltage. Higher clocking frequency (CLK_{VTC}) leads to a higher bandwidth but also a higher input-referred offset voltage due to the mismatch and higher ramp gain (with reference to Fig. 17(b)).

As mentioned in Section III-A and also indicated via formulas (6), (8) and (10), the effect of timing error mismatch (i.e. Δt) on the output of the Dickson CP comparator, when the input signals are connected together (see Fig. 17), is varied and depends on the dominant source of Δt. On the other hand, the discrete-time nature of the Dickson CP comparator, which is caused by the use of high frequency clocking to generate the output ramp signal, alongside with the varied effect of mismatch error on the time gap error, results in the discrete probability distribution in Fig. 18.

IV. Circuit Implementation

The proposed time-mode flash ADC is implemented in the low-power (LP) flavor of TSMC 28-nm CMOS technology. Fig. 19 shows the architecture consisting of a subthreshold core operating at the single 0.36 V supply, a low-voltage differential-signaling (LVDS) receiver for the Dickson CPs clock (CLK_{VTC}) and output voltage level shifters for transmitting the digital output to the off-chip data acquisition. The subthreshold core is made of six sub-ADCs, a clock generator block mainly consisting of inverters and buffers, thermometer-to-binary encoders (T2B) and a digital adder. Fig. 19(b) presents the schematic diagram of each sub-ADC consisting of a transmission-gate sample-and-hold (S&H) controlled by the sampling clock CLK_{ref}, a resistor ladder generating the reference voltages for the Dickson CPs and the previously described nine identical ADC slices. The threshold-crossing logic comprises the latches, converting the amplitude-domain input analog information into time-domain information. The PD generates logic 1 or 0 whenever V_{in} is respectively higher or lower than $V_{ref,k}$. The 9-bit output of each sub-ADC is thermometer encoded and, similarly to voltage-mode flash ADCs, it is firstly converted into binary by the T2B encoders and then summed to the other sub-ADCs outputs.

The Dickson charge-pumps, previously presented in Fig. 2, are implemented as four cascaded stages and employ 12 fF MOM capacitors for both the inter-stage loads C and the output C_{out}. The output voltage ramp generated by the CPs exceeds the supply V_{DD} by more than a factor of 2. The frequency of CLK_{VTC} is set to 200 MHz. From a top-level perspective, the ADC arrangement consisting of 6 sub-sections, each made of 9 sub-ADCs slices, simplifies the physical layout and increases the symmetry to reduce the effect of mismatches.

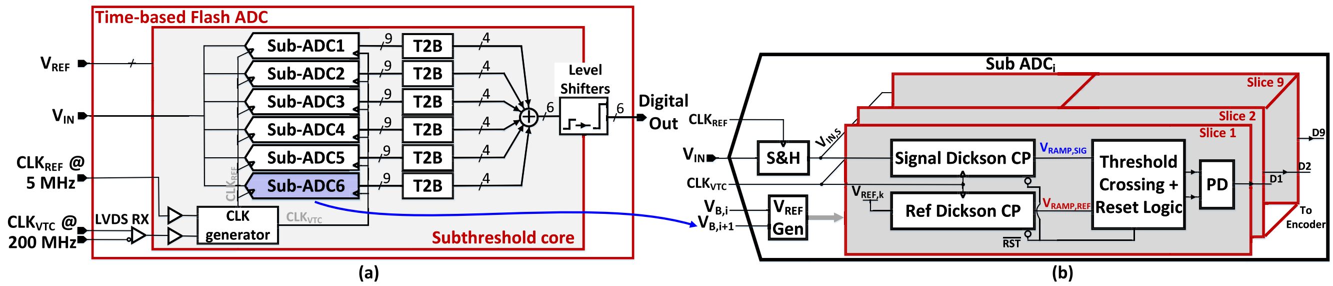

Fig. 19. (a) Architecture of the proposed ultra-low-voltage time-mode flash ADC, and (b) sub-ADC diagram.

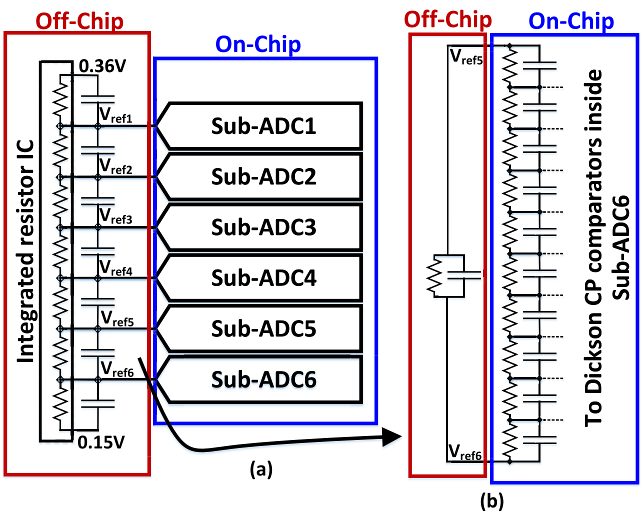

Fig. 20. (a) Off-chip reference voltage divider topology. (b) interaction of off-chip and on-chip voltage reference generator.

In the proposed system, the reference voltage divider circuit consumes power, which is due to the input charge pumping capacitor of the Dickson CP (i.e. C), shown in Fig. 2. By using large decoupling capacitors for the voltage reference generator (i.e. 12 pf for each stage), the reference voltage will be stable since the charge pumping capacitor size of the Dickson CP is $\sim$1000$\times$ smaller than the decoupling capacitor of the voltage reference generator. Same method is also applied for the sample & hold circuit.

Fig. 20 shows the resistor reference voltage divider comprising the on-chip and off-chip components. The off-chip voltage reference divider circuit uses integrated resistors, available on the market as an IC pack, which guarantees more than 99.9% matching accuracy, thus making them suitable for the reference voltage divider. Generated voltage references from the off-chip integrated resistor IC are fed into the chip and the internal voltage resistor divider provides the required reference voltages for each Dickson CP comparator. Large off-chip and on-chip decoupling capacitors in the reference voltage generator filter out high frequency ripples, thus making the reference voltage clean and stable.

Fig. 21 illustrates the LVDS clock receiver used as an input interface and buffer for CLK_{VTC}. External current is provided for biasing and two CMOS inverters are used to gradually shift down the clock's high-level voltage, from 1.8 V to 1 V, and then finally to 0.36 V, so as to be compatible with the sub-threshold ADC core supply voltage. It is worth mentioning that the used 1.8 V and 1 V are for the test setup system and I/O path and not for the core of the designed ADC. Fig. 22 shows the schematic of output level shifters, revealing a cross-coupled structure followed by two cascaded inverters.

Fig. 23 shows the digital encoder topology at the output of the ADC, prior to transmitting the digital ADC signals to the output data acquisition.

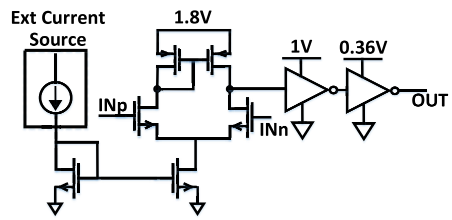

Fig. 21. LVDS RX circuit.

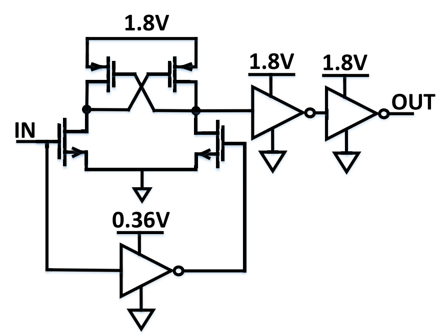

Fig. 22. Circuit schematic of level shifter.

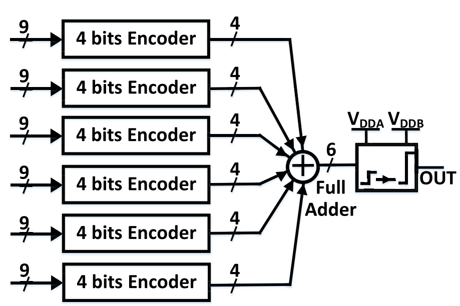

Fig. 23. Digital encoder topology.

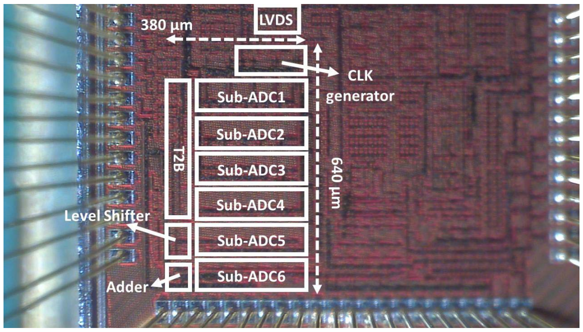

Fig. 24. Die micrograph.

The proposed structure has the advantage of being operational in sub-threshold voltage due to the use of the Dickson CP circuit as the VTC. Comparing with conventional ramp based ADC, the proposed structure can set the input common mode voltage of the comparator to V_{DD}, which increases its speed. Using two identical Dickson CPs as the VTC and single-bit phase detector (i.e. PD) can also relieve the proposed ADC from the effects of the non-linearity of the generated ramp signal in the output of each Dickson CP circuit, since the non-linearity of the ramps can cancel out each other. By setting the frequency of the CLK_{VTC} in the Dickson CP, the slope of the generated ramp can be adjusted, resulting in a tunable bandwidth and power consumption of the proposed system. In conventional time-based ADCs, the bandwidth tunability has different challenges due to the fixed resolution of the following TDC block while in the proposed system these challenges are solved by using the one bit phase detector and time processing approach. The proposed time-based flash ADC can be operational at very small supply voltages and can be used in IoT front-end applications without any need for bulky DC-DC converter.

V. Measurement Results

The proposed ADC, whose chip micrograph is shown in Fig. 24, is fabricated in TSMC 28 nm LP CMOS and occupies an area of 0.22 mm^2. The total power consumed by the ADC running at the maximum conversion rate of 5 MS/s is 88 μW, also including the 0.36 V input buffers inside the output voltage level-shifters. The consumed power is broken down as: 41% for the sub-ADCs (including the two identical Dickson CPs in each slice, PD, V_{ref} generator, including 1.9 μW burned by the off-chip reference generator circuit, S&H and reset logic), 48% for the CLK generator and buffers and 11% by the T2B encoders and digital adder. The digital output of the ADC is synchronously sampled using a logic analyzer.

The static linearity characterized at the 0.36 V nominal supply, 5 MS/s sampling rate and with a 10 kHz input sinewave is shown in Fig. 25, demonstrating a differential (DNL) and integral nonlinearity (INL) respectively equal to +1.4/−0.83 LSB and +1.6/−1.3 LSB.

The dynamic linearity characterization of the ADC is presented in Fig. 26. It displays spectra of the low-frequency

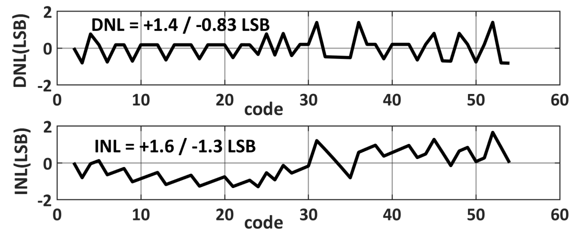

Fig. 25. DNL & INL measurement results.

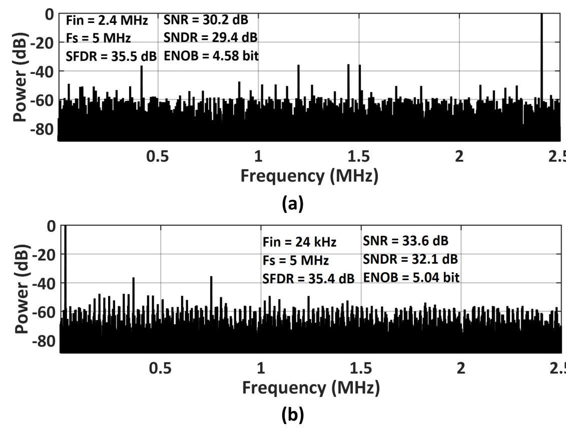

Fig. 26. Dynamic characterization measurement results: (a) 2.4 MHz, (b) 24 kHz input sine wave signal.

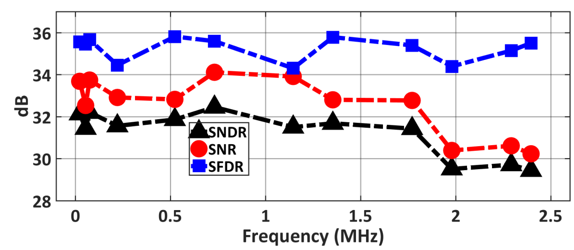

Fig. 27. Dynamic parameters vs. input frequency.

(24 kHz input sinewave) and near-Nyquist (2.4 MHz) inputs at the maximum conversion rate of 5 MS/s. At the low input frequency, the measured SFDR and SNDR are 32.1 and 35.4 dB, respectively, resulting in an effective number of bits (ENOB) of 5.04. At Nyquist frequency, SFDR, SNDR and ENOB are equal to 35.5 dB, 29.4 dB and 4.58 bit, respectively. As shown in Fig. 26, several tones of the measured power spectrum have high power, which is due to the dependency of the effects of non-linearity of the Dickson CPs on the input level of analog signal, as discussed in Section III-A, and also it matches with the MATLAB modeling simulations in Fig. 12.

Fig. 27 shows the measured SFDR, SNR and SNDR for different input sine-wave frequencies, while the SNDR characterization over three different ICs at 5 MS/s sampling frequency and versus the input sine-wave frequency is shown in Fig. 28, demonstrating less than 10% performance variation for the three measured ICs. Due to the large sample & hold capacitor that helps with providing enough charge for the input

TABLE I
PERFORMANCE SUMMARY AND COMPARISON TABLE

	[1]	[2]	[32]	[33]	[34]	[38]	[39]	[9]	[40]	[21]	**This Work**
Architecture	SAR	SAR	SAR	SAR	Pipline	ZC TD	Two-step	PPM	TI Ramp	CP	**TD flash**
Technology (nm)	40	65	90	90	90	180	180	65	130	90	**28**
Sampling Rate (MS/s)	0.2	0.1	0.1	0.25	160	20	3.4	1	250	100	**5**
Supply Voltage (V)	0.45	0.6	0.5	0.4	0.55	1.8	1.8	1	1.1	1	**0.36**
SNDR (dB)	55.63	57.14	66.2	53.7	37.88	44.2	59.1	49.3	49.95	37.1	**29.4**
ENOB	8.94	9.19	10.7	8.62	6	7.04	9.52	7.89	8 8	5.8	**4.6**
FoM (fJ/c-s)	0.85	1.5	4.82	2.02	240	1600	1150	98	399	237	**735**
Power (μW)	0.084	0.088	0.81	0.2	2430	4640	2900	14	25300	1390	**88**
DNL (LSB)	0.44	0.96	0.7	0.47	1.8	0.72	0.47	0.28	0.57	0.96	**1.4**
INL (LSB)	0.45	0.87	0.87	0.53	1.3	1.07	0.6	0.49	0.63	0.6	**1.6**
Area (mm^2)	0.006	0.2	0.1	0.048	0.25	0.84	0.072	0.06	0.55	0.044	**0.24**

FOM = Power / (sampling rate $\times$ 2^{ENOB})

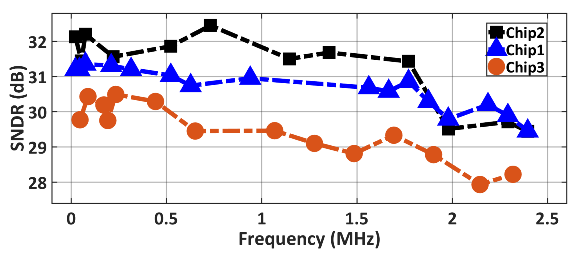

Fig. 28. SNDR variation for three different samples, across input frequency.

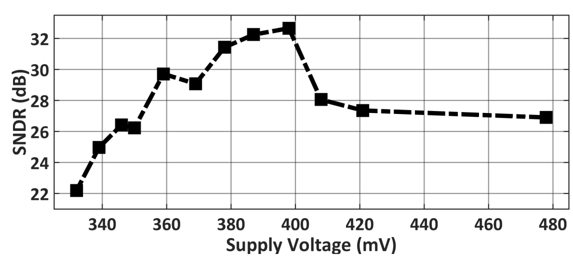

Fig. 29. Measured SNDR across VDD.

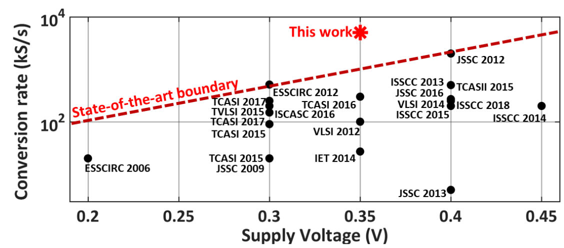

Fig. 30. Conversion rate versus supply voltage benchmarking.

capacitor of the Dickson CP, the measured SNDR drops by 3 dB at higher frequencies, as shown in Fig. 27.

Fig. 29 plots the SNDR versus supply voltage, swept from 330 to 480 mV, at 2.4 MHz input frequency and 5 MS/s conversion rate. It exhibits less than 10% variation in the range above 340 mV. At low supply voltages, the system is very sensitive to noise, resulting in low SNDR. With increasing the supply voltage, SNDR increases gradually due to the higher SNR of the system. Further increase in the supply voltage makes the generated ramp signals steeper and so the timing gap between the reference and signal ramps (i.e. $V_{\text{ramp,ref}}$ and $V_{\text{ramp,sig}}$ in Fig. 3) will be reduced. By reducing this time gap, the generated signals will be more sensitive to the phase noise of the phase detector, leading to further decrease in the SNDR at high supply voltages.

Table I summarizes the ADC performance and compares it to published ADCs. The proposed ADC achieves the high conversion rate at the lowest supply voltage, thanks to the use of Dickson CPs as the voltage-to-time converters, generating comparison voltages at the supply level.

Fig. 30 presents a benchmark landscape of the proposed ADC in the panorama of state-of-the-art subthreshold ADCs in terms of conversion rate versus supply voltage. The proposed converter achieves the highest conversion speed in a completely digital-friendly implementation, avoiding current sources and OTAs.

VI. CONCLUSION

This paper presented a subthreshold time-mode flash ADC working under an ultra-low 360 mV supply. It makes use of arrays of Dickson charge pumps as voltage-to-time converters in order to encode the input voltage into time information (i.e. timestamps of digital transition edges), which is more amenable to the deep-subthreshold regime. The achieved effective resolution is 5 bits and the maximum achieved sampling rate is 5 MS/s, which is the record among near and sub-threshold designs. The proposed structure does not need any calibration and is insensitive to the non-linearity of the Dickson CP's output ramp signal.

The effects of representative scenarios of circuit nonidealities on the ADC performance are investigated both analytically and by means of behavioral modeling simulations. Delay characteristic requirements of the used latches and Dickson CPs are also formalized.

The ADC prototype is fabricated in TSMC 28-nm LP CMOS and occupies an active area of 0.24 mm^2. The proposed system achieves the fastest conversion rate compared to the prior art in subthreshold ADCs, relies on its mostly digital implementation as well as on the time-mode operation.

ACKNOWLEDGMENT

The authors would like to thank TSMC for chip fabrication, Dr. P. E. P. Filho and V. A. Nguyen for their technical discussions and MCCI for technical support.

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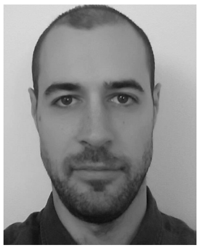

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