

Experimental Verification of the Impact of Analog CMS on CIS Readout Noise

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Abstract—In this article, the impact of the combination of the column-level gain and the correlated multiple sampling (CMS) on the noise of CMOS image sensor (CIS) readout chains is first analyzed. The theory is then validated experimentally with CIS readout chains embedding two different pixels, a variable gain column-level amplifier (CLA) and a passive switched-capacitor (SC) CMS circuit. The noise measurements include photon transfer curves (PTCs) for different gains and pixels and they show reasonably well that CMS reduces the 1/f noise by about 33% for order 8 as expected theoretically.

Index Terms—CMOS image sensors, correlated multiple sampling, low light application, low noise design, pixel design.

I. INTRODUCTION

LOW noise image sensors are widely used in applications such as surveillance, security, night vision and consumer electronics [1]–[3], where a good low light performance is fundamental. Nevertheless, the feature of high sensitivity is also very useful in applications like microscopy, high-precision scientific imaging and 3D vision based on indirect-Time-of-Flight (I-ToF) imagers [4]–[6]. The current state-of-the-art in low noise CIS exhibits sub-electron input-referred total noise [7], which represents a step towards the single photon detection capability for these sensors [8]. To achieve such a low input-referred noise, reduction techniques at different levels need to be implemented. At process level, changes in the standard flow are used in [9]–[11], whereas only pixel-level optimizations and circuit techniques are used in [12], [13]. Once the contribution of the column-level stages is reduced by using high column-level voltage gain, the noise contribution from the pixel becomes the dominant noise source, particularly the one generated by the in-pixel source follower (SF). At pixel-level, the degrees of freedom left to designers are generally limited. For example, in [14] the noise contribution of the SF is lowered by using an in-pixel thin oxide pMOS SF. Different circuit techniques compatible with different pixels can be implemented instead at column-level. A higher column-level gain corresponds in fact to a reduced bandwidth, hence a reduction

in the total integrated thermal noise. The high gain also mitigates the noise contribution of the next stages at the cost of a lower dynamic range. The CMS is an alternative to reduce not only the thermal noise, but also to decrease the low frequency [15]–[17] and Random Telegraph Signal (RTS) noise [18].

Different implementations of the CMS are reported in the literature, which exploit both analog and digital techniques. The typical analog implementation of the CMS cumulates the sum of M consecutive samples by using an integrator circuit [11]. However, this solution may suffer from a dynamic range reduction. Digital implementations for the CMS [19]–[21] require multiple analog-to-digital conversions, which requires faster analog-to-digital converter (ADC) resulting in higher power consumption. In this work, the SC CMS circuit described in [22] is implemented for the first time in a 0.18 μm CIS technology. This circuit takes advantage of a simple SC circuit to average the reset and the signal output samples and perform the CMS, without the need of any additional circuits, feedback loops or multiple analog-to-digital conversions.

The aim of this work is to precisely analyze the impact of the combination of the column-level gain and the CMS on the input-referred noise and then to validate the theoretical model with measurements made on CIS readout chains embedding two different pixels, a column-level amplifier and a passive SC analog CMS.

This paper is organized as follows: in Section II, the operation principles of the pixel, the CLA and the CMS in a conventional low noise CIS readout chain are briefly described. In Section III, the various noise sources in CIS are summarized, while the formulas for the temporal readout noise in CIS are recalled, together with the main noise reduction techniques. In Section IV, the implemented readout chains are described, from the pixels, to the amplifier and the SC CMS circuit. The experimental setup together with the readout characterization and the noise measurements are given in Section V. Finally, the conclusions of this work are drawn in Section VI.

II. LOW NOISE CIS READOUT CHAINS

Fig. 1(a) shows the block diagram of a conventional low noise CIS. At the center of the diagram, the pixel array contains all pixels in a number of n rows and m columns. Each pixel is made of a pinned photodiode (PPD) together with four transistors (4T). The PPD is a device made of a buried n-well and a highly doped p^+ shallow layer, which implements a

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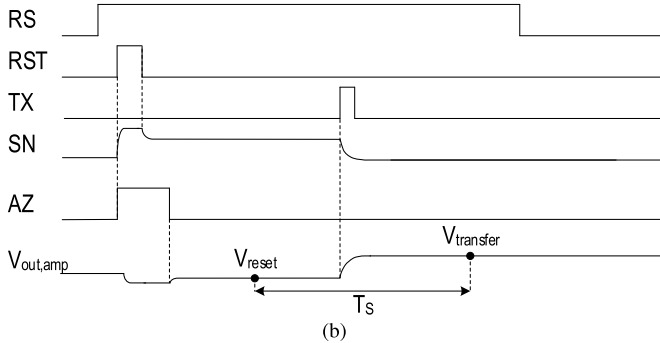
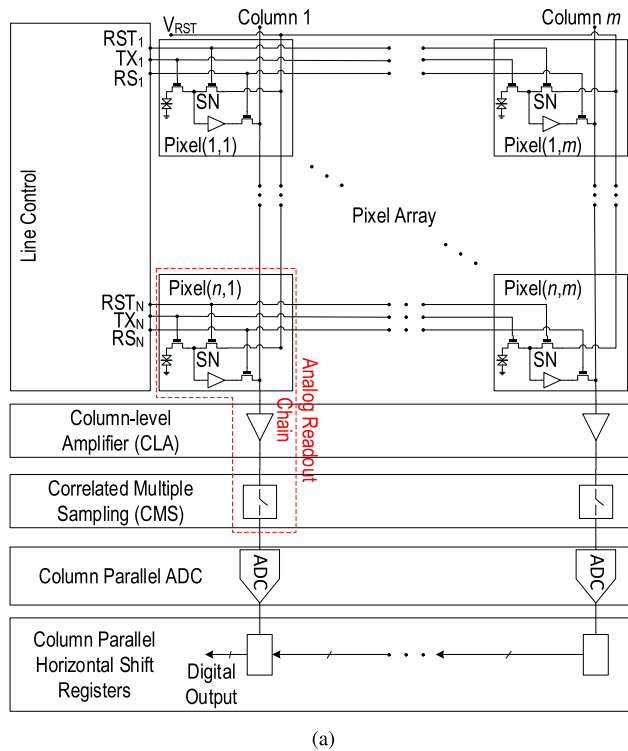


Fig. 1. (a) Block diagram of a low noise CIS. (b) Timing diagram of a low noise CIS readout chain.

potential well for the photoelectrons to be stored [23], [24]. The four transistors are the transfer gate (TX), the reset transistor (RST), the row select (RS) and a single stage in-pixel amplifier. Typically, the latter can be implemented either as a common source (CS) [13], [25] or as a SF. In this work, a SF topology is used inside each pixel in order to take advantage of the large voltage swing, the robustness against the reset switch non-ideality [26] and the process spatial variations. The Line Control block in Fig. 1(a) controls each row and enables the signals according to the array readout scheme. The timing diagram of the control and output signals for the low noise CIS is shown in Fig. 1(b). The pixel is selected during the entire readout operation by the high value of the RS signal. First, a pulse on RST allows to set the sense node (SN) voltage to V_{RST} , while an auto-zero (AZ) operation is performed on the CLA. The AZ allows to store on the input capacitance of the amplifier a voltage value including the offset and the low frequency noise of the amplifier itself [26]. Once stored, this value is subtracted from the signal applied

at the input. This is a simple and common way to reduce the offset and the low frequency fluctuations in a voltage amplifier stage [26]. The output of the pixel is connected to the column line, which connects to the input of the CLA. The latter introduces a certain amount of voltage gain in order to increase the overall conversion gain, CG , which is also fundamental to decrease the impact of the blocks following the amplifier on the input-referred noise [27]. After the SN and the output of the amplifier are settled, the first sample, V_{reset} , of a correlated double sampling (CDS) can be stored. At the end of the light integration time, the photogenerated electrons in the PPD are transferred to the SN by applying a pulse to TX. When the SN and the amplifier settle to a value proportional to the transferred amount of charges, a second sample of the output, $V_{transfer}$, is stored. The difference between these two samples is performed and the obtained value is passed to the following stage. Thanks to the correlated sampling operation, the kT/C noise sampled at the SN after the reset operation can be canceled. In fact, both samples involved in the difference embed the same frozen kT/C component [15]. After the stage for correlated sampling, a column-parallel ADC conversion is performed. The outputs of the various ADCs are shifted in an horizontal shift register in order to have a single digital output for the image sensor.

III. REVIEW OF NOISE IN CIS READOUT CHAINS

A. Noise Sources

In a CIS, the signal is corrupted by numerous noise sources and the noise can be injected at different levels: during the photoelectron generation at the PPD, during the charge transfer from the PPD to the SN or at the level of the readout circuit. The mechanisms behind these noise sources are also different. For example, the photon shot noise (PSN) is due to the nature of the light, whereas the dark current noise (DCN) and the transfer noise depend on device defects; the fixed pattern noise (FPN) is caused by pixel-to-pixel or column-to-column non-uniformities, and the thermal, the flicker and the shot noise sources are generated by the electronic devices [28]. Some of the aforementioned noise sources, such as the PSN and the FPN, are also signal-dependent noise sources, hence their variance depends on the level of the input light [29]. To evaluate the role of each noise source in different applications, the signal-to-noise ratio (SNR) can be expressed as

$$SNR = 10 \log \left[\frac{N^2}{\sigma_{Sh}^2 + \sigma_D^2 + \sigma_T^2 + \sigma_F^2 + \sigma_R^2} \right], \quad (1)$$

where N is the average number of photoelectrons stored in the PPD, σ_{Sh}^2 the PSN variance, σ_D^2 the dark current shot noise (DCSN) variance, σ_T^2 the transfer noise variance, σ_F^2 the FPN variance and σ_R^2 the total input-referred read noise, which includes the thermal, $1/f$ and shot noise contributions generated by the readout circuit and can be assumed to be signal independent. The other variances are signal-dependent and can be expressed as follows: σ_{Sh}^2 is equal to N and σ_D^2 to N_D , the average number of electrons generated in the dark inside the PPD for a given integration time; σ_T^2 is equal to the charge transfer inefficiency (CTI) times N and σ_F^2 the CG variance,

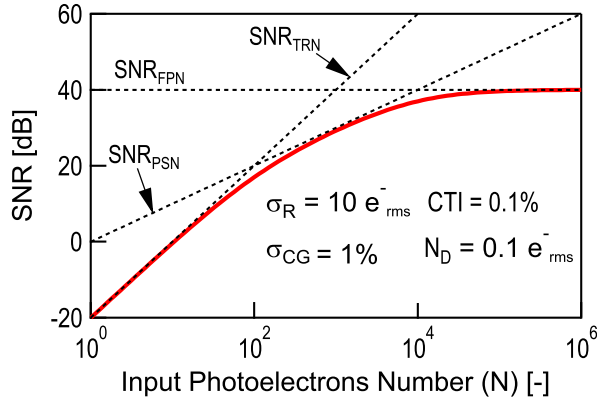


Fig. 2. Plotted in red, the total SNR as a function of the input photoelectrons number, N . In dashed lines, the SNRs which take into account only the TRN, the PSN and the FPN. These lines show the range of photoelectrons where each noise source is dominant.

σ_{CG}^2 , times N^2 . Fig. 2 shows the SNR as a function of the photoelectron number N , for typical values of $N_D = 0.1 e_{rms}^-$, a CTI of 0.1% and a $\sigma_{CG} = 1\%$ for the FPN. σ_R is assumed to be equal to $10 e_{rms}^-$ in Fig. 2. The SNR which includes only the Temporal Read Noise (TRN) is named SNR_{TRN} , and, equivalently, SNR_{PSN} is introduced for the PSN and SNR_{FPN} for the FPN. These quantities are plotted in dashed lines to highlight the contribution of each noise source in different ranges of illumination. The figure shows that the signal-dependent noise sources dominate the noise at high signal level, the PSN at mid range and the FPN at higher signal levels, whereas, at low signal level, the TRN is the dominant noise source. This shows the importance of minimizing the TRN for low light imaging.

B. Readout Noise

A detailed noise analysis for a low noise CIS readout chain is presented in [30]. The total noise variance in a readout chain composed by a single pixel, a CLA and a generic CMS circuit is derived by calculating all the transfer functions and by defining the power spectral density (PSD) of each noise source. In this analysis, the noise sources coming from the different devices are assumed to be statistically independent while the shot noise contribution of the gate leakage current is neglected [31]. The expressions of the input-referred charge noise variances for the thermal and flicker noise derived in [29] are reported in this paper. These expressions make use of the EKV formalism, which is described in [32] and are fundamental to evaluate the impact of process and design parameters on CIS noise performance.

The total input-referred noise charge variance for the thermal noise derived in [29] is given by

$$\overline{Q_{th}^2} = \alpha_{th} \cdot \frac{kT}{A_{col} C} \left[\frac{\gamma_{SF} G_{mA} \left(\frac{2}{3} C_{ox} WL + 2 C_{ex} W + C_p \right)^2}{G_{mSF}} + \frac{\gamma_A}{A_{CG}^2} \right], \quad (2)$$

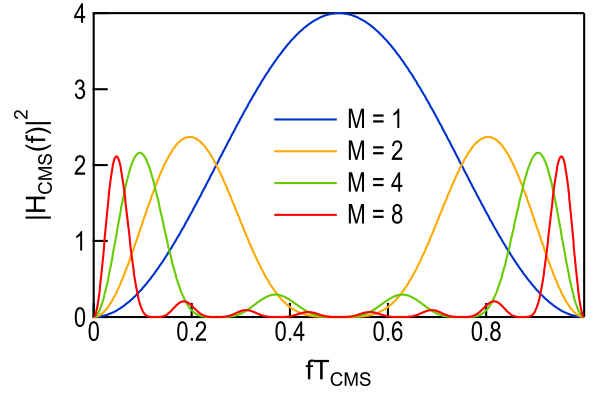


Fig. 3. The term $|H_{CMS}(f)|^2$ as a function of the frequency normalized to the CMS sampling period T_{CMS} , for four different values of the CMS order.

where k is the Boltzmann constant, T the temperature expressed in Kelvin, A_{col} the CLA gain and A_{CG} the pixel conversion gain (in V/C); C is equal to $C_L + C_{in}/(A_{col} + 1)$, where C_L and C_{in} are the amplifier load and input capacitances, respectively, γ_{SF} and γ_A are the excess noise factors of the in-pixel SF and the amplifier [32], $G_{m,SF}$ and $G_{m,A}$ the SF and the amplifier transconductances. The SF gate size are expressed as W and L , C_{ox} is the oxide capacitance per unit area and C_{ex} the extrinsic capacitance per unit width of the in-pixel SF transistor. The latter consists of the overlap and the fringing field capacitances of the SF transistor, which does not include C_p , the sum of the parasitic capacitances at the SN. In (2), α_{th} is a unitless parameter, defined in Appendix (13), that is inversely proportional to the CMS order, M , showing the noise reduction feature of CMS on thermal noise [29].

The CMS consists in averaging M samples of the SN reset voltage and M other samples of the same SN voltage after having transferred the photogenerated charges from the PPD to the SN. The difference between the two averages is the signal voltage proportional to the photo-integrated charge. In Appendix, the impact of the CMS process on the input-referred noise is discussed. It is shown that it can be evaluated by using only the noise PSD and the square magnitude of the CMS transfer function, $|H_{CMS}(f)|^2$, plotted in Fig. 3 as a function of the frequency normalized to the CMS sampling period, T_{CMS} , and for different values of M . The area delimited by $|H_{CMS}(f)|^2$ reduces when increasing the value of M , hence the thermal noise variance at the output of the CMS is inversely proportional to M .

The thermal noise reduction with M is in agreement with Fig. 4 that shows a numerical evaluation of α_{th} normalized to $2/M$ and plotted as a function of $f_c T_{CMS}$, the product between the readout chain cut-off frequency and the CMS sampling period. From the figure, α_{th} is approximately equal to $2/M$ when enough settling time is given to the signal between the CMS samples ($f_c T_{CMS} \geq 1$). This clearly illustrates quantitatively the reduction of the thermal noise thanks to the noise averaging provided by the CMS process.

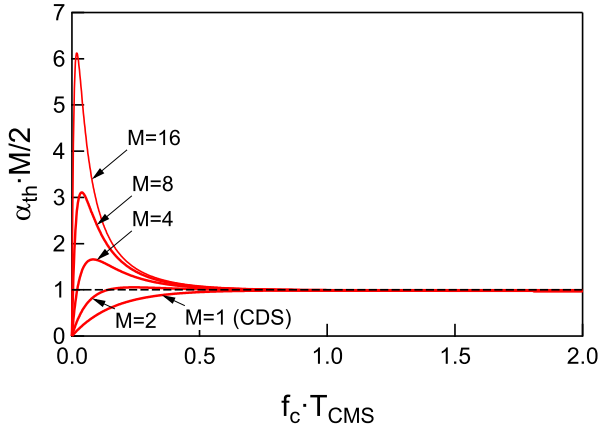


Fig. 4. The parameter α_{th} is multiplied by $M/2$ and plotted as a function of $f_c \cdot T_{CMS}$ for different values of M .

On the other hand, the input-referred $1/f$ noise charge variance derived in [29] leads to the following expression

$$\overline{Q_{1/f}^2} = \alpha_{1/f} \cdot \frac{K_F \left(C_p + 2 C_{ex} W + \frac{2}{3} C_{ox} W L \right)^2}{C_{ox}^2 W L}, \quad (3)$$

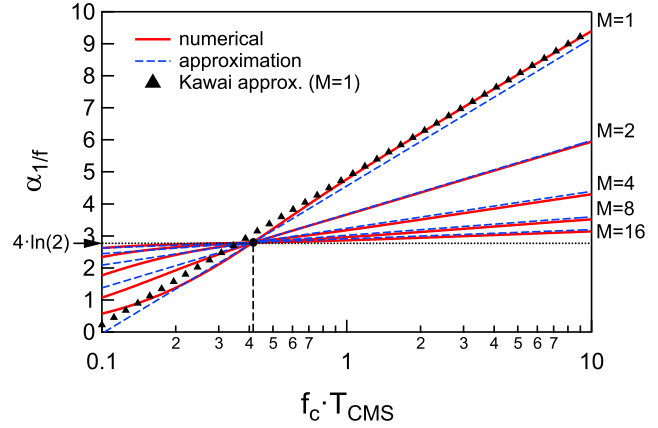
where the parameter K_F is expressed in [32] as

$$K_F = K_G k T q^2 \lambda N_t. \quad (4)$$

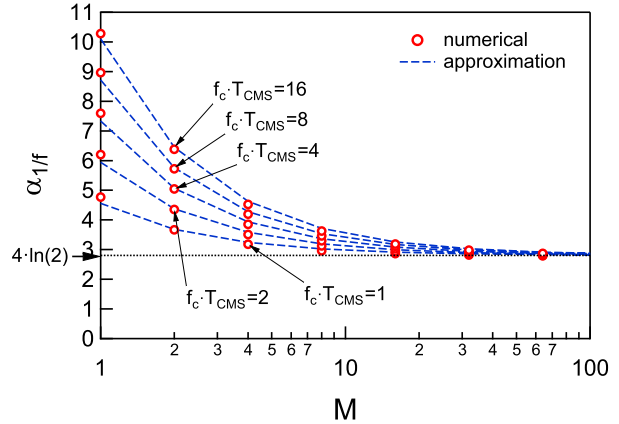
In (4), K_G is a bias-dependent parameter close to unity when the transistor is operating in the weak and moderate inversion [32], q the electron charge, λ is the tunneling attenuation distance (≈ 0.1 nm) [33] and N_t the oxide trap density. The reported input-referred flicker noise variance takes only into account the dominating flicker noise contribution generated by the in-pixel SF, whereas the flicker noise of the CLA featuring larger devices can be neglected thanks to the autozero process [26]. In (3), $\alpha_{1/f}$ is a unitless circuit design parameter that includes the effect of the CMS on the $1/f$ noise [12], [22], as shown in Appendix.

Based on Fig.3, the CMS has a high-pass characteristic since it introduces a zero in the transfer function which cancels the $1/f$ noise. However, the maximum of $|H_{CMS}(f)|^2$ decreases and at the same time moves to lower frequencies when increasing M .

In order to evaluate the impact of CMS on the $1/f$ noise, the parameter $\alpha_{1/f}$ defined in (17) in the Appendix is numerically calculated for different values of M . This parameter is plotted in Fig.5(a), as a function of $f_c T_{CMS}$ for M ranging from 1 to 16. Fig.5(a) shows that $\alpha_{1/f}$ increases logarithmically with $f_c T_{CMS}$ for each value of M . This means that the time between the samples should be kept at the minimum value that ensures the signal to settle ($f_c T_{CMS} = 1$). The logarithmic dependence is used in the approximation derived by [16] and [17] for CDS ($M = 1$) and given in (18) in the Appendix. The latter is plotted with triangle symbols in Fig.5(a) which match very well the numerical values for $f_c T_{CMS} > 1$. Unfortunately, no approximation of $\alpha_{1/f}$ exists today for $M > 1$. A new approximation is proposed in Appendix by (19) that accounts for the increase of $\alpha_{1/f}$ with the log of $f_c T_{CMS}$ with a slope



(a)



(b)

Fig. 5. (a) $\alpha_{1/f}$ as a function of $f_c \cdot T_{CMS}$ for different values of M . (b) The same parameter is plotted as a function of M to emphasize the plateau of the residual flicker noise reduction with M .

equal to $2/M$ and ultimately tending to $4 \ln(2) = 2.77$ for very large M (actually $M \rightarrow \infty$). This approximation is plotted in Fig.5(a) by the dashed lines which fit reasonably well the numerical results. The same parameter is plotted in Fig.5(b) versus M and for different values of $f_c T_{CMS}$, showing a good fit with the numerical values. This figure illustrates that the residual $1/f$ noise can be reduced by the CMS up to $M = 16$, above which the aforementioned plateau corresponding to $4 \ln(2) = 2.77$ is reached. This figure also shows that higher CMS orders make $\alpha_{1/f}$ less dependent on $f_c T_{CMS}$.

Based on the above expressions for the thermal and $1/f$ input-referred charge variances and before describing the implementation of the measured chip, the main techniques for noise reduction are summarized. Looking at expressions (2) and (3), it is possible to determine the design and the process parameters which can reduce the input-referred TRN. Regarding thermal noise, at column-level it is possible to implement a high gain amplifier with a minimum number of transistors and a precise bandwidth, together with a CDS or a CMS circuit. Moreover, if the SN capacitance, including C_p and the SF capacitors, is reduced then the pixel conversion gain, A_{CG} , increases. Once the thermal noise is minimized, the flicker noise originated from the SF becomes the dominant noise source in the readout circuit [30]. The transistors outside the

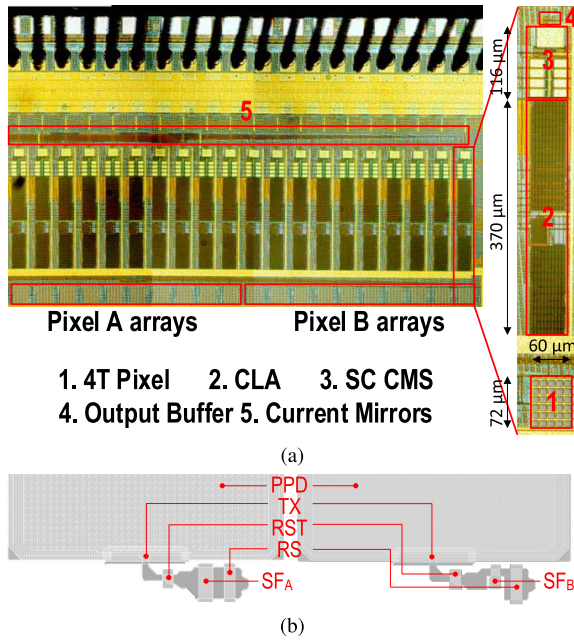


Fig. 6. (a) Chip micrograph showing the main blocks of the readout chains with biasing circuits and buffers. (b) Layout of the pixels A and B with the PPD and the TX, RST, RS and SF transistors. The two SFs differ in their gate sizes.

pixel are designed with a gate area large enough in order to exhibit low flicker noise. For the SF transistor, the optimized gate dimensions, together with the highest oxide capacitance per unit area, C_{ox} , and the lowest flicker noise parameter, K_F , are the solutions to minimize the noise. In [18], a minimum width and an optimal length are shown to give the minimal $1/f$ noise. In addition to these techniques, CMS is used to further reduce the thermal noise, by a factor of $1/M$, and the flicker noise up to $M = 16$ [18].

IV. AN ANALOG CIRCUIT IMPLEMENTATION COMBINING GAIN AND PASSIVE SC CMS CIRCUIT

This section presents the CIS readout chain designed in a $0.18\ \mu\text{m}$ CIS technology to explore the combined impact of the column-level gain, A_{col} , and the CMS order, M , on the input-referred TRN noise. In Fig. 6(a), a chip micrograph with a lateral zoom of a single readout chain is shown. The red rectangles in the figure are numbered to define the different implemented blocks, which consist in the two pixels, the CLA, the SC CMS, the output buffers and the current mirrors.

A. Pixel Design

The layout of the two pixels implemented in a $0.18\ \mu\text{m}$ CIS technology is shown in Fig. 6(b). The two pixels differ in the size and the type of the nMOS SF transistor: in Pixel A, the SF is a n-channel native transistor featuring an aspect ratio of $1.2\ \mu\text{m}/0.6\ \mu\text{m}$, while Pixel B features a standard nMOS SF with an aspect ratio of $0.22\ \mu\text{m}/0.35\ \mu\text{m}$. The bias current of each pixel is named I_{dSF} and it is set by an external current reference to $2\ \mu\text{A}$. Both pixels have about the same value of parasitic capacitance at the SN, C_p , which is estimated to $3\ \text{fF}$. The aspect ratio of Pixel B is more than three times smaller

than the one of Pixel A to assess the impact of the SF sizing on noise. As discussed in the previous section, the reduction of the W and the use of an optimal L for the SF transistor is one of the solution in order to achieve the lowest $1/f$ noise [18]. Based on this analysis, a better noise performance is expected from Pixel B. The compact layout for the two pixels results in a fill factor of 80% with a pixel pitch of $12\ \mu\text{m}$.

B. Column-Level Amplifier

The schematic and the timing diagram of the CIS readout chain are shown in Figs. 7(a) and 7(b). For the sake of simplicity, in the circuit schematic the two different pixels refer to the same readout chain, but in the actual implementation each pixel has a separate readout chain. As shown in Fig. 7(a), the CLA is implemented with an adjustable gain. The closed-loop gain of this amplifier is set by the ratio between C_f and C_{in} : a different value of C_f can be chosen thanks to the two selection switches in series with each capacitor from C_{f1} to C_{f6} . The programmable value of C_f allows to change A_{col} between 1 and 128.

The CLA is implemented as a single-ended transconductance gain stage and its schematic is shown in Fig. 7(a). Since there is enough voltage headroom, cascode transistors are used to maximize the DC gain without increasing the noise. The noise contribution of the current source M_4 is made negligible compared to that of the driver transistor M_1 by choosing $G_{m1} > G_{m4}$. The flicker noise contribution of the CLA is strongly reduced thanks to the autozero [26]. Additionally, the transistor area of the CLA are made much larger than the in-pixel SF. This is a reasonable choice due to the relaxed constraint on the area at column-level compared to the tight area constraints set for the pixel. When the high closed-loop gains are used, the charge injection coming from the AZ transistor becomes critical, because it can dramatically decrease the dynamic range of the amplifier. This phenomena is compensated by the use of properly sized dummy transistors in series with the switches [26], as shown in Fig. 7(a).

C. Passive Switched Capacitor CMS Circuit

The parallel connection of two identical capacitors leads to a process of charge sharing that average their initial voltages. If M consecutive samples with a T_{CMS} sampling period are stored on M different capacitors, connecting them all together at the instant MT_{CMS} , results in averaging the M samples. If the average is calculated progressively and the intermediate results are stored in capacitors that can be reused, a minimum number of capacitors is required. Based on [22], $n + 1$ capacitors are needed for averaging 2^n samples.

Fig. 7(a) shows the implemented CMS circuit. The latter is composed by an averaging and a subtractor block. The averaging block consists of five equal capacitors for averaging 8 samples of the reset and signal levels, before and after the charge transfer, and to store the two averages on capacitors C_4 and C_5 , respectively. The maximum CMS order of 8 is chosen according to the theoretical limit of the $1/f$ noise reduction, discussed in the previous Section. The second block based on SF buffers and a bootstrap capacitor, C_6 , is used

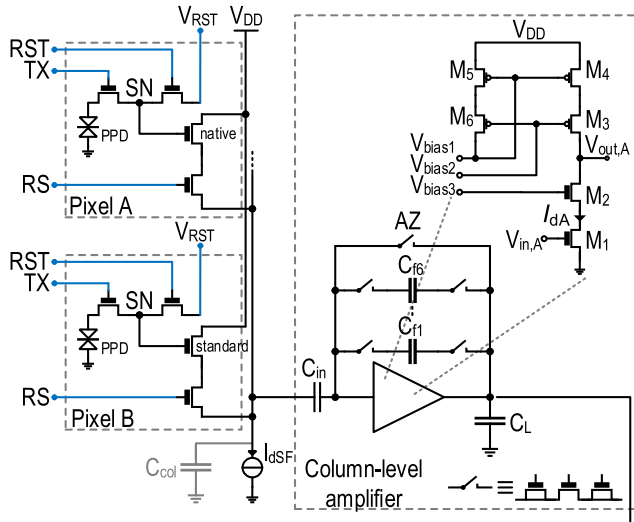


Fig. 7. (a) Schematic of the implemented CIS readout chain with a 4T pixel, the capacitive amplifier and SC CMS. (b) Timing diagram of the readout chain with all the control signals for the SC CMS for M equal to 8.

to subtract the two averages and to obtain the final output value. The circuit is explained below with the help of the timing diagram of Fig. 7(b), which assumes $M = 8$. Initially, switches S_1 , S_2 and S_3 are closed. A first sample, V_1 , is then stored in C_4 as S_3 opens. After a time T_{CMS} from the last event, S_1 is also opened to store the next sample, V_2 , in C_1 . After the two samples are taken, S_2 and S_3 are closed while

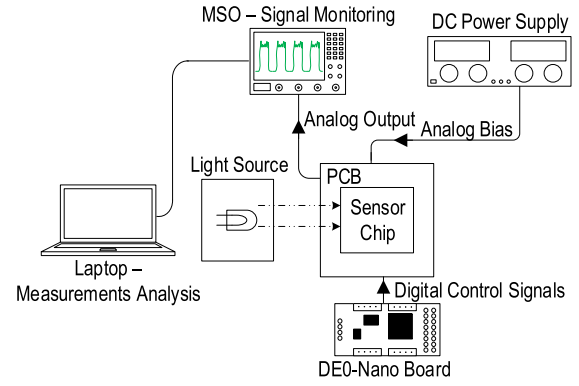


Fig. 8. Setup for the characterization and the noise measurements of the readout chains implemented on the chip.

S_1 is opened and the first two samples are averaged. This average is held on C_4 . The same operations are repeated between capacitors C_1 and C_2 , as shown in Fig. 7(b). After that, the average between four samples is stored on C_4 by closing S_3 and S_5 . Other two iterations on C_3 and on C_2 allow to store the average of eight samples on C_4 . During the averaging of the signal level, the leakage charges from C_4 to C_5 are a possible issue. Hence, it is critical the design of the complementary switches with dummy transistors in series used in the SC CMS and shown in Fig. 7(a). Compared to more traditional CMS implementations, the proposed CMS circuit requires a minimum number of capacitors and does not need any additional active circuits. A T_{CMS} equal to $1 \mu s$ is chosen in order to ensure the settling of the output after charge transfer, the values of 400 fF and 1 pF are used for the averaging capacitors and the bootstrap capacitor, respectively. As explained below in Section V-A, the logic circuit to control the switches is implemented externally with an FPGA. Since these signals are common to all the implemented readout columns, the required additional area overhead of this circuit can be considered negligible in an on-chip implementation.

V. MEASUREMENTS RESULTS

In order to evaluate the noise, first the CG for each value of A_{col} has to be measured. The readout noise is in fact measured at the output of the chain for the various gain values and CMS orders and then referred to the input by using CG . When all measurements are plotted, it is possible to derive the trends of noise reduction and compare with the theoretical model presented above. In this section, the measurement setup is first introduced, the conversion gain measurements are then presented and the input-referred noise is finally discussed.

A. Experimental Setup

The measurement setup is shown in Fig. 8. The sensor chip is packaged and mounted on a PCB, where all connectors and power supply filters for low noise requirements are placed. All the control signals for the readout and the SC CMS are generated by the Cyclone-V FPGA of the DE0-Nano Board [34]. The analog voltage and current references are generated externally, as well as the 3.3 V voltage supply. The output of each

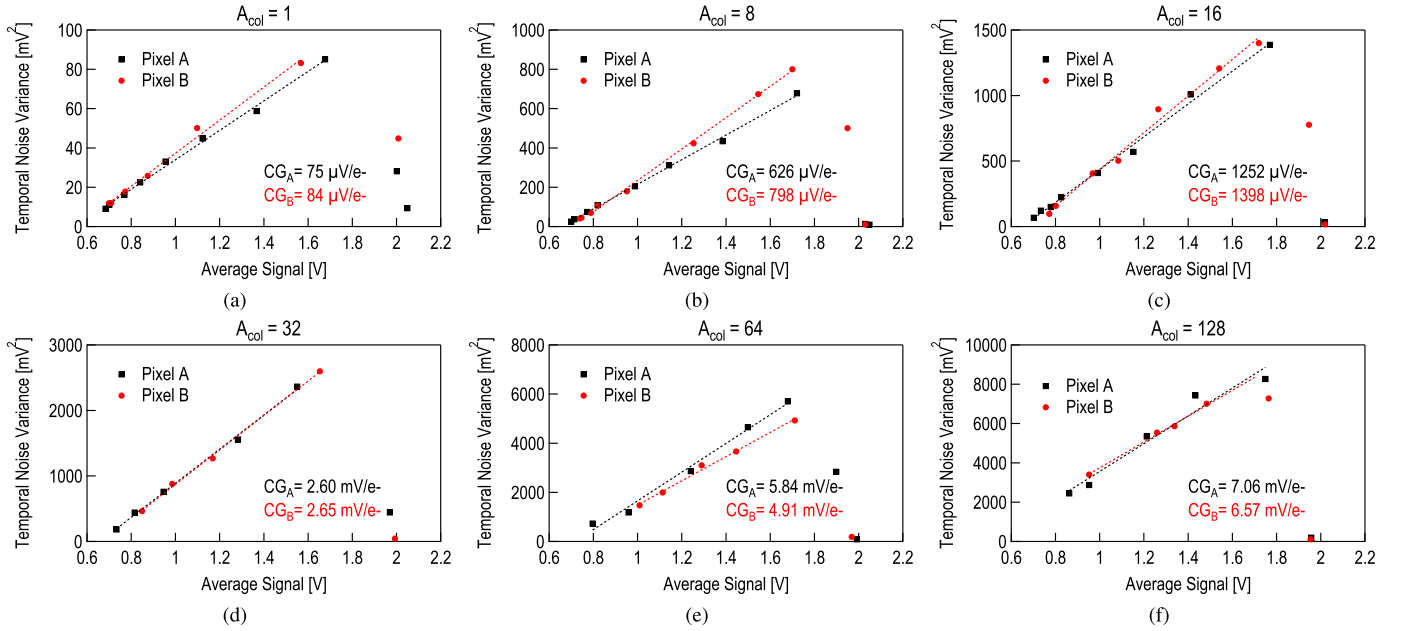


Fig. 9. PTCs of the readout chain for different values of the CLA gain (from 1 to 128), in order from (a) to (f). The overall CG is reported in each figure for both pixels.

readout chain is selected directly on the PCB. The output signal is monitored on the MSO-S 804A oscilloscope and the data acquisition is performed with a Visual Basic script executed on a laptop. The input of the oscilloscope has an integrated 10 bit ADC. The PTC measurements require a variable input light, which is implemented with a voltage tunable LED source fixed on the top of the sensor. The data require a step of averaging performed during the data processing in the Matlab® environment. This reduces the impact of the quantization noise of the scope ADC.

B. Conversion Gain Measurement

The PTC is the technique used to obtain the value of the readout conversion gain, CG [28]. When the sensor is limited by the PSN, the variance of the output is proportional to the average output value and the coefficient of proportionality corresponds to CG . Hence, the latter has been extracted from the output noise variance versus input signal strength for values of the CLA gain ranging from 1 to 128 by estimating the slope of the linear part of the PTC before saturation, as shown in Fig. 9.

During the performed measurements, the sensor is exposed to a uniform input light and a voltage source allows to increase the illumination level. The obtained CG values for each A_{col} gain value are reported inside the corresponding figure, while the dashed lines are the linear approximation of the measured values, which are reported with markers. When the CLA gain is equal to one, the readout conversion gain, CG , corresponds to the pixel conversion gain, A_{CG} , used in (2). The measured pixel conversion gain for Pixel A is $75\mu\text{V}/e^-$ and $84\mu\text{V}/e^-$ for Pixel B, which is due to the different SF designs. This small difference in the pixel conversion gain means that the total SN capacitance is dominated by C_p in this particular

design and that the contributions of the in-pixel SF to the SN capacitance slightly influence the value of A_{CG} .

At about 1.8 V, almost all the curves in Fig. 9 deviate from the linear behavior, because the readout chain reaches the saturation at the level of the amplifier. This shows that the dynamic range in all configurations is limited by the readout chain and not by the full-well capacity of the PPD. For $A_{col} = 1$, the fact that the PTC collapses around 1.8 V, allows to estimate the readout handling capacity, which results in $45\,000e^-$. This value is suitable for applications requiring high dynamic range (HDR) imaging.

C. Temporal Read Noise

The input-referred noise is calculated from the measured output noise voltage and the extracted CG . The output voltage samples are stored after performing 1000 readouts operations with a T_{CMS} of $1\mu\text{s}$. The TX is kept off during all the measurement procedure. The CLA gain is varied along six different values and the implemented CMS orders are 1, 2, 4 and 8. At the column-level gain of 32, the amplifier limits the bandwidth to about 250 kHz. As mentioned in Section III-B, this bandwidth limitation is key for limiting the thermal noise contribution. Figs. 10(a) and 10(b) show the impact of the CLA gain on the total noise. Unlike simulation results shown in [35], the noise contributions originating from different noise mechanisms (thermal, flicker and shot) can not be completely separated. For unity CLA gain value, the noise contributions of the stages following the amplifier e.g. kT/C noise of the CMS network, voltage buffers, ADC, is not reduced and adds to the noise of the SF and the CLA. This explains the noise level jump between the noise measured with $A_{col} = 1$ and $A_{col} = 8$. Based on (2) and unlike $1/f$ noise, the thermal noise is expected to decrease following a $1/\sqrt{A_{col}}$ law. In log scale,

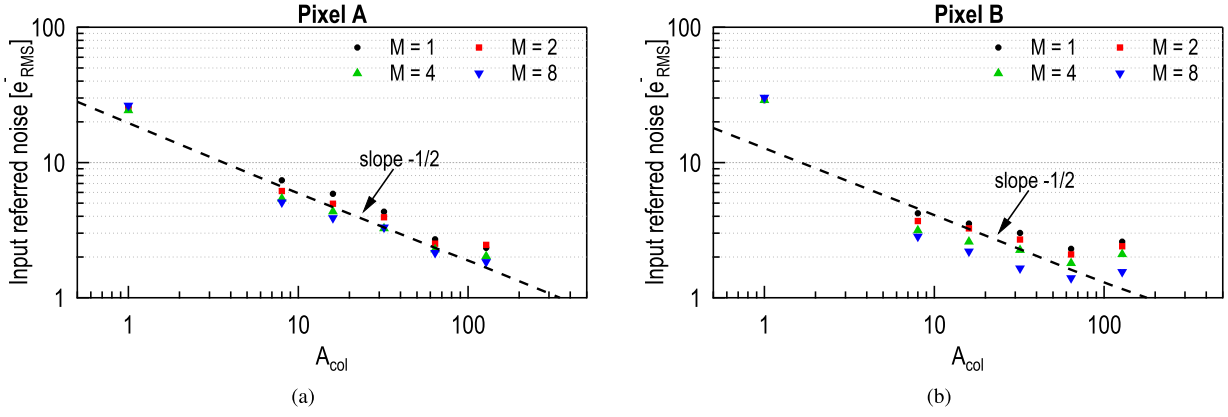


Fig. 10. Input-referred noise for both pixels as a function of the CLA gain value. The expected trend for thermal noise reduction is plotted with a dashed line.

this translates into a linear trend with $-1/2$ slope. This trend is plotted with a dashed line in Figs. 10(a) and 10(b). A similar behavior is observed in Pixel A for A_{col} between 8 and 64 and in pixel B between 8 and 32. This allows to define the thermal noise as the dominating noise mechanism for these gain values. For higher gain values, the thermal noise is reduced to a value close or below the $1/f$ noise. According to (3), the $1/f$ noise does not scale as $1/A_{col}$, since it accounts for the $1/f$ noise of the SF only, which is injected before the CLA. This explains the limitation of the noise reduction for A_{col} above 32.

The same measurements are plotted for both pixels as a function of the CMS order and for different values of A_{col} in Figs. 11(a) and 11(b). In these figures, the measurement results are compared with the following proposed expression for the total noise

$$\overline{Q_{n,tot}} = \sqrt{\frac{\sigma_{th}^2}{M A_{col} C} + \alpha_{1/f} \sigma_{1/f}^2 + \sigma_{floor}^2}, \quad (5)$$

which is based on (2) and (3). In the proposed formula, the thermal and the flicker noise parameters, σ_{th}^2 and $\sigma_{1/f}^2$, are introduced, as well as the noise floor, σ_{floor}^2 . σ_{th}^2 and $\sigma_{1/f}^2$ depend only on process and design parameters and, by using (2) and (3), they can be expressed as

$$\sigma_{th}^2 = 2kT \left[\frac{\gamma_{SF} G_{mA} \left(\frac{2}{3} C_{ox} WL + 2 C_{ex} W + C_p \right)^2}{G_{mSF}} + \frac{\gamma_A}{A_{CG}^2} \right] \quad (6)$$

and

$$\sigma_{1/f}^2 = \frac{K_F \left(C_p + 2 C_{ex} W + \frac{2}{3} C_{ox} WL \right)^2}{C_{ox}^2 WL}. \quad (7)$$

The noise floor is introduced to model all noise sources which are not included in (2) and (3) but still need to be accounted for. The latter is mainly corresponding to the noise introduced after the CMS subtractor of Fig. 7(a), which includes the noise of the measurement electronics.

To reach a matching between the measurements and the model results, σ_{th}^2 , $\sigma_{1/f}^2$ and σ_{floor}^2 are used as fitting parameters. The estimated values of the process and design parameters

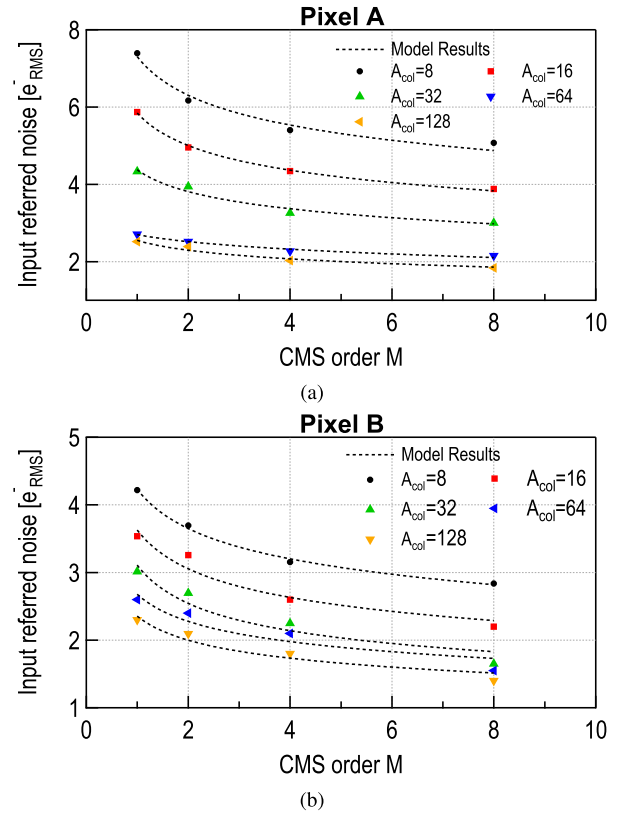


Fig. 11. Input-referred total noise for Pixel A (a) and Pixel B (b) as a function of the CMS order M. The measurements are compared with the total noise expression proposed in (5).

used to match with the measurement results as well as the expected values for σ_{th} and $\sigma_{1/f}$ are reported in Table I. An excellent match between the measured noise and the one calculated using (5) is obtained for the values of σ_{th} , $\sigma_{1/f}$ and σ_{floor} shown in Fig. 12 for each value of A_{col} . In the same figure, σ_{th} and $\sigma_{1/f}$ are compared with the expected values from the model, which are plotted with dashed lines, and a good matching is obtained. This validates the theoretical results on the impact of the gain and the CMS on the noise as well as the use of the process and the design parameters involved in (2) and (3). As expected from (6) and (7), the values of σ_{th} and $\sigma_{1/f}$ obtained from the numerical fitting

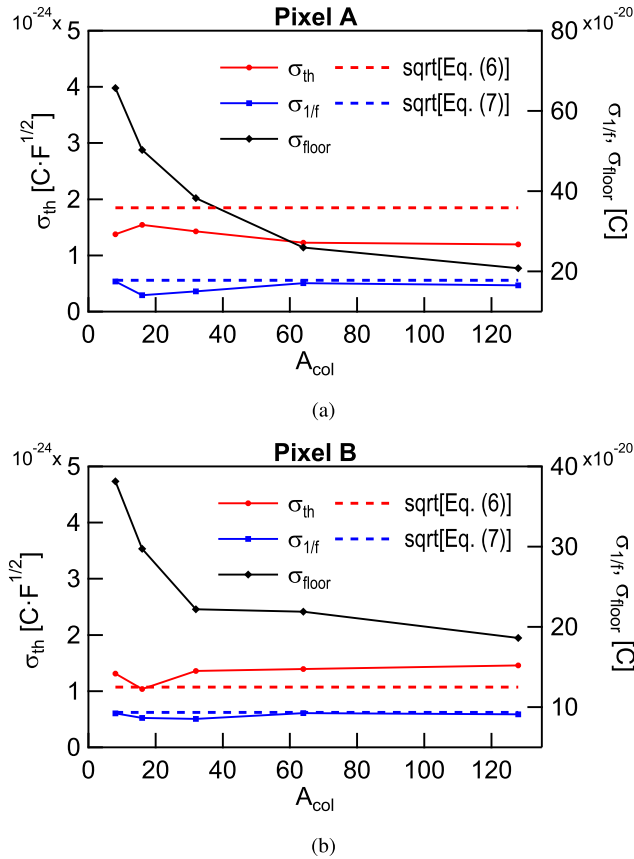


Fig. 12. The square root of the fitting parameters σ_{th}^2 (on the left axis), $\sigma_{1/f}^2$ and σ_{floor}^2 (on the right axis) is plotted for each value of the column-level gain for Pixel A (a) and Pixel B (b).

TABLE I
VALUES OF THE PROCESS AND DESIGN PARAMETERS

| | Pixel A | Pixel B |
|---|-----------------------|-----------------------|
| C_{ox} [fF μm^{-2}] | 4.5 | 4.5 |
| C_{in} [pF] | 1 | 1 |
| C_L [fF] | 400 | 400 |
| γ_{SF} [-] | 5 | 5 |
| γ_A [-] | 5 | 5 |
| W [μm] | 1.2 | 0.22 |
| L [μm] | 0.6 | 0.35 |
| I_{dSF} [μA] | 2 | 2 |
| I_{dA} [μA] | 10 | 10 |
| C_{ex} [fF μm^{-1}] | 0.45 | 0.45 |
| C_p [fF] | 1.6 | 1.6 |
| T_{CMS} [μs] | 1 | 1 |
| $C_{1...5}$ [fF] | 400 | 400 |
| C_6 [pF] | 1 | 1 |
| N_t [$\text{eV}^{-1} \text{cm}^{-3}$] | $3 \cdot 10^{17}$ | $5 \cdot 10^{16}$ |
| σ_{th} [$\text{C}\cdot\text{F}^{1/2}$] | $1.85 \cdot 10^{-24}$ | $1.07 \cdot 10^{-24}$ |
| $\sigma_{1/f}$ [C] | $1.78 \cdot 10^{-19}$ | $9.35 \cdot 10^{-20}$ |

are slightly influenced by A_{col} . The value of σ_{floor}^2 is indeed reduced under the effect of a higher gain, in agreement with the statement in Section III-B.

VI. CONCLUSION

In this paper a review of the main noise contributors to a CIS readout chain is first presented, showing that the TRN plays a key role at low light conditions. A conventional CLA and a passive SC CMS circuit are investigated for the total readout noise reduction. CIS readout chains exploiting two different pixel types and the combination of these analog techniques are implemented in a $0.18 \mu\text{m}$ CIS technology. The two pixel types are used to confirm the noise results for two different in-pixel SF. Measurement results confirm that column-level amplification plays the key role of mitigating the noise contribution of the next stages and reduces thermal noise following a $1/\sqrt{A_{col}}$ trend. CMS reduces thermal noise in the same way, but can not replace column level amplification in the reduction of the noise originating from the next stages. On the other hand, when combined the two techniques play complementary roles. With a moderate column-level gain, the CMS reduces both the thermal and the residual $1/f$ noise without an impact on the dynamic range and the readout time.

APPENDIX

The impact of CMS on thermal and $1/f$ noise variances has first been investigated as early as 1982 by Kansy in [15] for CDS ($M = 1$). The same year, Hopkinson and Lumb [16] studied noise reduction techniques in CCD, extending the work of Kansy to various implementations and to $M > 1$. In 2005, Kawai and Kawahito [17] derived the PSD of the noise at the output of a digital CMS. A detailed analysis of the analog CMS has been derived by Boukhayma [29] and Enz and Boukhayma [36] giving the PSD of the analog CMS output noise as

$$S_{n,CMS}(f) = \sum_{n=-\infty}^{+\infty} |H_n(f)|^2 \cdot S_n \left(f - \frac{n}{2MT_{CMS}} \right), \quad (8)$$

where $|H_n(f)|^2$ is given by

$$|H_n(f)|^2 = \text{sinc}^2(\pi f \cdot 2MT_{CMS}) \cdot \left| H_{CMS} \left(f - \frac{n}{2MT_{CMS}} \right) \right|^2. \quad (9)$$

and $\text{sinc}(x) = \sin(x)/x$ accounts for the hold of each sample over a full period $2M \cdot T_{CMS}$. The square magnitude of the CMS transfer function $|H_{CMS}(f)|^2$ in (9) is given by

$$|H_{CMS}(f)|^2 = \left(\frac{2}{M} \right)^2 \cdot \frac{\sin^4(\pi f \cdot M \cdot T_{CMS})}{\sin^2(\pi f \cdot T_{CMS})}, \quad (10)$$

which is plotted in Fig.3 versus the normalized frequency $f \cdot T_{CMS}$ for different values of M ranging from 1 to 8.

The variance of the CMS output voltage is obtained by integrating the PSD given by (8) over frequency. Thanks to power conservation in the CMS circuit, it is shown in [29] that this integral is actually equal to the integral of the signal before sampling, resulting in

$$\int_{-\infty}^{+\infty} S_{n,CMS}(f) = \int_{-\infty}^{+\infty} |H_{CMS}(f)|^2 \cdot S_n(f) df. \quad (11)$$

This means that the CMS output variance only depends on the square magnitude of the CMS transfer function (9) and the

input noise PSD $S_n(f)$. For a white noise input PSD, the CMS output variance is therefore proportional to the area below the curves shown in Fig. 3.

The impact of the CMS process on a low-pass filtered white noise with a bandwidth f_c and given by

$$S_n(f) = S_{n,\text{th}}(f) = \frac{S_0}{1 + \left(\frac{f}{f_c}\right)^2}, \quad (12)$$

can be evaluated with the help of the parameter α_{th} defined as the CMS output noise variance $V_{n,\text{CMS,th}}^2$ due to this white noise, normalized to the total white noise power at the input $\pi f_c \cdot S_0$

$$\alpha_{\text{th}} \triangleq \frac{V_{n,\text{CMS,th}}^2}{\pi f_c \cdot S_0} = \frac{2}{\pi f_c} \int_0^\infty \frac{|H_{\text{CMS}}(f)|^2}{1 + \left(\frac{f}{f_c}\right)^2} df. \quad (13)$$

Eq. (13) can be integrated analytically for $M = 1$, resulting in

$$\alpha_{\text{th}}|_{M=1} = 2e^{-\pi f_c \cdot T_{\text{CMS}}} \cdot \sinh(\pi f_c \cdot T_{\text{CMS}}) \quad (14)$$

and for $M = 2$, leading to

$$\alpha_{\text{th}}|_{M=2} = \frac{1}{2} e^{-6\pi f_c \cdot T_{\text{CMS}}} \cdot \left[e^{4\pi f_c \cdot T_{\text{CMS}}} \cdot (1 + 4 \sinh(2\pi f_c \cdot T_{\text{CMS}})) - 1 \right]. \quad (15)$$

Unfortunately, no simple closed-form expressions can be obtained for $M \geq 3$ and (13) needs to be computed numerically which shows that α_{th} is actually proportional to $2/M$. Indeed, the factor 2 comes from the subtraction of two uncorrelated averages and the factor $1/M$ is due to the noise averaging in each half period of the CMS process. This property is illustrated in Fig. 4 which shows the product $\alpha_{\text{th}} \cdot M/2$ versus $f_c \cdot T_{\text{CMS}}$ for different values of M ranging from 1 to 16. As expected, $\alpha_{\text{th}} \cdot M/2$ tends to unity for $f_c \cdot T_{\text{CMS}} > 1/2$ and for all values of M .

Similarly, the impact of CMS on a low-pass filtered $1/f$ noise having a PSD given by

$$S_{n,1/f} = \frac{K_f}{|f|} \cdot \frac{1}{1 + \left(\frac{f}{f_c}\right)^2}, \quad (16)$$

can be evaluated from the parameter $\alpha_{1/f}$ defined as

$$\alpha_{1/f} \triangleq \frac{V_{n,\text{CMS},1/f}^2}{K_f} = \int_0^\infty \frac{1}{f} \cdot \frac{|H_{\text{CMS}}(f)|^2}{1 + \left(\frac{f}{f_c}\right)^2} \cdot df, \quad (17)$$

where $V_{n,\text{CMS},1/f}^2$ is the CMS output variance due to the low-pass filtered $1/f$ input noise. There is unfortunately no simple closed-form expression for the integral given by (17). The latter has been computed numerically and is plotted in Fig. 5(a) versus $f_c \cdot T_{\text{CMS}}$ for different values of M ranging from 1 to 16. Choosing a log scale for the x-axis in Fig. 5(a) shows that $\alpha_{1/f}$ actually scales linearly with $\ln(2\pi f_c \cdot T_{\text{CMS}})$ for $f_c \cdot T_{\text{CMS}} > 4.15$ and that the slope is inversely proportional to M . A simple approximation of (17) in the case of CDS ($M = 1$) was proposed in [16] and [17] as

$$\alpha_{1/f} \cong 2\gamma + 2 \ln(2\pi f_c \cdot T_{\text{CDS}}), \quad (18)$$

where $\gamma \cong 0.577$ is the Euler constant and T_{CDS} the time between the two CDS samples. The CDS approximation given by (18) is plotted in Fig. 5(a) with the triangle symbol which shows a good match for $f_c \cdot T_{\text{CDS}} > 1$. Unfortunately, today no simple approximation of (17) has been derived for $M > 1$. As already observed in [16] and [17], for very large values of M (actually $M \rightarrow \infty$), $\alpha_{1/f}$ saturates to $4 \ln(2) \cong 2.77$, which corresponds to the dotted horizontal line in Fig. 5(a). Having a closer look at Fig. 5(a), we see that all the curves computed numerically for $M = 1, 2, 4, 8, 16$ cross roughly at a point given by $f_c \cdot T_{\text{CMS}} \cong 4.15$ and $\alpha_{1/f} = 4 \ln(2) \cong 2.77$. A simple approximation can then be derived from this observation and from the fact that the lines in the lin-log plot scale as $2/M$. This results in the newly proposed approximation given by

$$\alpha_{1/f} \cong 4 \ln(2) + \frac{2}{M} \cdot \ln\left(\frac{f_c \cdot T_{\text{CMS}}}{0.415}\right), \quad (19)$$

which fits the numerical values reasonably well for M ranging from 1 to 16 as shown by the dashed lines in Fig. 5(a). The interesting new feature of the approximation given by (19) is that it captures the scaling of the $1/f$ noise reduction with the CMS order M as illustrated in Fig. 5(b) for different values of $f_c \cdot T_{\text{CMS}}$. It also shows that no substantial $1/f$ noise reduction is achieved when choosing M larger than 16.

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