# A Novel Digital-Intensive Hybrid Polar-I/Q RF Transmitter Architecture

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***Abstract*— A novel digital-intensive hybrid transmitter (TX) architecture is presented, combining conventional inphase and quadrature (I/Q) with constrained phase modulation. The proposed architecture utilizes an RF-DAC with phase modulated RF clock and adjusted I/Q components. By incorporating phase modulation the quadrature component is kept small while the inphase component approaches the complex signal envelope. Compared to a digital-quadrature TX architecture this results in a significantly reduced average and peak RF-DAC cell utilization. Therefore, the RF-DAC can be operated in less back-off at higher average output power and drain efficiency. The phase modulation is constrained in order to relax the phase modulators system requirements. Compared to a digital polar TX architecture utilizing an RF digital phase-locked loop with two-point phase modulation, this results in reduced frequency modulation and digital-controlled oscillator tuning range requirements. In addition, the design effort is further shifted from analog to digital domain in order to better exploit the benefits of CMOS technology scaling.**

***Index Terms*— Wireless communication, digital polar transmitter, digital quadrature transmitter, hybrid polar-I/Q transmitter, phase modulation, quadrature modulation, RF digital-to-analog converter (RF-DAC), RF digital power amplifier (RF-DPA), RF digital phase-locked loop (RF-DPLL).**

## I. Introduction

WIRELESS transceivers for multi-band, multi-standard mobile handset applications operating in the sub-6 GHz range are usually implemented in ultra-deep submicron CMOS technology. To fully utilize the advantages of shrinking process structures, digital-intensive transmitter (TX) and receiver architectures have been developed [1], replacing analog functionality by digital circuits. Compared to analog implementations, these architectures show a

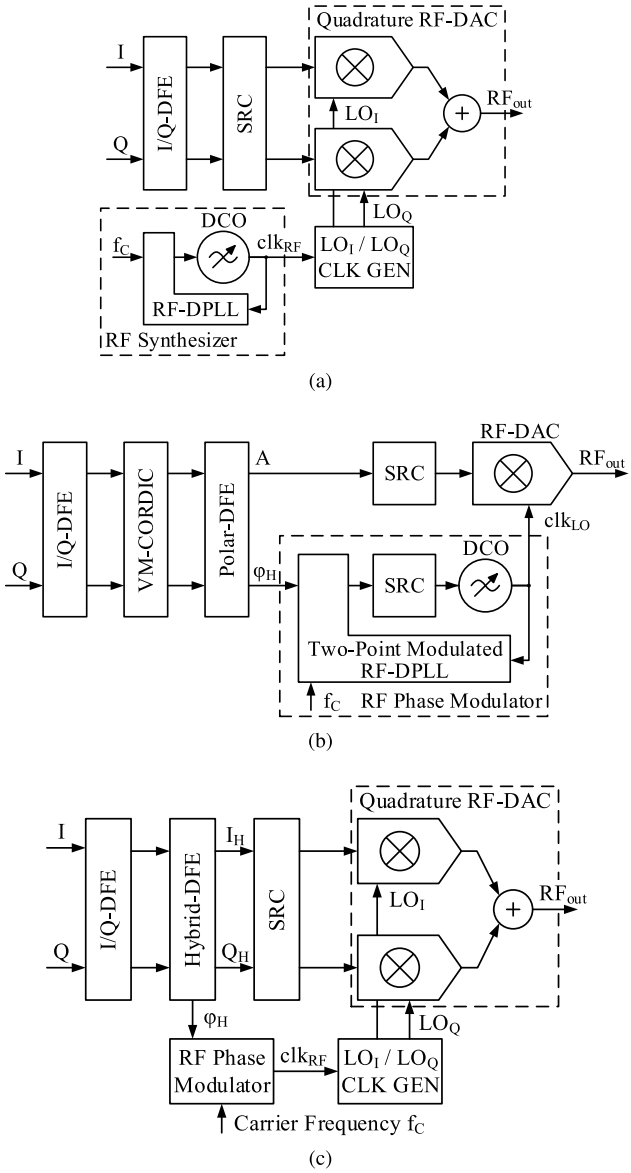


Fig. 1. Digital-intensive TX architectures. (a) Quadrature TX with dedicated I/Q RF-DACs. (b) Polar TX with RF-DPLL based phase modulator. (c) Proposed hybrid polar-I/Q TX combining constrained phase and adjusted I/Q modulation.

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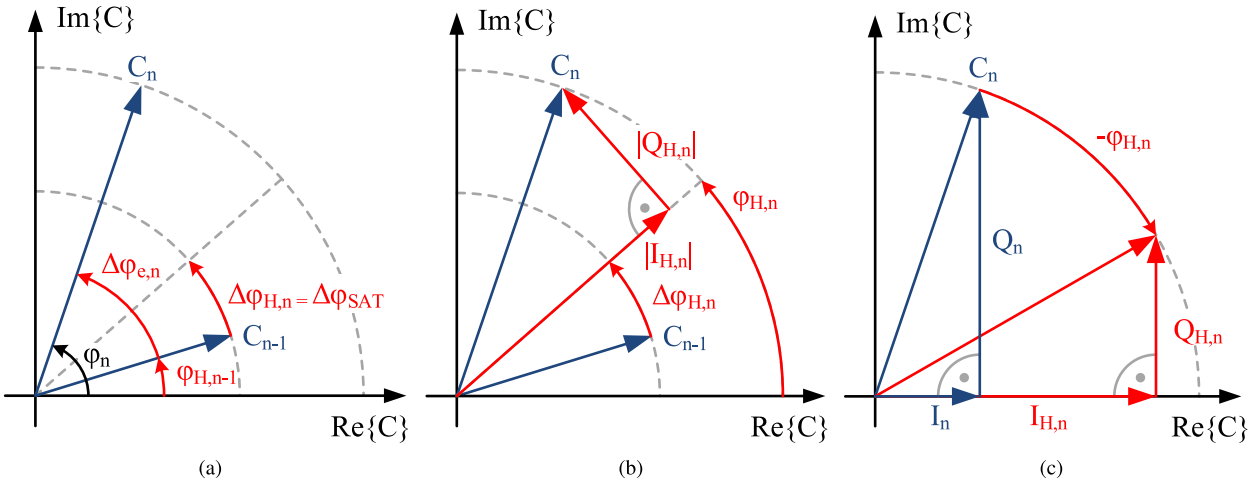


Fig. 2. Complex pointer diagrams illustrating the hybrid polar-I/Q modulation methodology in the event of phase saturation. (a) Saturation of desired phase change. (b) Transition from $C_{n-1}$ to $C_n$ by constrained phase change $\Delta\varphi_{\mathrm{H},n}$ and hybrid I/Q components $I_{\mathrm{H},n}$, $Q_{\mathrm{H},n}$. (c) Calculation of $I_{\mathrm{H},n}$ and $Q_{\mathrm{H},n}$ by rotational transformation.

reduced process, voltage and temperature dependency, better scalability and simplified system re-configuration.

With the development of RF digital-to-analog converters (RF-DACs) [2], [3] directly operating at the channel frequency, digital-intensive polar and quadrature TX architectures as shown in Fig. 1 have become of focus [4]–[6].

First, due to the utilization of high dynamic range RF-DACs, superior out-of-band spectral emission performance is achieved [7], [8]. This enables the use of low-complexity passive and active output matching networks [9], [10] based on integrated transformers avoiding the need for off-chip band-pass filters [11]. Second, by utilizing switched-capacitor circuits, power efficiency, linearity and scalability has further been improved compared to first current-steering based implementations [12]. In a further step, combining the RF-DAC and power amplifier (PA) functionality on a single die, fully integrated RF digital PA (RF-DPA) implementations, capable of delivering high output powers, have been shown [12]–[17].

In recent publications, direct digital-quadrature TX based on 50% as well as 25% duty-cycle RF-DPA implementations supporting different wireless standards and modulation schemes have been shown. In [18], a 50% duty-cycle implementation based on a current-steering Class-D RF-DPA is presented. The implementation utilizes a combination of unitary-weighted and binary-weighted power cells as well as sign switching based on local oscillator (LO) clock polarity inversion. Measurements of the implemented TX are shown, supporting orthogonal frequency-division multiplexing for wireless LAN with up to 80 MHz supported channel bandwidth. A 25% duty-cycle implementation interleaving the conduction time of both RF-DAC outputs within one RF clock cycle is shown in [8]. By this approach, certain effects like nonlinearity and therefore signal distortion arising with insufficient isolation between inphase and quadrature (I/Q) RF-DAC outputs are reduced. However, higher effort has to be spent for generating and gating the 25% duty-cycle LOs. In addition, the RF-DAC cells are operating on twice the channel frequency which results in reduced drain efficiency and limits the applicability with respect to higher channel frequencies. Recently, a digital-intensive multi-band, multi-standard polar TX implemented in 28-nm CMOS utilizing switched capacitor, signed magnitude RF-DACs [19] with external PAs and two-point phase modulated RF digital phase-locked loop (DPLL) [20] has been shown. The polar TX supports 40 MHz contiguous intra-band carrier aggregation in LTE uplink while also covering 2G and 3G cellular standards with FDD and TDD bands ranging from 700 MHz up to 3.8 GHz.

By comparing digital-intensive polar and quadrature TX it turns out that both architectures show opposed characteristics. In terms of average output power and efficiency, the digital quadrature TX illustrated in Fig. 1(a) shows an inherent drawback compared to the digital polar TX shown in Fig. 1(b). Since the envelope $A_n$ of the complex modulation signal $C_n = I_n + jQ_n$ is given by the orthogonal summing

$$A_n = |C_n| = \sqrt{I_n^2 + Q_n^2}, \tag{1}$$

the RF-DAC size, achievable output power and drain efficiency are affected. The number of active RF-DAC cells can be given by the sum of $|I_n| + |Q_n|$. In order to achieve the same output power being directly proportional to $A_n^2$, the digital quadrature TX requires more RF-DAC cells compared to the polar TX. As consequence, the RF-DAC has to operate in a higher back-off region which results in a lower drain efficiency and average output power.

A 50% duty-cycle digital quadrature TX implementation with RF-DPA based on shared, unitary-weighted and dedicated, binary-weighted power cells is shown in [21]. The cell sharing between the I/Q components represents one way to improve the power efficiency. Here, the total number of cells and therefore RF-DAC size can be reduced for the same achievable output power compared to implementations with dedicated I/Q cells. However, increased signal distortion is likely to result from the diamond-profile signal clipping which

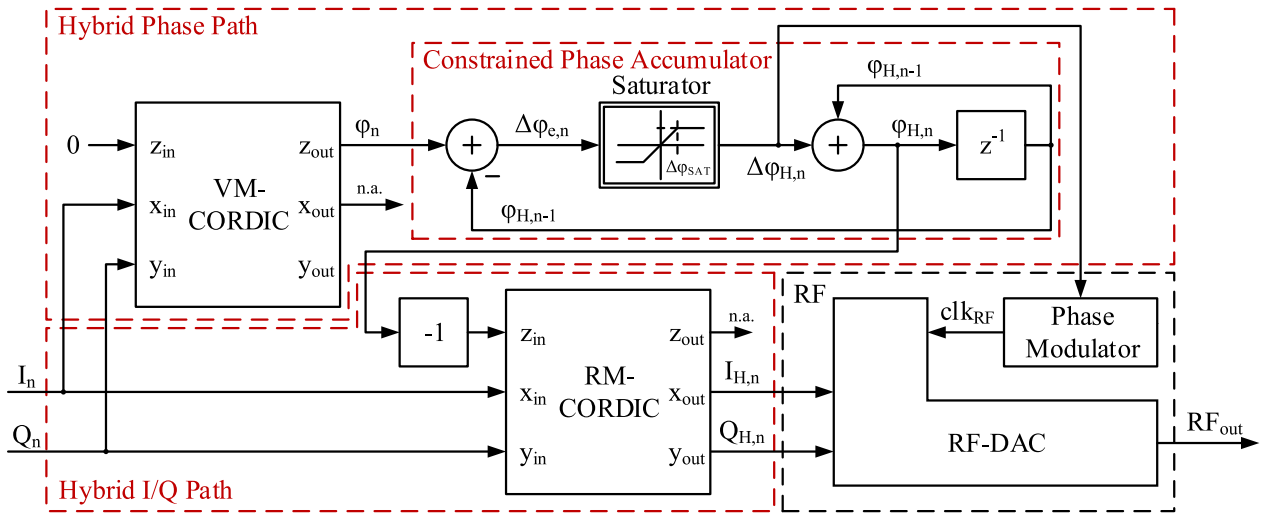


Fig. 3. Hybrid-DFE implementation with phase path signal processing (top) and rotational transformation of I/Q components (bottom).

is necessary to avoid simultaneous allocation of cells by the I/Q components. Another cell sharing approach based on time-divison multiplexing is shown in [22], avoiding the diamond-profile clipping of [21] at the drawback of a more complex clocking concept and lower drain efficiency.

The digital polar TX, on the other hand, requires significantly more effort in digital signal processing and suffers from bandwidth expansion due to the nonlinear transformation of the complex modulation signal from Cartesian to polar coordinates. This results for example in sampling rate conversion (SRC) errors when operating in the polar signal domain and therefore in increased signal distortion [23]. Another problem is given by the digital phase modulation of the LO itself which results in spectral replicas mixing back to the carrier frequency by the harmonics of the rectangular clock signal [24]. Those effects increase with signal bandwidth and are especially critical for non-constant envelope modulation schemes. To some extend, they can be compensated by a higher sampling rate of the Cartesian-to-polar conversion and the polar digital front-end (DFE) [25]. However, this results in an increased DFE power consumption and digital-controlled oscillator (DCO) tuning range further complicating the RF-DPLL phase modulator design. The increased DCO tuning range requirement is a consequence of the frequency modulation signal $f_{\mathrm{MOD},n}$ scaling with the sampling rate $F_\mathrm{s}$ for the Cartesian-to-polar conversion [26], given by

$$f_{\mathrm{MOD},n} = \frac{1}{2\pi}\frac{d\varphi}{dt} \approx \frac{F_\mathrm{s}}{2\pi}\underbrace{(\varphi_n - \varphi_{n-1})}_{\Delta\varphi_n} \tag{2}$$

with the integer-valued index $n$ representing the time-discrete sample instances. This results in a tuning range requirement of $\pm F_\mathrm{s}/2$ since large phase jumps of up to $\pm\pi$ between adjacent samples can originate whenever the complex trajectory passes close to the origin of the complex plane. Therefore, a trade-off between reduced in-band as well as out-of-band signal distortion and increased DCO tuning range requirement results. Moreover, the handling of second-order effects like DCO nonlinearity and delay matching in the phase modulator and between phase and amplitude modulation paths becomes more challenging [27]. In [26], the concept of hole punching the complex baseband signal as first presented in [28] is adopted. Here, the objective is to limit instantaneous phase changes and therefore the maximum excitation of the $f_{\mathrm{MOD},n}$ signal in case of trajectory crossings close to the origin. While this is necessary to reduce DCO tuning range requirements, higher in-band and out-of-band signal distortion arises [29] which results in a similar trade-off as described before. As consequence, the applicability of the RF-DPLL phase modulator in terms of wide-band modulation is limited [30].

A multiphase TX concept is presented in [31], improving the RF-DPA drain efficiency by a polar-like segmentation of the constellation diagram. Here, a complex sample is represented by two vectors with adjacent LO phases smaller than $\pi/2$, abandoning the orthogonal property but therefore reducing the associated drop in average output power and drain efficiency. The approach requires to place the digital signal processing for generating the multiphase data and performing digital pre-distortion close to RF rate prior to the RF-DPA. This represents a major disadvantage since all the required multiphase signal processing logic has to operate on the sampling rate defined by the last SRC stage. To meet out-of-band spectral emission requirements very high sampling rates can be required in order to shift spectral replicas originating from the zero-order-hold operation of the RF-DPA to higher carrier offset frequencies. This becomes especially important in combination with wide-band, low-order matching networks integrated on-chip since they usually show a significantly lower stop-band attenuation compared to external filters. Also, the LO generation and data synchronization becomes more complicated due to the larger number of required LO phases. Therefore, a trade-off between RF-DPA efficiency and power consumption of the additional digital signal processing on RF rate results.

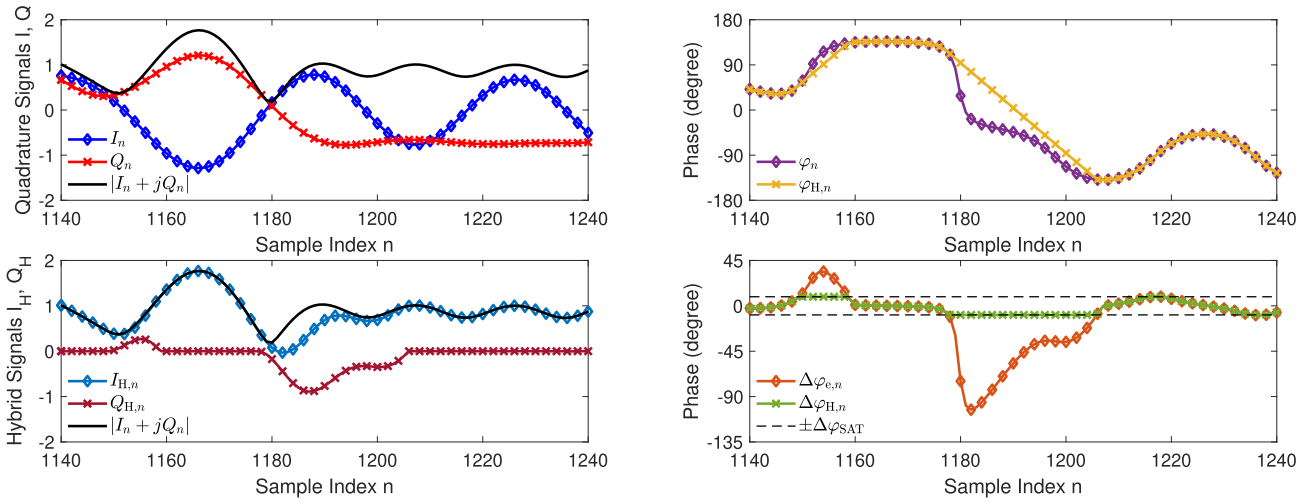


Fig. 4. Hybrid-DFE simulation results for LTE uplink, with 20 MHz channel bandwidth, 16-QAM symbol mapping and full RB allocation at $F_S = 307.2$ MHz and $\Delta\varphi_{SAT} = 9°$. (a) Hybrid-DFE input signals (top) and hybrid I/Q path output signals (bottom). (b) Hybrid phase path signals with the VM-CORDIC output and absolute constrained phase (top) as well as the desired and constrained phase change (bottom).

In this paper, a hybrid TX architecture as shown in Fig. 1(c) combining inphase, quadrature and constrained phase modulation is proposed. The approach inherits the superior RF-DAC drain efficiency and average output power of the digital polar TX. By constraining the phase modulation while adjusting the I/Q components accordingly, tuning range requirements of the RF-DPLL based phase modulator can be relaxed significantly. The methodology is further explained in Section II while the mapping to a DFE implementation is discussed in Section III. A brief description of the hybrid-DFE in context of a digital-intensive TX architecture based on RF-DPLL two-point phase modulator and shared-cell RF-DAC is given in Section IV. Simulation results of the proposed hybrid TX architecture for single carrier - frequency division multiple access, as utilized channel access and modulation scheme in LTE uplink, are presented throughout the paper. Results characterizing the overall TX performance and impact on RF-DAC drain efficiency and average output power are shown in Section V.

## II. Modulation Methodology

The approach of combining a constrained phase with I/Q modulation is illustrated by the diagrams of Fig. 2 showing the transition between two samples $C_{n-1}$ and $C_n$ of a complex modulation signal trajectory. The phase difference $\Delta\varphi_{e,n}$ between desired phase $\varphi_n$ of $C_n$ and prior constrained phase $\varphi_{H,n-1}$ related to $C_{n-1}$ can be given by

$$\Delta\varphi_{e,n} = \varphi_n - \varphi_{H,n-1}. \tag{3}$$

As shown in Fig. 2(a), the phase difference $\Delta\varphi_{e,n}$ is saturated in case it exceeds a given limit of $\pm\Delta\varphi_{SAT}$ according to

$$\Delta\varphi_{H,n} = \begin{cases} \Delta\varphi_{SAT} & \text{if } \Delta\varphi_{e,n} > \Delta\varphi_{SAT} \\ -\Delta\varphi_{SAT} & \text{if } \Delta\varphi_{e,n} < -\Delta\varphi_{SAT} \\ \Delta\varphi_{e,n} & \text{otherwise} \end{cases} \tag{4}$$

with $\Delta\varphi_{H,n}$ representing the constrained phase change. Therefore, the absolute constrained phase can be given by

$$\varphi_{H,n} = \sum_{k=1}^{n} \Delta\varphi_{H,k} = \varphi_{H,n-1} + \Delta\varphi_{H,n}. \tag{5}$$

According to (2), this results in a limitation of the RF-DPLL frequency modulation signal $f_{MOD,n}$ to $\pm f_{SAT}$ given by

$$-f_{SAT} \le f_{MOD,n} \le f_{SAT} \text{ with } f_{SAT} = F_s \frac{\Delta\varphi_{SAT}}{2\pi}. \tag{6}$$

As illustrated in Fig. 2(b) the constrained phase $\varphi_{H,n}$ describes the phase offset of the orthogonal, hybrid I/Q components $I_{H,n}$ and $Q_{H,n}$. Given the hybrid signal components, the complex modulation signal calculates to

$$C_n = (I_{H,n} + j\,Q_{H,n}) e^{j\varphi_{H,n}}. \tag{7}$$

By expanding and rewriting (7) in matrix form it becomes obvious that the conventional I/Q components can be calculated by a rotational transformation of the hybrid I/Q components as

$$\begin{pmatrix} I_n \\ Q_n \end{pmatrix} = \underbrace{\begin{pmatrix} \cos(\varphi_{H,n}) & -\sin(\varphi_{H,n}) \\ \sin(\varphi_{H,n}) & \cos(\varphi_{H,n}) \end{pmatrix}}_{\text{rotation matrix } R_{(\varphi_{H,n})}} \begin{pmatrix} I_{H,n} \\ Q_{H,n} \end{pmatrix}. \tag{8}$$

Vice versa, the hybrid I/Q components can be calculated by multiplying both sides of (8) with the inverse rotation matrix $R^{-1}_{(\varphi_{H,n})}$. Since the rotation matrix is orthogonal we get

$$R^{-1}_{(\varphi_{H,n})} = R^{T}_{(\varphi_{H,n})} = R_{(-\varphi_{H,n})} \tag{9}$$

and (8) can be written as

$$\begin{pmatrix} I_{H,n} \\ Q_{H,n} \end{pmatrix} = R_{(-\varphi_{H,n})} \begin{pmatrix} I_n \\ Q_n \end{pmatrix} \tag{10}$$

which equals a rotation of the complex modulation signal $C_n$ by the constrained phase but in opposite direction as shown in Fig. 2(c).

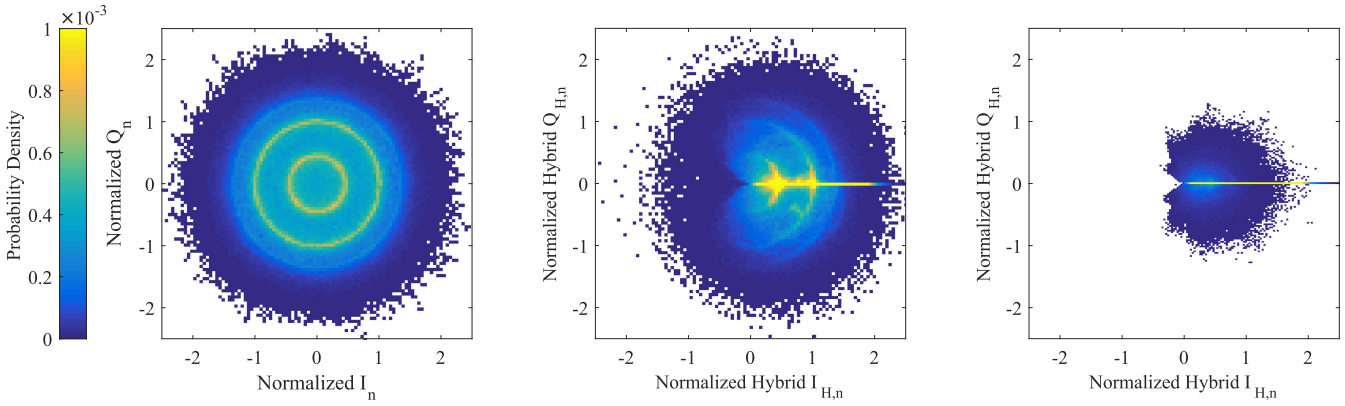


Fig. 5. Bivariate probability distribution of normalized I/Q signal components applied to the RF-DAC. Conventional I/Q modulation (left) and hybrid polar-I/Q modulation with $f_{\mathrm{SAT}} = 7.2$ MHz (middle) and $f_{\mathrm{SAT}} = 14.4$ MHz (right) for LTE uplink at 20 MHz channel bandwidth, 16-QAM symbol mapping and full RB allocation.

In case the phase saturation limits approach $\pm\pi$, the hybrid modulation operates as polar system since (4) becomes

$$\lim_{\Delta\varphi_{\mathrm{SAT}}\to\pi} \Delta\varphi_{\mathrm{H},n} = \Delta\varphi_{\mathrm{e},n}. \tag{11}$$

By inserting (3) and (5) in (11) we get $\varphi_{\mathrm{H},n} = \varphi_n$. With consideration of (1) and the trigonometric relations

$$\cos(\varphi_n) = \frac{I_n}{A_n}; \quad \sin(\varphi_n) = \frac{Q_n}{A_n}, \tag{12}$$

$I_{\mathrm{H},n}$ approaches the complex signal envelope of $C_n$, since

$$I_{\mathrm{H},n} = \cos(\varphi_n) I_n + \sin(\varphi_n) Q_n = \frac{I_n^2}{A_n} + \frac{Q_n^2}{A_n} = A_n. \tag{13}$$

Likewise, $Q_{\mathrm{H},n}$ tends towards 0 which results in

$$\lim_{\Delta\varphi_{\mathrm{SAT}}\to\pi} \begin{pmatrix} I_{\mathrm{H},n} \\ Q_{\mathrm{H},n} \end{pmatrix} = \begin{pmatrix} A_n \\ 0 \end{pmatrix}. \tag{14}$$

On the other hand, if the phase saturation limits approach 0, the rotation matrix becomes the identity matrix since no phase modulation is allowed and the hybrid modulation scheme therefore behaves like a conventional quadrature system, i.e.

$$\lim_{\Delta\varphi_{\mathrm{SAT}}\to 0} \begin{pmatrix} I_{\mathrm{H},n} \\ Q_{\mathrm{H},n} \end{pmatrix} = \begin{pmatrix} I_n \\ Q_n \end{pmatrix}. \tag{15}$$

In the shown approach an adjustable but constant saturation has been chosen as constraint. However, also a more complex constraining like a low-pass filtering of the desired phase or a combination of saturation and filtering, etc. could be applied according to the utilized phase modulator circuitry.

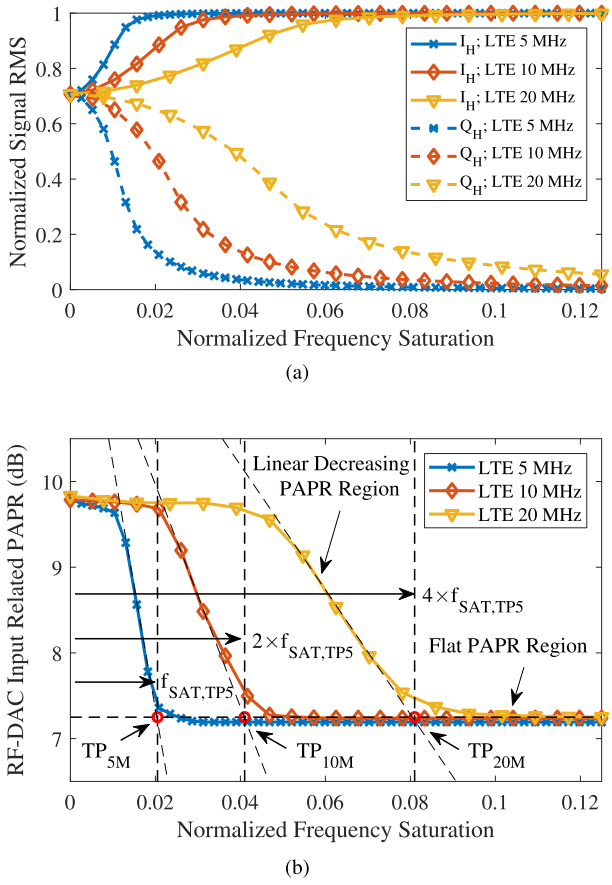


Fig. 6. Hybrid signal characteristics over frequency saturation $f_{\mathrm{SAT}}$ normalized to $F_s/2$ for different LTE channel bandwidths. (a) RMS of $I_{\mathrm{H},n}$ and $Q_{\mathrm{H},n}$ normalized to the complex signal RMS. (b) RF-DAC input related $\mathrm{PAPR}_{99.99\%}$ of $|I_{\mathrm{H},n}| + |Q_{\mathrm{H},n}|$.

## III. Digital Front-End Implementation

A DFE implementation of the proposed modulation scheme is shown in the block diagram of Fig. 3. The upper part represents the hybrid phase path processing. The inphase and quadrature signals $I_n$, $Q_n$ are transformed to the phase and amplitude signals $\varphi_n$, $A_n$ by the vectoring mode coordinate rotation digital computer (VM-CORDIC). The phase difference $\Delta\varphi_{\mathrm{e},n}$ between the desired phase $\varphi_n$ and the prior constrained phase sample $\varphi_{\mathrm{H},n-1}$ is saturated if it exceeds $\pm\Delta\varphi_{\mathrm{SAT}}$. The resulting constrained phase change $\Delta\varphi_{\mathrm{H},n}$ is accumulated to generate the absolute, constrained phase $\varphi_{\mathrm{H},n}$ by the phase accumulator loop.

The lower part of the block diagram represents the hybrid I/Q path processing. A rotation-mode coordinate rotation digital computer (RM-CORDIC) transforms the input signals $I_n$, $Q_n$ to the hybrid components $I_{\mathrm{H},n}$, $Q_{\mathrm{H},n}$ according to (10). The hybrid signal components $I_{\mathrm{H},n}$, $Q_{\mathrm{H},n}$ and constrained

phase change $\Delta\varphi_{\mathrm{H},n}$ are then applied to the RF part of the TX, further described in Section IV.

### A. Hybrid-DFE Simulation Results

A behavioral model of the DFE architecture has been implemented in MATLAB. Simulation results for LTE uplink transmission with 20 MHz channel bandwidth, 16-QAM symbol mapping and full resource block (RB) allocation are shown in Fig. 4. The hybrid-DFE operates at a sampling frequency of $F_{\mathrm{S}} = 307.2$ MHz and selected phase saturation level of $\Delta\varphi_{\mathrm{SAT}} = 9°$. Note that according to (6), this corresponds to a frequency modulation saturating at $f_{\mathrm{SAT}} = 7.68$ MHz. Compared to a conventional RF-DPLL two-point phase modulator without any trajectory modifications, the required DCO frequency tuning range is in this example reduced down to 5%. The complex input signal components given by $I_n$ and $Q_n$, hybrid signal components given by $I_{\mathrm{H},n}$, $Q_{\mathrm{H},n}$ and $\Delta\varphi_{\mathrm{H},n}$ applied to the RF part as well as the internal hybrid phase path signals $\varphi_n$, $\varphi_{\mathrm{H},n}$ and $\Delta\varphi_{\mathrm{e},n}$ are extracted. By comparing the input and hybrid-DFE output signals it can be seen that the hybrid inphase component $I_{\mathrm{H},n}$ converges to the complex signal envelope for most of the time, significantly reducing the excitation of the quadrature component $Q_{\mathrm{H},n}$. Also, it can be seen that the constrained phase change signal $\Delta\varphi_{\mathrm{H},n}$ clips at the specified saturation level resulting in the accumulated constrained phase $\varphi_{\mathrm{H},n}$ lagging the desired phase $\varphi_n$. For those instances the hybrid quadrature component $Q_{\mathrm{H},n}$ is then required to compensate for the increased phase error $\Delta\varphi_{\mathrm{e},n}$.

### B. Hybrid Signal Characteristics

By incorporating phase modulation the proposed hybrid approach reduces the excitation of the hybrid quadrature component $Q_{\mathrm{H},n}$. This becomes evident by comparing the bivariate distributions of the LTE uplink signal for conventional and hybrid signal representations as shown in Fig. 5. The hybrid approach concentrates the $I_{\mathrm{H},n}$ and $Q_{\mathrm{H},n}$ components around the real axis with the spread of $Q_{\mathrm{H},n}$ being reduced with increasing saturation levels. The RMS of both $I_{\mathrm{H},n}$ and $Q_{\mathrm{H},n}$ components normalized to the complex input signal RMS are shown in Fig. 6(a). It can be seen that with increasing frequency saturation levels the components shift from a balanced distribution to almost inphase only. According to (14), the RMS of $I_{\mathrm{H},n}$ converges to the complex signal RMS and the RMS of $Q_{\mathrm{H},n}$ converges to 0. In addition, a reduced signal peaking results, characterized by the peak-to-average power ratio (PAPR) of $|I_{\mathrm{H},n}|+|Q_{\mathrm{H},n}|$ as shown in Fig. 6(c) and given by (26) of Appendix VI-A. The RF-DAC input related PAPR determines the required back-off operation and therefore the achievable average output power and drain efficiency which is further discussed in Section V-A.

The hybrid signal characteristics highly dependent on the input signal statistics in combination with the chosen saturation level. With increasing channel bandwidths and symbol rates, larger phase changes appear more frequently. Given a certain frequency saturation level this results in larger deviations between constrained and desired phase which are compensated by an increased utilization of the hybrid quadrature component $Q_{\mathrm{H},n}$. In Fig. 6(b) it can be seen that the defined turnover points (TPs) scale linearly with the LTE channel bandwidth. The TPs are reflecting the transition between the linear decreasing PAPR region and flat PAPR region given by the polar lower limit with respect to the normalized frequency saturation. This allows for example to determine the required frequency saturation given a certain RF-DAC input related PAPR target and signal bandwidth. For the considered LTE uplink signals the frequency saturation at TP given by $f_{\mathrm{SAT,TP}}$ over signal bandwidth[1] $\mathrm{BW}_{\mathrm{signal}}$ is empirically found to be constant and can be given as

$$\lambda = \frac{f_{\mathrm{SAT,TP}}}{\mathrm{BW}_{\mathrm{signal}}} \approx 0.7. \tag{16}$$

Therefore, a recalculation of the required frequency saturation can be done for different transmission bandwidths by multiplication of $\lambda$ with the wanted transmission bandwidth.

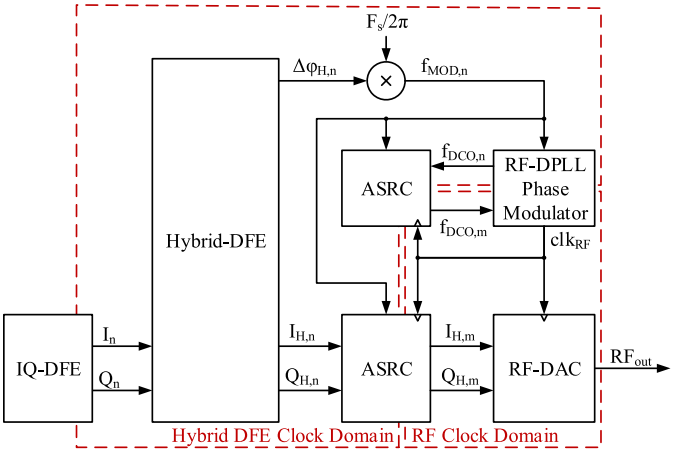


Fig. 7. Proposed digital-intensive hybrid polar-I/Q TX architecture. Chip-external front-end components like PA, duplex filter or antenna are not illustrated.

## IV. Transmitter Architecture

A high level implementation of the digital-intensive hybrid polar-I/Q TX is shown in the block diagram of Fig. 7. The I/Q-DFE provides the upsampled baseband I/Q signals $I_n$ and $Q_n$ with $n$ being the sample index with respect to the hybrid-DFE sampling rate. Subsequently, the hybrid-DFE generates the hybrid components $I_{\mathrm{H},n}$, $Q_{\mathrm{H},n}$ and $\Delta\varphi_{\mathrm{H},n}$ according to Fig. 3 as described in Section III. The constrained phase change $\Delta\varphi_{\mathrm{H},n}$ is then scaled by $F_{\mathrm{S}}/2\pi$ resulting in the frequency modulation signal $f_{\mathrm{MOD},n}$ which is applied to the RF-DPLL based phase modulator. The hybrid I/Q components $I_{\mathrm{H},n}$, $Q_{\mathrm{H},n}$ and the RF-DPLL internal DCO frequency modulation signal $f_{\mathrm{DCO},n}$ are processed by arbitrary sampling rate converters (ASRCs) which upsample and interpolate the data to the modulated RF clock. The upsampled frequency modulation signal $f_{\mathrm{DCO},m}$, with $m$ being the sample index with respect to the RF clock domain sampling rate, is then applied to the DCO. The DCO generates a phase modulated RF clock $clk_{\mathrm{RF}}$ for any digital logic operating on RF rate including

[1]For determining the empirical constant $\lambda$, the effective LTE uplink transmission bandwidth without guard intervals at the channel edges has been considered.

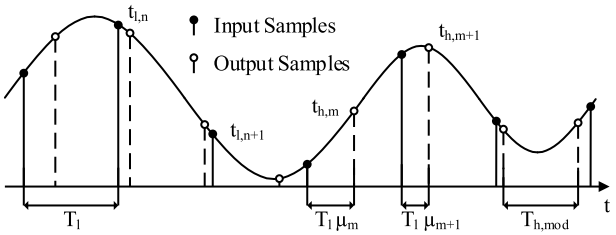


Fig. 8. Exemplary process of upsampling data from a uniform low-rate data grid to a non-uniform high-rate data grid.

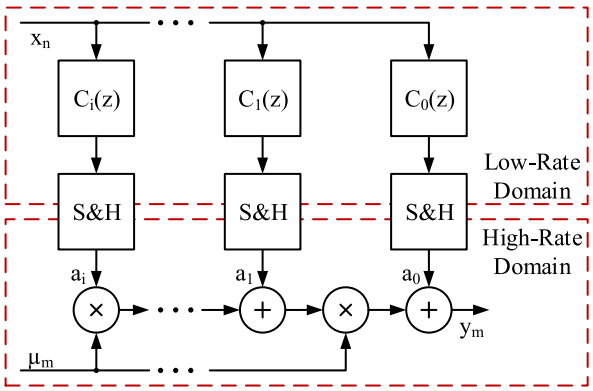


Fig. 9. The basic Farrow structure separated in a low- and high-rate processing domain which are connected by means of Sample-and-Hold (S&H) blocks.

the RF-DAC. Likewise, the upsampled hybrid components $I_{\mathrm{H},m}$ and $Q_{\mathrm{H},m}$ are applied to the RF-DAC.

The following Section IV-A describes the employed concepts for SRC, with a further segmentation in I/Q-DFE and hybrid components upsampling. Subsequently, the RF-DPLL based phase modulator and the switched-capacitor RF-DAC are presented for this TX architecture in Sections IV-B and IV-C, respectively.

### A. Sampling Rate Conversion

In general the sampling rate in the TX increases from the baseband towards the antenna. In the further course of this paper, the notation of upsampling and interpolation is used interchangeably. The purpose of interpolation is to attenuate the images of the baseband signal according to the requirements on out-of-band spectral emissions of the RF signal. In order to achieve the required performance it is common that state-of-the-art digital-intensive TX chains for multi-band, multi-standard mobile handset applications employ multiple SRCs. The hybrid polar-I/Q TX architecture shown in Fig. 7 is based on two different concepts for SRC.

In the IQ-DFE the baseband signal is upsampled to a higher sampling rate. Even though the interpolation ratios vary for different radio access technologies (RATs), bands or requirements of the subsequent hybrid-DFE, the possible range of ratios is limited to integer or pre-defined fractional factors. In addition the digital signal processing (DSP) is triggered by a single clock source only. These boundary conditions together with the band-limited I/Q signals allow the application of conventional low-pass interpolation. A possible implementation could be based on cascaded integrator-comb (CIC) filters for

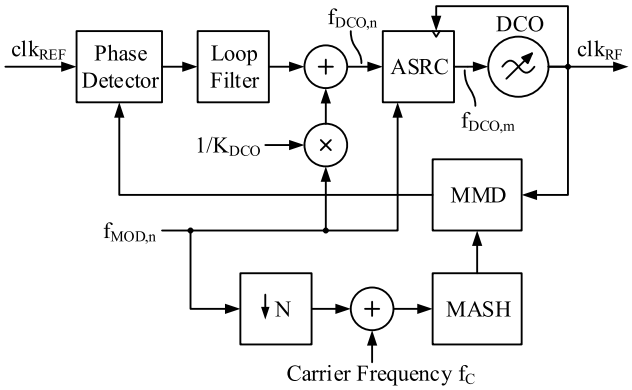


Fig. 10. RF-DPLL with two-point phase modulation [20].

interpolation ratios equal to powers of two or fractional sampling rate converters (FSRCs) realized as filters in polyphase structure for constant fractional interpolation ratios [32], [33]. For the simulation results provided in Section V the baseband signal is upsampled by means of zero-padding in the frequency domain. The set of available target sampling rates was defined to multiples of the reference clock operating at 38.4 MHz. With respect to this set, the sampling rate $F_{\mathrm{s}}$ of the hybrid-DFE has been chosen so that the overall TX path fulfills the requirements in terms of in-band and out-of-band signal distortion.

In digital-intensive TX, power consumption and manufacturing cost can be decreased by relaxing analog anti-aliasing filter requirements with the intention to integrate the filter on-chip. However, such an approach increases the demand on the spectral performance of the RF signal in the digital domain prior to the RF-DAC. Measures to achieve the required performance are given by interpolation or generation of RF-DAC input samples at the TX channel frequency or an integer fraction of it at low signal distortion [11].

The RM-CORDIC in the hybrid-DFE calculates the hybrid I/Q signals $I_{\mathrm{H},n}$ and $Q_{\mathrm{H},n}$ which are already upsampled with respect to the baseband data. In order to generate the high-rate signals $I_{\mathrm{H},m}$ and $Q_{\mathrm{H},m}$ at the instantaneous RF rate, the application of an ASRC is required. FSRCs exploit pre-defined fractional but constant interpolation ratios which can be represented by an integer based rational fraction approximation resulting in a low count of inter-sample positions. In contrast, ASRCs are capable of upsampling data by arbitrary time-variant interpolation ratios. In the proposed TX architecture the initial upsampling of $I_{\mathrm{H},n}$ and $Q_{\mathrm{H},n}$ as well as the interpolation target frequency depend on RAT, output power and operating frequency band. Additionally and due to the polar characteristic of the hybrid TX, the interpolation target frequency (i.e. the rate of the ASRC output data) is modulated. Consequently, the resulting interpolation ratio is time-variant and has to be considered within the ASRC. Because the same boundary conditions are to be found in the RF-DPLL, an ASRC is employed to upsample the DCO frequency tuning word $f_{\mathrm{DCO},n}$ from the low-rate to the modulated high-rate clock domain. Since the upsampled DCO tuning word signal $f_{\mathrm{DCO},m}$ directly controls the instantaneous target sampling rate this upsampling is referred to as data-dependent interpolation.

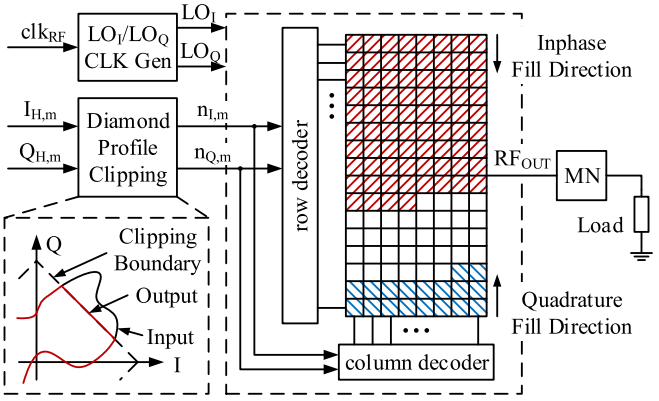


Fig. 11. Shared-cell RF-DAC with diamond-profile signal clipping.

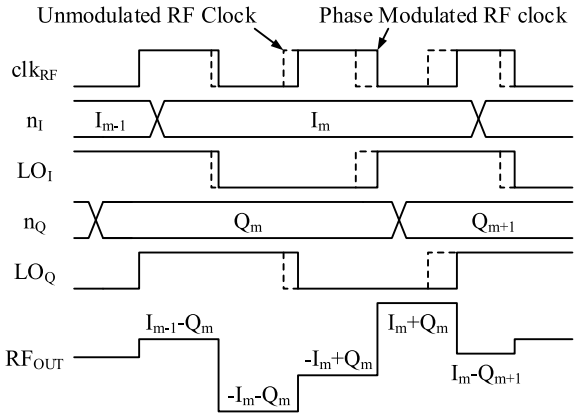


Fig. 12. Assumed ideal RF waveform generation inside the RF-DAC.

Figure 8 depicts the process of interpolation by means of an exemplary signal. The input signal is sampled at an uniform time grid with the low-rate period $T_\mathrm{l}$. The upsampled signal is sampled at the non-uniform time grid with the modulated period $T_{\mathrm{h},m}$. The instantaneous interpolation ratio can be defined as

$$R_{\mathrm{ASRC},m} = \frac{T_\mathrm{l}}{T_{\mathrm{h},m}} \tag{17}$$

with l referring to the low-rate and h to the high-rate clock domain.

The relative positioning of the output samples with respect to the input data is defined by the time-variant intersample time $\mu_m$. With $\mu_m \in [0, 1)$ referring to an equidistant low-rate period $T_\mathrm{l}$; it can be calculated to

$$\mu_m = \frac{t_{\mathrm{h},m}}{T_\mathrm{l}} - \underbrace{\lfloor \frac{t_{\mathrm{h},m}}{T_\mathrm{l}} \rfloor}_{\xi_m}. \tag{18}$$

For the purpose of implementation it is appropriate to consider a time-continuous representation of the interpolated output samples $y(t_{\mathrm{h},m})$ with the input samples $x(t_{\mathrm{l},n} = nT_\mathrm{l})$ and the low-pass filter impulse response $h_\mathrm{LP}$ which is defined by the convolution

$$y(t_{\mathrm{h},m}) = \sum_{n=-\infty}^{\infty} x(nT_\mathrm{l}) h_\mathrm{LP}(t_{\mathrm{h},m} - t_{\mathrm{l},n}). \tag{19}$$

With the aid of $\mu_m$, the absolute time difference $t_{\mathrm{h},m} - t_{\mathrm{l},n}$ between any low- and high-rate samples can be expressed as

$$t_{\mathrm{h},m} - t_{\mathrm{l},n} = (\mu_m + \xi_m - n)T_\mathrm{l} \tag{20}$$

which also yields

$$\mu_m + \xi_m = \frac{1}{T_\mathrm{l}} \sum_{k=0}^{m} T_{\mathrm{h},k} = m\overline{R} \tag{21}$$

where $\overline{R}$ is the average interpolation ratio from $t(0)$ till $t_{\mathrm{h},m}$. In (18) – (21), it is demonstrated that $\mu_m$ can yield arbitrary values during the interpolation process. Considering $h_\mathrm{LP} = h_\mathrm{LP}(\mu_m, \xi_m, n)$ in (19) it becomes clear that the major design obstacle for the ASRC is to find an efficient implementation which evaluates the continuous impulse response at arbitrary positions [34], [35].

One method is to describe $h_\mathrm{LP}(t)$ by means of piecewise polynomial segments between two input samples $x_n$ and $x_{n+1}$. For this approach the Farrow structure is one of the efficient ways of implementation [36]. Figure 9 shows the basic Farrow structure. In the low-rate domain, a set of $I + 1$ finite impulse response (FIR) filters of length $J$ calculate the coefficients

$$a_i = \sum_{j=-J/2}^{J/2-1} x(nT_\mathrm{l} - j)c_i(j) \tag{22}$$

of the $I^{th}$ order interpolation polynomial which can be expressed as

$$y(t_{\mathrm{h},m}) = \sum_{i=0}^{I} a_i \mu_m^i. \tag{23}$$

The polynomial is evaluated in the high-rate domain by means of the Horner scheme. The advantage of this structure can be given by the constant filter coefficients $c_i(j)$ at the low-rate domain with only $\mu_m$ being time-variant. This basic variation of the Farrow structure can be further optimized, e.g. by the application of an offset on $\mu_m$ to obtain symmetrical FIR filter coefficients [37].

For the presented simulation results Lagrange interpolation is applied in all ASRCs. The hybrid I/Q components are interpolated based on 2$^{\mathrm{nd}}$ order Lagrange polynomials which turned out as sufficient to achieve the required spectral performance. Since Lagrange interpolation yields $I = J$ when applied on the Farrow structure, it is possible to further simplify its realization to the Newton structure resulting in a highly power efficient hardware implementation [38].

Finally, the polar-like signal characteristic of the hybrid components $I_{\mathrm{H},n}$, $Q_{\mathrm{H},n}$ and $f_{\mathrm{MOD},n}$ has to be highlighted. A significant bandwidth expansion of the hybrid components in comparison to the I/Q baseband input signal results due to the nonlinear transformations in the hybrid-DFE. This property complicates the signal interpolation and introduces in-band and out-of-band signal distortion after interpolation [23]. However, different possibilities exist to achieve interpolation in the polar signal domain with low distortion. The

TABLE I

EXEMPLARY RF-DAC PARAMETRIZATION UTILIZED FOR CODE-DEPENDENT DRAIN EFFICIENCY CALCULATION

| Parameter | Value | Unit |
|---|---|---|
| Supply Voltage $U_{\mathrm{VDD}}$ | 1.1 | (V) |
| Channel Frequency $f_0$ | 2.4 | (GHz) |
| Number of Unitary Cells $N$ | 1024 | - |
| Transformed Load $R_{\mathrm{TL}}$ | 2.25 | ($\Omega$) |
| Switch Resistance $R_{\mathrm{SW}}$ | 350 | ($\Omega$) |
| Loaded MN Quality Factor $Q_{\mathrm{MN}}$ | 2.5 | - |
| Inductance L1 Quality Factor $Q_{\mathrm{L1}}$ | 15 | - |
| Inductance L2 Quality Factor $Q_{\mathrm{L2}}$ | 15 | - |
| Technology Parameter $\beta$ | 0.035 | - |

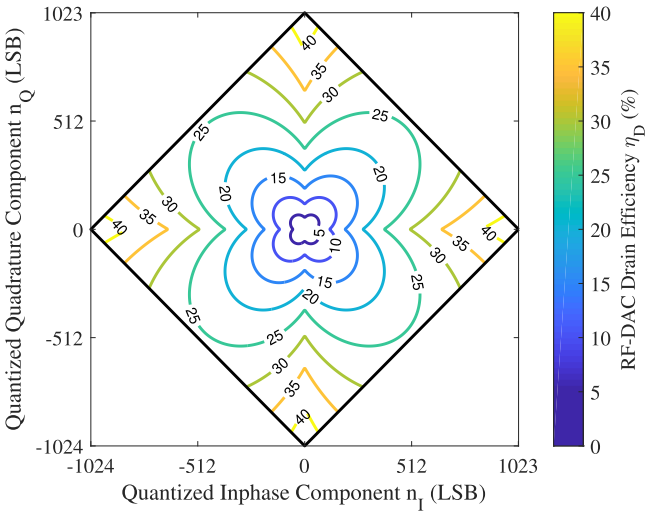


Fig. 13. Contour plot illustrating the RF-DAC drain efficiency $\eta_{\mathrm{D}}$ over I/Q input codewords according to (31) and parametrization given in Table I. The codewords are quantized according to the total number of unitary-weighted cells $N$ with additional sign representing the MSB.

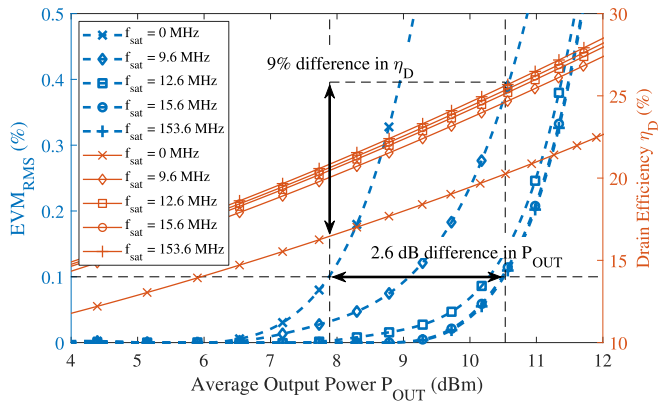


Fig. 14. $\mathrm{EVM_{RMS}}$ and RF-DAC drain efficiency $\eta_{\mathrm{D}}$ over average output power $P_{\mathrm{out}}$ for different frequency saturation levels $f_{\mathrm{SAT}}$ and LTE uplink transmission with 20 MHz channel bandwidth and full RB allocation.

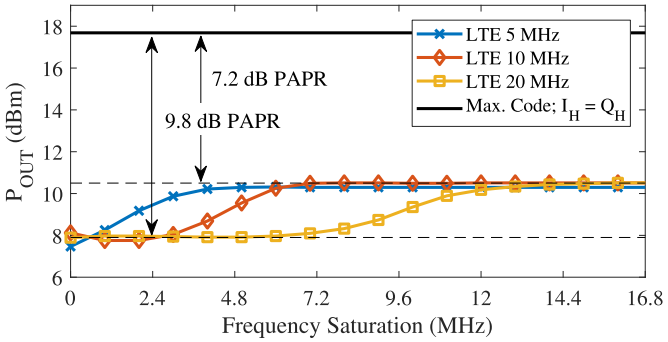


Fig. 15. Achievable average output power $P_{\mathrm{out}}$ at 0.1% $\mathrm{EVM_{RMS}}$ degradation over frequency saturation $f_{\mathrm{SAT}}$ for different LTE channel bandwidths.

most common measures include a high oversampling of the low-rate I/Q signals prior to the CORDIC, hole punching of the complex baseband signal as well as novel adaptive interpolation algorithms [26], [39]. For the presented approach, a high oversampling of the I/Q baseband signal has been chosen to achieve a low signal distortion after the ASRCs.

### B. RF-DPLL Based Phase Modulator

A simplified fractional-N RF-DPLL block diagram with two-point phase modulation is illustrated in Fig. 10. A more detailed description of a highly reconfigurable implementation for a polar TX supporting cellular communication standards up to 4G LTE-A is for example shown in [20]. The phase modulation is realized by a frequency modulation of the DCO whereas the frequency modulation signal $f_{\mathrm{MOD},n}$ is injected at two points of the RF-DPLL in a feed-forward fashion to avoid a disturbance of the control loop.

By constraining the phase modulation and therefore limiting the excitation of the frequency modulation signal to a fraction of $\pm F_{\mathrm{s}}/2$, a significant reduction of the DCO fine-tuning range can be achieved. This results for example in a lower number of required DCO cores and more importantly in a decoupling of the DCO fine-tuning range and the DFE sampling rate. Consequently, the DFE sampling rate can be chosen according to the requirements for in-band signal distortion and out-of-band spectral emission without the aforementioned trade-off as will be shown in Section V.

### C. Switched-Capacitor RF-DAC

A quadrature RF-DAC as illustrated in Fig. 11 with 50% LO duty cycle operation is considered. Furthermore, a sharing of the unitary-weighted cells between the I/Q signal components as shown in [21] is assumed. The shared-cell approach is beneficial in order to fully exploit the advantage of the hybrid modulation scheme. As shown in Fig. 6(b), the RF-DAC input related PAPR for the sum of the quantized I/Q components $|n_{\mathrm{I}}| + |n_{\mathrm{Q}}|$ is reduced with increasing frequency saturation. Therefore, a lower RF-DAC cell utilization and back-off operation results. A diamond-profile signal clipping is placed prior to the RF-DAC in order to restrict the signal trajectory to the useful region given by $|n_{\mathrm{I}}| + |n_{\mathrm{Q}}| < N$ with $N$ representing the number of unitary-weighted RF-DAC cells. This is necessary to avoid a simultaneous allocation of unitary-cells by the I/Q components. Figure 12 illustrates the waveform generation on RF rate prior to a filtering by the matching network. To avoid any RF-DAC implementation specific effects an ideal recombina-

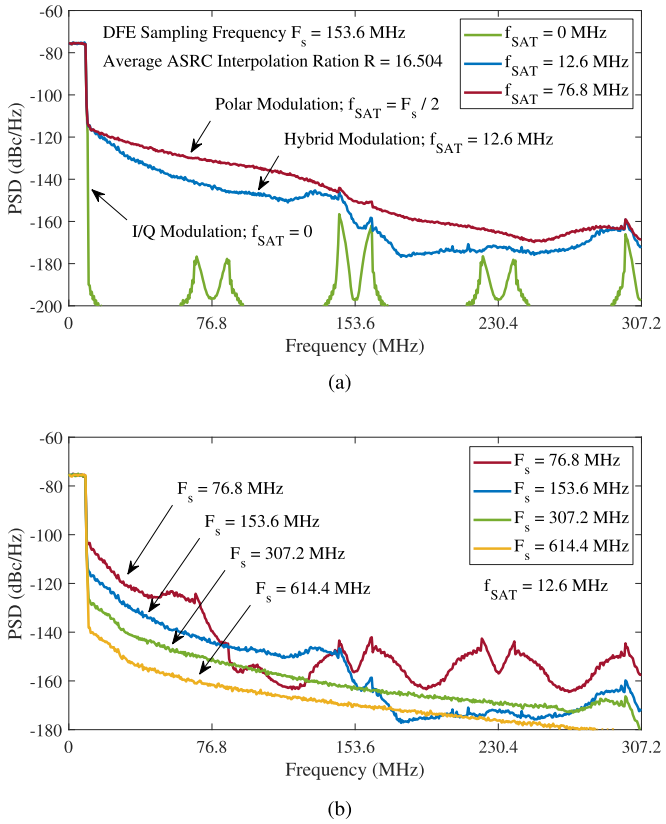


Fig. 16. TX power spectrum for 20 MHz LTE uplink transmission with ideal recombination of the complex signal after ASRC. (a) For conventional I/Q, polar and hybrid modulation at $F_S = 153.6$ MHz. (b) For hybrid modulation at $f_{SAT} = 12.6$ MHz and different DFE sampling rates.

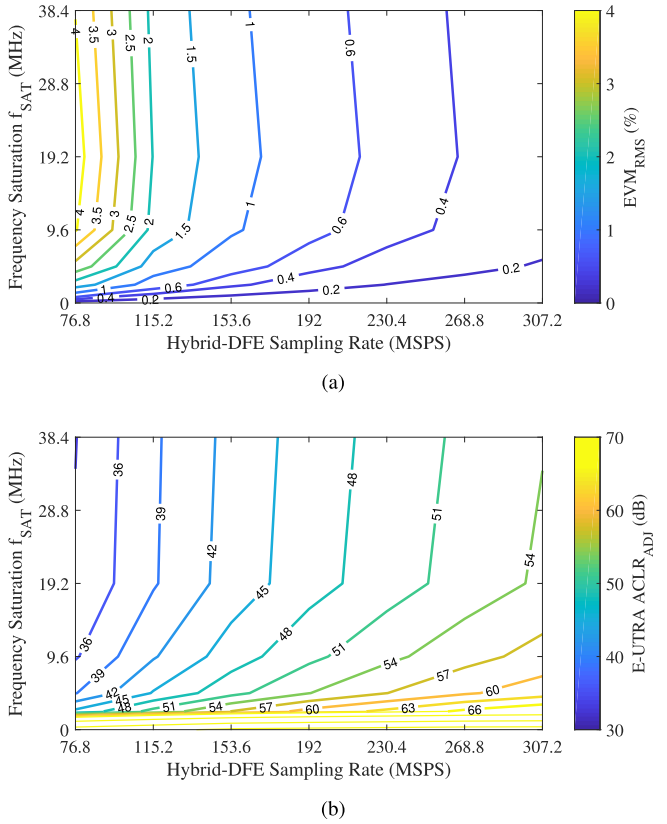


Fig. 17. Contour plots showing in-band and out-of-band distortion over hybrid-DFE sampling rate and frequency saturation for 20 MHz LTE uplink transmission with ideal recombination of the complex signal after ASRC. (a) Demodulated ASRC output EVM. (b) E-UTRA adjacent channel ACLR.

tion with the rectangular LO is considered, approximating the ideal direct upconversion by the LO fundamental.

## V. Simulation Results

A TX system including the hybrid-DFE, ideal RF-DPLL phase modulator and 14-bit shared-cell RF-DAC is implemented in MATLAB. The RF-DAC core is assumed to be split into 10-bit unitary-weighted cells for the MSBs and 4-bit binary-weighted cells for the LSBs. The mentioned split becomes relevant for calculation of the average output power and drain efficiency as shown in Section V-A.

### *A. RF-DAC Average Output Power and Drain Efficiency*

To evaluate the benefit of the hybrid modulation approach in a more practical context a drain efficiency model for a switched-capacitor RF-DAC is derived in Appendix VI-B. Linked with the resulting hybrid I/Q signal components the model is utilized to evaluate the effect on average RF-DAC drain efficiency and output power in back-off operation.

For the switched-capacitor RF-DAC parametrization given in TABLE 1 the code-dependent drain efficiency $\eta_D$ as shown in the contour plot of Fig. 13 results. The resulting RF-DAC drain efficiency over average output power $P_{out}$ is shown in Fig. 14 for different frequency saturation levels. The figure also shows the in-band signal distortion which increases with higher output power due to the diamond-profile signal clipping. Given a certain distortion limit characterized by an error vector magnitude (EVM) degradation of 0.1%, approximately 2.6 dB higher output power and 9% higher drain efficiency can be achieved compared to the conventional quadrature system. Furthermore, with the frequency saturation limit being less than 10% of the full scale range given by $\pm F_S/2$, only a fraction of the DCO fine-tuning range as would be required by a conventional polar system is necessary.

Figure 15 shows the achievable average output for different LTE channel bandwidths as well as the maximum output power for the constant code case with all cells being active. The figure also depicts the relation between the average output power in back-off operation and the RF-DAC input related PAPR. According to Fig. 6(b), a lower input related PAPR results for increasing frequency saturation levels. Therefore, a larger signal gain can be selected until the signal starts to clip which results in an increased average output power.

### *B. In-Band Distortion and Out-of-Band Spectral Emission*

Simulation results characterizing the introduced signal distortion after processing by the ASRCs for FDD-LTE uplink with 20 MHz channel bandwidth operating in band 7 are shown in Fig. 16 and Fig. 17. The ASRCs are configured for a second-order interpolation, directly upsampling the hybrid signal components from DFE to RF rate. Fig. 16 shows the power spectral density (PSD) of the recombined complex signal in

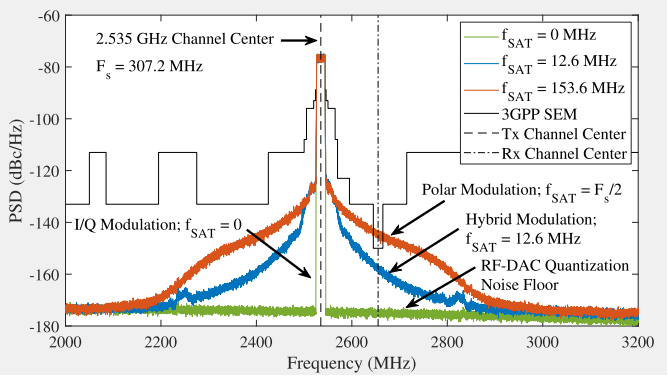


Fig. 18. TX power spectrum at RF-DAC output for different frequency saturation levels, ideal phase modulation and waveform generation as shown in Fig. 12 for a DFE sampling rate of $F_S = 307.2$ MHz.

equivalent baseband domain for different frequency saturation levels and DFE sampling rates. The in-band distortion given by the signals EVM and out-of-band distortion characterized by the adjacent channel leakage ratio (ACLR) are shown in the contour plots of Fig. 17. An increased in-band distortion and out-of-band spectral degradation can be observed compared to exclusive I/Q operation with $f_{SAT} = 0$. It can be seen that with increasing saturation levels also the introduced distortion increases, approaching the polar operation for $f_{SAT} = F_S/2$. This results from interpolation errors arising in the ASRCs when operating on the hybrid modulation signals but can be countered by a higher DFE sampling rate. Nevertheless, it becomes apparent that for the hybrid approach lower spectral emission levels can be achieved compared to polar operation.

Figure 18 shows the power spectrum of the RF-DAC output signal $RF_{\text{out}}$ for different frequency saturation levels and a DFE sampling rate of $F_S = 307.2$ MHz. Besides of meeting general 3GPP spectral emission mask requirements one important property for the TX is given by its spectral emissions at the receive duplex distance resulting in a degradation of the receiver sensitivity. In compliance to Fig. 16, a significant spectral emission at the duplex distance is observed for the polar configuration. For the hybrid approach a lower spectral emission is observed which results in potentially lower sampling rates of the DFE as would be required by the polar system.

## VI. Conclusion

A novel hybrid polar-I/Q methodology combining I/Q with constrained phase modulation has been presented. A digital-intensive hybrid TX architecture implementing a DFE based on VM-CORDIC and RM-CORDIC for deriving the hybrid signal components from I/Q input data is shown. The phase modulation is realized by means of an RF-DPLL with two-point modulation generating a phase-modulated LO. ASRCs with data-dependent interpolation are utilized to upsample and interpolate the hybrid signal components to the modulated RF clock. The hybrid I/Q signals are applied to a shared-cell quadrature RF-DAC with diamond-profile signal clipping. Simulation results of the entire TX chain are presented for LTE uplink transmission based on a minimalistic TX model considering ASRC error contribution with ideal RF-DPLL phase modulator and RF-DAC. Also, the impact on RF-DAC drain efficiency and average output power for back-off operation is evaluated. It is shown that a similar benefit in average output power and drain efficiency as for a polar system can be achieved while only a fraction of the RF-DPLL phase modulator tuning range is required. In terms of in-band signal distortion the hybrid TX shows similar degradation as seen in the digital polar TX. However, a lower out-of-band spectral emission is achieved due to the decreased bandwidth expansion of the constrained phase modulation signal.

## Appendix

### A. RF-DAC Input Related Crest Factor and PAPR

For the switched-capacitor quadrature RF-DAC with cell sharing between the I/Q components the signal is clipped according to a diamond profile [21]. For this case, signal distortion arises when the number of active RF-DAC cells exceeds the total number of unitary cells $N$. To avoid additional signal distortion introduced by the clipping, the RF-DAC has to operate in back-off which can be characterized by its maximum output power and the crest factor or PAPR of the applied signal. Therefore, the linear summation $|I_{\text{H},n}| + |Q_{\text{H},n}|$ being directly proportional to the number of active cells is considered for describing certain signal characteristics related to the RF-DAC input. The crest factor $CF(p)$ can be given by

$$CF(p) = \frac{F_X^{-1}(p)}{\sqrt{\frac{1}{M}\sum_{n=0}^{M-1}\left(I_{\text{H},n}^2 + Q_{\text{H},n}^2\right)}} \tag{24}$$

with $p \in [0, 1]$ being the considered percentile of the stochastic process $X_n = |I_{\text{H},n}| + |Q_{\text{H},n}|$ and $F_X^{-1}(p)$ beeing the inverse of the cumulative distribution function of $X_n$ given as

$$F_X(x) = P(X_n \leq x) \text{ with } X_n = |I_{\text{H},n}| + |Q_{\text{H},n}|. \tag{25}$$

The RF-DAC related PAPR is defined as the square of $F_X^{-1}(p)$ divided by the square of the complex signal RMS and therefore directly relates to the crest factor as

$$PAPR(p) = 20\log_{10}(CF(p)). \tag{26}$$

### B. RF-DAC Drain Efficiency

The considered switched-capacitor RF-DAC architecture based on shared, unitary-weighted power cells in combination with LO sign-switching and diamond-profile signal clipping as shown in [21] is depicted in Fig. 19. Due to the cell sharing between the I/Q components the total number of cells and therefore RF-DAC size can be reduced compared to implementations with dedicated I/Q cells. In order to calculate average output power and drain efficiency, several code dependent loss mechanisms as illustrated by the equivalent circuits shown in Fig. 20 have to be considered.

First, a dynamic loss in the CMOS inverter stage as described in [40] results from simultaneous switching of PMOS and NMOS transistors as well as due to parasitic input

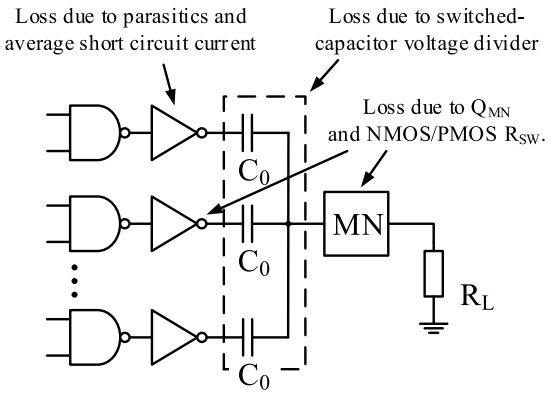


Fig. 19. Exemplary switched-capacitor RF-DAC unitary-weighted cell architecture with markup of the considered loss mechanisms.

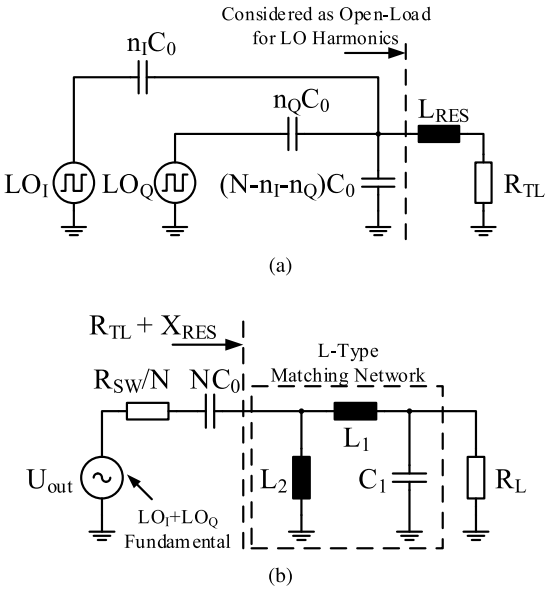


Fig. 20. Equivalent circuit models for RF-DAC drain efficiency calculation with (a) capacitive voltage divider related loss and (b) switch resistance as well as matching network insertion loss.

and output capacitances. The average power dissipated by the inverter $P_{switch}$ calculates to

$$P_{\text{switch}} = \beta \frac{(\frac{2}{\pi})^2\ U_{\text{VDD}}^2}{2\ R_{\text{SW}}}(n_{\text{I}} + n_{\text{Q}}). \tag{27}$$

with $n_{\text{I}}$ and $n_{\text{Q}}$ describing the quantized codewords acting on the unitary-weighted RF-DAC cells. The technology parameter $\beta$ is independent from the CMOS inverter size but shows a linear dependency on rise- and fall-times of the switching and operating frequency [40].

Second, due to the switched capacitive voltage divider as shown in Fig. 20(a), charge is applied and removed at rising and falling $\text{LO}_{\text{I}}$ and $\text{LO}_{\text{Q}}$ clock edges which results in a dynamic loss. As shown in [31], the power loss $P_{\text{cdiv}}$ for the quadrature RF-DAC calculates to

$$P_{\text{cdiv}} = [n_{\text{I}}(N - n_{\text{I}}) + n_{\text{Q}}(N - n_{\text{Q}}) + 2\ n_{\text{I}}n_{\text{Q}}]\frac{U_{\text{VDD}}^2 f_0}{N^2}. \tag{28}$$

Third, additional insertion loss results due to the effective NMOS/PMOS switch resistance given by $R_{\text{SW}}/N$ and limited quality factors $Q_{\text{MN}}$, $Q_{\text{L1}}$ and $Q_{\text{L2}}$ of the L-Type matching network [12]. Their contributions to the total RF-DAC drain efficiency are determined according to the equivalent circuit illustrated in Fig. 20(b). The product of resistive loss and matching network related loss can be given as

$$\eta_{\text{IL}} = \left(\frac{1 - Q_{\text{MN}}/Q_{\text{L1}}}{1 + Q_{\text{MN}}/Q_{\text{L2}}}\right)\left(\frac{R_{\text{TL}}}{R_{\text{TL}} + R_{\text{SW}}/N}\right)^2. \tag{29}$$

The code dependent RF-DAC output power $P_{\text{out}}$ and drain efficiency $\eta_{\text{D}}$ calculate to

$$P_{\text{out}} = \eta_{\text{IL}} \frac{(\frac{2}{\pi})^2\ U_{\text{VDD}}^2(n_{\text{I}}^2 + 2\ n_{\text{I}}n_{\text{Q}} + n_{\text{Q}}^2)}{2\ R_{\text{TL}}N^2}, \tag{30}$$

$$\eta_{\text{D}} = \frac{P_{\text{out}}}{P_{\text{in}}} = \frac{P_{\text{out}}}{P_{\text{out}}/\eta_{\text{IL}} + P_{\text{switch}} + P_{\text{cdiv}}}. \tag{31}$$

## ACKNOWLEDGMENT

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