Guest Editorial Special Issue on Circuits and Systems for the Internet of Things—From Sensing to Sensemaking

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THE Internet of Things (IoT) refers to the interconnection of everyday objects endowed with sensing, processing, communication and energy management capabilities [item 1) in the Appendix] (the "IoT nodes"). Being at the beginning of its "S curve" in terms of stage of adoption [item 2) in the Appendix] (see "innovators" in Fig. 1), the IoT promises to be the next big wave that will further raise the technological and economic impact of the semiconductor industry. More than a decade from now, the massive adoption of IoT technologies (see "late majority" in Fig. 1) is expected to expand the number of connected devices per person to the order of a thousand, thus reaching an unprecedented scale of trillions of connected devices [item 3) in the Appendix].

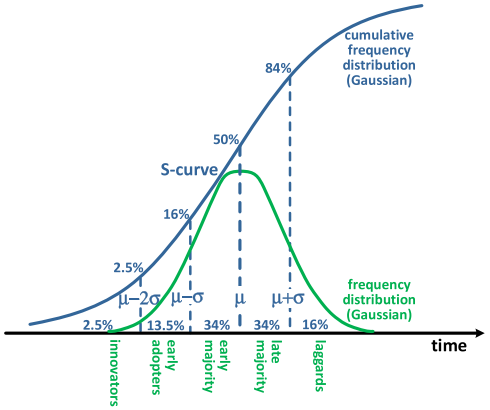

Fig. 1. The S-curve describes the stages of adoption of innovation as cumulative distribution of the time of adoption. The IoT is progressing around the left tail of the curve ("innovators").

I. Trends

In spite of being a recent technological trend, the IoT has its roots on observations made in the late 90s [item 4) in the Appendix], and on the seminal work on the "smart dust" concept a few years before [item 5) in the Appendix], [item 6) in the Appendix], among others. On a broader perspective, the IoT is the natural consequence of long-term trends that have been observed in the related areas of semiconductor economics, technology scaling and consequent trends in terms of size and energy efficiency of compute/processing systems, as well as connectivity. These trends are discussed in the following to provide a long-term view on the evolution of the IoT.

The semiconductor industry has consistently grown fast in the past decades, thus fostering relentless (exponential) cost reduction in integrated systems. According to the learning curve shown in Fig. 2, the cost per transistor has historically decreased to 55% of its original value when doubling the overall number of manufactured transistors, thanks to the efficiency improvements enabled by advances in silicon manufacturing, design and testing [item 1) in the Appendix], [item 7) in the Appendix]. Along with transistor shrinking,

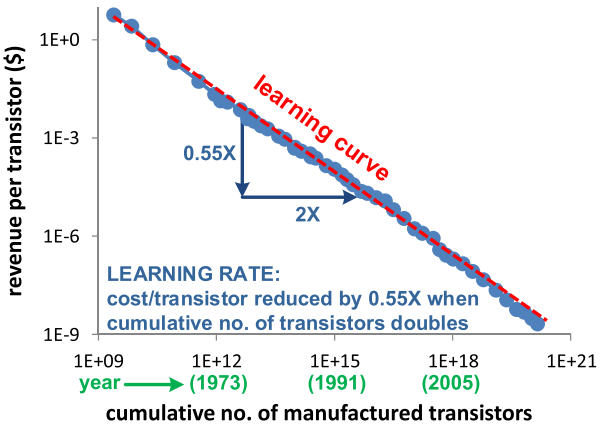

Fig. 2. Continuous improvements in integrated circuit manufacturing, design and testing have led to 0.55X cost reduction per transistor when doubling the number of cumulative number of transistors manufactured.

this cost reduction has fueled the increase of chip complexity as quantified by Moore's law [item 8) in the Appendix], with 2X more transistors per chip every 18-24 months. Consequently, energy efficiency has improved at the pace

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Digital Object Identifier 10.1109/TCSI.2017.2730678

of 2X every 18 months, both in computers (Koomey's law [item 9) in the Appendix]) and Digital Signal Processors (Gene's law [item 10) in the Appendix]). The concurrent increase in the transistor count per silicon die and the power reduction in electronic systems has determined a reduction in the size of computing subsystems at the same pace [item 11) in the Appendix]. This evolution has spurred the mobile era, and is progressively making IoT nodes more pervasive.

Internet connectivity has a fundamental role in IoT, and hence defines a large part of its economic value. According to the popular Metcalfe's law [item 12) in the Appendix], the value of a telecommunication network is proportional to the square of the number of connected users of the system. However, Metcalfe's law does not apply to the IoT since it assumes that all connections bring equal value. This certainly not true in IoT, since many nodes are part of private sub-networks (e.g., in a factory floor), perform mostly unidirectional communication, with lack of interoperability further limiting inter-node communication. Accordingly, the value of IoT will be approximately super-linear with the number of IoT nodes, but certainly slower than a square law. A plausible estimate is Briscoe's law [item 13) in the Appendix], which predicts that the value of very large-scale networks is $n \cdot \log(n)$, being n the number of nodes.

The push and the pull effect of these technological trends are now converging to create a virtuous circle that promises unprecedented benefits to society. Several megatrends are indeed well aligned with the evolution of the IoT. For example, geo socialization, assistive and proactive robotics, data-driven decision making and control, remote physical interaction, participatory sensing and sharing economy require technologies that enable pervasive, efficient and real-time management of shared resources, encouraging their responsible use and create a better match between demand and supply [item 1) in the Appendix]. Furthermore, structured physical data coming from IoT nodes is expected to make artificial intelligence-based decision making more effective, since its computational effort with structured data is estimated to be only logarithmic in the space of decision choices [item 14) in the Appendix].

From a human-centric perspective, IoT will allow effective sharing of scarce resources on a larger scale, and make technology transparent and more user friendly, while delivering services that are more powerful. And we do hope its benefits will trickle down to communities and individuals, thus making advanced technology relevant for better living conditions of the humankind [item 15) in the Appendix].

II. The Challenges Ahead

The vision towards 1 Tera connected IoT nodes supporting planetary-scale applications such as environment monitoring, wellness, resource management and global security, implies extremely miniaturized integrated systems with very long lifetime (e.g., a decade) that are autonomous in many respects, from functionality, to energy, to the way they interact with the physical world and the network infrastructure. This consideration poses severe challenges in the broad area of circuits and systems (see Fig. 3). In particular, requirements

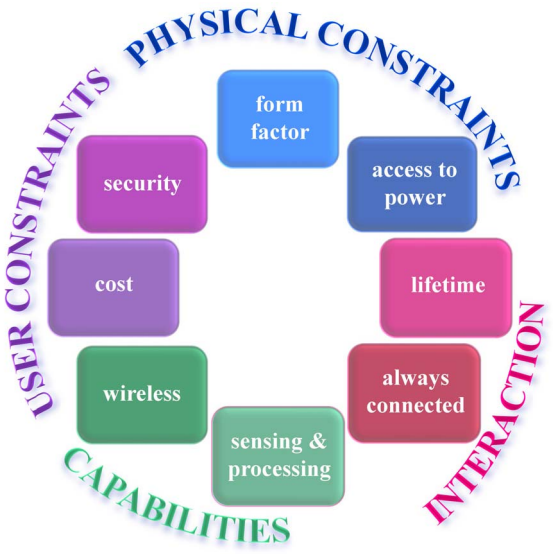
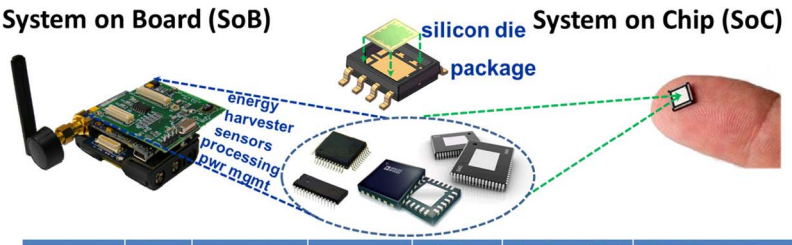


Fig. 3. IoT node requirements [item 1) in the Appendix].

can be clustered according to user constraints, physical constraints, capabilities and interaction [item 1) in the Appendix], [item 16) in the Appendix]. These include: i) the need for unprecedentedly high energy efficiency and low standby power, ii) ultra-low voltage operation and inexpensive resiliency-enhancement techniques, iii) very low cost across the entire chain from design to verification, and manufacturing, iv) systematic over-design margin elimination from the circuit to the application level, v) highly power-efficient circuits for wireless communications, vi) cyber-security assurance down to single chip level despite highly-constrained resources, vii) the need for early extraction of essential information from physical data within the IoT nodes themselves, to enable distributed learning/sensemaking and hence true IoT energy and network scalability.

Unfortunately, we are still far from meeting the node requirements that will make the IoT vision become a reality [item 17) in the Appendix], as summarized in Fig. 4. Due to the gargantuan scale of the IoT, we need to address these challenges through holistic approaches that embrace multiple levels of abstraction (verticality) and building blocks of the on-chip sensing/sensemaking chain (transversality). Nowadays, vertical approaches are progressively becoming more customary to exceed the artificial boundaries created by the levels of abstraction, and enable advances that transcend their traditional limits. On the other hand, more research is needed to devise transversal methods that leverage the interaction within the sensing/sensemaking chain, from analog interfaces to processing, power delivery, wireless communications and HW/SW-level information security, while expanding into systems, data representation and algorithmic frameworks. Novel design methodologies and tools to support this broader view will have to be developed as well [item 18) in the Appendix], [item 19) in the Appendix]. In these respects, and enlarging the domain of IoT considerably, important research has been reported [item 20) in the Appendix].



	size	cost	power	lifetime	design effort	development cost
IoT target	mm	~1$	<1-10μW	5-20yrs	low	low
SoB	5cm	10s-100s$	1-100mW	months	<0.5man-yrs	10-100k$
SoC	mm	1-10$	1-10μW	10yrs	>10man-yrs	5-10M$

Fig. 4. State of the art vs. IoT target, from the IoT database (repository of 150+ commercial IoT nodes, Sensor Hubs and MicroController Units) – available at http://www.green-ic.org/iotdb.

III. Content of This Special Issue

This special issue intends to represent the state of the research on IoT that addresses some of the challenges presented above. Four invited papers open the issue. All other papers are organized around seven thematic areas that span from sensing to sensemaking, to applications: i) analog and sensors, ii) power conversion and harvesting, iii) processing and memories, iv) architectures and sensemaking, v) security, vi) wireless communications, and vii) applications. These sections cover research on sub-systems that are typically present in any IoT node. The application part offers a view on how IoT nodes can be leveraged in several industrial domains. An overview of the content of the papers in this special issue is presented below, with most of the papers presenting experimental demonstration.

A. Invited Papers

The invited paper by De Micheli from EPFL presents an overview and a vision on how many-sensor cyber-medical systems will redesign healthcare, diagnostics and drug administration. The invited paper by Jang *et al.* from the University of Michigan - Ann Arbor is organized into two parts, and gives an overview of techniques for aggressive IoT node miniaturization, using a GNSS logger as a case study. The invited paper by Li *et al.* from Stanford explores memory-centric computing, and the opportunities that 3D resistive RAMs offer in terms of energy efficiency, and promising endurance for IoT applications. Experimental demonstrations are also presented in all above papers.

1) Analog and Sensors: The contribution by Wang *et al.* from University of California at San Diego presents the design of an ultra-low power CMOS temperature sensor for use in environmental monitoring, using a current-to-time converter and a time-to-digital converter in 0.18μm. The paper by Wang *et al.* from the University of Washington presents an always-on comparator capable of detecting mV-range voltage signals while consuming sub-nW power. The paper by Ko *et al.* from Georgia Tech presents a single-chip image sensor node with embedded energy harvesting, having the ability to perform moving object detection in situ, thus reducing the wireless communication power. The contribution by Duarte *et al.* from Universidade Federal do Rio de Janeiro and the Universidad de Sevilla introduces image sensors with in-sensor processing, embedding per-pixel pre-processing structures for Gaussian spatial filtering. The contribution by Bellasi *et al.* from the University of Bologna introduces an energy-efficient all-digital frequency-lock loop for generic IoT nodes, as demonstrated at both 65nm and 28nm.

2) Power Conversion and Harvesting: The paper by Rawy *et al.* from Nanyang Technological University introduces an ultra-low power maximum power point tracking circuit in 65nm with a wide tracking range. In the contribution by Wan et al. from the Hong Kong University of Science and Technology, reconfigurable arrays of thermoelectric generators are explored to achieve maximum power point tracking over a wide range of temperature gradients, as experimentally demonstrated in 0.35μm. The paper by Mondal *et al.* from IIT Guwahati introduces an efficient micro-scale solar power management architecture, as demonstrated in 0.18μm. The paper by Savanth et al. from the University of Southampton presents an energy harvesting system using reciprocal power conversion, and avoiding conventional redundancy by using bidirectional power conversion, as demonstrated in 65nm. The paper by Gharehbaghi *et al.* from the Middle East Technical University discussed the modeling and the optimization of threshold self-compensated rectifiers.

3) Processing and Memories: The contribution by Bonetti *et al.* from EPFL and STMicroelectronics introduces run-time quality-scalable multipliers in FIR filters demonstrated in 28nm, and an optimization methodology to dynamically trade off quality and energy. The paper by Na *et al.* from Georgia Tech provides a methodology to couple clock and data-path voltage variations to mitigate pessimism in the estimated timing slack of digital circuits, and improve their energy efficiency. The paper by Le *et al.* from the University of Illinois at Urbana-Champaign explores guided-processing as an approach that overcomes the limits of conventional duty cycling in terms of energy efficiency, and related the tradeoff between energy and false-alarm and miss rate. The contribution by Abu Lebdeh *et al.* from Khalifa University introduces memristor-based logic that is efficiently mapped into memristive crossbar memories, with benefits in terms of energy latency and area, compared with conventional implementations. The paper by Grover *et al.* from

STMicroelectronics and LETI investigates the opportunities offered by the co-design of cell, assist schemes and the layout to achieve wide voltage range operation in SRAMs, as experimentally demonstrated in 28nm FDSOI technology.

4) Architectures and Sensemaking: The contribution by Duch *et al.* from EPFL and USI is focused on wireless body sensor nodes, and introduces a computing architecture for ultra-low power processing of bio-signals. The paper from Strauch *et al.* from EDAptix introduces a solution for virtual peripherals to allow adaptation to multiple interfaces and wider inter-operability. The contribution by Cao *et al.* from Georgia Tech explores in-situ data analytics in energy-constrained imaging sensor nodes for context-aware acquisition and processing, to make wireless communication infrequent and mitigate its impact on the node average power. The paper by Conti *et al.* from ETH and University of Bologna explores tightly-coupled multi-core cluster architecture augmented with specialized blocks for energy-efficient near-sensor data analytics. The contribution by Zhou *et al.* from Texas A&M University explores level crossing sampling (LCS) for power-efficient analog-to-digital conversion in spike-like signals, and related data compression with enhanced robustness against wireless interference.

5) Security: The paper by Chung *et al.* from the National Chiao Tung University introduces countermeasures to power analysis attacks to address the related security threats of IoT nodes performing stream cipher-based encryption. The paper by Gao *et al.* from the University of Adelaide investigates PUF sensors and a communication protocol that counteracts eavesdropping and detects man-in-the-middle manipulation of the sensed value, for secure distributed sensing. The contribution by Lara-Nino *et al.* from CINVESTAV investigates lightweight symmetric ciphers for extremely constrained environments.

6) Wireless Communications: The contribution by Mcallister *et al.* from the Institute of Electronics, Communications and Information Technology presents a variant of Selective Spanning Fast Enumeration, using fast symbol enumeration and other techniques that increase performance without significantly affecting accuracy. The contribution by Chi *et al.* from Tsinghua University discusses a NB-IoT wireless transceiver using a digital polar architecture. The paper by Angelopoulos *et al.* from MIT investigates random linear network coding for improved utilization of network resources, and related chip demonstration.

7) Applications: The paper by Chiang *et al.* from National Chia Yi University introduces a monitoring CMOS seawater salinity device for fish farming. The paper by Shrivastava *et al.* from University of Virginia and Northeastern University addresses the challenge to enable long-lifetime systems-on-chip through highly efficient energy harvesting circuits that are able to extract power starting from very low voltages. The paper by Huang *et al.* from the University of California at Berkeley introduces a bio-inspired front-end for olfactory sensory systems encompassing feature extraction, learning, and recognition. The contribution by Yasin *et al.* from New York University and Khalifa University of Science and Technology and Research discusses an ultra-low power and secure IoT sensing and pre-processing platform for predicting ventricular arrhythmia using ECG signals.

ACKNOWLEDGEMENTS

This special issue would not have been possible without the contribution of many people. First, the authors are indebted with the hundreds of reviewers who have contributed to make this special issue a reality and the abundant submissions neatly manageable. The authors are also grateful to the TCAS-I Editor-in-Chief Prof. Andreas Demosthenous and the Deputy Editor-in-Chief Prof. Eduardo da Silva for their constant and highly responsive support. Also, the authors thank Leigh Ann Testa for her tireless support on the submission and review cycle management.

APPENDIX
RELATED WORK

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He has authored or co-authored over 230 publications on journals and conference proceedings. One of them is the second most downloaded TCAS-I paper in 2013. He has co-authored three books from Springer, including the *Enabling the Internet of Things-From Integrated Circuits to Integrated Systems* (2017). His primary research interests include ultra-low power VLSI circuits, self-powered and wireless nodes, near-threshold circuits for green computing, energy-quality scalable VLSI circuits, circuit techniques for emerging technologies, and hardware-level security, among the others.

From 2009 to 2010, he was a Distinguished Lecturer of the IEEE Circuits and Systems Society, for which he is/was also member of the Board of Governors from 2015 to 2017, and the Chair of the VLSI Systems and Applications Technical Committee from 2010 to 2012. He served as guest editor of various journal special issues. He currently serves as an Associate Editor-in-Chief of the IEEE TRANSACTIONS ON VLSI SYSTEMS. He also serves as an associate editor of a number of journals. He was the Technical Program Chair for ICECS, VARI, NEWCAS, ICM, PRIME, SOCC, and the Track Chair in a number of conferences such as the ICCD, ISCAS, ICECS, VLSI-SoC, APCCAS, and ICM.

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