A 33fJ/Step SAR Capacitance-to-Digital Converter Using a Chain of Inverter-Based Amplifiers

Hesham Omran, Abdulaziz Alhoshany, Hamzah Alahmadi, and Khaled N. Salama, *Senior Member, IEEE*

***Abstract*— A $12-bit$ energy-efficient capacitive sensor interface circuit that fully relies on capacitance-domain successive approximation (SAR) technique is presented. Analysis shows that for SAR capacitance-to-digital converter (CDC) comparator offset voltage will result in parasitic-dependent conversion errors, which necessitates using an offset cancellation technique. Based on the presented analysis, a SAR CDC that uses a chain of cascode inverter-based amplifiers with near-threshold biasing is proposed to provide robust, energy-efficient, and fast operation. A hybrid coarse-fine capacitive digital-to-analog converter (CapDAC) achieves $11.7-bit$ effective resolution, and provides 83% area saving compared to a conventional binary weighted implementation. The prototype fabricated in a $0.18\mu m$ CMOS technology is experimentally verified using MEMS capacitive pressure sensor. Experimental results show an energy efficiency figure-of-merit (FoM) of $33fJ/Step$ which outperforms the state-of-the-art. The CDC output is insensitive to analog references; thus, a very low temperature sensitivity of $2.3ppm/°C$ is achieved without the need for calibration.**

***Index Terms*— Capacitance-to-digital converter (CDC), capacitive sensor interface circuit, capacitor array, CMOS, energy-efficient, low-power, MEMS pressure sensor readout circuit, successive-approximation (SAR).**

I. Introduction

ENERGY efficiency is a key requirement for wireless sensor nodes, biomedical implants, and wearable devices [1], [2]. The energy consumption of the sensor node needs to be minimized to avoid battery replacement, or even better, to enable the device to survive on energy harvested from the ambient. Capacitive sensors do not consume static power; thus, they are attractive from an energy efficiency perspective. In addition, they can be used in a wide range of applications, such as pressure sensing [3], displacement sensing [4], flow sensing [5], humidity sensing [6], and chemical sensing of volatile organic compounds (VOCs) [7], [8], which can be used as biomarkers for non-invasive lung cancer detection [9].

Manuscript received March 19, 2016; revised July 25, 2016 and August 22, 2016; accepted September 9, 2016. Date of publication November 15, 2016; date of current version January 26, 2017. This work was supported by King Abdullah University of Science and Technology (KAUST) and by KAUST Advanced Membranes and Porous Materials Center (AMPMC) under grant FCC/1/1972-05-01. This paper was recommended by Associate Editor Z. Tan.

H. Omran is with the Integrated Circuits Lab, Faculty of Engineering, Ain Shams University, Cairo 11566, Egypt (e-mail: hesham.omran@eng.asu.edu.eg).

A. Alhoshany, H. Alahmadi, and K. N. Salama are with King Abdullah University of Science and Technology (KAUST), Computer, Electrical and Mathematical Science and Engineering Division (CEMSE), Thuwal 23955-6900, Saudi Arabia (e-mail: abdulaziz.alhoshany@kaust.edu.sa; hamzah.alahmadi@kaust.edu.sa; khaled.salama@kaust.edu.sa).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TCSI.2016.2608905

Typically, the wireless transceiver is the most power-hungry block in a sensor node; however, it is only operated for a short time at distant intermittent time intervals to transmit aggregate data. On the other hand, the sensor readout circuit is more frequently operated for a longer time to acquire and digitize measurements; thus, its energy consumption can be significantly larger. For instance, an implantable intraocular pressure monitoring system for glaucoma patients is reported in [2], where the capacitive pressure sensor readout circuit, i.e., the capacitance-to-digital converter (CDC), consumes 93% of the active energy consumption. Thus, optimizing the CDC energy efficiency is crucial to optimizing the energy consumption of capacitive sensor nodes.

Conventionally, a CDC is implemented by converting the sensor capacitance to an analog voltage and then digitizing the voltage using an analog-to-digital converter (ADC). The ADC can be implemented with minimal analog components and very low power dissipation [10], [11]. However, signal conditioning and buffering stages preceding the ADC typically use OTAs; thus, they can be more complex and more power-consuming than the ADC itself [12]–[15]. On the other hand, recent implementations favor direct digitization of the sensor capacitance, where the sensor is integrated in the ADC architecture to perform direct capacitance-to-digital conversion [6], [16]–[24]. In a semi-digital CDC approach, the capacitance is converted to a time-domain parameter of a digital signal [16]–[18], e.g., period modulation [16]. However, the time-modulated signal needs to be digitized using a time-to-digital converter, e.g., a fast digital counter and a high frequency stable reference clock, which results in increased power consumption. Another approach is to use $\Sigma\Delta$ CDCs, which can provide fine absolute resolution [4], [6]; however, $\Sigma\Delta$ CDCs suffer from limited capacitance range and use power-hungry OTAs running at a relatively fast oversampling clock.

ADCs that employ successive approximation register (SAR) technique are well known for their excellent energy efficiency [10], [11]. A SAR CDC that resembles a conventional low-power SAR ADC was proposed in [25]; however, the comparator offset voltage results in parasitic-dependent conversion errors, as will be shown in Section II. A SAR CDC architecture that addresses the offset error limitation was proposed in [21]; however, it uses an OTA that dominates the power consumption, and degrades the energy efficiency. An energy-efficient SAR CDC that uses an inverter-based OTA was proposed in [24]; however, it requires the use of two matched capacitive sensing elements, suffers from static power consumption, and does not fully address the offset error limitation.

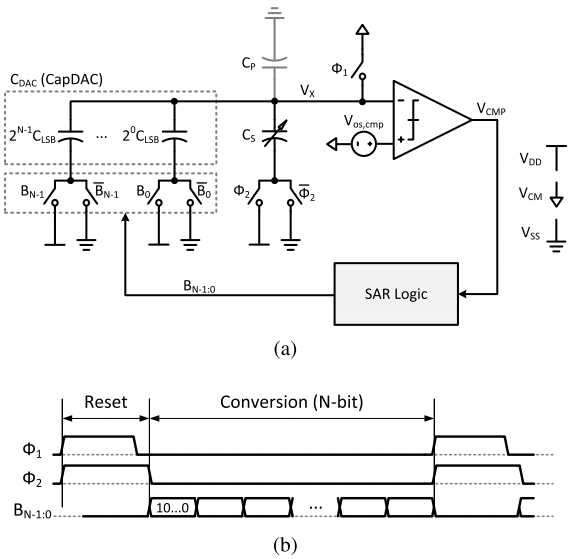


Fig. 1. (a) Schematic of conventional SAR CDC. C_S is the sensor capacitor, C_{DAC} is a binary weighted CapDAC, and C_P is a parasitic capacitor. (b) Timing and operation phases of SAR CDC.

In this work, we propose an energy-efficient CDC that fully relies on SAR algorithm while providing both robust operation and excellent energy efficiency. The proposed CDC employs a chain of energy-efficient cascode inverter-based amplifiers to fully overcome offset-induced errors with a minimum impact on power consumption. Near-threshold biasing and a dynamic comparator are used to minimize static power consumption. The CDC is optimized and implemented in a $0.18\mu m$ CMOS technology and achieves an energy efficiency figure-of-merit (FoM) of $33fJ/Step$, which is the best reported FoM to the best of the authors' knowledge. The CDC output is insensitive to analog references, resulting in a very low temperature sensitivity of $2.3ppm/°C$ without the need for calibration. In addition, we analyze the contributions of different noise sources, and discuss the resolution limitations due to both thermal noise and mismatch.

The rest of the paper is organized as follows. Section II discusses the operation and the limitations of a conventional SAR CDC. Section III describes and analyzes the proposed SAR CDC. Section IV discusses the mismatch-limited resolution and the implementation of the CapDAC. Section V presents measurement results. Finally, Section VI concludes the paper.

II. Successive Approximation CDC

A. Circuit Operation

The schematic of a conventional SAR CDC is shown in Fig. 1 a, where C_S is the unknown sensor capacitor, C_{DAC} is a reference capacitor implemented as an $N-bit$ binary weighted CapDAC, and C_P models the parasitic capacitance. C_S, C_{DAC}, and C_P are typically in the picofarad range. The circuit operation is divided into two phases as shown in Fig. 1 b. During the reset phase, the charge stored is given by

$$Q_1 = C_S\left(V_{CM} - V_{DD}\right) + C_{DAC}V_{CM} + C_P V_{CM}. \quad (1)$$

Next, in the conversion phase, V_X is floating, the bottom plate of C_S is connected to V_{SS}, and the bottom plates of C_{DAC} elements are either connected to V_{DD} or V_{SS} depending on the SAR logic output ($B_{N-1:0}$). The equivalent capacitance of the elements connected to V_{DD} and V_{SS} are denoted as $C_{DAC,ON}$ and $C_{DAC,OFF}$, respectively. The charge stored in this phase is given by

$$\begin{aligned} Q_2 = {} & C_S V_X + C_{DAC,ON}\left(V_X - V_{DD}\right) \\ & + C_{DAC,OFF}V_X + C_P V_X. \end{aligned} \quad (2)$$

Since charge is conserved, from (1) and (2), the differential voltage at the comparator input terminals (ΔV) can be written as

$$\Delta V = \frac{C_S - C_{DAC,ON}}{C_{IN}} \cdot V_{DD} + V_{os,cmp} \quad (3)$$

where $V_{os,cmp}$ is the comparator offset voltage, and C_{IN} is the total input capacitance connected to V_X, i.e., $C_{IN} = C_S + C_{DAC} + C_P$. Equation (3) can be rewritten as

$$\Delta V = \frac{(C_S + C_{err}) - C_{DAC,ON}}{C_{IN}} \cdot V_{DD}, \quad (4)$$

where C_{err} is the capacitance conversion error due to offset voltage and is given by

$$C_{err} = \frac{V_{os,cmp}}{V_{DD}} \cdot C_{IN}. \quad (5)$$

Based on the comparator output (V_{CMP}), the logic in the feedback loop uses SAR algorithm to change C_{DAC} till ΔV is minimized–that is, until $C_{DAC,ON}$ is matched to $(C_S + C_{err})$ within the resolution of the smallest unit capacitor in the CapDAC (C_{LSB}), i.e., the least significant bit (LSB).

B. Offset Error Limitation

As given by (5), the comparator offset voltage manifests itself as a conversion error that is a function of C_S, C_P, and V_{DD}. In order to limit the conversion error to one LSB, the peak-to-peak value of C_{err} needs to be less than C_{LSB}. Hence, noting that $V_{os,cmp}$ is a statistical variable, for a three-sigma yield of 99.73%, the condition satisfying this requirement is

$$C_{LSB} > \frac{6V_{os,rms}}{V_{DD}} \cdot C_{IN}, \quad (6)$$

where $V_{os,rms}$ is the rms offset voltage.

Generally, C_S is an off-chip capacitive sensor; thus, node V_X is associated with a large parasitic capacitance due to the pads and the bondwire [26], in addition to the parasitic capacitance of the CapDAC elements. Assuming that the interface is required to handle a parasitic capacitance as large as the full-scale sensor capacitor (C_{FS}), the maximum input capacitance is $C_{IN,max} \approx 3C_{FS}$. Thus, substituting in (6), the offset-limited achievable resolution (R) in bits can be written as

$$R = \log_2 \frac{C_{FS}}{C_{LSB}} < \log_2 \frac{V_{DD}}{V_{os,rms}} - 4.17, \quad (7)$$

where it can be noticed that the achievable resolution is very poor especially for low supply voltage, e.g., only $\approx 4.8 - bit$ resolution is achievable for $V_{os,rms} = 2mV$ and $V_{DD} = 1V$.

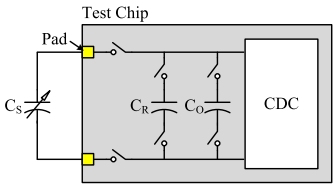


Fig. 2. Schematic of the two-point calibration circuit used to cancel gain and offset errors.

Another way to handle the conversion error given by (5) is to divide it into three components: the component proportional to C_S is then treated as a gain error, and the component proportional to C_{DAC} is treated as an offset error. In order to cancel these gain and offset errors, a two-point auto-calibration scheme can be used as shown in Fig. 2 [16]. On-chip switches are used to facilitate the performance of the following three measurements: $(C_S + C_O)$, $(C_R + C_O)$, and C_O, where C_R and C_O are on-chip reference capacitors. The ideal ratiometric output (μ_{ideal}) is then given by

$$\mu_{ideal} = \frac{(C_S + C_O) - C_O}{(C_R + C_O) - C_O} = \frac{C_S}{C_R}. \tag{8}$$

When $V_{os,cmp}$ is considered, the ratiometric output (μ) is approximately given by

$$\mu \approx \frac{C_S}{C_R}\left(1 + \frac{V_{os,cmp}}{V_{DD}}\left(\frac{C_{P1} - C_{P3}}{C_S} - \frac{C_{P2} - C_{P3}}{C_R}\right)\right), \tag{9}$$

where C_{P1}, C_{P2}, and C_{P3} are the parasitic capacitors associated with the three aforementioned measurements, respectively.

Equation (9) reveals that the gain and offset errors due to C_S and C_{DAC} will be canceled; however, the third error component due to C_P will not be canceled, because the parasitic capacitance associated with each measurement is different. Moreover, C_P constitutes parasitic capacitances of the switches, IO pad, and ESD circuitry, which are not stable. In addition, the off-chip parasitic capacitance can drift due to humidity, mechanical stress, and temperature [27]. Besides, the price paid for the calibration is tripling the conversion time: i.e., a three-fold degradation in energy efficiency.

Digital offset compensation techniques can be used to reduce the offset of a low-power dynamic comparator; however, the residual offset voltage can still be as large as several millivolts [28], [29]. In order to overcome this offset error limitation, it is necessary to use an analog offset cancellation technique [30]. Since a large input capacitance already exists, input offset storage can be used where the offset voltage is stored on the input capacitance during the reset phase (i.e., auto-zeroing), as will be discussed in the following section.

III. SAR CDC Using Inverter-Based Amplifier

A. Circuit Operation

The schematic of the proposed $12-bit$ SAR CDC is shown in Fig. 3 and the timing diagram is shown in Fig. 4. The circuit uses a chain of identical inverters, where the first inverter (I1) acts as a preamplifier with offset cancellation, and the remaining inverters (I2 to I5) act as open-loop preamplifiers for a dynamic latch comparator. An inverter-based amplifier is inherently energy-efficient because both the PMOS and NMOS transistors contribute to the transconductance; thus, for the same bias current, the transconductance of the amplifier, and consequently the energy efficiency, is doubled [6], [31], [32].

During the reset phase, only the first inverter stage (I1) is enabled, Φ_1 is HIGH (i.e., the feedback switch is closed), and both V_X and V_{OUT} are equal to the switching threshold of I1(V_{M1}), not to be confused with the transistor threshold voltage. The inverter switching threshold (V_M) is the trip-point voltage at the middle of the inverter transfer characteristics. The inverter built-in V_M replaces the common mode voltage (V_{CM}) that is used in Fig. 1(a). The switching threshold of I1(V_{M1}) is stored on the input capacitance; thus, the offset voltage of the first inverter stage is canceled (i.e., auto-zeroing).

During the conversion phase, the remaining inverter stages (I2 to I5) are enabled, the feedback switch is open, and the stored charge is redistributed according to the CapDAC digital input. Applying charge conservation, the output of I1 is

$$V_{OUT1} = V_{M1} + \frac{C_S - C_{DAC,ON}}{C_{IN}/A_o} \cdot V_{DD}, \tag{10}$$

where A_o is the open-loop gain of the inverter-based amplifier. The delta input of I2 is the deviation of V_{OUT} from the switching threshold of I2(V_{M2}); thus, it is given by

$$\Delta V = \frac{(C_S + C_{err}) - C_{DAC,ON}}{C_{IN}/A_o} \cdot V_{DD}, \tag{11}$$

where the capacitance conversion error (C_{err}) is given by

$$C_{err} = \frac{V_{os}}{V_{DD}} \cdot \frac{C_{IN}}{A_o}, \tag{12}$$

where in this case the offset voltage (V_{os}) is equal to $(V_{M1} - V_{M2})$, i.e., the residual offset voltage is the mismatch between the switching thresholds of I1 and I2. The mismatch in the switching thresholds of subsequent inverter stages is not important as the signal will be already amplified by I1 and I2. In contrast to (5), the conversion error given by (12) is a function of the gain of the inverter; thus, the inverter gain is the design knob that can be used to achieve the required resolution.

Equation (12) shows that the conversion error is still dependent on the sensor and parasitic capacitance. However, by properly selecting the inverter gain, the required conditions on C_{err} can be satisfied. To limit the peak-to-peak value of C_{err} to one LSB, the condition on the amplifier open-loop gain for a three-sigma yield is given by

$$A_o > \frac{18V_{os,rms}}{V_{DD}} \cdot 2^R. \tag{13}$$

Monte Carlo simulation of the switching threshold mismatch is shown in Fig. 5(a), where the rms offset voltage ($V_{os,rms}$) is $\approx 2mV$. For $R = 12 - bit$, $V_{DD} = 0.8V$, and $V_{os,rms} = 2mV$, the minimum required gain is $\approx$ 185. In order to satisfy this requirement, the gain of the inverter is increased by implementing each inverter in the chain as a cascode stage

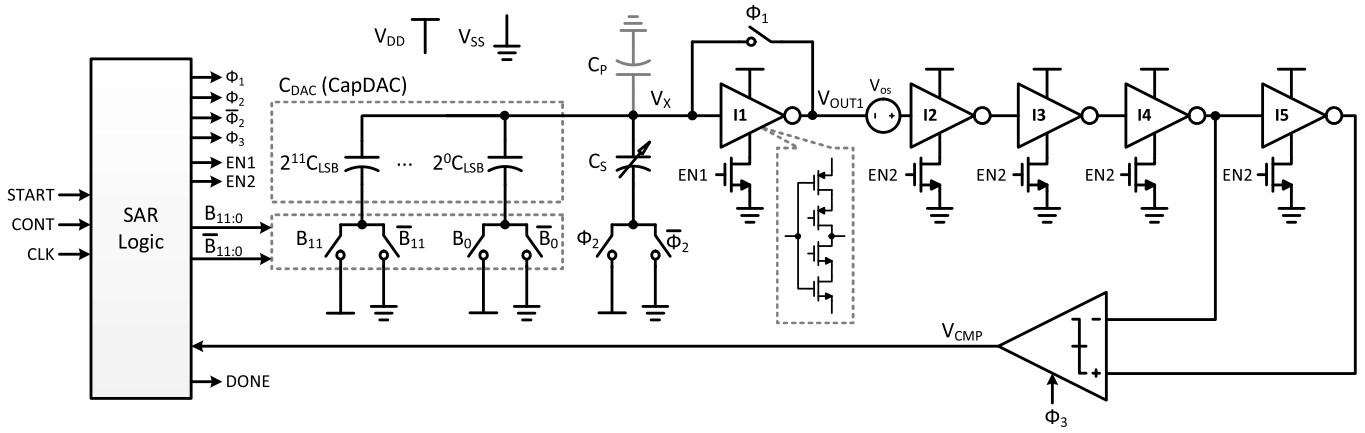


Fig. 3. Schematic of the proposed SAR CDC.

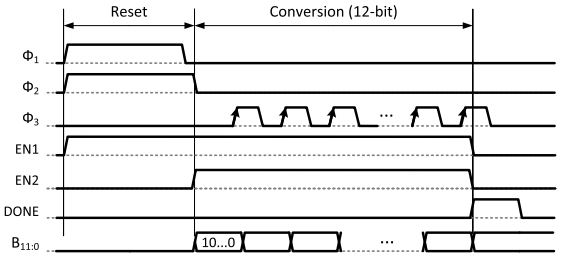


Fig. 4. Timing diagram and operation phases of the proposed SAR CDC.

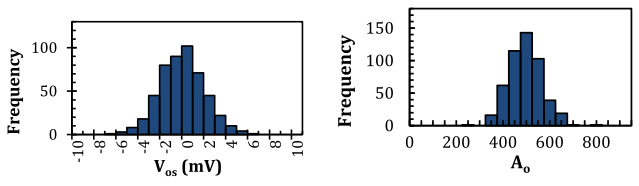


Fig. 5. (a) Histogram of 500 MC simulation runs of inverter switching threshold mismatch, i.e., V_{os}. The standard deviation ($V_{os,rms}$) is $\approx 2mV$. (b) Histogram of 500 MC simulation runs of inverter open-loop DC gain (A_o). The mean value is ≈ 471 and the standard deviation is ≈ 70.

as shown in the inset in Fig. 3. Monte Carlo simulation of the inverter gain is shown in Fig. 5(b), where the nominal gain is $\approx$471 and the standard deviation is ≈ 70; thus, the minimum gain requirement is achieved with a sufficient margin under process variations.

B. Noise Analysis

For the purpose of noise analysis, the inverter-based amplifier is modeled as a single transconductance stage, with a transconductance of G_m and an output-pole $\omega_p = \frac{1}{R_{OUT}C_{OUT}}$. To simplify the analysis, it is assumed that $C_{IN} \gg C_{OUT}$, $A_o = G_m R_{OUT} \gg 1$, and $R_{OUT} \gg R_{ON}$, where R_{ON} is the switch ON resistance. Several noise sources contribute to the total noise, namely, (1) the feedback reset switch, (2) the switches associated with C_S, (3) the switches associated with the CapDAC, and (4) the amplifier. First, noise power from the reset switch ON resistance is sampled and stored in C_{IN} when the switch is opened. Using nodal analysis to solve for $v_X(s)$ yields

$$v_X(s) \approx \frac{i_n R_{ON}}{G_m R_{OUT}} \cdot \frac{1-\frac{s}{s_z}}{\left(1-\frac{s}{s_{p1}}\right)\left(1-\frac{s}{s_{p2}}\right)} \tag{14}$$

where $i_n^2(f) = \frac{4kT}{R_{ON}}$, $s_z \approx -\frac{1}{R_{OUT}C_{OUT}}$, $s_{p1} \approx -\frac{G_m}{C_{IN}}$, and $s_{p2} \approx -\frac{1}{R_{ON}C_{OUT}}$, k is the Boltzmann constant, and T is the temperature in Kelvin. The input-referred mean-square (MS) noise voltage due to the feedback switch ON resistance is then given by

$$v_{n1,rms}^2 \approx \frac{kTC_{OUT}}{C_{IN}^2}. \tag{15}$$

Second, the noise due to C_S switches is divided into two components, where the first component is the sampled noise when the reset switch is opened and the second component is the voltage noise generated during the conversion phase. By assuming that $C_{IN} \gg C_S$, it can be shown that a pessimistic estimate of the MS noise voltage is given by

$$v_{n2,rms}^2 \approx \frac{kTC_S^3}{C_{IN}^4} + \frac{kTR_{ON}\omega_p C_S^2}{C_{IN}^2}. \tag{16}$$

Third, the MS noise voltage due to the CapDAC switches is similarly given by

$$v_{n3,rms}^2 \approx \frac{kTC_{FS}^3}{C_{IN}^4}\sum_{i=1}^{N}\left(\frac{1}{2^{3i}}\right) + \frac{kTR_{ON}\omega_p C_{FS}^2}{C_{IN}^2}\sum_{i=1}^{N}\left(\frac{1}{2^{2i}}\right), \tag{17}$$

where the two summations converge to $1/7$ and $1/3$, respectively, for $N \to \infty$. Fourth, the amplifier noise is sampled and stored in C_{IN} when the reset switch is opened. An additional noise component is generated during the conversion phase. The MS output noise voltage due to these two components is given by

$$v_{n4,rms}^2 \approx kT\gamma\left(\frac{1}{C_{IN}} + \frac{\omega_p}{G_m}\right), \tag{18}$$

where γ is a noise parameter equal to $2/3$ for a long channel device.

The previous analytical expressions were verified using Cadence Spectre transient noise simulations. The noise can be transferred to the capacitance-domain noting that $\Delta V = \frac{\Delta C}{C_{IN}} \cdot V_{DD}$; thus the total MS capacitance noise is given by

$$C^2_{nt,rms} \approx \left(\frac{C_{IN}}{V_{DD}}\right)^2 \sum_{i=1}^{4} v^2_{ni,rms} \tag{19}$$

The maximum noise occurs at $C_S = C_{FS}$ and $C_{IN} = C_{IN,max} \approx 3C_{FS}$. Thus, the maximum MS noise is given by

$$C^2_{nt,rms,max} \approx \frac{kTC_{FS}}{V^2_{DD}} \left[3\gamma + \omega_p C_{FS} \left(\frac{4}{3} R_{ON} + \frac{9\gamma}{G_m}\right)\right] \tag{20}$$

For an energy efficient design, the noise is dominated by the amplifier rather than the switch ON resistance [33], i.e., $\frac{4}{3} R_{ON} \ll \frac{9\gamma}{G_m}$. Thus, $C^2_{nt,rms,max}$ is approximately given by

$$C^2_{nt,rms,max} \approx \frac{3kT\gamma C_{FS}}{V^2_{DD}} \left(1 + \frac{3\omega_p C_{FS}}{G_m}\right). \tag{21}$$

Substituting in (21) with the parameters of the implemented prototype ($V_{DD} = 0.8V$, $C_{FS} = 12.66pF$, $C_{LSB} = 3.75fF$, $\omega_p = 1Mr/s$, and $G_m = 150\mu S$) yields $C_{nt,rms,max} = 0.45fFrms$. The total noise from Spectre transient noise simulation results is $0.47fFrms$ which is quite close to the analytical value given the approximations put forward. The rms quantization noise is equal to $C_{LSB,rms} = \frac{C_{LSB}}{\sqrt{12}} = 1.1fFrms$; thus, the thermal noise is less than the quantization noise, i.e., the design is quantization noise-limited. This result was experimentally verified as will be shown in Section V. In order to avoid performance loss due to supply noise, the inverter-chain needs to be powered by a low-noise LDO. The sensitivity to supply noise can be mitigated by using a differential architecture.

C. Design Trade-Offs and Details

The inverter-based amplifier determines the noise, power consumption, and speed of the proposed CDC. The design of the amplifier is affected by several trade-offs. Minimum channel length (L) offers best energy efficiency and highest speed; however, it is not possible to achieve the gain requirement with minimum L, even while using cascode. In addition, the flicker noise of the NMOS transistor is excessive for small L. Increasing the width (W) improves the performance at the expense of increased power consumption and parasitics. Lower supply voltage gives better energy efficiency; however, it results in sharp degradation in speed [34]. Although the physical signals of interest are typically slowly varying, e.g., intraocular pressure, operation at a very low speed—i.e., long conversion time—has several drawbacks. First, the circuit operation relies on the charge stored at V_X; thus, it can be affected by leakage currents. Second, slow conversion time can result in conversion errors if the capacitive sensor (C_S) changes during conversion. Third, the circuit will be more prone to the effects of low-frequency noise, drifts, and variations. In addition, lower supply voltage will make the circuit more sensitive to offset voltage and noise. For a

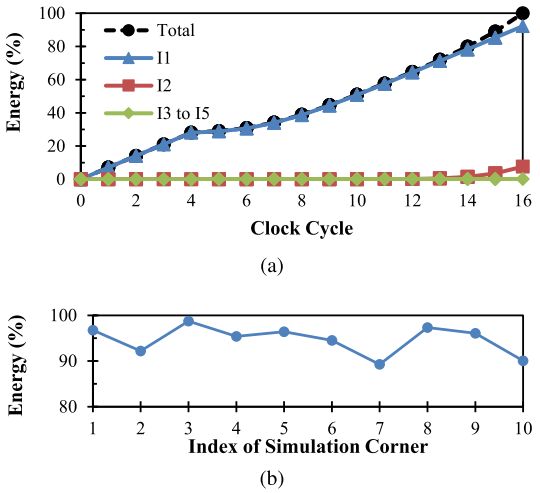


Fig. 6. (a) Energy consumed in I1 to I5 as a percent of the total energy consumption of the inverter chain, calculated from Spectre transient simulation results. The first four clock cycles are dedicated to the reset phase, followed by twelve clock cycles in the conversion phase. (b) Percent of energy consumed in I1 at different simulation corners.

compromise between energy efficiency and speed, the inverters should be biased at $V_{DD} \approx 0.8V$, such that each transistor is biased near its threshold voltage [31], [34], where the transistors are sized such that $V_M \sim V_{DD}/2$ and the transistor threshold voltage is $\approx 0.4V$. In order to address these design trade-offs, transistor sizing and V_{DD} were determined using Cadence ADE GXL global optimization with the following criteria: (1) achieving the gain requirement, (2) circuit noise less than the quantization noise, (3) clock period of $1\mu s$, and (4) maximum energy efficiency (minimum FoM). The optimization results confirmed the selection of $V_{DD} = 0.8V$.

Conceptually, only one inverter stage (I1) can be used, where the two inputs of the dynamic comparator are connected to the input and output of I1. However, the voltage change at the input and output of I1 is quite small (few millivolts or less); thus, it can be disturbed by the kickback noise of the dynamic comparator which can be as large as 10s of millivolts. Therefore, in order to protect these sensitive nodes, at least three inverter stages are required. A total of five inverter stages were used in the implemented prototype to provide more gain and reduce the probability of metastability, where the additional stages (I2 to I5) have minor impact on energy consumption and speed. As illustrated in Fig. 6(a), during the reset phase (first four clock cycles), the energy consumed in $I1$ increases at its maximum rate, while $I2$ to $I5$ are disabled. Next, in the conversion phase, $I1$ energy gradually increases at an accelerating rate, as V_X is successively approximated towards V_{M1}. By virtue of near-threshold biasing, either the pull-up or the pull-down transistors in $I2$ and the subsequent stages will be biased in the subthreshold region and thus dissipate negligible current. The energy consumed in $I1$ is $\gtrsim 90\%$ of the total energy consumed in the inverter-chain at different simulation corners as shown in Fig. 6(b).

Fig. 7(a) shows the worst case delay in the inverter chain when the output of I1 changes from zero to $V_{M1} + \frac{LSB}{2}$, where it is clear that the effect of I2 to I5 on speed is neg-

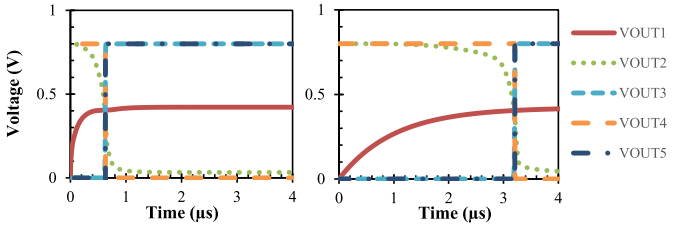


Fig. 7. Worst case delay transient simulation results for (a) inverter-based amplifier non-linear settling and (b) ideal linear settling. V_{OUT1} to V_{OUT5} are the outputs of the five stages in the chain.

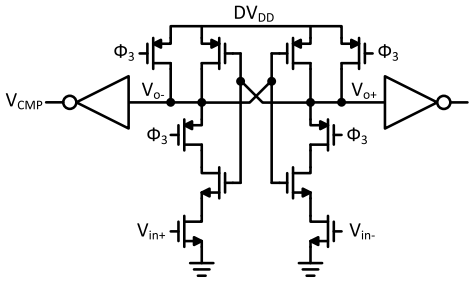


Fig. 8. Schematic of the dynamic latch comparator (level-shifter).

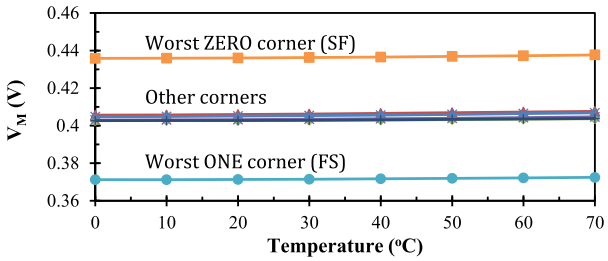


Fig. 9. Simulation result showing the variation of the inverter switching threshold (V_M) vs. temperature at different process corners.

ligible because they are biased by a larger overdrive voltage. Fig. 7 compares the non-linear settling behavior of the inverter with the linear settling of an ideal transconductance stage that has the same gain and bandwidth, where it can be seen that the inverter-based amplifier offers $\sim 5\times$ improvement in speed. The output of I5 is strong enough to drive digital logic. However, a higher digital supply voltage is used ($1.2V$) in order to decrease the ON resistance of the switches; thus, a dynamic comparator (shown in Fig. 8) is still used to act as a level-shifter (as seen in Fig. 3).

The comparator decision depends only on the sign of ΔV as given by (11); thus, it is independent of the absolute value of V_M. Therefore, as long as V_M remains constant throughout the conversion cycle, the temperature dependence of V_M will not affect the conversion result. Fig. 9 shows that for the temperature range from $0°C$ to $70°C$ the variation of V_M is quite small ($\leq 2mV$) at different process corners; thus, even if the temperature changes by few degrees Celsius during the conversion cycle, the conversion result will not be affected. Since $\Delta C_{max} \leq C_{FS}/2$, the maximum deviation of V_X around V_M is $\leq V_{DD}/4$; thus, V_X will not approach the supply rails.

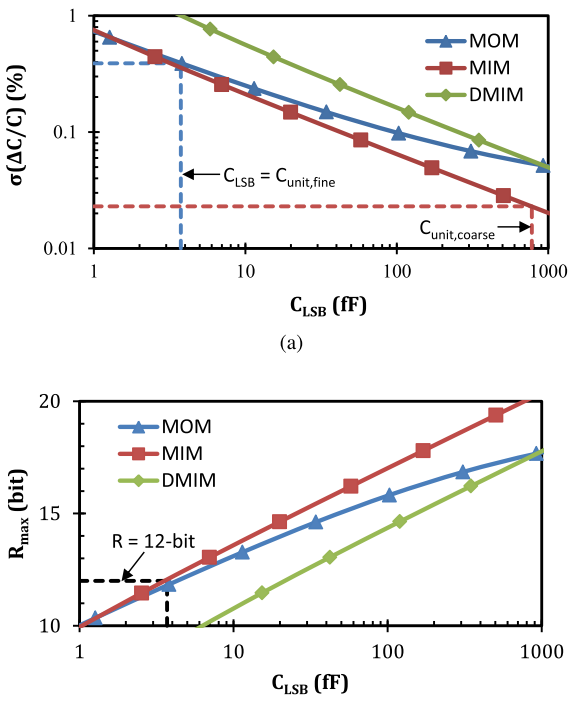


Fig. 10. (a) Standard deviation of unit capacitor mismatch and (b) maximum achievable mismatch-limited resolution vs. capacitance of unit capacitor (C_{LSB}). The dotted lines indicate the points used in the proposed design.

The robustness of the proposed interface against temperature variations was experimentally verified as will be shown in Section V.

IV. Capacitive Digital-to-Analog Converter

A. Mismatch-Limited Resolution

As discussed in Section III-B, the resolution is limited by the quantization noise, i.e., the mismatch of the CapDAC. The CapDAC unit capacitor (C_{LSB}) sets the absolute resolution of the readout circuit, while the number of bits of the CapDAC sets the dynamic range. For the $0.18\mu m$ CMOS technology used to implement the proposed prototype, three types of capacitors are available: parallel-plate metal-insulator-metal (MIM) capacitor; dual MIM (DMIM) capacitor (built by vertically stacking two MIM capacitors); and metal-oxide-metal (MOM) capacitor that utilizes the lateral electric field between standard interconnect metal layers.

A binary-weighted array implementation is considered, as it is more energy-efficient compared to an array that uses an attenuation capacitor, when linearity is taken into consideration [35]. In order to achieve fine absolute resolution and wide dynamic range, C_{LSB} needs to be minimized while the number of bits needs to be maximized. However, these two requirements are conflicting, because the smaller the unit capacitor the worse the matching and consequently the smaller the number of bits. Using the mismatch models provided by the foundry, the standard deviation of unit capacitor mismatch for each type of the aforementioned capacitors is shown in Fig. 10(a) vs. C_{LSB}. For a binary weighted CapDAC, the

worst-case differential non-linearity (DNL) occurs at the mid-scale transition, where all the unit capacitors in the array are switched. Thus, assuming a three-sigma worst-case DNL specification equal to half LSB, the maximum achievable mismatch-limited resolution is given by [36]

$$R_{max} = \log_2\left(\frac{1}{18\sigma^2\left(\Delta C/C\right)} + 1\right) \tag{22}$$

which is plotted in Fig. 10(b).

Several conclusions can be drawn from Fig. 10. First, DMIM shows the worst mismatch behavior, which is expected because it has the highest capacitance density. Second, for a fine absolute resolution ($C_{LSB} < 5fF$), both MOM and MIM show similar mismatch characteristics. Third, for a $12-bit$ resolution, the finest possible absolute resolution is $\approx 3.7fF$. For the employed technology, the capacitance density of an MIM capacitor is about 15 times that of an MOM capacitor; however, the strict layout design rules of MIM capacitors impose a limit on the smallest MIM capacitor to be $31fF$. On the other hand, an MOM capacitor can be customly crafted as a layout parasitic element. Hence, it can be arbitrarily small, where the observed design rules are simply the metal width and spacing of the interconnect layer.

B. CapDAC Implementation

In order to achieve a compromise between absolute resolution and silicon area, a coarse-fine implementation for the $12-bit$ CapDAC is employed. An $8-bit$ MOM fine CapDAC is combined with a $4-bit$ MIM coarse CapDAC. The fine CapDAC has $C_{unit,fine} = C_{LSB} = 3.75fF$ and full-scale capacitance of $0.96pF$. The coarse CapDAC has $C_{unit,coarse} = 0.78pF$, which is smaller than the fine CapDAC full-scale to ensure continuous capacitance range under process variations. The overall full-scale capacitance (C_{FS}) of the interface is $12.66pF$; thus, the effective resolution is $\approx 11.7-bit$. The silicon area occupied by the fine and coarse CapDACs is only 17% of the area of a $12-bit$ binary weighted MOM implementation. In addition to the 83% area-saving, the coarse-fine implementation reduces the array parasitics and decreases the routing complexity. A common-centroid layout and dummy structures are used for both CapDACs to minimize systematic mismatch.

In order to reconstruct the binary digital output from the coarse and fine parts one calibration point is required. The coarse output is multiplied by a scaling factor and then added to the fine output to yield the final conversion result. This operation can be implemented with a simple digital circuit or can be integrated in the post-processing routine that maps the capacitance of the sensor to the physical quantity being measured (e.g., pressure). The scaling factor can be determined by detecting when the coarse output is incremented (or decremented) by one, and storing the fine output of the preceding (or current) conversion cycle. This process is done only once and can be triggered by the capacitive sensor itself (which is typically slowly varying). For the implemented prototype, the MOM capacitor is implemented in Metal4 layer to reduce the parasitics. Since MOM and MIM capacitors have different temperature coefficients, the scaling factor will have a peak-to-peak variation of 0.29% in the temperature range from $0°C$ to $70°C$, which may result in increased non-linearity and missing codes, and necessitates the use of multiple calibration points. This problem can be eliminated while maintaining the area efficiency by implementing the coarse CapDAC using multilevel MOM capacitors.

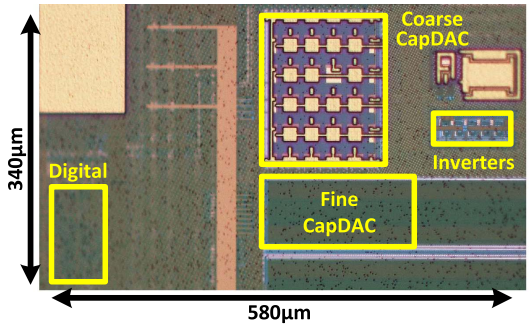


Fig. 11. Die micrograph of the fabricated SAR CDC.

It should be noted that the worst-case absolute DNL of a $12-bit$ array with a unit capacitor $C_{unit,fine}$ is the same as the worst-case absolute DNL of a $4-bit$ array with a unit capacitor $C_{unit,coarse} = 2^8 \cdot C_{unit,fine}$, i.e., if the number of bits is reduced by $k-bit$ and the unit capacitor is multiplied by a factor of 2^k, the mid-scale transition worst-case absolute DNL remains unchanged. Hence, the matching considerations discussed in the previous subsection are properly observed in the proposed coarse-fine implementation. For the chosen $C_{unit,coarse}$, the standard deviation of mismatch is 0.023% as shown in Fig. 10 a. This translates to $\sigma_{DNL} = 0.49fF$ for the $4-bit$ coarse CapDAC [10], [36]; thus, $3\sigma_{DNL}$ is less than half-LSB of the fine CapDAC. Therefore, by observing the mismatch-limited resolution discussed in the previous subsection, only one calibration point is required for the whole coarse-fine capacitance range. The linearity of the coarse and fine CapDACs was experimentally verified as will be presented in the next section.

V. Measurement Results

A. Die Micrograph

Fig. 11 shows a die photo of the proposed SAR CDC fabricated in a $0.18\mu m$ CMOS technology. The area of a rectangle enclosing the design is $0.2mm^2$, while the silicon area occupied by the design blocks is only $0.055mm^2$, where $\approx$ 82% of the area is occupied by the CapDACs. A digital serial peripheral interface (SPI) is implemented on-chip to facilitate reading/writing of control signals and reading conversion result. A LabVIEW interface is designed for test equipment control, measurement automation, and data acquisition.

B. CapDAC Characterization

The fine and coarse CapDACs were characterized using direct capacitance measurement [37], [38]. The input code is swept and the capacitance is measured using an LCR

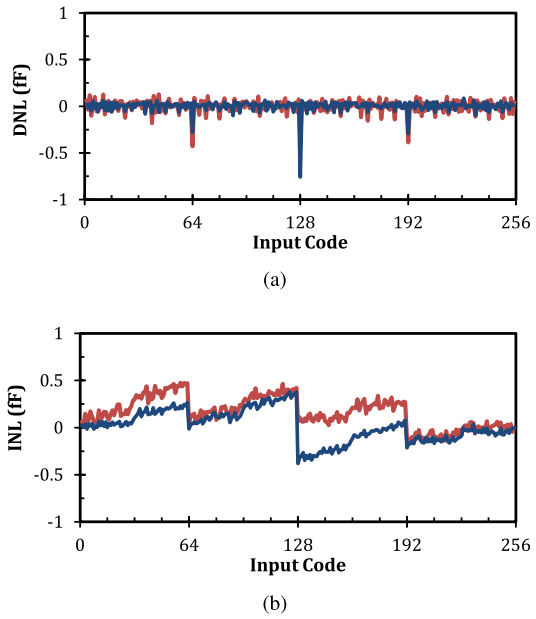


Fig. 12. Measured DNL and INL of two fine CapDACs vs. fine CapDAC input code.

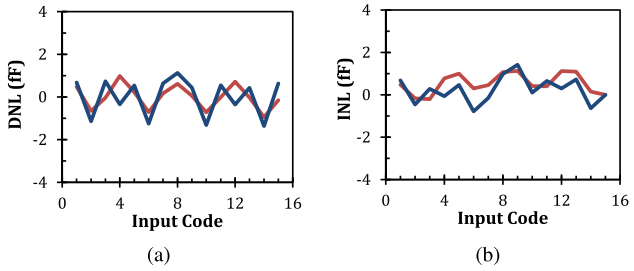


Fig. 13. Measured DNL and INL of two coarse CapDACs vs. coarse CapDAC input code.

meter (Agilent E4980A). The average measured values for $C_{unit,fine}$ and $C_{unit,coarse}$ are $3.73fF$ and $781fF$, respectively. Fig. 12 shows the measured DNL and INL of the fine CapDAC, where they have an absolute maximum of $0.75fF$ and $0.38fF$, respectively (i.e., $0.2LSB$ and $0.1LSB$, respectively). The measured DNL and INL of the coarse CapDAC are shown in Fig. 13, where they have an absolute maximum of $1.36fF$ and $1.42fF$, respectively (i.e., $0.36LSB$ and $0.38LSB$, respectively, where the LSB is $C_{unit,fine}$). The maximum linearity error of the coarse CapDAC is less than half-LSB; thus, only one calibration point is sufficient for the complete coarse-fine capacitance range.

C. CDC Characterization

In order to test the functionality and performance of CDCs, designers typically resort to three techniques. First, applying a varying reference voltage to emulate a varying sensor capacitance [4], [6], [13], [22], [39], [40]. Second, using discrete capacitors or an on-chip capacitor array as a dummy sensor [16], [17], [19]–[21]. Third, using a real capacitive sensor where the capacitance of the sensor changes with a

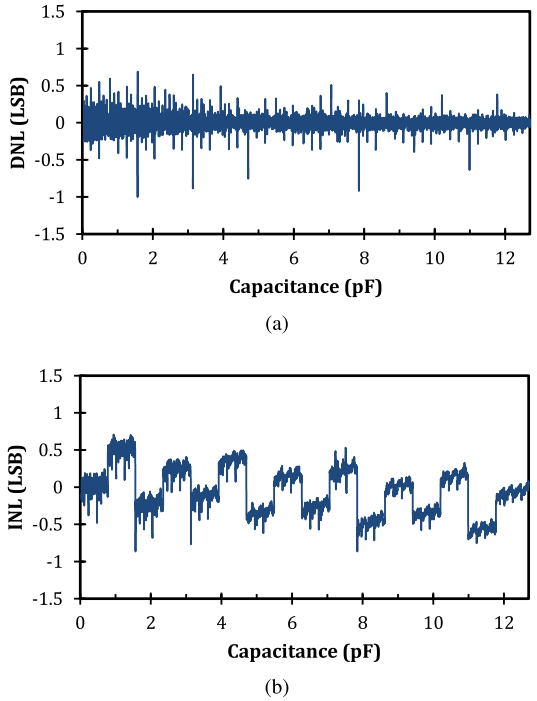


Fig. 14. Measured DNL and INL of the SAR CDC vs. equivalent sensor capacitance. The measurement is performed at once over the complete coarse-fine range and a single calibration point is used to reconstruct the output.

physical parameter, e.g., pressure, displacement, and humidity [4], [6], [13], [17], [19]–[22], [39]. In this work, all the three aforementioned techniques were employed.

The DNL and INL of the CDC were measured using standard histogram (code density) test. An Agilent B2962A low-noise source is used to generate a low-noise ramp waveform with $>14-bit$ linearity. The ramp waveform is applied in place of the reference voltage of the capacitive sensor (C_S). Setting $C_S = C_{FS}$ and sweeping the reference voltage from zero to V_{DD} emulate sweeping the sensor capacitance from zero to C_{FS} [13]. Fig. 14 shows the results of the CDC DNL/INL measurement performed at once for the complete coarse-fine capacitance range. The coarse-fine scaling factor was determined off-chip for flexibility. The DNL is limited between $0.67LSB$ and $-0.98LSB$, while the INL is limited between $0.71LSB$ and $-0.86LSB$. The transitions of the coarse output are clearly visible in the INL plot.

To further evaluate the linearity of the interface, the four-point linearity measurement described in [16] was used. Two sets of capacitors were characterized, where the four-point measurement of each set showed better than $12-bit$ linearity. In order to verify the functionality of the interface over its full dynamic range, a dummy capacitive sensor was integrated on-chip. The measured SAR CDC output vs. dummy sensor capacitance is shown in Fig. 15, where it has excellent linearity ($R^2 = 1.0000$).

The operation of the fabricated prototype was further verified using a MEMS capacitive pressure sensor [41]. A schematic of the pressure sensing test setup is shown in Fig. 16 [19]. The MEMS sensor is placed inside a hermetic test that is equipped with gas ports and electrical ports. The test

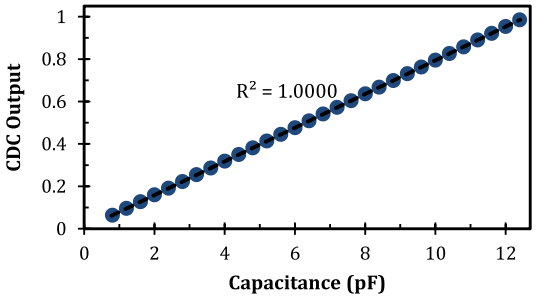


Fig. 15. Measured conversion output of the SAR CDC (normalized) vs. dummy sensor capacitance.

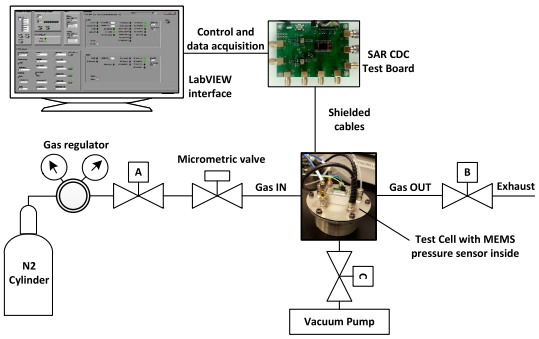
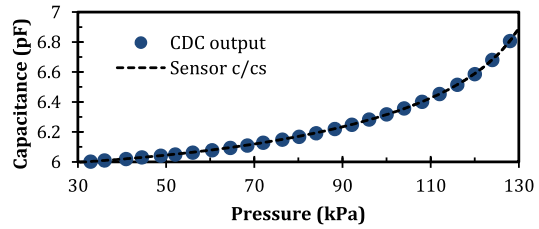
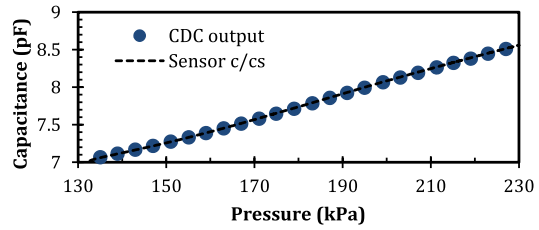


Fig. 16. Schematic of the pressure sensing test setup.



(a)



(b)

Fig. 17. Measured CDC output overlaid on the MEMS capacitive pressure sensor characteristics, where the pressure sensor is operated in (a) barometric pressure mode and (b) high pressure mode.

cell is evacuated using a vacuum pump and then compressed Nitrogen is allowed to flow in through a micrometric valve to gradually increase the pressure. The pressure sensor is first characterized using an Agilent E4980A LCR meter. Fig. 17 shows measured SAR CDC output vs. pressure of the test cell, where the CDC output follows the non-linear sensor characteristics.

Measured total power consumption for the SAR CDC is shown in Fig. 18. Power consumption increases with increasing the sensor capacitance (C_S). The power breakdown is

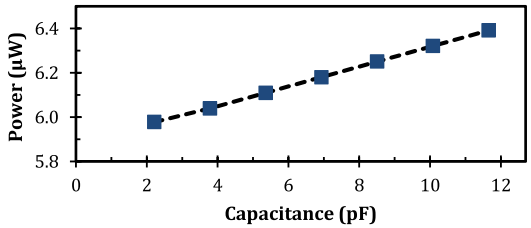


Fig. 18. Measured total power consumption for the SAR CDC vs. sensor capacitance (C_S).

TABLE I
MEASURED POWER BREAK-DOWN AND TOTAL POWER CONSUMPTION

	Power Consumption (μW)	Percentage
Inverter chain	3.34	52%
CapDAC and C_S	1.25	19%
Digital	1.85	29%
Total	6.44	100%

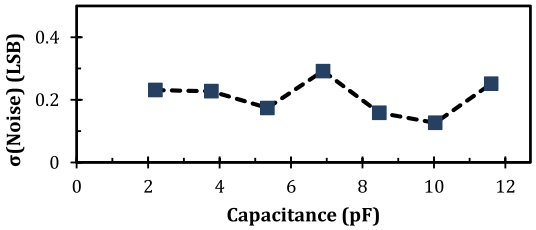


Fig. 19. Measured rms noise of the SAR CDC conversion output vs. sensor capacitance (C_S).

shown in Table I, where more than 50% of the power is consumed in the inverter chain. The power consumed in both the CapDAC and C_S is only 19% of the total power. Thus, using non-conventional switching schemes for the CapDAC will have minor impact on the overall power consumption [42], especially when noting that this usually adds more complexity to the logic.

Fig. 19 shows the measured SAR CDC output code standard deviation (rms noise) at different sensor capacitances. The measurement of the rms noise is limited by the quantization noise of the CDC where the conversion output varies by a single LSB when a fixed sensor capacitor is measured. This verifies that the resolution of the readout circuit is limited by the CapDAC quantization noise rather than the thermal noise. The rms quantization noise is $1.1fFrms$ and the estimated thermal noise from simulations is $0.47fFrms$; thus, the total rms noise is $\sqrt{1.1^2+0.47^2} = 1.2fFrms$.

The proposed design has inherently low temperature sensitivity because it does not depend on analog references. The sensor capacitor is directly compared to the reference capacitors in the CapDAC, where the conversion output is only a function of the capacitance comparison result, rather than a reference clock, current, or voltage. In order to demonstrate the low temperature sensitivity of the proposed CDC, the conversion output variation was characterized vs. temperature using a temperature test chamber (espec SU-221). Fig. 20 shows that the peak-to-peak output code deviation in the temperature

TABLE II
PERFORMANCE SUMMARY AND COMPARISON

	AD7153 [43]	JSSC 2013 [6]	TCAS-II 2015 [40]	JSSC 2015 [23]	ISSCC 2015 [17]	ISSCC 2015 [20]	S&A 2016 [24]	ISSCC 2014 [13]	VLSI 2014 [22]	**This Work**
Architecture	$\Sigma\Delta$	$\Sigma\Delta$	C/T	C/T	C/T	C/T	SAR	C/V+SAR	SAR+$\Sigma\Delta$	**SAR**
Output format	Digital code	Bit stream[a]	Digital code	Digital code	PM[b]	Digital code	Digital code	Digital code	Digital code	**Digital code**
Technology (μm)	N/R	160	90	180	160	40	180	180	180	**180**
Area (mm^2)	N/R	0.28[a]	0.3	0.1	0.05[b, c]	N/R[d]	0.1	0.49	0.46	**0.2**[h]
Supply Voltage (V)	3.3	1.2	0.6 & 1	0.6 & 1.2	1	0.45 & 1	0.9 & 1	0.9 & 1.2	1.4	**0.8 & 1.2**
Power (μW)	330	10.3[a]	5.5	0.11	14[b]	1.84	3.84	0.16	33.7	**6.44**
Conv. Time (μs)	5000	800	640	6400	210[e]	19[e]	42.5	4000	230	**16**
Cap. Range[f] (pF)	4	0.52	4	4	8	10.6[g]	16.14	10	24	**12.66**
Abs. Resolution $(fFrms)$	0.28	0.07	4.5	8.7	1.4	12.3	1.3	6	0.16	**1.2**
Resolution (bit)	12	11.1	8	7	10.6	8	11.8	8.9	15.4	**11.6**
FoM $(fJ/step)$	403,000	3,760[a]	13,800	5,300	1,870[b]	141	46	1,330	179	**33**

*C/T: Capacitance-to-time, PM: Period modulation, N/R: Not reported.

[a] Power consumption and area of digital decimation filter are not included. [b] Power consumption and area of time-to-digital converter are not included.

[c] Off-chip reference capacitor is employed. [d] Area of on-chip reference capacitor is not reported.

[e] Multiple measurement cycles are required to cancel the effect of parasitics/references. Conversion time and FoM are reported for a single cycle only.

[f] Only the capacitance range that is covered by the reported conversion time is considered.

[g] The capacitance range can be extended but with degraded energy efficiency.

[h] The area of a rectangle enclosing the design is $0.2mm^2$, while the silicon area occupied by the design blocks is $0.055mm^2$.

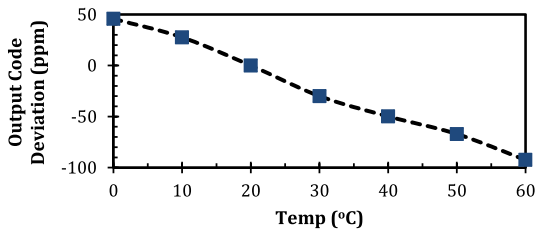


Fig. 20. Deviation of SAR CDC output code vs. temperature.

range from $0°C$ to $60°C$ is only $139ppm$, i.e., $0.47LSB$. This translates to a temperature sensitivity of $2.3ppm/°C$, which is three orders of magnitude better than the design in [20]. Even after the design in [20] undergoes calibration, the proposed design still has $6.7\times$ better temperature sensitivity without the need for calibration.

D. Comparison and Discussion

Table II shows a summary of the performance of the proposed interface and a comparison with state-of-the-art CDCs with resolution $\geq 7-bit$. The energy efficiency of different CDCs can be evaluated by using the energy efficiency figure-of-merit (FoM) which is calculated as [17], [20]

$$FoM = \frac{P \times T_{conv}}{2^R}, \tag{23}$$

where P is the power consumption, T_{conv} is the conversion time, and R is the effective resolution in bits, which is calculated as [17], [20], [22], [44]

$$R = \frac{SNR - 1.76}{6.02}, \tag{24}$$

where the signal-to-noise ratio (SNR) is given by

$$SNR = 20\log\left(\frac{Capacitance\ Range/2\sqrt{2}}{Absolute\ Resolution}\right) \tag{25}$$

where the absolute resolution is the rms capacitance resolution. It should be noted that SNR and not $SNDR$ is used for CDC FoM calculation, i.e., linearity errors are not taken into account [16], [17], [20], [22], [44]. The energy efficiency FoM is a function of the CDC conversion time; thus, the capacitance range considered in Table II corresponds to the range that is covered by the reported conversion time for each CDC.

The proposed CDC achieves an effective resolution of $11.6-bit$ and a FoM of $33fJ/step$, which is the best reported CDC energy efficiency FoM. The achieved FoM is more than two orders of magnitude better than the best reported $\Sigma\Delta$ CDC FoM [6], and 77% better than the best reported C/T CDC FoM [20]. Compared to [22] which employs a hybrid SAR + $\Sigma\Delta$ technique, the proposed CDC has 82% better FoM, $14.5\times$ faster conversion time, and $8.3\times$ smaller area. Compared to previous SAR CDC implementation [24], the proposed CDC has 28% better FoM, and 62% higher speed.

Energy efficiency can be improved by biasing transistors in the sub-threshold region; however, the circuit speed is sacrificed. Therefore, for a fair comparison, the energy efficiency should be compared at a given performance point. Thus, the energy efficiency FoM of state-of-the-art CDCs is plotted

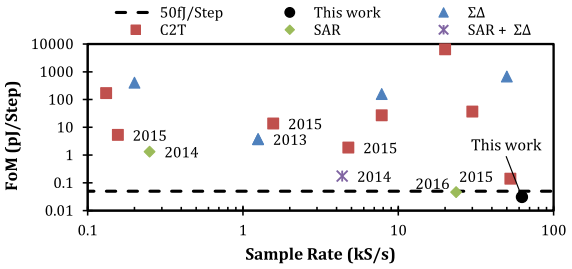


Fig. 21. Energy efficiency FoM vs. conversion sample rate for state-of-the-art CDCs.

vs. conversion sample rate in Fig. 21. The proposed CDC achieves both the highest sample rate and the best energy efficiency. Compared to the nearest design in the FoM vs sample rate chart [20], the proposed CDC has 11.2× better absolute resolution. In addition, the design in [20] requires four measurement cycles in order to cancel the sensitivity to analog references, temperature, and parasitics; thus, the sample rate of the proposed CDC is effectively 4.8× higher.

VI. Conclusion

Conventional SAR CDC has poor resolution that is limited by comparator offset error. A SAR CDC that uses an inverter-based amplifier is proposed to address this problem while maintaining excellent energy efficiency. The inverter-based amplifier doubles the transconductance for the same current, has fast non-linear settling, and uses near-threshold biasing to achieve excellent energy efficiency and fast operation. Direct capacitance domain comparison is employed which results in a very low temperature sensitivity of $2.3 ppm/°C$. A hybrid CapDAC using MIM and MOM capacitors is implemented allowing covering wide dynamic range in a compact area. An energy efficiency FoM of $33 fJ/Step$ is achieved, which is the best CDC FoM reported to date.

Acknowledgment

The authors would like to thank the reviewers for their valuable and stimulating comments.

References

[1] J. Yick, B. Mukherjee, and D. Ghosal, "Wireless sensor network survey," *Comput. Netw.*, vol. 52, no. 12, pp. 2292–2330, Aug. 2008.

[2] M. H. Ghaed *et al.*, "Circuits for a cubic-millimeter energy-autonomous wireless intraocular pressure monitor," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 60, no. 12, pp. 3152–3162, Dec. 2013.

[3] A. Sundararajan and S. M. R. Hasan, "Release etching and characterization of MEMS capacitive pressure sensors integrated on a standard 8-metal 130 nm CMOS process," *Sens. Actuators A, Phys.*, vol. 212, pp. 68–79, Jun. 2014.

[4] S. Xia, K. Makinwa, and S. Nihtianov, "A capacitance-to-digital converter for displacement sensing with 17b resolution and 20μs conversion time," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2012, pp. 198–200.

[5] S. D. Nguyen, I. Paprotny, P. K. Wright, and R. M. White, "MEMS capacitive flow sensor for natural gas pipelines," *Sens. Actuators A, Phys.*, vol. 231, pp. 28–34, Jul. 2015.

[6] Z. Tan, R. Daamen, A. Humbert, Y. V. Ponomarev, Y. Chae, and M. A. P. Pertijs, "A 1.2-V 8.3-nJ CMOS humidity sensor for RFID applications," *IEEE J. Solid-State Circuits*, vol. 48, no. 10, pp. 2469–2477, Oct. 2013.

[7] A. M. Kummer and A. Hierlemann, "Configurable electrodes for capacitive-type sensors and chemical sensors," *IEEE Sensors J.*, vol. 6, no. 1, pp. 3–10, Feb. 2006.

[8] C. Sapsanis *et al.*, "Insights on capacitive interdigitated electrodes coated with MOF thin films: Humidity and VOCs sensing as a case study," *Sensors*, vol. 15, no. 8, p. 18153, 2015.

[9] P. J. Mazzone, "Exhaled breath volatile organic compound biomarkers in lung cancer," *J. Breath Res.*, vol. 6, no. 2, p. 027106, May 2012.

[10] P. J. A. Harpe *et al.*, "A 26 μW 8 bit 10 MS/s asynchronous SAR ADC for low energy radios," *IEEE J. Solid-State Circuits*, vol. 46, no. 7, pp. 1585–1595, Jul. 2011.

[11] Y.-H. Chung, M.-H. Wu, and H.-S. Li, "A 12-bit 8.47-fJ/conversion-step capacitor-swapping SAR ADC in 110-nm CMOS," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 62, no. 1, pp. 10–18, Jan. 2015.

[12] W. Bracke, R. Puers, and C. van Hoof, "Ultra low power capacitive sensor interfaces," in *Analog Circuits and Signal Processing Series*. New York, NY, USA: Springer, 2007.

[13] H. Ha, D. Sylvester, D. Blaauw, and J.-Y. Sim, "A 160nW 63.9fJ/conversion-step capacitance-to-digital converter for ultra-low-power wireless sensor nodes," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2014, pp. 220–221.

[14] Z. Zhu and Y. Liang, "A 0.6-V 38-nW 9.4-ENOB 20-kS/s SAR ADC in 0.18-μm CMOS for medical implant devices," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 62, no. 9, pp. 2167–2176, Sep. 2015.

[15] M. Kramer, E. Janssen, K. Doris, and B. Murmann, "A 14 b 35 MS/s SAR ADC achieving 75 dB SNDR and 99 dB SFDR with loop-embedded input buffer in 40 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 50, no. 12, pp. 2891–2900, Dec. 2015.

[16] Z. Tan, S. H. Shalmany, G. C. M. Meijer, and M. A. P. Pertijs, "An energy-efficient 15-bit capacitive-sensor interface based on period modulation," *IEEE J. Solid-State Circuits*, vol. 47, no. 7, pp. 1703–1711, Jul. 2012.

[17] Y. He, Z. Y. Chang, L. Pakula, S. H. Shalmany, and M. Pertijs, "A 0.05mm^2 1V capacitance-to-digital converter based on period modulation," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC)*, Feb. 2015, pp. 1–3.

[18] A. K. George, J. Lee, Z. H. Kong, and M. Je, "A 0.8 V supply- and temperature-insensitive capacitance-to-digital converter in 0.18-μm CMOS," *IEEE Sensors J.*, vol. 16, no. 13, pp. 5354–5364, Jul. 2016.

[19] H. Omran, M. Arsalan, and K. N. Salama, "7.9 pJ/step energy-efficient multi-slope 13-bit capacitance-to-digital converter," *IEEE Trans. Circuits Syst. II, Express Briefs*, vol. 61, no. 8, pp. 589–593, Aug. 2014.

[20] W. Jung, S. Jeong, S. Oh, D. Sylvester, and D. Blaauw, "A 0.7pF-to-10nF fully digital capacitance-to-digital converter using iterative delay-chain discharge," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC)*, Feb. 2015, pp. 1–3.

[21] H. Omran, M. Arsalan, and K. N. Salama, "A robust parasitic-insensitive successive approximation capacitance-to-digital converter," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, Sep. 2014, pp. 1–4.

[22] S. Oh, W. Jung, K. Yang, D. Blaauw, and D. Sylvester, "15.4b incremental sigma-delta capacitance-to-digital converter with zoom-in 9b asynchronous SAR," in *Symp. VLSI Circuits Dig. Tech. Papers*, Jun. 2014, pp. 1–2.

[23] S. Oh *et al.*, "A dual-slope capacitance-to-digital converter integrated in an implantable pressure-sensing system," *IEEE J. Solid-State Circuits*, vol. 50, no. 7, pp. 1581–1591, Jul. 2015.

[24] A. Alhoshany, H. Omran, and K. N. Salama, "A 45.8 fJ/Step, energy-efficient, differential SAR capacitance-to-digital converter for capacitive pressure sensing," *Sens. Actuators A, Phys.*, vol. 245, pp. 10–18, Jul. 2016.

[25] K. Tanaka, Y. Kuramochi, T. Kurashina, K. Okada, and A. Matsuzawa, "A 0.026mm^2 capacitance-to-digital converter for biotelemetry applications using a charge redistribution technique," in *Proc. IEEE Asian Solid-State Circuits Conf. (ASSCC)*, Nov. 2007, pp. 244–247.

[26] S. Wang *et al.*, "A power-efficient capacitive read-out circuit with parasitic-cancellation for MEMS cochlea sensors," *IEEE Trans. Biomed. Circuits Syst.*, vol. 10, no. 1, pp. 25–37, Feb. 2016.

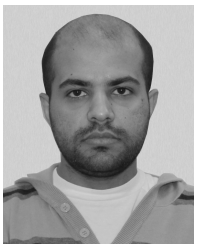
[27] P. Lajevardi, V. Petkov, and B. Murmann, "A $\Delta\Sigma$ interface for MEMS accelerometers using electrostatic spring constant modulation for cancellation of bondwire capacitance drift," *IEEE J. Solid-State Circuits*, vol. 48, no. 1, pp. 265–275, Jan. 2013.

[28] K.-L. J. Wong and C.-K. K. Yang, "Offset compensation in comparators with minimum input-referred supply noise," *IEEE J. Solid-State Circuits*, vol. 39, no. 5, pp. 837–840, May 2004.

[29] M. El-Chammas and B. Murmann, "A 12-Gs/s 81-mW 5-bit time-interleaved flash ADC with background timing skew calibration," *IEEE J. Solid-State Circuits*, vol. 46, no. 4, pp. 838–847, Apr. 2011.

[30] C. C. Enz and G. C. Temes, "Circuit techniques for reducing the effects of op-amp imperfections: Autozeroing, correlated double sampling, and chopper stabilization," *Proc. IEEE*, vol. 84, no. 11, pp. 1584–1614, Nov. 1996.
[31] Y. Chae and G. Han, "Low voltage, low power, inverter-based switched-capacitor delta-sigma modulator," *IEEE J. Solid-State Circuits*, vol. 44, no. 2, pp. 458–472, Feb. 2009.
[32] Y. Chae, K. Souri, and K. A. Makinwa, "A 6.3 μW 20 bit incremental zoom-ADC with 6 ppm INL and 1 μV offset," *IEEE J. Solid-State Circuits*, vol. 48, no. 12, pp. 3019–3027, Dec. 2013.
[33] R. Schreier, J. Silva, J. Steensgaard, and G. C. Temes, "Design-oriented estimation of thermal noise in switched-capacitor circuits," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 52, no. 11, pp. 2358–2368, Nov. 2005.
[34] R. G. Dreslinski, M. Wieckowski, D. Blaauw, D. Sylvester, and T. Mudge, "Near-threshold computing: Reclaiming Moore's law through energy efficient integrated circuits," *Proc. IEEE*, vol. 98, no. 2, pp. 253–266, Feb. 2010.
[35] M. Saberi, R. Lotfi, K. Mafinezhad, and W. Serdijn, "Analysis of power consumption and linearity in capacitive digital-to-analog converters used in successive approximation ADCs," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 58, no. 8, pp. 1736–1748, Aug. 2011.
[36] H. Omran, M. Arsalan, and K. N. Salama, "An integrated energy-efficient capacitive sensor digital interface circuit," *Sens. Actuators A, Phys.*, vol. 216, pp. 43–51, Sep. 2014.
[37] H. Omran, R. ElAfandy, M. Arsalan, and K. Salama, "Direct mismatch characterization of femtofarad capacitors," *IEEE Trans. Circuits Syst. II, Express Briefs*, vol. 63, no. 2, pp. 151–155, Feb. 2016.
[38] H. Omran, H. Alahmadi, and K. N. Salama, "Matching properties of femtofarad and sub-femtofarad MOM capacitors," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 63, no. 6, pp. 763–772, Jun. 2016.
[39] S. Oh *et al.*, "Dual-slope capacitance to digital converter integrated in an implantable pressure sensing system," in *Proc. 40th Eur. Solid State Circuits Conf. (ESSCIRC)*, Sep. 2014, pp. 295–298.
[40] N. T. Trung and P. Häfliger, "A submicrowatt implantable capacitive sensor system for biomedical applications," *IEEE Trans. Circuits Syst. II, Express Briefs*, vol. 62, no. 2, pp. 209–213, Feb. 2015.
[41] Protron Mikrotechnik GmbH. (Jan. 2012). *Micro-Machined Capacitive Absolute Pressure Sensors Datasheet*. [Online]. Available: http://www.protron.de
[42] H. Lee, S. Park, C. Lim, and C. Kim, "A 100-nW 9.1-ENOB 20-kS/s SAR ADC for portable pulse oximeter," *IEEE Trans. Circuits Syst. II, Express Briefs*, vol. 62, no. 4, pp. 357–361, Apr. 2015.
[43] Analog Devices. *AD7153 Datasheet*. [Online]. Available: http://www.analog.com
[44] S. Oh, W. Jung, H. Ha, J.-Y. Sim, and D. Blaauw, "Energy-efficient CDCs for millimeter sensor nodes," in *Efficient Sensor Interfaces, Advanced Amplifiers and Low Power RF Systems*. New York, NY, USA: Springer, 2016, pp. 45–63.

Hesham Omran received the B.Sc. (with honors) and M.Sc. degrees from Ain Shams University, Cairo, Egypt, in 2007 and 2010, respectively, and the Ph.D. degree from King Abdullah University of Science and Technology (KAUST), Saudi Arabia, in 2015, all in electrical engineering. From 2008 to 2011, he was a Research and Teaching Assistant with the Integrated Circuits Lab (ICL), Ain Shams University, and a Design Engineer with Si-Ware Systems (SWS), Cairo. From 2011 to 2016 he was a Researcher with the Sensors Lab, KAUST. He held internships with Bosch Research and Technology Center, Palo Alto, CA, USA, and with Mentor Graphics, Cairo. He has published 20+ papers in international journals and conferences. In 2016, he rejoined the Integrated Circuits Lab (ICL), Ain Shams University, as an Assistant Professor. His research interests include sensing microsystems, mixed-signal integrated circuit design, and FPGA-based systems.



Abdulaziz Alhoshany received the B.S. degree in electrical engineering (with first honors) in 2009 from Qassim University, Saudi Arabia, and the M.S. degree in electrical engineering from Arizona State University, Tempe, AZ, USA, in 2013. He is currently working toward the Ph.D. degree in electrical engineering at King Abdullah University of Science and Technology (KAUST), Saudi Arabia. His main research interests involve the design of low power, energy-efficient circuits and systems for sensing applications and high-performance data converters.

Hamzah Alahmadi received the B.S. degree in electrical engineering from Purdue University, West Lafayette, IN, USA, in 2016. He is currently working towards his M.S. degree in electrical engineering at King Abdullah University of Science and Technology (KAUST), Saudi Arabia. He had the privilege to be selected by KAUST with 50 other high school students in Saudi Arabia to be awarded the KAUST Gifted Student Program (KGSP) scholarship. During Summer 2014, he worked at the e-Lab at Purdue University to transfer data wirelessly from brain monitoring devices. In Summer 2015, he did an internship at the Sensors Lab at KAUST, working on characterizing mixed-signal integrated circuits and sensor readout systems. He has also been involved in the Global Development Team at Purdue to lead the power distribution design in Bangang, Cameroon.

Khaled N. Salama (S'97–M'05–SM'10) received the B.S. degree (with honors) from the Department of Electronics and Communications, Cairo University, Cairo, Egypt, in 1997, and the M.S. and Ph.D. degrees from the Department of Electrical Engineering, Stanford University, Stanford, CA, USA, in 2000 and 2005, respectively. He was an Assistant Professor at Rensselaer Polytechnic Institute, NY, USA, between 2005 and 2009. He joined King Abdullah University of Science and Technology, Saudi Arabia, in January 2009, where he is currently an Associate Professor, and was the founding Program Chair until August 2011. His work on CMOS sensors for molecular detection has been funded by the National Institutes of Health (NIH) and the Defense Advanced Research Projects Agency (DARPA), awarded the Stanford–Berkeley Innovators Challenge Award in biological sciences and was acquired by Lumina Inc. He is the author of 150 papers and 14 patents on low-power mixed-signal circuits for intelligent fully integrated sensors and nonlinear electronics specially memristor devices.