A Cryogenic 1 GSa/s, Soft-Core FPGA ADC for Quantum Computing Applications

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***Abstract*— We propose an analog-to-digital converter (ADC) architecture, implemented in an FPGA, that is fully reconfigurable and easy to calibrate. This approach allows to alter the design, according to the system requirements, with simple modifications in the firmware. Therefore it can be used in a wide range of operating conditions, including a harsh cryogenic environment. The proposed architecture employs time-to-digital converters (TDCs) and phase interpolation techniques to reach a sampling rate, higher than the clock frequency (maximum 400 MHz), up to 1.2 GSa/s. The resulting FPGA ADC can achieve a 6 bit resolution (ENOB) over a 0.9 to 1.6 V input range and an effective resolution bandwidth (ERBW) of 15 MHz. This implies that the ADC has an effective Nyquist rate of 30 MHz, with an oversampling ratio of 40×. The system non-linearities are less than 1 LSB. The main advantages of this architecture are its scalability and reconfigurability, enabling applications with changing demands on one single platform.**

***Index Terms*— ADC, analog-to-digital converter, calibration, cryogenic, FPGA, reconfigurable, TDC, time-to-digital converter.**

I. Introduction

THE interaction between the analog and digital world has always been a challenge. Special design techniques are required to make a good analog front-end. As analog-to-digital conversion is needed in numerous applications, ranging from sensor nodes, industrial control to (quantum) physics experiments; various ADCs with a wide range of specifications exists.

Each application has its own set of requirements, making it hard to reuse the same ADC design. The standard approach would be to combine an off-the-shelf ADC that matches the requirements with the digital system, either a system-on-chip or a reconfigurable device. However, after the system is set, the specifications can generally no longer be altered. Therefore the system, using an external ADC, is limited in terms of flexibility, scalability, reconfigurability and overall system size.

A better approach would be to create a more flexible system with an integrated reconfigurable ADC. This allows to have one platform suitable for many applications that only needs to be adapted with a firm- and/or software change and a calibration in the new environment. The most suitable platform to build a flexible system is in a reconfigurable logic device, i.e., a complex programmable logic device (CPLD) or an (field-programmable gate array) FPGA.

The need for interaction with the analog world and the digital reconfigurable devices has been recognized by FPGA manufacturers. Xilinx includes an on-chip ADC (XADC) in the 7 Family generation of FPGAs, Altera in the MAX-10 FPGA and Microsemi in their Fusion Mixed Signal FPGAs. Although this integration has some advantages, such as lower power, smaller system size and easier interfacing, it is still not very flexible. It rules out the possibility to change the conversion rate, the number of ADC channels and above all it takes die space solely reserved for the ADC, whether it is used or not.

In this paper, we propose a better solution using a soft-core ADC architecture, implemented in an FPGA. Except for some small resistors on the periphery of the FPGA, the ADC is completely integrated into the reconfigurable hardware blocks. Therefore the ADC can be easily interfaced with the remainder of the digital circuitry; it can be scaled to the required sampling rate or resolution and even allows ADCs with different specifications in one system. Above all, it allows calibration to each new environment the system is operating in, i.e., changes in voltage, temperature or chip can be calibrated out. We aim to show the effectiveness of our calibration techniques by operating the ADC both at room temperature (300 K) and in a cryogenic environment (15 K).

The basis of the design is the use of low-voltage differential signaling (LVDS) buffers as comparators and fast time-to-digital converters to perform the actual conversion. For the start-up calibration of the system, we employ the IO delay blocks to equalize the delays to each TDC and we use a masking circuit to precisely set the length of the TDC to match the reference period. The complete system is implemented, synthesized and routed in a Xilinx Artix 7 FPGA, placed together with the external resistors on a dedicated PCB to maximize the ADC performance and allow testing the same set-up both at room temperature and cryogenic temperatures.

This ADC architecture cannot replace all ASIC ADCs, however it extends the possibilities of the FPGA with minimal hardware changes and can be used together with hard-core ASIC ADCs.

The remainder of this paper is organized as follows. In Section II we review the state-of-the-art of low cost ADCs implemented using reconfigurable devices and we review FPGAs operating in a cryogenic environment together with cryogenic ASIC ADCs. Section III describes the complete design of the ADC architecture and the calibration procedure is detailed in Section IV. Section V reports the performance

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of our design in terms of standard ADC specifications and compares them with results reported in literature (both FPGA and ASIC ADCs).

II. Related Work

In the past years, the problem of creating ADCs directly in the FPGA was addressed by [1] and [2], among others. Those implementations are based on delta-sigma modulators, operating at a relatively low sampling rate, in the order of tens of kHz, due to the need for a feedback-loop between input and output.

Previous works also propose ADC designs based on TDCs for the actual conversion. These implementations rely on the creation of an analog reference ramp through a passive network outside the FPGA.

[3] used an RC-filter with 3 resistors and 1 capacitor to create the reference ramp. This reference ramp was then compared with the analog input signal in the FPGAs differential inputs. The time between crossing input and reference ramp was measured in a TDC based on clock phase interpolation, limiting the overall performance and resolution.

An implementation of the ADC with a TDC based on the carry chain was first presented by [4], however the reference ramp was generated externally. This limits the flexibility, speed and compactness of the design as an additional component is required to generate the ramp.

[5] is most relevant for this work. The ADC design employs a carry chain TDC for high timing resolution and generates the reference ramp with a single resistor, using the parasitic capacitance of the LVDS buffers to create the RC-ramp. In this follow-up work the design is improved by combining multiple LVDS buffers with different phases of the clock to achieve a higher sampling rate, furthermore we added extensive auto-calibration features to achieve significantly better performance.

With the vast amount of research dedicated to quantum computing in recent years, the search for systems operating at cryogenic temperatures has intensified. As most quantum bits (qubits) are operating in sub-Kelvin cryogenic temperatures, there is a substantial temperature difference (almost 300 K) to overcome between qubits and measurement electronics at room temperature. Employing cryogenic circuits at 4 K substantially decreases both the physical and thermal distance to the qubits, reducing the heat load into the cryogenic system and potentially improving performance due to shorter wiring.

One possibility is to place an FPGA in the cryogenic environment for processing of the quantum measurement data. [6]–[8] have shown the feasibility of operating an FPGA at 77 K. They focus on deep space applications or cryogenic digital data links for physics experiments. Both Xilinx (Virtex 2, Virtex 5, Spartan 3), Microsemi (IGLOO series) and Altera FPGAs (Stratix II) are fully or partially working at 77 K. [9]–[11] propose the use of cryogenic FPGAs operating at 4 K as the quantum controller. A Spartan 3 and most recently an Artix 7 were shown to be operating at 4 K. Extensive characterization of the Artix 7 was done by [11] confirming all required components of the proposed ADC implementation to be working in cryogenic conditions.

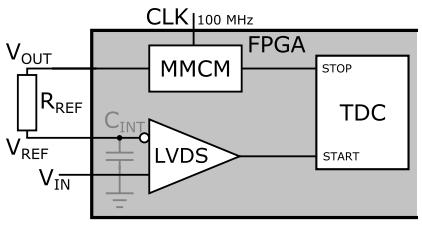


Fig. 1. Block diagram of the operating principle of the proposed ADC architecture. The architecture comprises a TDC, a LVDS comparator, a MMCM and a resistor R_{REF}. The analog signal V_{IN} is digitized, after conversion of the analog quantity to time, in the TDC.

Comparison of ASIC and FPGA implementations of ADCs is unfair, as it is well known that even state-of-the-art FPGAs cannot reach the performance reported by recent ASICs. However at cryogenic temperatures, there is only a very limited set of ADCs reported in literature [12]–[19], usually with performance limitations due to significant changes in analog behavior of the various components at cryogenic temperatures. Therefore it is especially interesting to compare our cryogenic FPGA ADC with these ASIC implementations. Cryogenic ADCs reported to date are limited in sampling rate up to a few hundred kHz and resolutions up to 11 bits.

To study the requirements of the ADC for quantum computing applications, we took as example superconducting qubits. The read-out of a superconducting qubit system has evolved in the past years from using high resolution ADCs to higher sampling rate ADCs. In 2012, an ADWIN was used for the read-out, i.e., a 14 bit ADC with 2 MSa/s [20]. In 2015, a 8 bit ADC with 20 MSa/s replaced the slower ADWIN [21]. Currently, those ADCs are replaced by 200 MSa/s 8 bit ADCs, namely the ADC08200 from Texas Instruments with an ENOB of 7 bits at 100 MHz. In other groups, both 500 MSa/s ADCs [22] and 1 GSa/s ADCs are already used [23], without stating their resolution.

This clearly shows the trend towards higher sampling rates, the end-result of the operation is nonetheless a single bit indicating whether the qubit is in the zero or one state. As high sampling rates are demanded, all current cryogenic ADCs are not suitable for the read-out of qubit systems.

III. System Architecture

The basic principle of the proposed ADC architecture is shown in Fig. 1. The system is built around a core consisting of a TDC, a mixed-mode clock manager (MMCM) and a LVDS input buffer. The MMCM receives an input clock of 100 MHz (from an external source) and generates a clock signal V_{OUT} (with 50% duty cycle) that charges and discharges the RC-circuit consisting of a SMD resistor R_{REF} and the parasitic input capacitance C_{INT} of the LVDS differential input buffer. The frequency of V_{OUT} can be tuned in order to increase or reduce the sampling rate. The generated RC-curve is optimal with a time constant in the order of $3\times$ the reference clock period, optimizing the ratio of curve linearity to input range.

The LVDS input buffer is used to compare the analog input signal V_{IN} with the RC reference ramp. A '1' at the output of the LVDS buffer is generated as long as the reference ramp

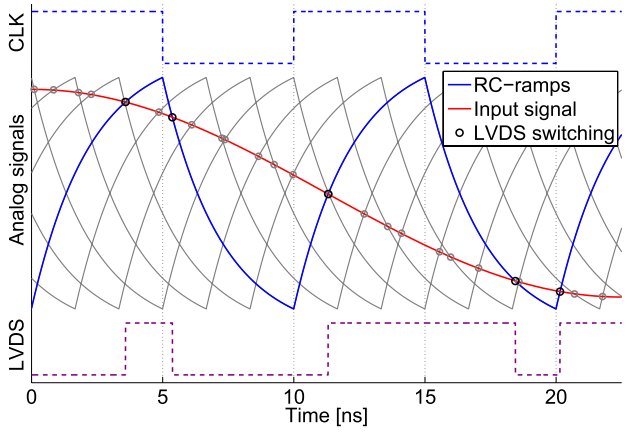
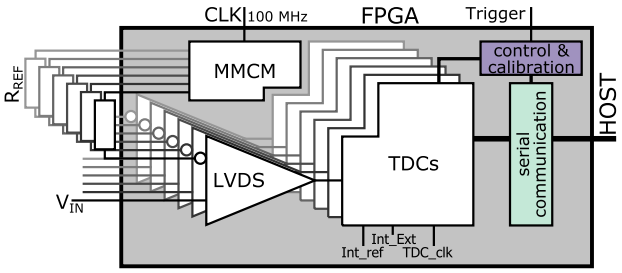
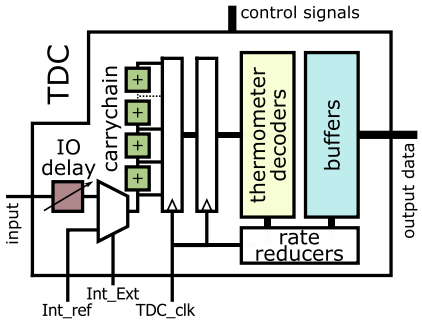


Fig. 2. Waveforms for a 1.2 GSa/s ADC using 6 phases of a 100 MHz base clock. In each 100 MHz clock period, 12 measurements (6 on the LVDS rising and 6 on the falling edge) are executed. The output clock for the first LVDS channel and its corresponding LVDS output are drawn as reference.



(a) The 6 separate measurement channels.



(b) The measurement block: the TDC.

Fig. 3. Detailed block diagram of the implementation of a 1.2 GSa/s ADC consisting of 6 output channels, 6 input buffers and 6 consecutive TDCs.

is higher than the analog input. The actual conversion to a digital ADC code is done with the TDC.

The TDC needs to be able to measure rising and falling edges. To do this, the TDC decoder is implemented as a bit counter, counting the number of ones in the carry chain. This technique also averages bubbles if they occur [5].

The sampling rate for this single channel is theoretically maximized to the maximum clock frequency, in the order of 400 MSa/s. To reach both a higher sampling rate and resolution we employ a multi-phase clock interpolation technique to sample the analog signal multiple times in one clock period. Therefore, instead of a single V_{OUT}, we make use of 6 V_{OUT} channels (thus 6 LVDS inputs), each with the same period, but increasingly shifted in phase by $1/6$ of that period.

The waveforms corresponding to a 1.2 GSa/s ADC architecture are depicted in Fig. 2. The MMCM generates a 100 MHz base clock and the 6 shifted phases. Each clock is routed to a dedicated resistor on the PCB and further towards the LVDS input. The input signal is routed towards the 6 LVDS buffers and can therefore be compared with the 6 phases of the clock. 12 measurements are generated in the 100 MHz clock period leading to a sampling rate of 1.2 GSa/s.

The complete implementation is detailed in Fig. 3. The principle from Fig. 1 is scaled to 6 channels, each channel is driven by its own clock phase (generated in the MMCM), which creates the 6 phase shifted RC-ramps. Those ramps are compared with the input signal in the LVDS buffer and it's output is routed towards the TDC.

The input stage of the TDC consists of an IO delay element (capable of delaying the input signal by various nanoseconds in steps of roughly 50 ps), which is used for the calibration procedure to align the input signals period with the carry chain (see Section IV for more details on the calibration). Furthermore, a multiplexer is implemented to be able to switch between the external input and an internal reference signal. The internal reference signal is the clock routed through another IO delay and is used to calibrate the carry chains required length. The length is trimmed to the reference clock period and a masking circuit is employed to disable the abundant part of the TDC, i.e., the part of the TDC that extends beyond the clock period. After the completion of the various TDC calibration steps, all TDCs (one for each channel) are covering exactly the TDC clock period (2.5 ns) and are properly synchronised to one another.

The TDC operates at 400 MHz (2.5 ns period), enabling a relatively short carry chain length of 200 carry blocks (the maximum length that fits in one clock domain of the Artix 7). This is done to minimize non-linearities and to reduce the overall FPGA logic utilization. With an average resolution of 16 ps per carry block, the carry chain covers a total of 3.2 ns.

The carry chain output is double-latched and decoded to a binary value in the thermometer decoder (implemented as a counter based tree structure). As the decoder is also running at 400 MHz, a rate reducer to 100 MHz is required to integrate the TDC with the remainder of the circuit.

The communication is implemented with a serial UART protocol, this protocol is chosen as the number of wires towards the cryogenic environment is limited and UART can be implemented with only 2 to 4 wires. However, the data needs to be buffered inside the FPGA as the transfer speed of UART is limited to roughly 750 kb/s in our set-up. The amount of data generated by the ADC is in the order of 1.2 GSa/s $\times$ 8 bits $\approx$10 Gb/s.

The majority of the post-processing is done after read-out on the host. For the interface an UART to USB controller was connected to the system to enable a simple interface between PC and FPGA. The FPGA was programmed using JTAG.

The PCB used for testing the FPGA ADC in room and cryogenic temperatures is depicted in Fig. 4. Due to size and connection limitations the number of components on the

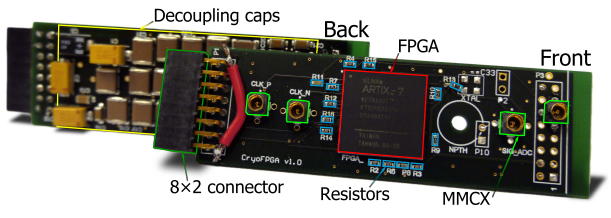


Fig. 4. Cryogenic FPGA PCB with the most important components highlighted. More details are given in [11].

PCB is reduced to the bare minimum, i.e., the FPGA is the sole active component present on the PCB. Extensive documentation on the PCB is presented in [11].

In the calibration section we discuss which steps are required for properly operating the ADC, such as the sorting of the codes from six different phases and the use of time stamps for further interpolation below the 830 ps ADC periods.

IV. System Calibration

In contrast to ASIC ADCs, that only need a small auto calibration or no calibration at all, our ADC needs an extensive calibration process to reach optimal performance. Although calibration takes time and resources, this extensive calibration can compensate for logic changes over a wide temperature range and allows the use of components with higher tolerances. The calibration consists of 4 steps and needs a total of 3 different input signals on the ADC. Two sawtooth and one sinusoidal signal, of which the frequencies are proportional to the sapling rate, are applied to the ADCs input during the calibration.

A. TDC Length Calibration

The wide temperature range brings significant changes to the timing inside the FPGA. To deal with timing differences, the used carry chain has been made longer than the sample period, which is 2.5 ns. The implemented carry chain consists of 200 delay elements and has a range of 3.2 ns at room temperature. Fig. 5 shows the problems that are created when the carry chain has more or less range than the sample period. In the case of a chain covering more time than the sample period, the last part of the chain will be a representation of data from the previous period. Data will be double-sampled, leading to an overestimation of the correct time. A chain that is too short will loose a part of the required measurable range, leading to an underestimation of the correct time in this lost range.

To equalize this values, the TDC has an option to disable elements at the end of the chain. The calibration of the TDC length is done by phase shifting a clock signal through the TDC, as can be seen in Fig. 6, only if the length of the TDC exactly matches with the clock period, the output values while shifting a clock through the line will always be the same. Too long TDCs will have an overestimation of the time in a certain range; too short TDCs will have an underestimation of the time in a certain spot.

By repeating the same measurement with increasingly more TDC blocks disabled, we can find the number of blocks for

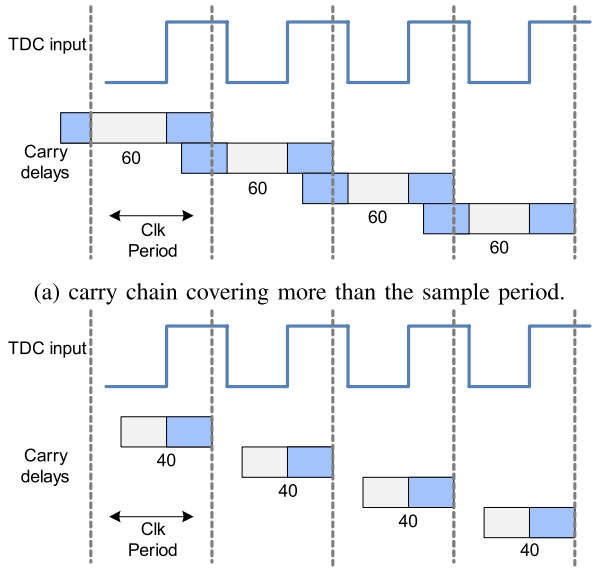


Fig. 5. Representations of carry chains that are either longer or shorter than the sample period. A line covering more time than the sample period leads to data being double processed. A too short line leads to data loss.

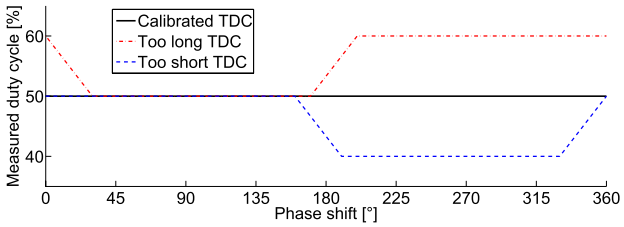


Fig. 6. Measured clock duty cycle with a too long, too short and a calibrated TDC, while phase shifting the clock input with 360 degrees through the carry chain. Only in the calibrated TDC, the average is constant at 50%.

which the output of the TDC is always the same, i.e., the smallest standard deviation over one complete 360 degrees rotation of the clock.

To cover a reference period of more than 2.5 ns, multiple consecutive measurements are summed together to form one time stamp per reference period. E.g. for the 1.2 GSa/s ADC, the reference period is 10 ns (however there is one measurement in both the LVDS rising and falling edge), thus 2 consecutive TDC measurements need to be combined.

B. TDC Alignment Calibration

After calibration of the TDC length, the TDC needs to be aligned with the reference period. We have to take into account the fact that one LVDS generates two outcomes in one reference period, one for the rising and one for the falling edge. Hereafter, we will refer to these as even, respectively odd, parity. Fig. 7 shows on top the *RC*-curve and a DC input signal in the bottom of the range. These two signals compared in the LVDS buffer lead to the result shown below for an unaligned TDC. The measured values are 0 and 20 for the first and second half of the clock period, which is not aligned to the reference period. Consequently one of the parities can

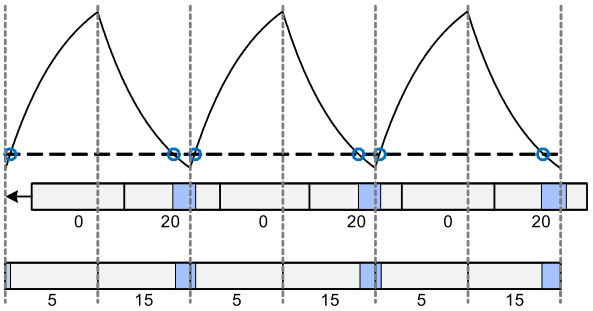


Fig. 7. Schematic view of the TDC alignment process. The measurement period of the TDC does not match with the reference period. The TDC is shifted to match both periods to one another.

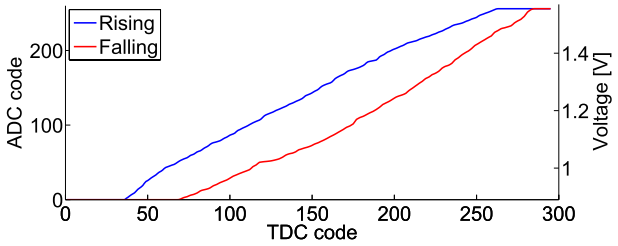


Fig. 8. The conversion graph from TDC to ADC code for the rising and falling edge of the RC-curve. The ramps are monotonically rising and in the calibration corrected for their RC distortion.

not measure the current input voltage. After alignment of TDC clock and reference period, the values are properly measured to be 5 respectively 15. Both parities can measure input voltages over the complete analog range.

By applying a slow ramp that exceeds the maximum and minimum input voltage, we can find the best alignment of the TDC, i.e., when the TDC parities have a maximum span. At a certain time after starting the ramp, the TDC values of the parities go from 0 to 1, indicating the start of the TDC span. The span ends as soon as the parities go from $max-1$ to max. By calculating the time between these events for both parities we can calculate the span. When doing this span measurement for all possible alignments we can find the alignment where both parities have the biggest span. That is the configuration in which the alignment is optimal.

C. TDC ADC Calibration

After completing the calibration of the TDCs, the voltage characteristics of the ADCs are calibrated. The transfer of input voltage to digital output is measured by applying a sawtooth on the input of the ADC. As there is a direct relation between input voltage and time after starting the sawtooth, the sample time can be converted to a voltage. For every LVDS input this calibration generates two look-up tables that convert TDC values to ADC values, one for the falling and one for the rising RC-curve.

An actual conversion graph can be seen in Fig. 8. Rising and falling curves are monotonically. This can be explained by the duty cycle measurement. As shown in Fig. 9 the outcome of the TDCs is positively correlated to time of measurement

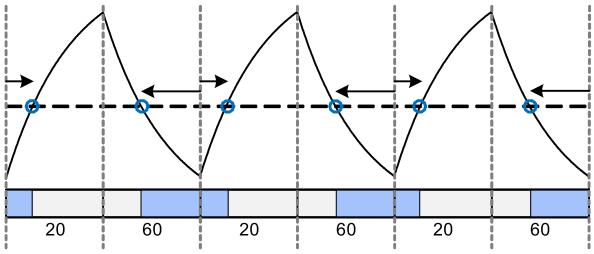


Fig. 9. The timing principle of the TDCs. The principle of counting ones in the thermometer decoder makes the generated time stamps to appear for the rising edge to be between the start of the reference period and the crossing point of the signal and ramp. For the falling edge, the calculated time is between the falling edge crossing point and the end of the reference period.

for the rising curve and negatively correlated to the falling curve.

D. ADC Synchronization

The entire design of this ADC depends on the accuracy of the ADC synchronization. After all, the results of the 6 interleaved channels can only be combined if the channels are accurately synchronized to each other.

With the previous calibration steps, each LVDS input behaves as a standalone ADC, generating two values in one period of the reference signal. To properly combine the values of six different channels, the time difference of each of the six phases has to be known.

To the inputs of all six channels, a sinusoid with a period covering 32 reference periods is applied. All ADCs measure this signal and a sinusoid is least squares fitted on each ADCs dataset. From each of the 6 fitted sinusoids, the phases is extracted. The phase is then converted to a time and for every ADC, the offset from the mean off all phases is extracted. By taking all these offsets into account, the ADCs timestamps can be properly sorted.

V. Results

The proposed ADC design was fully characterized. Both its versatility due to reconfigurability and the extensive calibration are discussed. The reconfigurability makes it possible to achieve a wide range of sampling rates and resolutions. The extensive calibration is tested by operating one particular ADC configuration (1.2 GSa/s ADC) at 300 K and 15 K. This particular configuration is finally compared with both FPGA and ASIC ADCs.

A. Performance of Reconfigurable Configurations

One of the most interesting aspects of this ADC is the possibility to switch between a number of configurations. The only requirements are a small firmware change and, for optimal range, a change in reference resistor for the creation of the RC-ramp.

The performance of ADCs, capable of sampling from 12.5 MSa/s up to 2.4 GSa/s, is shown in Fig. 10. For each ADC, the best (low input frequency) performance is reported. For a single channel, being only the rising or falling edge of

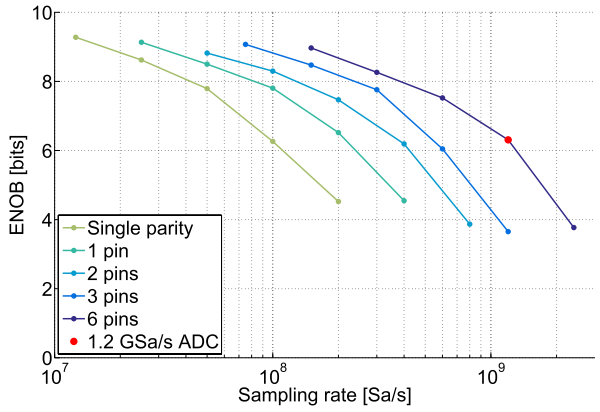


Fig. 10. ADC performance ENOB versus sampling rate at a 1 MHz input frequency. The ENOB is characterized over a wide range of possible configurations, for each configuration the maximum performance is given. Results are given for one parity (either the rising or falling edge of a single pin) and one to six pins interleaved.

one LVDS comparator, we can reach a performance of over 9 bits (ENOB) with a sampling rate of 12.5 MSa/s. The highest possible sampling rate is achieved with a reference period of 200 MHz on the 6 phase interleaved channels, leading to an impressive 2.4 GSa/s on an FPGA. With each pin added to the ADC, the performance can be improved, however the performance does not scale linearly with the number of pins added to the system. The performance at 2.4 GSa/s is slightly less than 4 bits, especially due to distortion and also due to interference between the different RCs of 200 MHz.

With our ADC we can achieve a wide variety of both sampling rates, a factor of 192 between highest and lowest, and effective resolution, a factor of 5 bits difference. This makes the ADC useful in many applications, in the range of possible configurations. The ADC operating at 1.2 GSa/s is studied in more detail in the following section.

B. Performance of a 1.2 GSa/s ADC at 300 K and 15 K

The 6 interleaved channels ADC is extensively investigated for its performance in terms of range, resolution, single shot precision, non-linearities and signal-to-noise ratio at room temperature (300 K) and immersed in liquid helium (15 K).

1) Full Range, Resolution and Power: The full range of the ADC is dependent on the frequency of the reference signal and to a certain extent the input frequency. The input capacitance is acting as a kind of low pass filter, reducing the input range.

The frequency of the reference signal together with the RC-filter determines how far on the RC-ramp the reference voltage will rise and fall. This is further limited by a finite switching time of the FPGA output pin, especially when switching from 0 to 1. This also implies that there will be a small offset voltage to the input of the ADC.

For the 1.2 GSa/s ADC the range is measured to be [0.9 1.6] V. The least significant bit (LSB) of the ADC represents 3 mV. Thus the full range spans approximately 8 bits. This range can be increased when the reference resistance is reduced. However this will result in more RC deformation and thus a worse DNL and single shot accuracy. The range does not vary significantly over temperature, thanks to the extensive calibration.

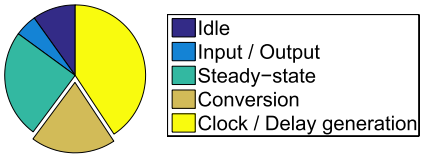


Fig. 11. Distribution of the dissipated ADC power to the various functions of the circuit in the FPGA at 300 K.

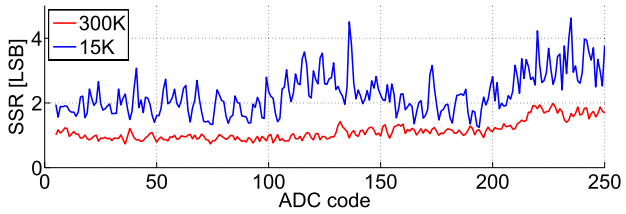


Fig. 12. Single shot measurement obtained by applying a DC voltage to the ADC input. Over the complete measurement range, the precision is 1.1 LSB (1σ) on average at 300 K and decreased to 2.3 LSB at 15 K.

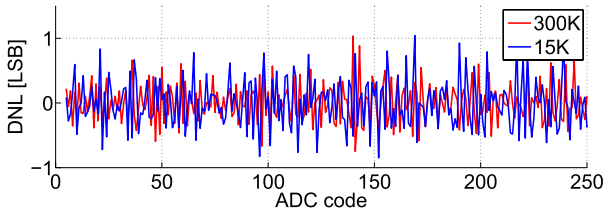
TABLE I
WORST CASE JITTER MEASURED FOR DIFFERENT FPGA COMPONENTS AT 300 K AND 15 K

FPGA components	Jitter [ps]	
	300K	15K
PLL	12	10
Carries	12	12
IO delay	24	45

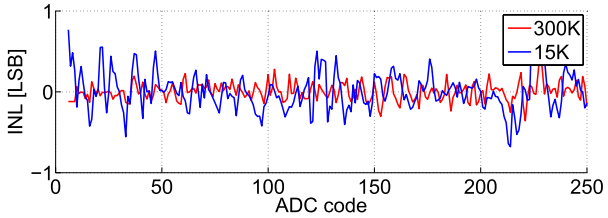
The power consumption of the FPGA based ADC is measured to be 750 mW at room temperature, including clock generation circuitry, data buffering and read-out. In Fig. 11 the distribution of the dissipated power to the various functions is depicted. It is dominated (around 40%) by the power consumption of the PLL and MMCM circuitry for generation of the high frequency clocks and the different clock phases. The actual conversion power is measured at around 200 mW. Especially at cryogenic temperatures, the clock generation power consumption increases, totalling the systems power consumption at 850 mW.

2) Single Shot Resolution/DC Accuracy: The single shot resolution (SSR) is the variation over time while measuring a constant/DC input value. It is measured by accumulating samples with a constant input over time. As the accuracy is dependent on the position in the full range, the performance over the complete range has to be studied.

The single shot measurement resolution is shown in Fig. 12. The resolution is always better than 2 LSB (1σ) and on average 1.1 LSB. This corresponds to an uncertainty in the measured voltage of roughly 3 mV. The ADCs SSR is mainly limited by clock jitter (from the PLL), carry chain jitter (delay line) and IO delay jitter. The jitter measured for these individual blocks is detailed in Table I. The combined jitter, or aperture jitter, can be calculated according to (1), yielding



(a) DNL



(b) INL

Fig. 13. Non-linearities (DNL and INL) extracted from ADC density test. The ADC density is produced by applying a ramp that exceeds both negative and positive input range to the input of the ADC.

30 ps and 48 ps, at 300 K and 15 K, respectively.

$$\sigma_a = \sqrt{\sigma^2_{\text{PLL}} + \sigma^2_{\text{carries}} + \sigma^2_{\text{IO delay}}} \tag{1}$$

The aperture jitter imposes an upper bound on the ADC performance (signal-to-noise ratio) following:

$$SNR_{\text{max}} = -20 \cdot \log\left(2\pi f_{\text{in}} \cdot \sigma_a\right) \tag{2}$$

in which f_{in} is the signal input frequency.

Considering an input frequency of 2 MHz, the best achievable SNR is in the order of 68 dB and 64 dB, respectively at 300 K and 15 K. At 40 MHz this is deteriorated to 42 (38) dB.

3) Non-Linearities: ADC non-linearities are identified using a density test. At the ADC input a slow ramp, exceeding both negative and positive input range, is generated. For each ADC code all occurrences are counted and stored in a histogram, from the histogram the non-linearities can be computed. With an ideal transfer, the counts $C(n)$ in each bin n are equal to the average number of counts $\overline{C} = \frac{\sum_{i=1}^{N} C(n)}{N}$.

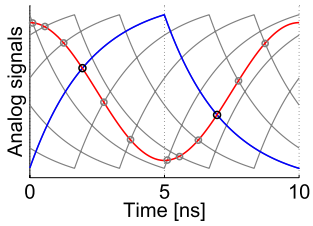
From the histogram the non-linearities can be computed with:

$$\text{DNL}(n) = \frac{C(n)}{\overline{C}} - 1 \tag{3a}$$

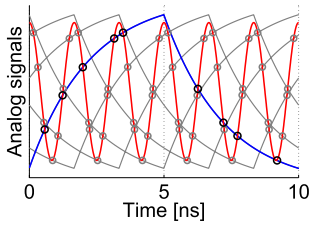
$$\text{INL}(n) = \sum_{i=1}^{n} \text{DNL}(i) \tag{3b}$$

The DNL and INL for the system, shown in Fig. 13, are in the range [-0.75 1.04] LSB and [-0.36 0.52] LSB, respectively. At 15 K, the non-linearities are similar, DNL and INL in the range [-0.85 1.04] LSB and [-0.68 0.77] LSB, after calibration.

Main contributors to the ADCs non-linearities are the intrinsic non-linear behavior of the exponential reference ramp on the analog side and the behavior of the TDC on the digital side. The non-linearities of the TDC are mainly caused by unevenly spaced delays in the carry chain and a non perfect clock distribution. Although these phenomena occur everywhere in the device, care should be taken not to place the carry chains in particular bad spots. All these problems can, at least partially, be overcome by the calibration to minimize systems non-linearities.



(a) 100 MHz input.



(b) 600 MHz input.

Fig. 14. Nyquist limitation of the ADC. (a) 100 MHz sinusoid that can be properly measured. (600 MHz sinusoid (at theoretical Nyquist frequency), which cannot be measured due to multiple transitions in one sample period, with reduced amplitude, to allow only one transition per period, makes proper conversion possible.

4) AC Performance: The ADCs signal-to-noise ratio (SNR), signal-to-noise-and-distortion ratio (SNDR), harmonic distortion (THD) and effective number of bits (ENOB) are estimated over frequency with a sinusoidal input signal. IM2 and IM3 are measured with a two tone test.

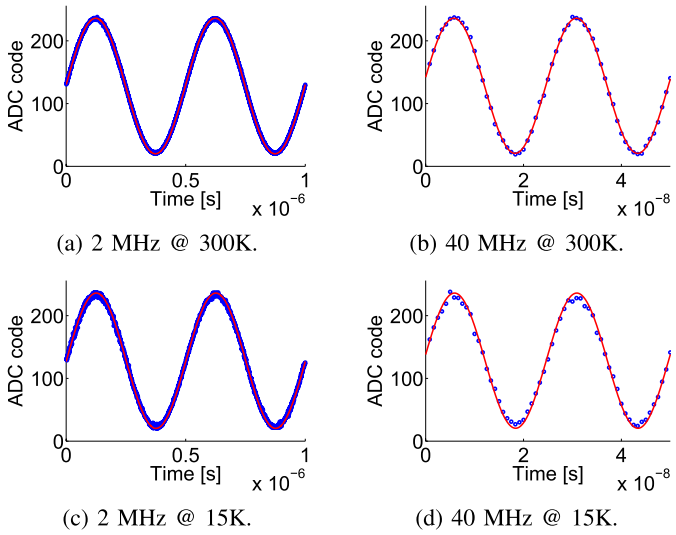
The amplitude of the input signal spans 90% of the ADC input range, in the results presented in this section unless otherwise stated, to avoid large distortion at the ends of the range. While a phase interlaced sampling method is used, the practical Nyquist frequency is the fastest individual sampling frequency (of a single phase), i.e., 100 MHz.

Above this frequency, the signal is faster than the individual phases, resulting in more than one transition in one sampling period, unless the input signal range is reduced to minimize the number of transitions per period to one. More than a single transition per period cannot be detected, resulting in incorrect time-stamps. In Fig. 14 this limit is sketched. Fig. 14(a) shows a 100 MHz sinusoid, which results in one transition per sample period (once on the rising and once on the falling edge), so it can be adequately measured. However the 600 MHz sinusoid, at the theoretical Nyquist rate (in (b)), has four to five transitions per sampling period, leading to inaccurate results. In the case the input amplitude is reduced, again a single transition per period can be reached, i.e., the signal can be properly measured.

The input sinusoidal signals are generated with a Rigol DG4202 function generator and low-pass filters are used to suppress out of band noise and harmonics.

In Fig. 15 digitized sinusoidal signals at both 300 K and 15 K are shown at input frequencies of 2 and 40 MHz. At cryogenic temperatures, the performance can be seen to be degraded especially for higher input frequencies (Fig. 15(d)). This degradation is caused by the jitter increase of the IO delay, as noted before, and by the significant decrease in decoupling capacitance at cryogenic temperatures. The decrease in total decoupling capacitance is causing more degradation at higher input frequencies as the current consumed by the FPGA is switching more frequently.

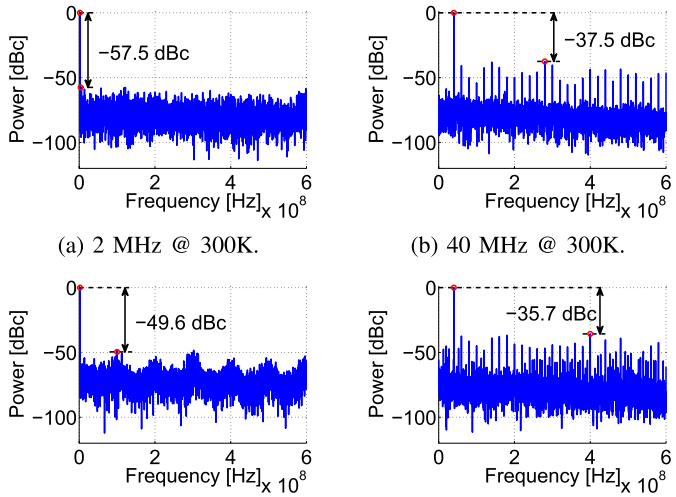
The frequency domain plots corresponding to the sinusoids depicted in Fig. 15 are obtained with a fast Fourier transform (FFT) in Fig. 16.



(a) 2 MHz @ 300K. (b) 40 MHz @ 300K.

(c) 2 MHz @ 15K. (d) 40 MHz @ 15K.

Fig. 15. Two periods of a 2 and 40 MHz sinusoid digitized at 1.2 GSa/s at 300 K and 15 K. The solid line is a best fitted sinusoid for reference.



(a) 2 MHz @ 300K. (b) 40 MHz @ 300K.

(c) 2 MHz @ 15K. (d) 40 MHz @ 15K.

Fig. 16. Frequency domain representation of the sinusoids depicted in Fig. 15. Frequency spectra were obtained from 48,000 samples while using a Blackman-Harris window of length 2^{14} shifted over the samples. Furthermore, the spurious-free-dynamic-range SFDR is indicated.

The various specifications derived from the frequency domain, such as SNR, SNDR, SFDR, THD and ENOB are summarized in Table II. From the SNR at low and high input frequency, first the aperture time t_a is found to be around 99 ps following (4a)

$$t_a = \frac{\sqrt{\left(10^{-\mathrm{SNR_{hf}}/20}\right)^2 - \left((1+\epsilon)/2^N\right)^2}}{2\pi f_{\mathrm{in,hf}}} \tag{4a}$$

$$\epsilon = 2^N \cdot 10^{-\mathrm{SNR_{lf}}/20} - 1 \tag{4b}$$

in which N is the 8.2 bits of our converter, $\mathrm{SNR_{hf}}$ the SNR at high input frequency and $\mathrm{SNR_{lf}}$ the SNR at low input frequency. 99 ps aperture time limits the performance, especially at higher frequencies, e.g., maximum SNR at 40 MHz is 32 dB.

TABLE II
ADC SPECIFICATIONS DERIVED FROM THE FREQUENCY DOMAIN AS PER FIG. 16

Specification		Input frequency [MHz] 2 300K	2 15K	40 300K	40 15K
SNR	[dB]	41.1	32.2	31.6	28.8
SNDR	[dB]	38.8	30.3	29.3	26.5
SFDR	[dBc]	57.5	49.6	37.5	35.7
THD	[dB]	-42.9	-34.6	-33.2	-30.3
ENOB	[bits]	6.2	4.7	4.6	4.1

The signal-to-noise-and-distortion ratio, defined as the power ratio of the signal to the sum of the remainder of the spectrum, was found to be 39 dB at 2 MHz, respectively 29 dB at 40 MHz, at room temperature. Immersed in liquid helium, the SNDR is reduced, especially at higher frequencies, due to the limitations noted before.

The SNR is comparable to the SNDR indicating little harmonic distortion, as also indicated by the THD, defined as the ratio of the sum of all signal harmonics by the power of the signal frequency itself. Significantly more harmonic distortion was present at high frequencies, moreover there is clear interference with the 100 MHz sampling frequency, either due to coupling into the analog signal or imperfect synchronization of the different phases. At cryogenic temperatures, the performance has dropped, the noise floor has increased and the harmonic distortion is more apparent.

From the SNDR, the ENOB is calculated with (5) to be 6.2, respectively 4.6 bits, at room temperature for low and high input frequencies. At cryogenic temperatures, the ENOB is reduced by 0.5 to 1.5 bit.

$$\mathrm{ENOB} = \frac{\mathrm{SNDR} - 1.76}{6.02} \tag{5}$$

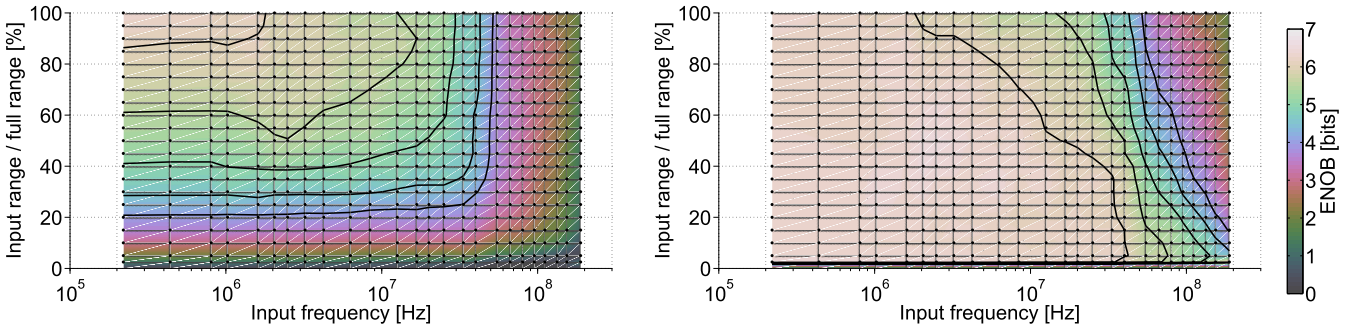
The ENOB over input frequency and input voltage range is shown in Fig. 17(a) at room temperature, averaging 10 measurement results per point. In (b) the ENOB is corrected for full scale ENOB_{FS} according to (6).

$$\mathrm{ENOB}_{FS} = \frac{\mathrm{SNDR} - 1.76 + 20\log\left(\frac{FS}{IR}\right)}{6.02} \tag{6}$$

in which FS is the full scale amplitude and IR the actual input range.

Finally, the ENOB is shown in Fig. 18 at both temperatures. The trend lines are drawn as a guideline, while at each input frequency 10 measurements are plotted with the standard deviation in the ENOB obtained over these measurements.

The effective resolution bandwidth is the input frequency at which the SNDR drops by 3 dB or the ENOB by 0.5 bit. The ERBW is in the order of 15 MHz at room temperature, but in the cryogenic environment it is roughly 25 MHz, due to the overall lower performance. Note that the ERBW is larger for smaller input amplitudes, due to less distortion (second contour line in Fig. 17(b)), and up to 60–70 MHz. With an effective bandwidth of 15 MHz, the effective Nyquist sampling rate is roughly 30 MHz, instead of 1.2 GSa/s. This can be used for oversampling (with an oversampling ratio of 40×) to increase resolution and reduce the noise.



(a) ENOB at 300K. (b) ENOB_{FS} at 300K.

Fig. 17. ENOB and ENOB_{FS} over input frequency and input range at 300 K. The result in (a) shows the actual ENOB measured, whereas (b) shows ENOB corrected for full scale as to show performance over the full range expressed in full scale ENOB. Contour lines are drawn at 6, 5.5, 4, 4.5 and 4 bits of ENOB.

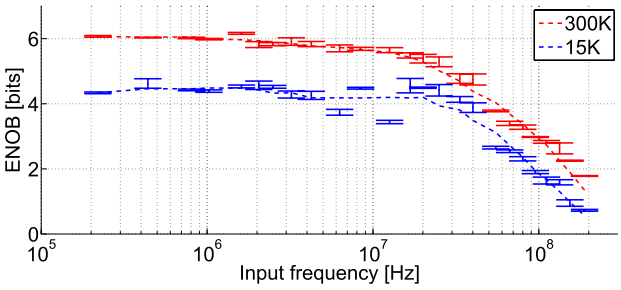
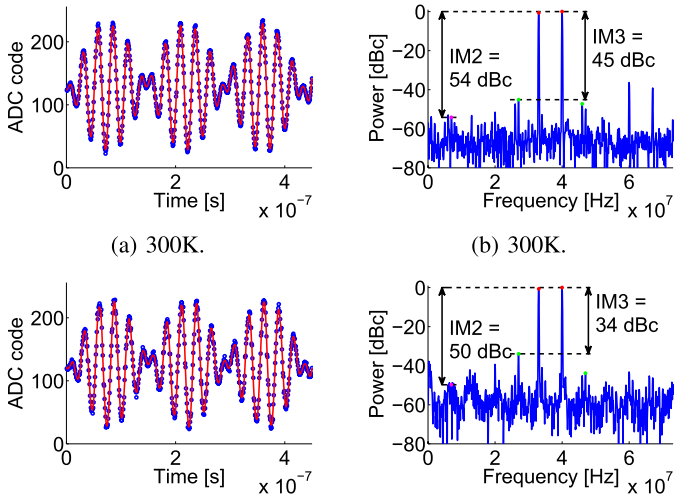


Fig. 18. ENOB over input frequency at both 300 K and 15 K. The resolution at 15 K is roughly reduced by 1.5 bit, due to higher IO delay jitter and reduced decoupling capacitance at low temperature.



(a) 300K. (b) 300K. (c) 15K. (d) 15K.

Fig. 19. IM2 and IM3 derived with a two tone test at 33 and 40 MHz.

The intermodulation distortion, IM2 and IM3, is acquired with a two tone test, one at 40 MHz and a second at 33 MHz. The result is depicted in Fig. 19 in time and frequency domain at both 300 K and 15 K. Besides significant power in IM2 and IM3 components, more cross-coupled harmonics are seen, especially at cryogenic temperatures. In room temperature however, second order harmonics from the two base tones are more apparent then at cryogenic.

5) Cross Device Performance: As the application is so close to the maximum capability of an FPGA and PCB, it is likely that there will be changes in performance from board to board. We had 3 boards at our disposal and tested the 1.2 GSa/s ADC on all the boards at room temperature. The performance of the ADCs on all three boards is very similar thanks to the advanced calibration of our ADC. The calibration can smooth out the performance over different devices making this ADC usable as a soft-core of which the performance can be well regulated.

C. Comparison of a 1.2 GSa/s FPGA ADC With Literature

Our FPGA ADC is first compared with other FPGA implementations at room temperature and the hard-core ADC, integrated as XADC, in Xilinx 7 series [24]. The other soft-core designs are based on single channel carry chain TDC [5], clock phase TDC [3] and delta sigma modulation [1], [2]. A comparison table is presented in Table III. Unfortunately, most general specifications are missing for the other reconfigurable ADC designs, nonetheless we tried to give a comprehensive overview.

The best performing ADC so far was found to be based on the carry chain TDC, however with our design we are capable of reaching both a higher sampling rate (6× faster) and, thanks to calibration, a higher resolution. However the ERBW of both ADCs is in the same order of magnitude. This most likely indicates an aperture time limitation of the LVDS buffers, which is in the order of 100 ps.

To compare directly with implementations as clock phase TDC, sigma-delta or especially ASICs is not fair. Nevertheless we can extrapolate the performance of our design, assuming it runs at a speed comparable to the other implementations.

Compared to clock phase TDC, we show (see Section V-A) that a resolution of 9 bits can be achieved with a 25 MSa/s in our system, thus outperforming the clock phase TDC implementation with 3 bit higher resolution.

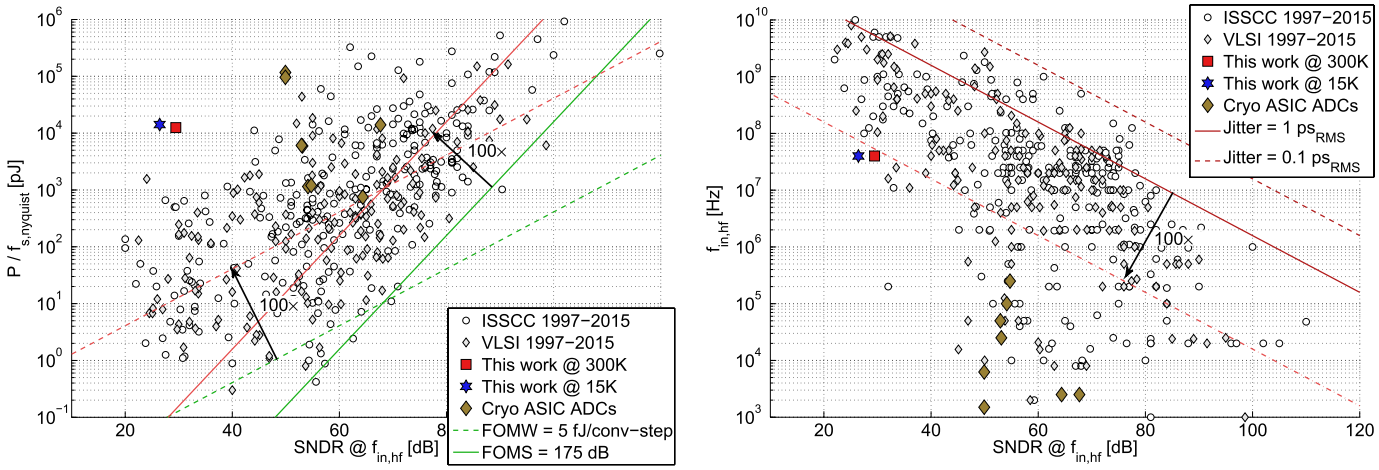
Comparing to the delta-sigma modulator, our ADC reaches a 9 bit resolution with a 25 MSa/s system, outperforming it in sampling speed with a factor of roughly 50×.

As a result, to the best of our knowledge, the ADC design proposed in this paper outperforms the sampling rate of all previously reported ADCs implemented using reconfigurable

TABLE III

COMPARISON BETWEEN OUR ARCHITECTURE AND PREVIOUS ADCS IMPLEMENTED IN RECONFIGURABLE HARDWARE. ADDITIONALLY WE COMPARE WITH THE XADC AVAILABLE IN XILINX 7 SERIES FPGAS. N/A IS USED TO INDICATE THAT THE CORRESPONDING DATA IS NOT AVAILABLE

ADC based on:		Multi-phase interleaving & carry chain TDC [this work]	carry chain TDC [5]	Clock phase TDC [3]	Delta Sigma Modulator [1], [2]	XADC [24]
Clock speed	[MHz]	400	200	360	100	
Conversion rate	[MSa/s]	1200	200	22.5	0.5 to 0.05	1
Voltage range	[V]	0.9 - 1.6	0 - 2.5	0 - 3.3	0 - 3.3	0 - 1.0
Digital range		8.2 bit	7.2 bit	6 bit	10 to 16 bit	12 bit
ENOB		6 bit (@ 1 MHz)	6 bit (@ 1 MHz)	*N/A*	9 bit	10 bit
Resolution (LSB)	[mV]	3	17	52	3	0.25
DNL	[LSB]	[-0.75 1.04]	[-0.9 1.4]	*N/A*	*N/A*	$\pm$ 1
INL	[LSB]	[-0.36 0.52]	[-1.1 1.6]	*N/A*	*N/A*	$\pm$ 2
Single shot resolution	[LSB]	1.1	2	*N/A*	*N/A*	1
Power consumption	[mW]	750	410	*N/A*	*N/A*	*N/A*
FPGA slices		$<$ 3555	$<$ 400	*N/A*	$<$ 80	dedicated
External components		7	1	4	2 - 3	0
Tested temperature range	[K]	15-300	300	300	300	300



(a) Energy vs. SNDR

(b) Aperture vs. SNDR

Fig. 20. Graphical comparison of the ADC presented in this work (square for 300 K, hexagram for 15 K) with different ASIC implementations of ADCs, using the following Figures of Merit: (a) energy per conversion versus SNDR, (b) frequency of the measured signal versus SNDR. The aperture error sets a limitation on the maximum frequency of the input signal that can be distinguished due to jitter. The comparison is done for both designs functioning at room temperature as well as cryogenic temperatures (featuring only a small set of ASIC ADCs [12]–[19]). Especially at cryogenic temperatures, our design compares favorably with ASIC implementations. The comparison is based on the survey maintained by Murmann [25].

logic, and although limited due to aperture limitations, also the widest effective resolution bandwidth.

To extend the comparison, we also compared our design with ASIC ADC implementations. To complete the comparison with ADCs found inside FPGAs, we compared our ADC to the ASIC XADC, found in Xilinx 7 series. We can extrapolate our performance to reach 10 bits of resolution at a rate of roughly 5 MSa/s. This shows that even with a soft-core ADC, a performance similar to that of an ASIC implementation can be reached, although not in terms of power consumption. Furthermore, the XADC is not reconfigurable, implying it is always sampling with 1 MSa/s. There are only two ADC channels available, whereas our design is only limited by the number of slices required to implement one channel. Although the XADC does not require any external components, as the reconfigurable ADCs do, it comes at the cost of occupying additional space on the FPGA die.

To compare more extensively with other ASIC ADCs, we used the ADC overview table collected by Murmann [25]. The results of this extensive comparison can be found in the Figure of Merit plots of Fig. 20. The Figures of Merit are intended to give an immediate ranking of the ADC in terms of speed, resolution and power consumption. In the figures our design is marked with a square (for 300 K) and a hexagram (for 15 K).

This comparison is not fair, as our design is implemented in a reconfigurable device. Even state of the art FPGAs cannot reach the performance generally achieved with recent ASIC designs. In contrast, we can see that, although the design is implemented in a reconfigurable device, it can match the performance of ASIC designs in somewhat older technologies.

Another interesting fact that can be seen is the trend of ASIC designs over the years. Thanks to Moore's law, the performance keeps improving over the years, due to lower feature size, resulting in lower power consumption and higher speed. For FPGAs we see a similar trend, smaller node sizes

will lead to a lower power consumption and a higher speed. This will again lead to a better performance of reconfigurable analog-to-digital converters.

A comparison of our ADC at cryogenic temperatures, is more complicated. There is only a small set of ASIC ADCs operating at cryogenic temperatures [12– 19], but still in a relatively wide temperature range, from 4 K up to 77 K. As analog behavior of devices changes, especially at the lower temperatures ($<$ 10 K), it is not entirely fair to compare all of them. However we tried to give a comprehensive overview by including all cryogenic implementations in the Murmann plots of Fig. 20 and compare them with our design.

The first thing to notice is the significant reduction in performance of the ASIC ADCs operating at cold, a reduction of over 100$\times$ compared to the best performing ADC at room temperature. These implementations are generally limited in sampling rate up to a few hundred kHz, whereas our ADC was capable of sampling at 1.2 GSa/s at cryogenic temperatures, although with an ERBW in tens of MHz range. In terms of resolution, a general trend shows lower ENOB at lower temperatures, as does our implementation (0.5–1.5 bit reduction). The main limitation is found in the power consumed by our ADC. Most of the cryogenic designs burn less than 1 mW, whereas the FPGA consumes over 850 mW at cryogenic temperatures, due to an increase in static power consumption of the FPGA in the cryogenic environment [11]. Nonetheless, we implemented a fully reconfigurable ADC at cryogenic temperatures, that is, to the best of our knowledge, the first cryogenic FPGA ADC and moreover the world's fastest cryogenic ADC (FPGA and ASIC).

VI. Conclusions

A completely reconfigurable design was presented, using a low cost Artix-7 FPGA. The design was demonstrated to operate from 12.5 MSa/s up to 2.4 GSa/s and can obtain a resolution as high as 9 bits (ENOB) up to 25 MSa/s. A full characterization has been done for the 1.2 GSa/s variant. Achieving an ENOB of 6 bits over an ERBW of 15 MHz makes the converter a non-Nyquist sampling ADC with 30 MHz Nyquist conversion rate and an oversampling ratio of 40$\times$. It has a single shot resolution of 1.1 LSB and a high linearity (DNL [-0.75 1.04] LSB and INL [-0.36 0.52] LSB). The same design was tested over multiple PCBs to demonstrate good cross-device performance thanks to the calibration for PVT variations. The ADCs were calibrated in terms of TDC length, TDC alignment and ADC synchronization. Thanks to the synchronization of single ADC channels, higher sampling rates can be achieved without losing much of the ENOB.

Besides changes in process and voltage from PCB to PCB, the PVT compensation has been demonstrated at cryogenic temperatures as low as 15 K. The ADC is performing in a wide temperature range, from 15 K to 300 K, but a small drop in performance is noticed at deep cryogenic temperatures due to higher jitter of IO delay components and lower decoupling capacitance in the cryogenic environment.

The system is completely soft-core and can be implemented in an FPGA, only 7 additional resistors need to be placed beside the FPGA (6 for the RC-curves and one 50 Ω closing resistor).

To the best of our knowledge, this is the fastest fully reconfigurable FPGA ADC reported to date, operating from deep cryogenic to room temperature. Moreover, we believe this is the fastest cryogenic ADC (ASIC or FPGA) presented to date. Thanks to the reconfigurability and calibration feature, this ADC can be used in many applications in a wide set of operating environments, such as a cryogenic environment for quantum computing applications, with specifications ranging from low sampling speed and high accuracy to very high sampling rates as 1.2 GSa/s.

VII. Acknowledgements

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