Analysis and Design of I/Q Charge-Sharing Band-Pass-Filter for Superheterodyne Receivers

Iman Madadi, Massoud Tohidian, and Robert Bogdan Staszewski

***Abstract*—A complex quadrature charge-sharing (CS) technique is proposed to implement a discrete-time band-pass filter (BPF) with a programmable bandwidth of 20–100 MHz. The BPF is part of a cellular superheterodyne receiver and completely determines the receiver frequency selectivity. It operates at the full sampling rate of up to 5.2 GHz corresponding to the 1.2 GHz RF input frequency, thus making it free from any aliasing or replicas in its transfer function. Furthermore, the advantage of CS-BPF over other band-pass filters such as N-path, active-RC, G_m-C, and biquad is described. A mathematical noise analysis of the CS-BPF and the comparison of simulations and calculations are presented. The entire 65 nm CMOS receiver, which does not include a front-end LNTA for test reasons, achieves a total gain of 35 dB, IRN of 1.5 $nV/\sqrt{Hz}$, out-of-band IIP3 of +10 dBm. It consumes 24 mA at 1.2 V power supply.**

***Index Terms*—CS-BPF, high-IF, IIR, noise, N-path, receiver, superheterodyne, switched-capacitor.**

I. Introduction

MONOLITHIC RF receivers (RX) have conventionally used a zero/low intermediate frequency (IF) due to straightforward silicon integration of low-pass channel-select filtering and avoidance of images (when zero-IF) or their easy baseband filtering (when low-IF) [1]–[6]. However, their drawbacks, such as poor 2$^{\text{nd}}$-order non-linearity, sensitivity to $1/f$ (flicker) noise and time-variant DC offsets, are all getting ever more severe with CMOS scaling. These problems could be solved with increasing the IF frequency, as was the norm in the pre-IC era with superheterodyne radios. However, to avoid the interferers and blockers at IF images, a high quality (Q)-factor band-pass filtering (BPF) is required, which is extremely difficult to implement in CMOS using continuous-time circuitry.

The integration problem of high-IF BPF was solved in [7], [8] and [9]. A high-Q complex frequency translation ("N-path") filtering at the high-IF stage was used in [7] as an alternative to the conventional CT BPF. However, that filter cannot reject images defined as interferers at odd harmonics of the IF frequency because the N-path filter *inherently* features replicas there. Therefore, there is an increased demand for highly integrated BPFs that would be free from any of those replicas and still compatible with CMOS scaling suitable for superheterodyne RX. In [8], [9], we have proposed a full-rate charge-sharing (CS) discrete-time (DT) operation that is largely free from replicas and which additionally offers a freedom to change the IF frequency in face of large blockers, thus avoiding desensitization.

In this paper, we describe in detail such high-IF DT BPF filter capable of realizing a fully integrated superheterodyne RX. The filter exploits passive switched-capacitor techniques and, as such, is amenable to CMOS scaling and is very robust to mismatches. Its center frequency and bandwidth are well controlled via clock frequency and capacitor ratios. Section II gives an overview of various types of bandpass filtering. Section III begins with basic principles of CS-BPF and then continues with detailed structure and continuous-time model of CS-BPF. The noise analysis of CS-BPF and circuit implementation of the front-end RX are presented in Section IV and Section V, respectively. The measurement results are demonstrated in Section VI.

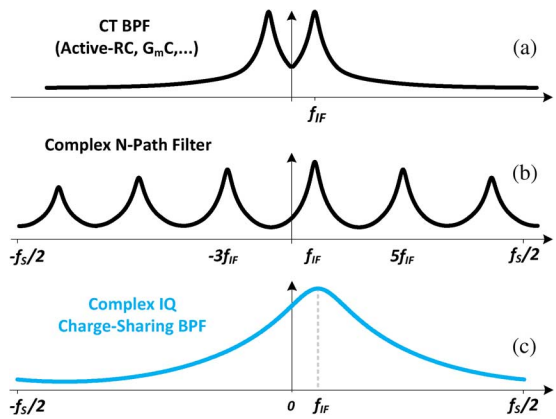

Fig. 1. Transfer function comparison of different types of BPFs (a) CT BPF, (b) Complex N-path, (c) DT CS-BPF.

II. Overview of Band-Pass Filtering

As an overview, transfer functions of different types of BPFs are compared in Fig. 1. CT filters, such as G_m-C and biquad, do not exhibit any aliasing or replicas but their structure is very complex and they consume a lot of power. Furthermore, their input-referred noise and linearity are much worse compared to other filters due to a number of active g_m-cells used. Active-RC filters are divided into two subcategories: sample-based and continuous-time. Both use opamps or g_m-cells as active components. They typically consume a lot of power and they also tend to be large in order to reduce flicker noise generated by the active devices.

Key advantage of the full-rate CS-BPF compared to the N-path filters [2], [10]–[13] is that its transfer function has only one peak in the entire sampling frequency domain of $-f_s/2$ to $f_s/2$, as shown in Fig. 1(c). Another advantage is that it features a theoretically infinite IIP2 compared to the limited

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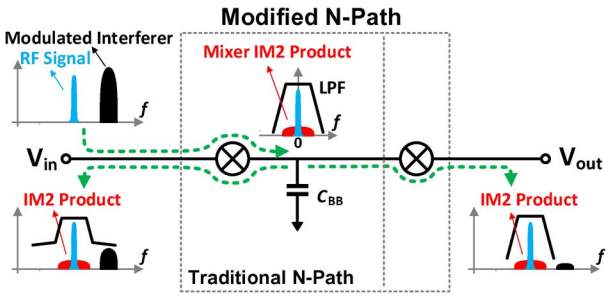

Fig. 2. N-path filter and its 2nd-order non-linearity.

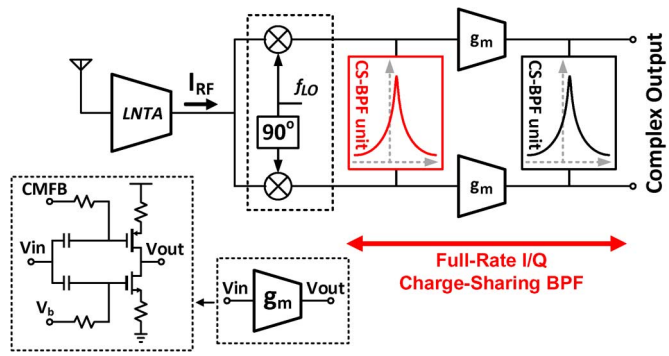

Fig. 3. Block diagram of the high-IF receiver containing the proposed BPF and schematic of IF gm cell.

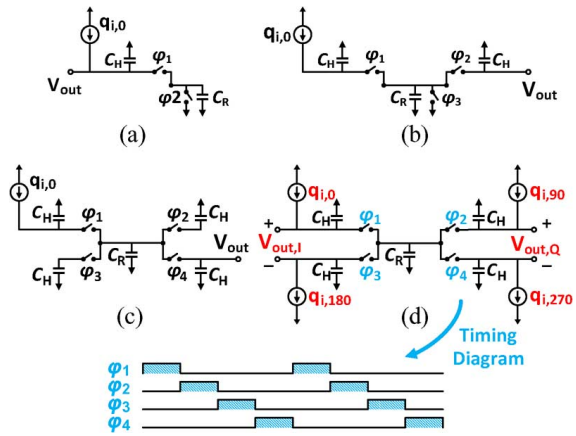

Fig. 4. Basic concepts of DT charge-sharing IIR filtering: (a) 1st-order real-valued LPF filter; (b) 2nd-order real-valued LPF filter; (c) 4th-order real-valued LPF filter; and (d) 1st-order complex-valued BPF filter.

IIP2 of N-path filters. The only drawback of DT CS-BPF compared to N-path filters is that it has a lower Q-factor, which can be solved by cascading several CS-BPF stages or using a positive feedback [13].

The simplified block diagram of an N-path filter is shown in Fig. 2, which comprises one mixer and baseband capacitor (C_{BB}) for a traditional N-path filter [12], or two mixers and C_{BB} for a modified N-path filter [14]. The input signal is down-converted to DC by the mixer, filtered by a low-pass filter, and then up-converted by the same [15] or another mixer [13], [14]. The 2nd-order non-linearity of the mixer depends on LO frequency, and any mismatch in the mixer switching transistors [16]. The typical IIP2 of the mixer is between 50–70 dB [17]. Therefore, as illustrated in Fig. 2, in both the traditional and modified N-path filters, the IM2 product can be generated due to the down-conversion to DC by the mixer, which coincides with the wanted signal. However, the CS-BPF does not experience any frequency translation, thus no IM2 products.

As an application example of such a BPF, the feedback-based superheterodyne RX utilizing a charge-sharing (CS) technique and N-path notch filter was proposed in [8]. Although the N-path notch filter is used as a channel select filter, the N-path folding is of no concern there due to the strong protection offered by the preceding high-IF CS filters. Also, in [9], a complete fully integrated superheterodyne RX using the CS technique and a BB filtering was proposed. The folding due to the lower sampling frequency of the BB filters is also of no real concern as it is protected by the preceding high-IF CS filters.

III. Charge-Sharing Bandpass Filter (CS-BPF)

The block diagram of the superheterodyne RX front-end is shown in Fig. 3. The RF signal of f_{RF} frequency is converted to current, $\mathrm{I_{RF}}$, via a low-noise transconductance amplifier (LNTA). Then, $\mathrm{I_{RF}}$ is down-converted to an intermediate frequency f_{IF} current $\mathrm{I_{IF}}$ by a passive mixer comprising commutating switches clocked at f_{LO} rate with rail-to-rail 25% duty-cycle. The $f_{IF} = |f_{LO} - f_{RF}|$ frequency could be in the 1–100 MHz range. However, to avoid the unnecessary increase in power of IF circuitry, f_{IF} should be placed just beyond the flicker noise corner of the devices comprising the RX circuitry [8]. Mixers driven by the 25% duty-cycle clocks have a higher conversion gain from RF to IF and also introduce less flicker noise compared to counterparts driven by the 50% duty-cycle clock [1]. Hence, this justifies our choice of the double-balanced mixer driven by the 25% clock.

The down-converted $\mathrm{I_{IF}}$ current flows into a complex full-rate I/Q CS-BPF. Multiple unit filters of 1st-order could be cascaded to get high-Q BPF centered at f_{IF}. The proposed filter provides enhanced RX selectivity and rejects unwanted blockers and images inherent to the high-IF architecture.

A. BPF Unit Structure

The well-known real-valued DT IIR low-pass filter (LPF) is shown in Fig. 4(a) [18]. The input charge packet is the integrated input current (provided by a g_m-cell) on C_H and C_R during φ_1 over a time window T_s. At φ_1 going inactive, C_R samples a portion, $C_R/(C_R + C_H)$, of the integrated input charge. As a result, the DT circuit shown in Fig. 4(a) has a 1st-order DT IIR characteristic, with C_R acting as a lossy component ("switch-capacitor resistor") that leaks the total charge out of the system. Therefore, it prevents the C_H voltage from overflowing, thus ensuring stability. The order of the Fig. 4(a) DT IIR filter can be further increased to 2nd or 4th, as shown in Fig. 4(b) and Fig. 4(c), respectively. At the end of φ_1, the sampled charge on C_R is just shared with another C_H capacitor. This mechanism can arbitrarily increase the IIR filter's order [19].

The basic quadrature (i.e., with four outputs) CS-BPF can be synthesized from the 4th-order DT IIR filter (with a single real output) by applying input charge packets $q_{i,0}$, $q_{i,90}$, $q_{i,180}$ and $q_{i,270}$ with a multiple of 90^o degree phase shifts, as shown in Fig. 4(d). During each phase of φ_1, φ_2, φ_3 and φ_4, four input charge packets are accumulated into their respective history capacitors, C_H. At the end of each phase, each C_R containing the previous packet is ready to be charge-shared with C_H containing the current input charge packet and the "history" charge. Therefore, in each phase, rotating capacitor C_R removes a charge proportional to $C_R/(C_H+C_R)$ from each C_H and then

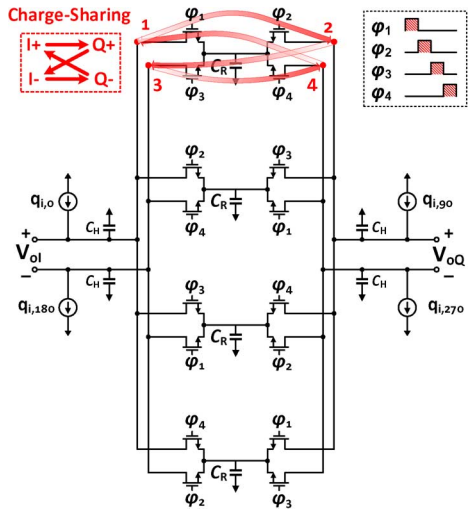

Fig. 5. Complex CS-BPF unit circuit.

delivers it to the next C_H. The four quadrature outputs can be read out at the sampling rate of $f_s = 1/T_s = f_{LO}$. In that case, The CS-BPF is not full-rate anymore and its sampling frequency would be equal to f_{LO}.

The basic concept of the I/Q charge-sharing filtering with *active* opamps was introduced in [20] for a different low-IF application with very low sampling rate of 1 Msample/s. In our work, the 5.2 Gsample/s CS-BPF is fully passive without any opamps, constructing DT filters that are much more robust to mismatches than the RC, LC and G_m-C type of filters because of the excellent capacitor matching in advanced CMOS. The other advantage of the proposed filter is that it is fully compatible with process scaling due to the filter's passive nature.

The schematic of the fully passive full-rate 1st-order CS-BPF unit is shown in Fig. 5. The time-domain I/Q output voltage expressions at $t = nT_s$, can be written as

$$V_{oI}[n] = \frac{C_H V_{oI}[n-1] - C_R V_{oQ}[n-1] + q_{in,I}[n]}{C_H + C_R}, \quad (1)$$

and

$$V_{oQ}[n] = \frac{C_H V_{oQ}[n-1] + C_R V_{oI}[n-1] + q_{in,Q}[n]}{C_H + C_R}. \quad (2)$$

By defining the complex input charge as $q_{in,C} = q_{in,I} + jq_{in,Q}$ and complex output voltage as $V_{oC} = V_{oI} + jV_{oQ}$, the z-domain complex transfer function of the filter can be derived as

$$H_{CS-BPF}(z) = \frac{V_{oC}(z)}{q_{in,C}(z)} = \frac{k}{1 - (a + j(1-a))\, z^{-1}}, \quad (3)$$

where, $k = 1/(C_H + C_R)$, $a = C_H/(C_H + C_R)$. The position of CS-BPF complex pole is determined by a. According to (3), the charge-sharing technique forms a 1st-order complex filter. The ideal transfer functions of the filter for different a coefficients are shown in Fig. 6. The CS-BPF is acting as a LPF centered at DC in the extreme case of $a = 1$, while for the extreme case of $a = 0$, CS-BPF is acting as an N-path filter centered at $f_s/4$. Also, the filter bandwidth increases, when $a < 0.5$, and decreases, when $a > 0.5$ with the increase of the center frequency f_c.

B. CS-BPF Continuous-Time Model

The switched-capacitor circuit of CS-BPF can be modeled as an RC network for frequencies of interest below $f_s/10$. The

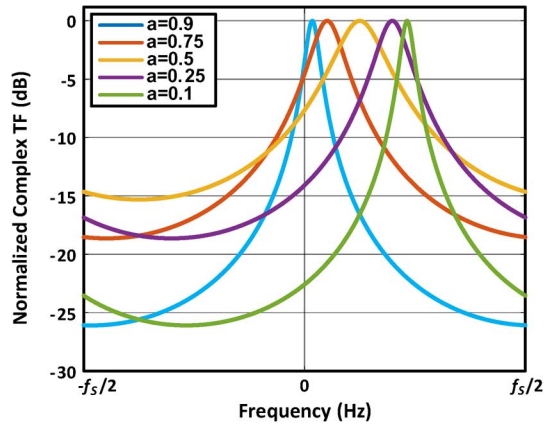

Fig. 6. Ideal CS-BPF transfer function.

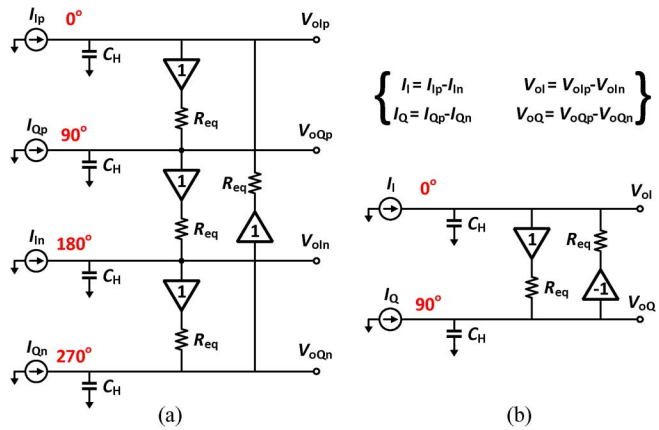

Fig. 7. Schematics of the continuous-time model of quadrature DT CS-BPF with: (a) single-ended and (b) differential inputs.

continuous-time (CT) equivalent model of the DT CS-BPF is shown in Fig. 7 for (a) single-ended and (b) differential inputs. Phase of input currents (I_{Ip}, I_{Qp}, I_{In} and I_{Qn}) should be 0^o, 90^o, 180^o and 270^o, respectively, that can be generated with the conventional quadrature current-commutating passive mixer. R_{eq} is an equivalent DT resistance of C_R and is equal to $1/(C_R f_s)$. The input currents are integrated into C_H's and the charge-sharing with C_R's is modeled with R_{eq} isolated by a unity-gain buffer to account for DT time-division duplexing (TDD) isolation between the quadrature paths. The CT transfer functions (TF) of Fig. 7(a) and (b) are ultimately the same. Since the differential input interpretation reduces the number of expressions to half, the differential TF analysis will be carried out below. The s-domain voltage-current expressions of the Fig. 7(b) circuit can be written as

$$V_{oI}(s) = I_I(s) \cdot \frac{R_{eq}}{1 + sR_{eq}C_H} - V_{oQ}(s) \cdot \frac{1}{1 + sR_{eq}C_H}, \quad (4)$$

and

$$V_{oQ}(s) = I_Q(s) \cdot \frac{R_{eq}}{1 + sR_{eq}C_H} + V_{oI}(s) \cdot \frac{1}{1 + sR_{eq}C_H}. \quad (5)$$

By defining a differential complex output as $V_{oC}(s) = V_{oI}(s) + jV_{oQ}(s)$, and differential complex input current as $I_{in,C}(s) = I_I(s) + jI_Q(s)$, the complex s-domain transfer function of the CS-BPF can be derived from (4) and (5) as

$$H(s)|_{s=j\omega} = \frac{V_{oC}(s)}{I_{in,C}(s)} = \frac{R_{eq}}{1 - j(1 - R_{eq}C_H\omega)}. \quad (6)$$

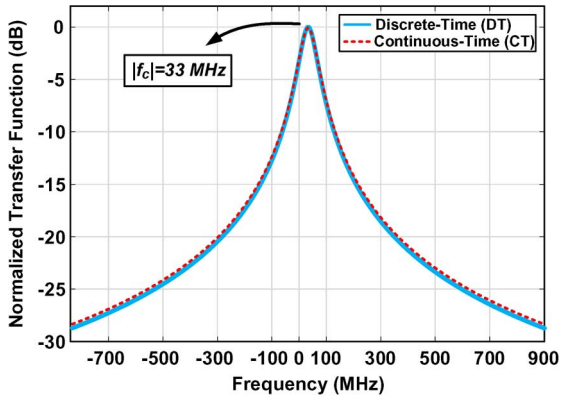

Fig. 8. Transfer function comparison between the discrete-time CS-BPF and its continuous-time model.

Consequently, the center frequency of the proposed CT-models lies at Fig. 7 is at

$$f_c = \frac{1}{2\pi R_{eq} C_H} \tag{7}$$

and the complex input impedance is equal to R_{eq}. Also, the bandwidth of the CS-BPF can be found from (6) and (3), which is equal to $1/(\pi R_{eq} C_H)$ for $a \approx 1$. Therefore, there is always a direct relationship of $f_c \approx BW/2$ for $a \approx 1$. It should be mentioned that (6) can be derived from (3) by performing a bilinear transformation with an approximation of $sT_s < 2$ and substituting $z = (2 + sT_s)/(2 - sT_s)$ and $s = j\omega$ into (3). As an example, for a CS-BPF with $C_R = 1$ pF, $C_H = 19$ pF and $f_s = 4$ GHz, we find $R_{eq} = 250\ \Omega$ and $f_c = 33.5$ MHz. The corresponding DT and CT transfer functions are plotted in Fig. 8 and show excellent agreement.

IV. Noise Analysis of CS-BPF

The total output noise of the CS-BPF contains the noise of all switches within the passive switched-capacitor network. At first, let us analyze the noise of the simplest switched-capacitor circuit in Subsection A. Afterwards, the detailed noise analysis of the CS-BPF will be described for DT/CT model in Subsection B.

A. Voltage Sampler Output Noise

A voltage sampler that includes noise of its switch is drawn In Fig. 9(a). Let us assume that V_{in} is zero. When the switch is turned on, it has a finite resistance R_{on}. A series voltage source models the resistor's thermal noise with a constant power spectral density (PSD), as shown in Fig. 9(b).

$$S_R(f) = 4kTR_{on}, \qquad f \geq 0 \tag{8}$$

where k is Boltzmann constant and T is the absolute temperature. When the switch is on, noise of the resistor is shaped by the RC filter with a time constant of $\tau = R_{on}C_R$ and then appears at the output. At the moment the switch is disconnected, the output noise is sampled and held on C_R. The periodical sampling at f_s causes noise folding from frequencies higher than $f_s/2$, to the 0-to-$f_s/2$ range where they add up, as shown in Fig. 9(c). If the time constant τ is much shorter than the turn-on time of the switch, it can be shown that the summation of all folded noise will be flat (i.e., white noise) [21]. As shown in Fig. 9(d), the single-sided noise spectral density of the sampled output noise is [21]

$$\overline{v_n^2}(f) = \frac{kT}{C_R f_s/2}, \quad 0 \leq f \leq f_s/2. \tag{9}$$

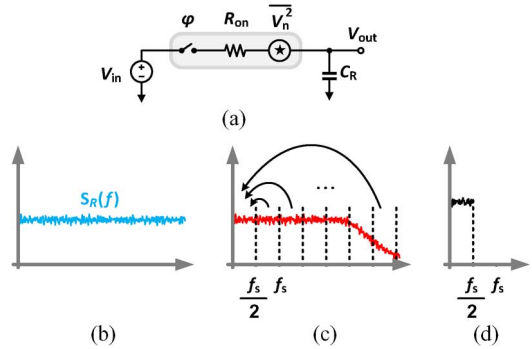

Fig. 9. (a) Noise circuit model of a voltage sampling process. (b) Noise of a switch resistance. (c) Noise shaped by RC filter. (d) Sampled noise.

It should be noted that the integrated power density of this noise over the entire frequency range is kT/C_R.

To simplify calculations for more complicated switched-capacitor circuits, we can make the following assumption: the continuous-time noise source with PSD of (8), can be considered as a discrete-time noise source with PDS described in (9). In this way it is not necessary anymore to consider the effect of RC filtering.

B. DT CS-BPF Noise Model

The simplified noise model of CS-BPF for only one C_R is shown in Fig. 10. The input charge packets are assumed zero and the switches are assumed ideal. The first purpose of the following calculations is to find the DT output noise levels $\overline{V_{oIp}}, \overline{V_{oQp}}, \overline{V_{oIn}}$, and $\overline{V_{oQn}}$ generated by input noise sources $\overline{V_{n1}^2}, \overline{V_{n2}^2}, \overline{V_{n3}^2}$ and $\overline{V_{n4}^2}$. The second purpose is to find the total pseudo-differential output noise of I or Q paths in both DT and CT models. The above mentioned input noise sources have two conditions: (1) they are uncorrelated, and (2) the stochastic value of each of them is equal to (9). We first assume $\overline{V_{n2}^2}, \overline{V_{n3}^2}$ and $\overline{V_{n4}^2}$ are zero, to calculate the noise transfer function only from $v_n = \sqrt{V_{n1}^2}$ to all outputs. The time-domain noise outputs at $t = nT_s$ with respect to the input noise source $v_n[n]$ can be written as

$$V_{oIp}[n] = aV_{oIp}[n-1] + bV_{oQn}[n-1] + bv_n[n], \tag{10}$$

$$V_{oQp}[n] = aV_{oQp}[n-1] + bV_{oIp}[n-1] - bv_n[n-1], \tag{11}$$

$$V_{oIn}[n] = aV_{oIn}[n-1] + bV_{oQp}[n-1], \tag{12}$$

and

$$V_{oQn}[n] = aV_{oQn}[n-1] + bV_{oIn}[n-1] \tag{13}$$

where, $a = C_H/(C_H + C_R)$, and $b = 1 - a$ are the same as before. By converting the time-domain expressions to z-domain, we find DT noise transfer functions as,

$$H_1 = \frac{V_{oIp}}{v_n} = -\frac{b(1-az^{-1})^3 - b^3 z^{-4}}{b^4 z^{-4} - (1-az^{-1})^4}, \tag{14}$$

$$H_2 = \frac{V_{oQp}}{v_n} = \frac{a(1-az^{-1})^3(1-z^{-1})}{b^4 z^{-4} - (1-az^{-1})^4} \cdot \left(\frac{bz^{-1}}{1-az^{-1}}\right), \tag{15}$$

$$H_3 = \frac{V_{oIn}}{v_n} = \frac{a(1-az^{-1})^3(1-z^{-1})}{b^4 z^{-4} - (1-az^{-1})^4} \cdot \left(\frac{bz^{-1}}{1-az^{-1}}\right)^2, \tag{16}$$

and

$$H_4 = \frac{V_{oQn}}{v_n} = \frac{a(1-az^{-1})^3(1-z^{-1})}{b^4 z^{-4} - (1-az^{-1})^4} \cdot \left(\frac{bz^{-1}}{1-az^{-1}}\right)^3. \tag{17}$$

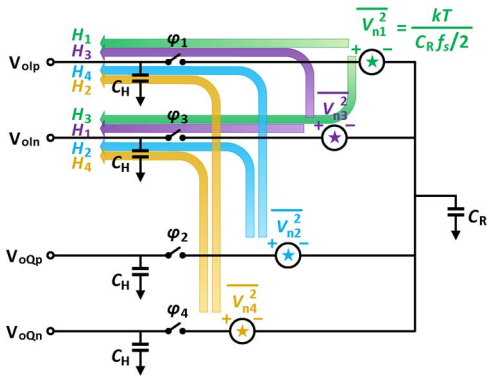

Fig. 10. CS-BPF noise model for only one of the switches.

The above expressions are derived based on the assumption of $\overline{V_{n2}^2}$, $\overline{V_{n3}^2}$ and $\overline{V_{n4}^2}$ being zero. It should be mentioned that, since the circuit is symmetric for all four input noise sources in Fig. 10, the noise TF of other DT input noise sources to output combinations are exactly the same as (14)–(17). The only difference is that the outputs in the expressions should be changed according to the DT input noise sources; for instance the noise TF of $\sqrt{V_{n3}^2}$ to V_{oIn} is the same as (14). The detailed noise TF for each DT input noise is also illustrated in Fig. 10. To calculate a differential DT output noise $(V_{on} = V_{oIp} - V_{oIn})$ with respect to all four input noise sources, we should consider that the differential DT output noise is composed of a sum of four uncorrelated noise contributions, as shown in Fig. 10. Also, each of them has two correlated noise contributions in the differential output. The correlated noises are shown with the same color (see Fig. 10). Therefore, we find the DT differential output noise PSD as

$$\overline{V_{on}^2} = \left|(H_1 - H_3)^2\right| \overline{V_{n1}^2} + \left|(H_4 - H_2)^2\right| \overline{V_{n2}^2} + \left|(H_3 - H_1)^2\right| \overline{V_{n3}^2} + \left|(H_2 - H_4)^2\right| \overline{V_{n4}^2}. \quad (18)$$

Since the absolute value of four input sources are the same, (18) can be simplified as

$$\overline{V_{on}^2} = \left(2\left|(H_1 - H_3)^2\right| + 2\left|(H_2 - H_4)^2\right|\right) \cdot \overline{V_{n1}^2}, \quad (19)$$

and by substituting $z = e^{j\omega/f_s}$, the differential output noise PSD is simplified to (20). (See equation at the bottom of the page.) The comparison of calculated output noise PSD based on (14)–(17) with transistor-level simulations are illustrated in Fig. 11, for $C_R = 4$ pF, $C_H = 19$ pF, and $f_s = f_{LO} = 1$ GHz. The differential output noise PSD of the CT model of Fig. 7 can be calculated based on the same approach; DT noise PSD derived in (20). We find the total CT differential output $(V_{oIp} - V_{oIn})$ noise PSD as

$$\overline{V_{on}^2}(\omega) = \left(\frac{2(R_{eq}C_H\omega)^2 + 4}{(R_{eq}C_H\omega)^4 + 4}\right) \cdot (4kTR_{eq}). \quad (21)$$

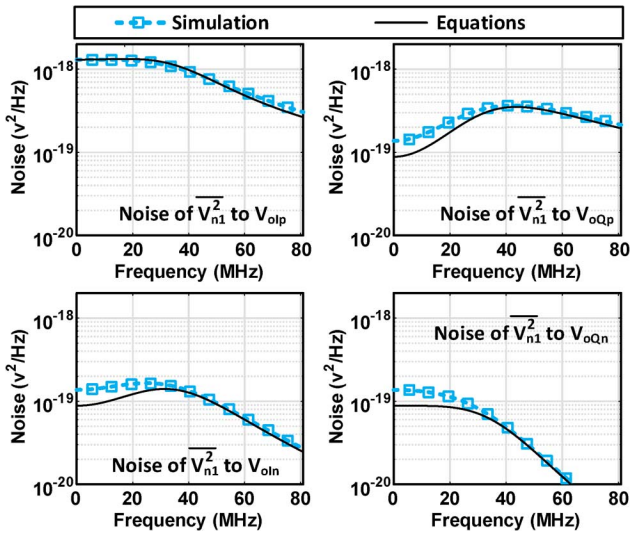

Fig. 11. Output noise PSD calculations compared with transistor-level simulations.

It should be pointed out that integrating the DT differential output noise PSD in (20) over 0-to-$f_s/2$ yields kT/C_T, with C_T being the total differential output capacitance equal to $(C_H + C_R)/2$. On the other hand, integrating the CT noise PSD in (21) over the entire range of 0 to ∞ is again equal to kT/C_T, with $C_T = C_H/2$. Note that the unity gain buffers in Fig. 7 are merely conceptual to account for the DT isolation, hence noiseless. If one were to implement the CT circuit of Fig. 7, noise contributions of the buffers would have to be accounted for. Consequently, the DT CS-BPF of Fig. 5 has a potential to out-perform its CT counterpart.

As the final verification, Fig. 12 compares the total output spot noise plots obtained via the diverse means: calculated DT, based on (20); calculated CT, based on (21); and schematic-simulated DT. The following conditions are used: $C_R = 4$ pF, $C_H = 19$ pF, and $f_s = f_{LO} = 1$ GHz. Although all simulations and calculations are performed for the CS-BPF with one C_R, the presented approach is valid for the full-rate CS-BPF with only one difference: the f_s in full-rate CS-BPF is 4 times higher than CS-BPF with one C_R.

V. Circuit Implementation

To accurately measure the BPF linearity, we have replaced the LNTA with a simple self-biased inverter-based transconductance amplifier (g_{mRF}) for higher IIP3, and designed for small transconductance as not to degrade the linearity. Since the gain provided by g_{mRF} is small, its contribution to the input-referred-noise (IRN) is predominant. The schematics of the g_{mRF} and RF mixer are shown in Fig. 13. The self-biasing of g_{mRF} is accomplished by R_c resistors connecting its input and output. The value of R_c in parallel with the output impedance of g_{mRF}

$$\overline{V_{on}^2} = \frac{2b^2\left(\left(\cos\left(\frac{w}{fs}\right)\right)^2 b - a\cos\left(\frac{w}{fs}\right) + a^2\right)}{(b^2+a^2)\left(\cos\left(\frac{w}{fs}\right)\right)^2 + (2b^3 - 4b^2 + 4b - 2)\cos\left(\frac{w}{fs}\right) + a^2(b^2+1)} \cdot \left(\frac{kT}{C_R f_s/2}\right) \quad (20)$$

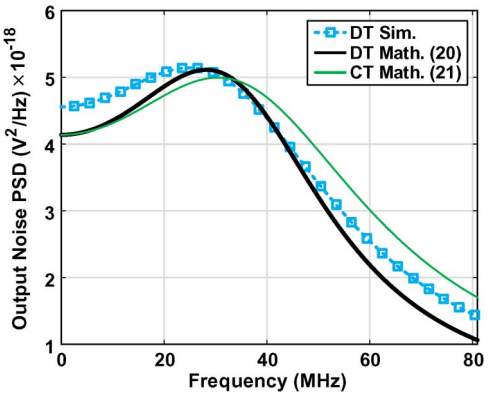

Fig. 12. Output noise PSD calculations compared with simulations.

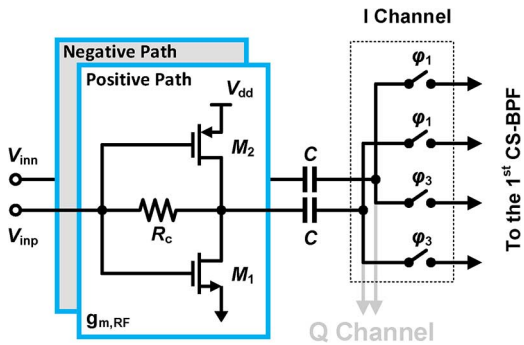

Fig. 13. Circuit implementation of g_{mRF} and mixer.

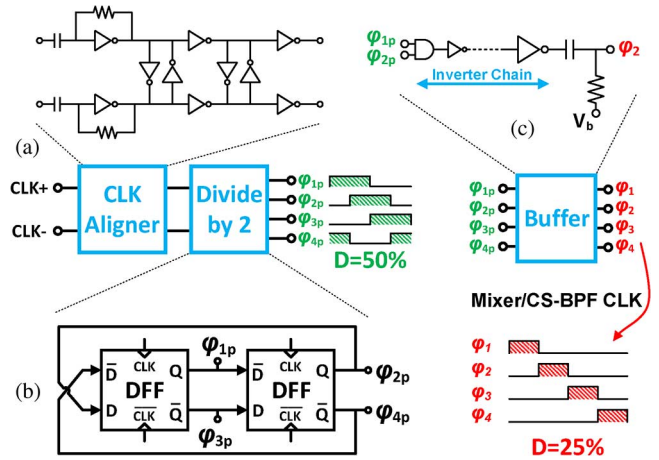

Fig. 14. Schematic of the clock generation circuit (a) CLK aligner circuit, (b) Divider and (c) 25% clock generation circuit with buffer stage.

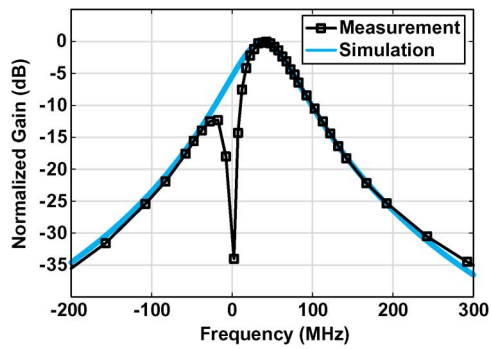

Fig. 15. Comparison of measured transfer function with an ideal transfer function that includes output impedance of g_m-cells.

should be high enough as not to degrade the Q of 1st CS-BPF. The DC block capacitors (C) are used to eliminate the DC current flowing into CS-BPF. The differential RF input voltage to g_{mRF} is converted to a pseudo-differential AC current feeding the commutating CMOS passive mixers of I and Q channels. The RF mixer in Fig. 13 is only shown for the I channel.

The clock phases φ_1 and φ_3 comprise a pseudo-differential 25% duty-cycle (D) LO clock driving the CMOS switches. Fig. 14 presents the clock generation circuit for both the mixer and CS-BPF. The differential input clock, CLK, with D $= 50\%$ is applied to the aligner circuitry that is responsible to compensate for any phase mismatch between the CLK+ and CLK- differential phases. The CLK aligner circuit (see Fig. 14(a)) consists of two inverters at the input to convert the sinusoidal inputs to the square-wave clock with D $= 50\%$ and the two stages of back-to-back inverters for further aligning the complementary edges of the square-wave clock.

As shown in Fig. 14(b), the divide-by-2 circuit consists of two D flip-flops arranged in the loop to generate the D $= 50\%$ clocks, φ_{1p}, φ_{2p}, φ_{3p} and φ_{4p}, with 25% delay between adjacent edges. The mixer clock is generated by the buffer shown in Fig. 14(c). The CS-BPF switches are driven by the clocks generated in another buffer with the same schematic as drawn in Fig. 14(c). It comprises AND gates and the chain of inverters for proper driving of the load capacitance of NMOS switches. Also, to increase the driving capability of sampling switch transistors in the quadrature mixer and CS-BPF, a clock boosting technique (using V_b, see Fig. 14(c)) is utilized to increase gate-source voltage while the pass transistor is turned on.

The CS-BPF operates at clock frequency f_{LO} with 25% duty-cycle clocks and its effective (i.e., differential I/Q) sampling frequency f_S is equal to $4f_{LO}$. Thus, the effective sampling time T_S is equal to $1/(4f_{LO})$. In order to maximize linearity, it is crucial to set the switch sizes of Fig. 5 in such a way that T_S would be between $3\tau - 4\tau$. τ is the $R_{on}C_R$ time constant of the DT circuit and R_{on} is an equivalent resistance of the sampling transistor in the triode region. The output resistance of the IF g_m-cell should be at least $3\times$ higher than R_{eq} in order to not decrease the Q and bandwidth of the following CS-BPF.

VI. Measurement Results

The proposed RX with the same structure as Fig. 3 but with three-stage CS-BPF together with its surrounding circuitry was fabricated in TSMC 1P7M 65 nm CMOS. The chip micrograph is shown in Fig. 19. The implemented RX occupies 0.45 mm^2 and consumes 24.5 mA at 1.2 V.

The measured complex transfer function of the RX is shown in Fig. 15. The measured curve is also compared to an ideal mathematic transfer function that includes the output impedance of all g_m-cells, which was extracted from transistor-level simulations. The measured curve shows a very good agreement with the mathematic modeling except for a notch at DC. It is due to the high-pass characteristic of a DC block capacitor in the g_m-cell (see Fig. 3) together with the resistor providing bias and common-mode voltages.

To demonstrate the CS-BPF reconfigurability, the measured transfer functions for different center frequencies f_c and bandwidths are depicted in Fig. 16. The transfer function rejection of the filter improves by increasing frequency without having any replica the same as Fig. 1(c). The measured center frequency of transfer functions are controlled by changing C_H (see (7)). C_H capacitors are implemented as a digitally switchable binary

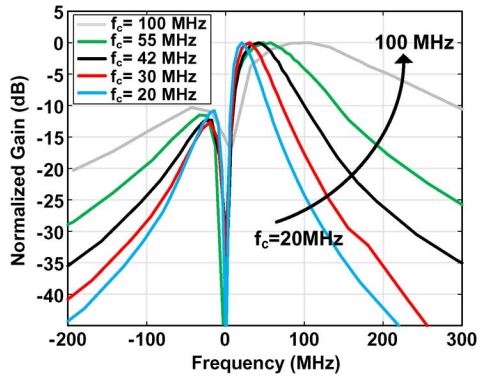

Fig. 16. Measured transfer function for different IF frequencies. Center frequency f_c aligns with f_{IF}.

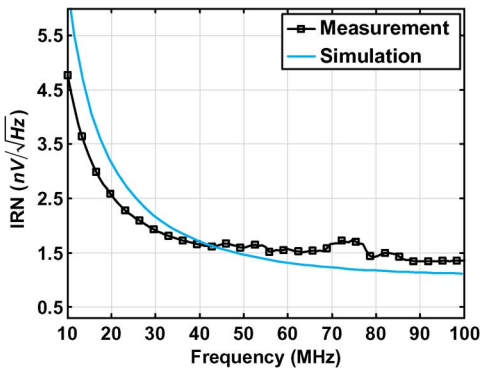

Fig. 17. Measured and simulated IRN for $C_H = 10$ pF and $C_R = 1$ pF.

weighted capacitor using the conventional MOM capacitors and MOS switches. Hence, the C_H value can be changed via 6 digital bits.

The complete front-end provides a total gain of 35 dB at the maximum gain setting. The measured and simulated IRN of the front-end are shown in Fig. 17 The abrupt increase in IRN at the low frequencies is caused by the flicker-noise of the g_m-cell at IF stage. As discussed in Section III, this curve suggests that the IF frequency should be placed at 30 MHz or a bit higher. Also, the reason that the measured IRN is high is that the front-end (g_{mRF} and 1st CS-BPF) gain is low not to sacrifice the linearity of the RX. As a consequence the higher IRN is measured.

Shown in Fig. 18, the out-of-band IIP3 of the RF frond-end ("$g_{mRF} + 1^{st}$ CS-BPF") is measured by applying two-tone at the input of the chip. The out-of-band two-tone frequencies are at 1100.009 MHz, 1200 MHz to have enough filtering at the output of RF frond-end for reducing the linearity contribution of the rest of the RX chain. The measured IIP3 is +9.5 dBm and we believe the measured IIP3 is chiefly limited by the linearity of the g_{mRF}-cell because the simulated IIP3 of the CS-BPF itself is more than +30 dBm. Table I shows summary of the filter and compares it to state-of-the-art. Compared to other designs except [12], the power consumption of our test chip is less but, the filter order of our test chip is two order higher than [12]. Compared to [13], the power consumption of our test chip is almost half for the highest sampling frequency. Also, CS-BPF provides higher reconfigurability, and wider BW selectivity of 24–125 MHz. Also, It has a digitally controllable IF center frequency range of 20–100 MHz larger than $1/f$ corner frequency, unlike other filters [12], [13]. Although, input g_m-cell has degraded linearity of the test chip, the in-band and out-of-band IIP3 of 0 dbm and +10 dBm is achieved, respectively.

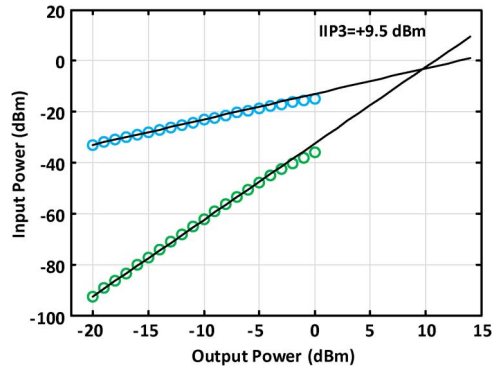

Fig. 18. The measured out-of-band IIP3 of the RF front-end ($g_{mRF} + 1^{st}CS - BPF$).

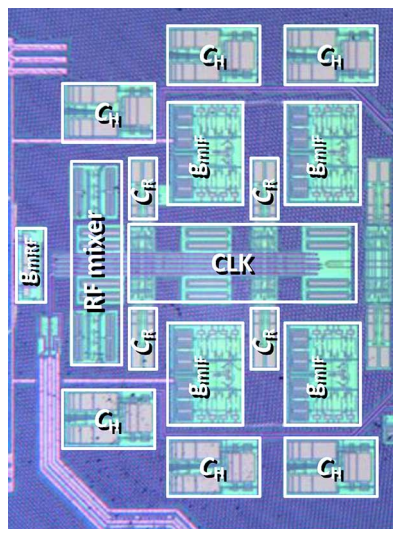

Fig. 19. Chip micrograph.

TABLE I
SUMMARY AND COMPARISON WITH STATE-OF-THE-ART

	This work	[7]	[12]	[13]
CMOS Tech. [nm]	65	65	65	65
Type	filter	receiver	filter	filter
Vdd [Volts]	1.2	1.2/2.5	1.2	1.2
Power [mW]	28	39	2-20	18-57
IRN [$nV/\sqrt{Hz}$]	1.5	0.87	0.9-1.3	0.87
IB-IIP3 [dBm]	0	N.A	N.A	−12
OB-IIP3 [dBm]	+9.5	N.A	+14	+26
BW [MH]	24—125	4	35	8
Filter order	6	6	2	6
IF Freq. [MHz]	20—100	62	—-	—-
Freq. Range [GHz]	0.5—1.2	1.8-2.2	0.1-1	0.1-1.2
Active Area [mm^2]	0.19	0.76	0.07	0.27

VII. CONCLUSION

Process-scalable fully integrated band-pass filters (BPF), free from replicas to be suitable for high-IF or superheterodyne receivers (RX) are in high demand to solve the issues related to continuous-time (CT) and N-path filters. In this paper, we propose and analyze a discrete-time (DT) charge-sharing (CS) BPF that is entirely passive and uses transistors only as switches. The center frequency of the proposed BPF filter is digitally controllable via clock frequency and capacitor ratios and thus insensitive to PVT variations. It is free from aliasing and replicas while operating at a GSample/s rate. The proposed filter performance

is verified in 65 nm CMOS for the wide RF frequency range of 0.5–1.2 GHz and a digitally controllable center frequency of 20–100 MHz. Measured noise performance and transfer function of the filter accurately fit both the mathematical theory and the CT schematic model. The experimental results indicate the proposed filter to be a prime candidate for future superheterodyne receivers.

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