

0.35-V SR-Enhanced Bulk-Driven OTA for Loads up to 10 nF

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Abstract—This study presents a low-voltage bulk-driven CMOS operational transconductance amplifier (OTA) operating in the subthreshold region designed to drive loads up to 10 nF, which is the largest value for this class of amplifiers. To meet this goal, the solution exploits the body terminal of various active devices leveraging local positive feedback to enhance the input transconductance gain and implementing dynamic threshold voltage control in the output transistors. This, along with a Slew Rate Enhancer section, significantly improves the OTA current driving capability. Experimental measurements conducted on a prototype, implemented in a 60-nm technology and supplied from 0.35 V, confirm the expected performance demonstrating a SR of 1.1 V/ms for a 10-nF load with a limited quiescent current consumption of 1.4 μ A.

Index Terms—Bulk-driven, CMOS analog integrated circuits, low-voltage, operational transconductance amplifier.

I. INTRODUCTION

THE growing demand for ultra-low-voltage, ultra-low-power integrated circuits (ICs) in portable, wearable, and implantable electronics, [1], [2], [3], necessitates the exploration of novel circuit topologies and design methodologies aimed to preserve the performance characteristics of well-established complementary metal-oxide-semiconductor (CMOS) solutions while optimizing, particularly in the analog domain, input/output voltage swing and minimizing required supply voltage.

To this end, the application of body-driven (BD) techniques has attracted considerable attention among circuit designers in

recent years [4], [5], [6], [7], [8]. This interest stems from the advantageous absence of a threshold voltage when driving MOS field-effect transistor (MOSFET) devices via their body terminals. The suitability of the BD approach has been proven, specifically in the realization of Operational Transconductance Amplifiers (OTAs) operating under supply voltages as low as 250 mV [9], [10], [11], [12], [13], [14], [15], [16], [17], [18], [19], [20], [21], [22], [23], [24], [25], [26], [27], [28], [29].

Notably, this methodology facilitates the attainment of the widest common-mode input range, approaching the rail-to-rail limit. Additionally, it often results in overall quiescent current consumption of a few microamperes or less, achieved through suitable biasing of MOSFETs in their sub-threshold region.

A severe limitation arises when comparing BD CMOS OTAs with standard gate-driven counterparts, wherein the constrained body transconductance, constituting a fraction of the gate transconductance, leads to a simultaneous reduction in overall voltage gain, gain-bandwidth product (GBW), and an increase of the equivalent input noise. Addressing this challenge is a prevalent trend in the current literature and involves the design of solutions aimed at improving the OTA's small signal performance, encompassing parameters such as gain, gain-bandwidth, and settling time. Techniques such as gain-boosting, partial positive feedback, quasi floating gate, and current recycling have been adopted [12], [15], [18], [20] concurrently accompanied by an effort in reducing quiescent current consumption [13], [14], [17]. Another issue with BD structures is the need to prevent the body-source junction from turning on. Fortunately, this is not a significant concern when the supply voltage is below 500 mV [6].

It is noteworthy that the adoption of extremely low supply voltages, on the order of a few hundred millivolts, mandates an equivalent maximum OTA output voltage swing, consequently rendering slew rate (SR) performance a matter of marginal interest in initial implementations which also targeted GBW limited to a few kilohertz. Nonetheless, as mentioned above, recent research has focused on endowing circuits with larger GBW and off-chip driving capabilities, prompting investigations into OTAs that demonstrate closed-loop stability with capacitive loads in the range of several tenths of picofarads [21], [22]. In this context, SR emerges as an important limiting factor in the amplifier's time response. Particularly, for class A but also class AB solutions, the combination of substantial load capacitance (hundreds of picofarads) and

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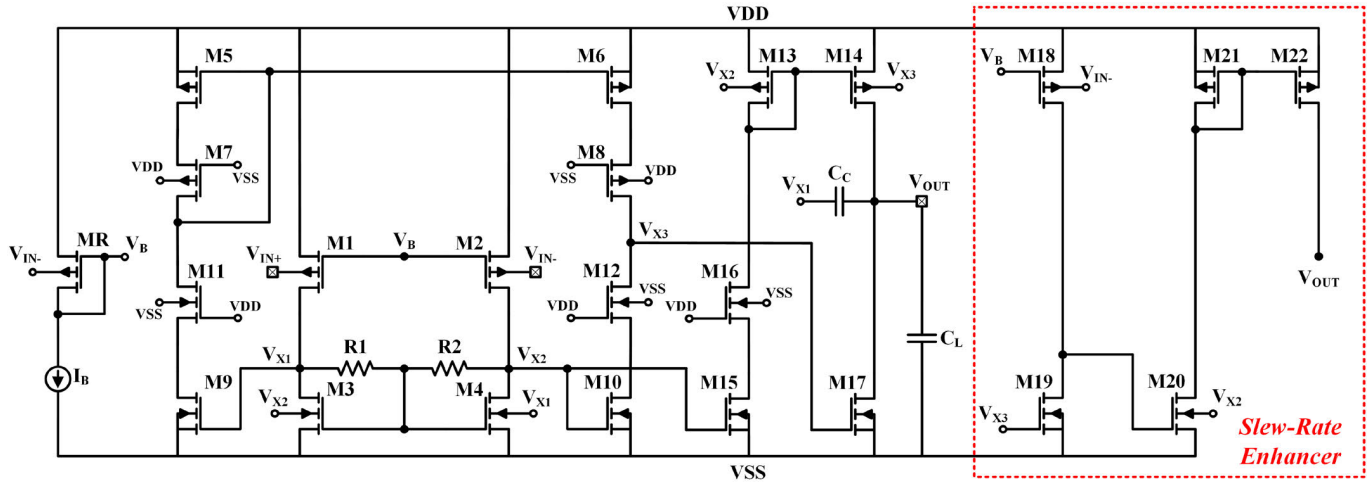


Fig. 1. Schematic diagram of the proposed BD OTA.

limited standby current (a few microamperes or less) may yield insufficient SR performance. Experimental observations have often indicated unbalanced positive and negative SR values in these scenarios. In light of this, a (limited) number of studies have delved into SR enhancement techniques, as exemplified by the findings detailed in [20] which showcased the feasibility of a 91-nA OTA effectively driving a 15-pF load and achieving a noteworthy SR of 8.6 V/ms. Other examples of class AB BD OTAs can be found in [12], [19], [22], and [25].

This manuscript delves into design solutions aimed at improving the SR performance of a tail-less BD OTA. Our approach involves leveraging the body terminal of various transistors, particularly those in the output stage's class AB section, to implement dynamic threshold voltage control. This strategy, combined with the integration of a SR Enhancer (SRE) subsection, enables the OTA to effectively drive load capacitors of up to 10 nF. Notably, the SRE operates in an off state under quiescent conditions, enhancing the output current in the weaker pull-up driving path. This contributes to an overall improvement in SR performance without a significant increase in quiescent current consumption. It is important to highlight that amplifiers capable of driving large capacitive loads, even in the nanofarad range with kilohertz bandwidth, are required in many applications, such as line drivers, low-dropout regulators (LDOs), LCD column drivers, micro-electro-mechanical systems (MEMS) sensors, headphone drivers, etc., [27], [31], [32], [33].

The paper is organized as follows. The presented solution is described in Sec. II, where particular focus is directed towards elucidating the primary novel design solutions and fundamental design equations. Section III delves into the simulations conducted to assess the proposed solution, while Section IV discusses the experimental results obtained. The paper is concluded with the authors presenting their findings and drawing conclusions.

II. THE PROPOSED SOLUTION

The proposed solution was derived from the configuration presented by the same authors in a prior work [22],

which provided effective quiescent current control and demonstrated also excellent small signal and large signal performance metrics. In the present study, we have incorporated several SR-enhancement techniques onto this established framework, thereby seeking further refinement in the amplifier's dynamic response characteristic even under lower quiescent current and larger capacitive load.

A. Topology, Biasing, and Large Signal Operation

The simplified schematic diagram of the proposed OTA is depicted in Figure 1. The input stage is realized through transistors M1 and M2, constituting a tail-less body-driven p-channel transistor pair. The quiescent current of this pair is established by I_B and diode-connected transistor MR. Consequently, the quiescent current flowing through M1 and M2 is determined by I_B multiplied by the mirror ratio $(W/L)_{1,2}/(W/L)_R$. Note that, owing to the OTA's input virtual short, these transistors share at DC the same body voltage and hence the same threshold voltage.

The active load for the input stage is formed by transistors M3 and M4, incorporating negative-feedback resistors R1, R2 crucial for the differential-mode gain. Moreover, this load configuration imparts differential capability to the inherently pseudo-differential pair [12]. Notably, local positive feedback is introduced by cross-connecting the body of M3 to the drain of M4 and the body of M4 to the drain of M3, thereby enhancing the equivalent input-stage transconductance [22].

The second stage, providing cascoded high-output-impedance and differential-to-single-ended conversion, is implemented by transistors M5-M12. The quiescent current in this stage is determined by the mirroring action between the pair M3, M4 and M9, M10, because, at DC, no current flows through resistors R1-R2, rendering M3 and M4 as diode-connected devices. Note that being $V_{BS3,4} = V_{GS3,4}$ while $V_{BS9,10} = 0$ this current mirror gain is found to be

$$\frac{I_{D9,10}}{I_{D3,4}} = \frac{(W/L)_{9,10}}{(W/L)_{3,4}} \left[1 - \frac{\gamma (\sqrt{2\phi_F + V_{GS3,4}} - \sqrt{2\phi_F})}{V_{GS3,4} - V_{Tn0}} \right]^{-2} \quad (1)$$

where the threshold voltage of a nMOS is expressed usual by

$$V_{Tn} = V_{Tn0} + \gamma \left(\sqrt{2\phi_F + V_{BS}} - \sqrt{2\phi_F} \right) \quad (2)$$

and being V_{Tn0} the zero-bias threshold, ϕ_F the Fermi potential and γ the body effect parameter. As a result, the current mirror ratio in (1) is lower than that of a conventional current mirror in which the factor in the square brackets equals 1.

The output stage, which drives the load capacitor C_L , is made up of common-source transistor M17, complemented by active load M13-M16. The quiescent current of the output branch is regulated by the current mirror gains of M3,4 to M15 and of M13 to M14. It is noteworthy that the pull-down output current supplied by M17 may exceed the quiescent value, akin to the pull-up current provided by M14, albeit to a lesser extent. Therefore, both M14 and M17 operate in class AB, but the positive-going output step exhibits a slower response than its negative-going counterpart owing to the diminished maximum possible variation of voltage V_{X2} (i.e., the gate-source voltage of M15) compared to V_{X3} (i.e., the gate-source voltage of M17) in Fig. 1.

To improve the positive SR of the basic solution, a first modification involves a dynamic adjustment of the gain in the current mirror formed by transistors M13-M14, dependent upon the required current level to be delivered. This objective is achieved by connecting the body of transistor M13 to the drain of M4 and the body of transistor M14 to the drain of M8 (M12), as illustrated in Fig.1. This configuration exploits the dependence of the threshold voltage of M13 and M14 to variations in V_{X2} and V_{X3} . Specifically, when the output stage is tasked with supplying current, an increase in V_{X2} and a corresponding reduction in V_{X3} occurs, thereby incrementing the threshold voltage of M13 and decrementing that of M14 and increasing in turn the current mirror gain.

As an illustration of the process involved, consider Fig. 2a, wherein a p-channel current mirror analogous to M13-M14 in Fig. 1 is implemented using transistors MC1-MC2. These transistors share identical aspect ratios of 40/0.5 and have bulk voltages V_{B1} and V_{B2} , respectively. The current mirror attains a unitary gain provided that the bulk voltages are equal (in our case $V_{B1} = V_{B2} = V_{DD} - 0.15$ V). Figure 2b depicts the current gain of the mirror in response to a variation in $V_{B1} - V_{B2}$. Notably, a substantial current gain increase, reaching up to a factor of five, is evident for $V_{B1} > V_{B2}$. Conversely, a current gain decrease is observed for $V_{B1} < V_{B2}$.

The second improvement is accomplished by the inclusion of a Slew-Rate Enhancer (SRE) section made up of transistors M18-M22. The objective of the SRE is to augment the current supplied by the OTA to the load, as done for instance in [27]. Essentially, it introduces an additional driving branch operating in parallel to transistor M14 and functions as follows. Transistor M18 serves as a constant current source, mirroring the current from MR, I_B , with a gain reduction determined by the ratio $(W/L)_{18}/(W/L)_R$. Note that the bulk of M18 is tied to IN $^-$ only to provide an accurate and predictable current mirror matching with MR. Concurrently, transistor M19, matched in V_{GS} with M17, is dimensioned such that under DC conditions, the nominal current through M17 multiplied by $(W/L)_{19}/(W/L)_{17}$ surpasses I_{D18} .

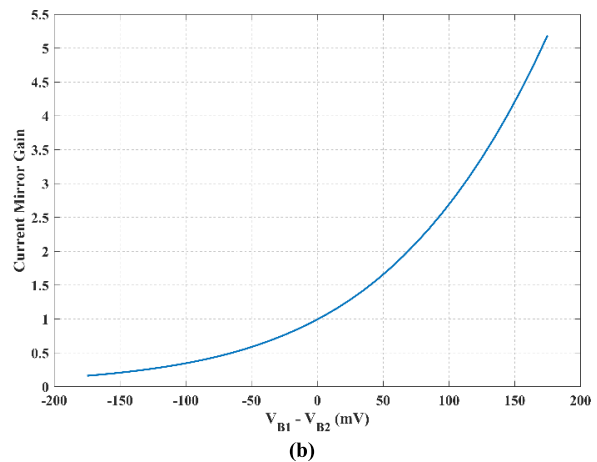
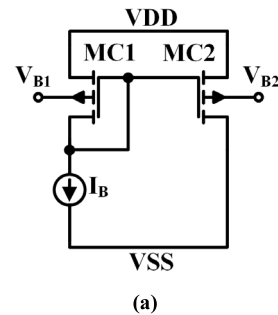


Fig. 2. Variable-gain current mirror: a) Schematic diagram, b) DC current-mirror gain I_{DC2}/I_{DC1} as a function of $V_{B1} - V_{B2}$. Transistors dimension is 40/0.5 with the models of a 60-nm CMOS technology.

Hence, under quiescent conditions, this configuration maintains a low drain voltage across M19, consequently deactivating transistors M20 and in turn M21 and M22. Under large signal conditions, when V_{IN+} increases and a similar increase in V_{OUT} is required, V_{X2} rises augmenting the current in M15 and M14, while V_{X3} decreases turning off M16. This action results in an elevation of the drain voltage across M19, turning on M20. Subsequently, through the mirror M21-M22, M22 contributes its drain current in parallel with that of M14, thereby reinforcing the current supplied to the load capacitor C_L . It is worth noting that the SR enhancement performance is further empowered by driving the bulk of M20 by V_{X2} , so that the threshold voltage of M20 decreases when I_{D20} must increase.

A concluding remark concerns the connection of the body of MR, and thereby of M18, to the inverting input, IN $^-$. This configuration is simpler compared to connecting these terminals to the common-mode input voltage, a step necessary in theory to nullify the common-mode gain of the input stage. This method eliminates the need for extracting the common mode of the two inputs.

B. Small-Signal Analysis

The overall OTA differential gain is given by

$$A_0 \approx G_{mb} r_{o1} g_{m9,10} r_{o2} g_{m17} r_{o3} \quad (3)$$

where g_{mi} is the gate transconductance of the i -th transistor and where r_{o1}, r_{o2} and r_{o3} are the output resistances of

TABLE I
STEP DIMENSION OF ACTIVE AND PASSIVE
COMPONENTS AND BIAS ELEMENTS

Device	W/L [$\mu\text{m}/\mu\text{m}$] \times Multiplicity	Device or Parameter	W/L [$\mu\text{m}/\mu\text{m}$] \times Multiplicity or Value
MR, M1, M2	$(50 / 0.5) \times 1$	M17	$(50 / 2) \times 3$
M3, M4	$(60 / 4) \times 1$	M18	$(2 / 0.5) \times 1$
M5, M6	$(50 / 1) \times 4$	M19	$(50 / 2) \times 1$
M7, M8	$(50 / 0.5) \times 2$	M20	$(20 / 0.5) \times 1$
M9, M10	$(60 / 4) \times 4$	M21, M22	$(50 / 0.5) \times 2$
M11, M12, M16	$(60 / 4) \times 3$	V _{DD}	0.35 V
M13	$(40 / 0.5) \times 1$	I _B	200 nA
M14	$(40 / 0.5) \times 14$	R1, R2	250 k Ω
M15	$(20 / 4) \times 5$	C _C	6.1 pF

the first, second, and third stage, respectively equal to $R_{1,2}/r_{d1,2}/r_{d3,4}$, $(g_{m12}r_{d12}r_{d10}) / (g_{m8}r_{d8}r_{d6})$, and r_{d14}/r_{d17} . Moreover, G_{mb} is the equivalent input transconductance expressed by

$$G_{mb} = \frac{g_{mb1,2}}{1 - g_{mb3,4}r_{o1}} \quad (4)$$

where $g_{mb1,2}$ and $g_{mb3,4}$ are the bulk transconductances of transistors M1-M2 and M3-M4, respectively.

As already mentioned, (4) shows that the differential-mode transconductance of the first stage is increased through positive feedback from the bulk-drain cross-connection of transistors M3 and M4. This result is similar to that found in [22]. During the design phase, careful attention should be given to ensuring that the denominator in (4) remains consistently positive across all process corners and temperature conditions. In summary, the strategy to achieve gain increase involves setting the denominator of (4) to be substantially less than 1 to avoid instability issues, as described in Sec. III.

Concerning frequency compensation, it is important to note that we follow the approach outlined in [22]. In this strategy, the dominant pole is established by Miller capacitor C_C for lower values of C_L (typically in the range of a few picofarads). However, compensation is shifted to the output pole for larger C_L values. This ensures OTA closed-loop stability over a wide range of load conditions. In this context, the dominant-pole angular frequency is found to be

$$\omega_{p1} \approx \frac{1}{g_{m9,10}g_{m14}r_{o1}r_{o2}r_{o3}C_C + r_{o3}C_L} \quad (5)$$

where the effect of C_C and C_L in the frequency compensation is apparent. The gain-bandwidth product, GBW, is of course given by the product of (3) and (5).

The proposed OTA was designed using a 65-nm CMOS bulk technology provided by TSMC and accessed through EURORACTICE. Component dimensions and bias elements are summarized in Table I. Supply is set to 0.35 V and the bias current I_B is 200 nA. A deliberately chosen lower overall current, compared to [22], is employed to accentuate the improvement in SR, albeit resulting in a lower GBW.

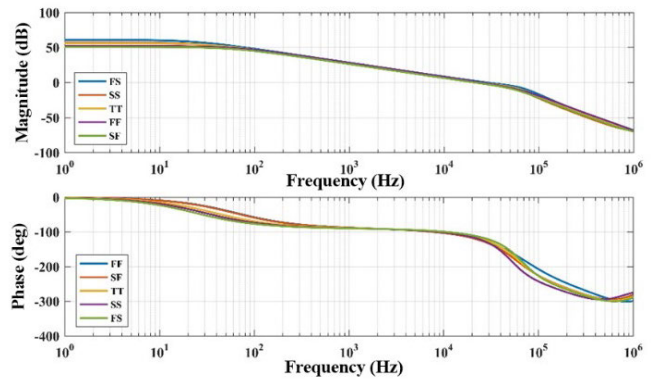


Fig. 3. Bode plots of OTA loop gain (magnitude and phase) across corners.

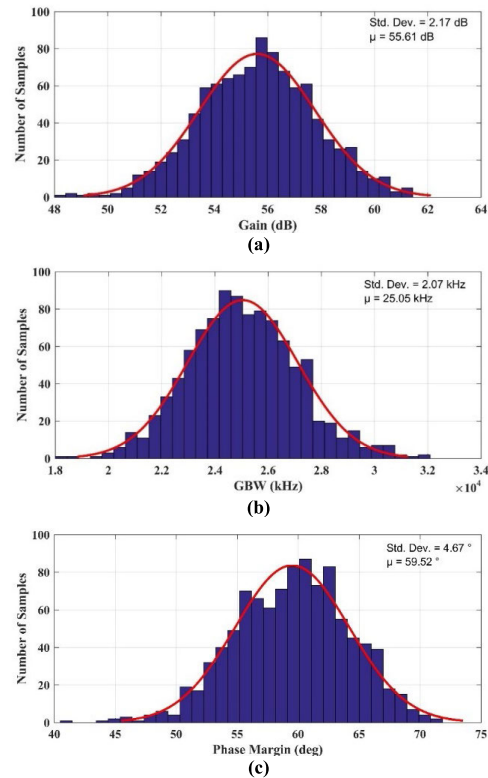


Fig. 4. Monte Carlo simulations of OTA DC gain (a), GBW (b), and PM (c).

III. DESIGN AND SIMULATION RESULTS

Some results of preliminary post-layout simulations are discussed in this section. The open loop frequency response (magnitude and phase) of the OTA with $C_L = 300$ pF is shown in Fig. 3 in nominal transistor conditions (TT case) and in the four process corners. The nominal DC gain is equal to 55.6 dB and the GBW is equal to 23 kHz. Phase margin (PM) is equal to 60° and the gain margin is equal to 8.9 dB. Note that $g_{mb3,4}r_{o1}$ was set about equal to 0.4, hence providing a 1.7 boost in the transconductance, as anticipated by (4). Stable performance is demonstrated also across the process corners from the same Fig. 3.

The robustness against process and mismatch variations was validated through Monte Carlo simulations, comprising 1000 iterations, as depicted in Fig. 4(a), (b), and (c) for DC gain, GBW, and PM, respectively, whose standard deviations are 2.17 dB, 2.07 kHz, and 4.67 degrees, respectively.

TABLE II
DC GAIN, GBW AND PM IN THE TYPICAL CORNER AT
DIFFERENT TEMPERATURE VALUES

Temp. [°C]	0	27	60	80	100
DC gain [dB]	55.1	55.6	56.2	55.6	51.9
GBW [MHz]	0.023	0.023	0.026	0.026	0.025
PM [deg]	52	60	68	72	76

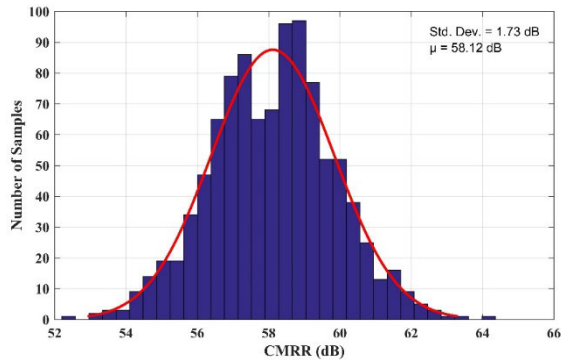


Fig. 5. Monte Carlo simulations of the CMRR.

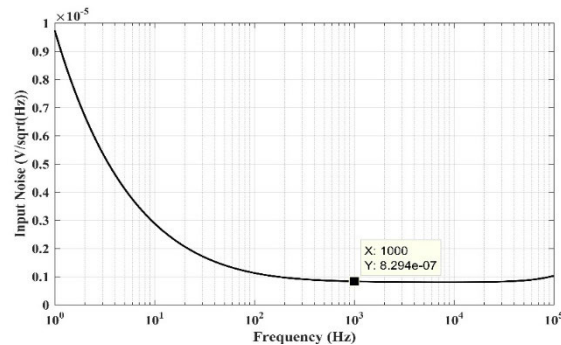


Fig. 6. Equivalent input noise.

Temperature-induced variations of the DC gain, GBW, and PM are simulated within the typical process model across a temperature span ranging from 0 °C to 100 °C. The summarized findings are presented in Table II, revealing nearly constant values of GBW with marginal variations in DC gain. Although PM exhibits a 24-degree variation, it remains within acceptable bounds, indicating satisfactory stability.

The simulation also included an assessment of the Common Mode Rejection Ratio (CMRR). The DC value achieved is 58.1 dB, representing a more than 15-dB improvement compared to the findings in [22]. Additionally, a Monte Carlo simulation of CMRR was performed, indicating a standard deviation of 1.73 dB, as depicted in Fig. 5.

The simulated input noise spectral density is shown in Fig. 6, at 1 kHz it is around 829 nV/√Hz (white noise).

Figure 7 shows the response to a 200-mV_{p-p} input step of the proposed SR-enhanced OTA in buffer configuration, compared to a version of the same OTA that does not include SR enhancement strategies, both driving 300 pF. In other words, with reference to Fig. 1, the latter case does not include the SRE section and transistors M13-M14 have their bulks conventionally tied to V_{DD} whereas M19

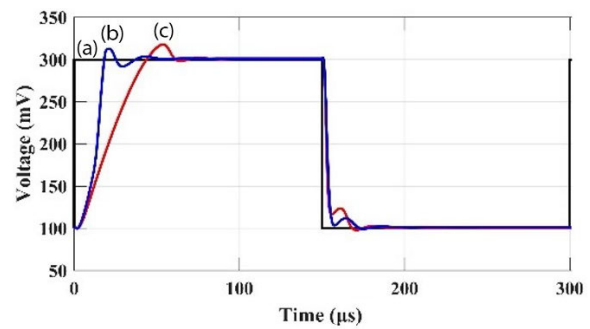


Fig. 7. Simulated time response of the OTA in buffer configuration ($C_L = 300$ pF): input 200-mV_{p-p} step (curve a), output with (curve b), and without (curve c) SRE techniques.

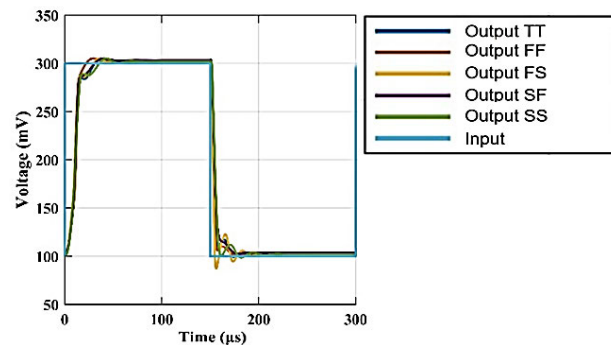


Fig. 8. Simulated output response of the OTA in unity gain to a 200-mV_{p-p} input step over five basic corners ($C_L = 300$ pF).

TABLE III
STEP RESPONSE OF THE OTA IN BUFFER CONFIGURATION
OVER CORNERS ($C_L = 300$ pF)

Corner	TT	FF	FS	SF	SS
SR+/SR- [V/ms]	23/-51	22/-61	21/-76	22/-33	18/-32
1% Settling Time (pos/neg) [μs]	37/34	30/22	36/33	40/45	41/52

to V_{SS}. Evidently, the positive-going output step exhibits a slower response compared to the negative-going counterpart. The application of the SR enhancement techniques markedly enhances this performance. Specifically, the positive SR without SRE is found to be 5 V/ms, while the positive SR value with SRE is notably improved, more than 4 times, to 23 V/ms.

The time response across the five fundamental process corners and under the identical conditions detailed above is illustrated in Fig. 8. The main outcomes are succinctly outlined in Table III. Remarkably, the SRE techniques render the positive Slew Rate (SR+) nearly insensitive to variations across the different corners.

IV. MEASUREMENT RESULTS AND COMPARISON WITH PRIOR ART

The micrograph of a fabricated prototype of the proposed circuit is illustrated in Fig. 9. The occupied area is 223 μm × 235 μm with the SRE accounting for approximately 13% of the total area. It is apparent that no area optimization technique was adopted for this prototype. The circuit is supplied with 0.35 V and the measured current consumption

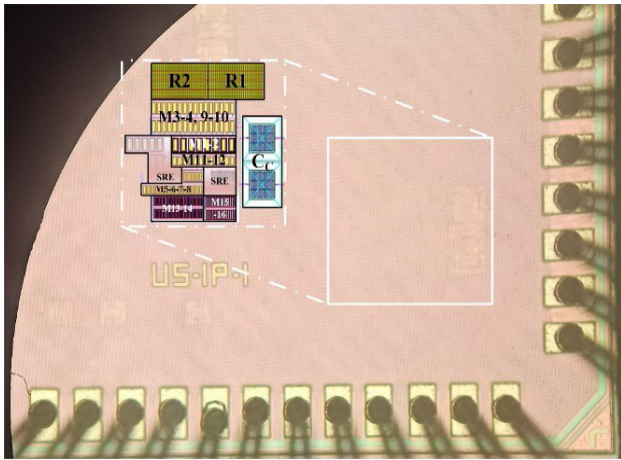
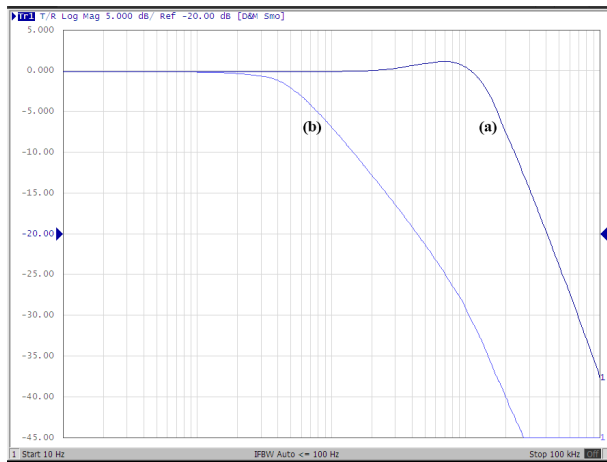
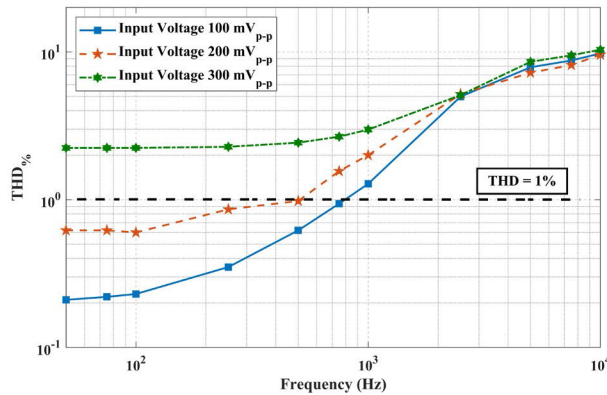
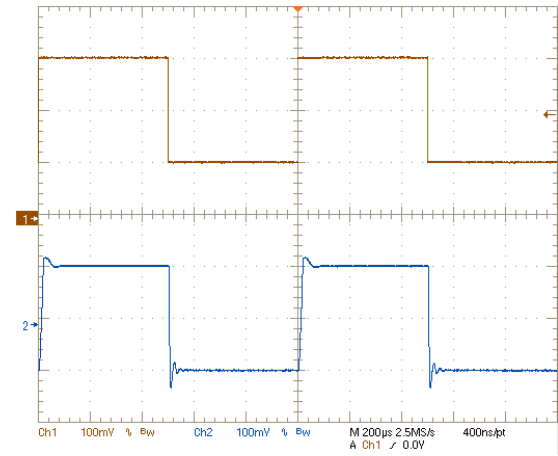
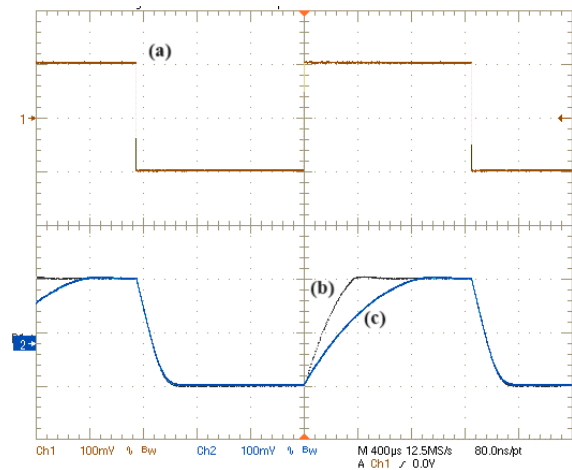


Fig. 9. Chip micrograph.

Fig. 10. Measured gain magnitude of the OTA in buffer configuration with $C_L = 300$ pF trace (a), and with $C_L = 10$ nF trace (b).Fig. 11. Measured THD (%) versus frequency of the OTA in buffer configuration ($C_L = 300$ pF) for three different inputs.

is $1.4 \mu\text{A}$. Fig. 10 depicts the gain magnitudes of the OTA in buffer configuration with 300-pF and 10-nF load capacitors. The -3dB frequency is around 16 kHz and 650 Hz, respectively.

The Total Harmonic Distortion (THD) of the output voltage versus frequency with the OTA in unity gain and with $C_L = 300$ pF, for different input amplitudes is shown in Fig. 11. THD below 1% is achieved for inputs below 200 mV_{p-p} and 500 Hz.

Fig. 12. Measured step response of the OTA in unity gain with $C_L = 100$ pF: 200-mVpp input step (upper trace) and output signal (lower trace).Fig. 13. Measured step response of the OTA in unity gain and with $C_L = 10$ nF: 200-mVpp input step (trace a), output (trace b) and output without SRE (trace c).TABLE IV
OTA MAIN PERFORMANCE ($C_L = 300$ pF)

Parameter [unit]	Value
Supply Voltage ($V_{DD}-V_{SS}$) [V]	0.35
DC Current [μA]	1.4
Offset maximum [mV], 5 samples	6.4
Input Common-Mode Range	$>90\%(V_{DD}-V_{SS})$
Max Input Current* [nA]	0.224
DC Gain [dB]*	>50 dB
GBW [kHz]	15.4
Phase Margin [deg]	65
Gain Margin [dB]	8.9
SR+/SR- [V/ms]	14.4/21.4
CMRR* @DC [dB]	58
PSRR*+* @DC [dB]	26.5
Input Ref. Noise* @1kHz [nV/ $\sqrt{\text{Hz}}$]	829
THD@500Hz, 200mV _{p-p} (%)	0.98

*Simulated values

Fig. 12 shows the response to a 200-mVpp step of the OTA in unity gain driving a 100-pF load. To highlight the effect of the adopted SR-enhancing techniques, Fig. 13 compares the response to the same input step of the OTA in unity

TABLE V
PERFORMANCE COMPARISON OF SUB-1V AMPLIFIERS

Ref.	[28] Qin	[12] Cabrera	[29] Grasso	[13] Kulej	[15] Kulej	[16] Woo	[22] Ballo	[26] Della Sala	Proposed		
Year	2016	2016	2017	2018	2020	2020	2023	2023	2024		
Op. mode*	GD	BD	GD	BD	BD	BD	BD	BD	BD		
Tech. [nm]	180	180	350	180	180	65	65	130	65		
Area [mm ² ×10 ⁻²]	1.82	1.98	1.43	0.82	0.98	0.23	0.106	0.234	5.2		
V _{DD} [V]	0.5	0.7	0.7	0.3	0.3	0.25	0.3	0.3	0.35		
I _Q [μA]	0.14	36	27	0.056	0.043	0.104	8.5	0.11	1.4		
C _L [pF]	40	20	10	20	30	15	50 150	35	300	1000	10000
DC gain [dB]	77	57	65	63	98.1	70	38	87	55		
GBW [MHz]	4 × 10 ⁻³	3	1	2.8 × 10 ⁻³	3.1 × 10 ⁻³	9.5 × 10 ⁻³	1.65 0.81	10.3 × 10 ⁻³	15.4 × 10 ⁻³	6.48 × 10 ⁻³	6.54 × 10 ⁻⁴
PM [deg]	56	60	60	61	54	88	70.3 71.3	58.3	65	73	82
PSRR @DC [dB]	52	52	50	62	61	38	44.7	46.6	26.5		
CMRR @DC [dB]	55	19	45	72	60	62.5	39.8	57.8	58		
SR** [V/μs]	2 × 10 ⁻³	1.8	0.25	6.4 × 10 ⁻³	4.2 × 10 ⁻³	2 × 10 ⁻³	0.11 0.07	2.5 × 10 ⁻³	14 × 10 ⁻³	10 × 10 ⁻³	1.1 × 10 ⁻³
IFOM _S [MHz·pF/μA] ⁽¹⁾	1.14	1.67	0.37	1.00	2.16	1.37	9.71 14.29	3.3	3.3	4.63	4.67
IFOM _L [V·pF/(μs·μA)] ⁽²⁾	0.57	1.0	0.09	2.29	2.93	0.29	0.65 1.24	0.80	3.0	7.14	7.85
IFOM _{AS} [MHz·pF/(μA·mm ²)] ⁽³⁾	62.64	84.34	25.87	121.95	220.41	595.65	9160.4 13481	1410.3	63.46	89.04	89.81
IFOM _{AL} [V·pF/(μs·μA·mm ²)] ⁽⁴⁾	31.32	50.51	6.29	279.27	298.98	126.09	613.21 1165.81	341.88	57.69	137.31	150.96

* GD: gate-driven; BD: bulk-driven; ** The minimum between SR+ and SR-.

$$^{(1)} IFOM_S = \frac{GBW}{I_Q} C_L, \quad ^{(2)} IFOM_L = \frac{SR}{I_Q} C_L, \quad ^{(3)} IFOM_{AS} = \frac{GBW}{I_Q \cdot Area} C_L, \quad ^{(4)} IFOM_{AL} = \frac{SR}{I_Q \cdot Area} C_L$$

gain loaded by 10 nF with and without the SR enhancer (traces b and c, respectively). The positive-going part of trace b is clearly improved, and it is now comparable with the negative going one. SR+ and SR- are 1.1 V/ms and 1.4 V/ms, respectively.

The main OTA performance parameters, with $C_L = 300$ pF, are summarized in Table IV. Measurement results match well with simulations. SR is large although slightly lower than what anticipated.

Finally, Table V compares the proposed OTA with the state of the art. It is apparent that our design is the sole to be able to drive up to 10 nF and with very good current efficiency, given the maximum value of the figure of merit IFOM_L (equal to $SR \cdot C_L / I_Q$) achieved. A very good IFOM_S is also observed. It is noteworthy, however, that this metric is not optimized intentionally through the utilization of an exceedingly low quiescent input stage current.

As a principal drawback, the OTA is characterized by the largest silicon area occupation. Indeed, while the SRE does not occupy a significant portion of the area, the OTA necessitates transistors with large overall aspect ratios to effectively drive the intended load capacitance. This aspect adversely affects our design when considering the figures of merit, IFOM_{AS} and IFOM_{AL}, as shown in the last two rows of Table V.

V. CONCLUSION

The paper builds upon a previously introduced low-voltage CMOS OTA that employs MOSFETs in the subthreshold region. The authors strategically leverage the body terminal

of various active devices to enhance large signal performance. In addition to implementing local positive feedback for improved input transconductance, the paper introduces dynamic threshold voltage control in the output transistors. This, combined with a Slew Rate Enhancer section, enables the OTA to efficiently drive a load capacitor (C_L) up to 10 nF, the largest reported for this class of amplifier. The frequency compensation scheme uses Miller compensation for low C_L and shifts to dominant-pole compensation for high C_L . Experimental measurements on a prototype in a 60-nm technology, powered by 0.35 V, confirm the expected performance providing the best large-signal figure of merit (IFOM_L).

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REFERENCES

- [1] T. He and C. Lee, "Evolving flexible sensors, wearable and implantable technologies towards BodyNET for advanced healthcare and reinforced life quality," *IEEE Open J. Circuits Syst.*, vol. 2, pp. 702–720, 2021.
- [2] R. Das, F. Moradi, and H. Heidari, "Biointegrated and wirelessly powered implantable brain devices: A review," *IEEE Trans. Biomed. Circuits Syst.*, vol. 14, no. 2, pp. 343–358, Apr. 2020.
- [3] Q. Shi et al., "Progress in wearable electronics/photonics—Moving toward the era of artificial intelligence and Internet of Things," *InfoMat*, vol. 2, no. 6, pp. 1131–1162, Jul. 2020.
- [4] S. Chatterjee, Y. Tsvividis, and P. Kinget, "0.5-V analog circuit techniques and their application in OTA and filter design," *IEEE J. Solid-State Circuits*, vol. 40, no. 12, pp. 2373–2387, Dec. 2005.

- [5] P. Monsurrò, G. Scotti, A. Trifiletti, and S. Pennisi, "Biasing technique via bulk terminal for minimum supply CMOS amplifiers," *Electron. Lett.*, vol. 41, no. 14, pp. 779–780, Jul. 2005.
- [6] P. Monsurro, S. Pennisi, G. Scotti, and A. Trifiletti, "Exploiting the body of MOS devices for high performance analog design," *IEEE Circuits Syst. Mag.*, vol. 11, no. 4, pp. 8–23, 4th Quart., 2011.
- [7] F. Khateb, S. B. A. Dabbous, and S. Vlassis, "A survey of nonconventional techniques for low-voltage low-power analog circuit design," *Radioengineering*, vol. 22, no. 2, pp. 415–427, 2013.
- [8] A. K. Moghaddam, J. H. Chuah, H. Ramiah, J. Ahmadian, P.-I. Mak, and R. P. Martins, "A 73.9%-efficiency CMOS rectifier using a lower DC feeding (LDCF) self-body-biasing technique for far-field RF energy-harvesting systems," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 64, no. 4, pp. 992–1002, Apr. 2017.
- [9] B. J. Blalock, P. E. Allen, and G. A. Rincon-Mora, "Designing 1-V Op amps using standard digital CMOS technology," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 45, no. 7, pp. 769–780, Jul. 1998.
- [10] L. H. C. Ferreira and S. R. Sonkusale, "A 60-dB gain OTA operating at 0.25-V power supply in 130-nm digital CMOS process," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 61, no. 6, pp. 1609–1617, Jun. 2014.
- [11] O. Abdelfattah, G. W. Roberts, I. Shih, and Y.-C. Shih, "An ultra-low-voltage CMOS process-insensitive self-biased OTA with rail-to-rail input range," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 62, no. 10, pp. 2380–2390, Oct. 2015.
- [12] E. Cabrera-Bernal, S. Pennisi, A. D. Grasso, A. Torralba, and R. G. Carvajal, "0.7-V three-stage class-AB CMOS operational transconductance amplifier," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 63, no. 11, pp. 1807–1815, Nov. 2016.
- [13] T. Kulej and F. Khateb, "Design and implementation of sub 0.5-V OTAs in 0.18- μm CMOS," *Int. J. Circuit Theory Appl.*, vol. 46, no. 6, pp. 1129–1143, Jun. 2018.
- [14] F. Khateb and T. Kulej, "Design and implementation of a 0.3-V differential difference amplifier," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 66, no. 2, pp. 513–523, Feb. 2019.
- [15] T. Kulej and F. Khateb, "A 0.3-V 98-dB rail-to-rail OTA in 0.18- μm CMOS," *IEEE Access*, vol. 8, pp. 27459–27467, 2020.
- [16] K.-C. Woo and B.-D. Yang, "A 0.25-V rail-to-rail three-stage OTA with an enhanced DC gain," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 67, no. 7, pp. 1179–1183, Jul. 2020.
- [17] A. Ballo, A. D. Grasso, and S. Pennisi, "0.4-V, 81.3-nA bulk-driven single-stage CMOS OTA with enhanced transconductance," *Electronics*, vol. 11, no. 17, p. 2704, Aug. 2022.
- [18] F. Khateb, M. Kumngern, T. Kulej, and D. Biolek, "0.5 V differential difference transconductance amplifier and its application in voltage-mode universal filter," *IEEE Access*, vol. 10, pp. 43209–43220, 2022.
- [19] F. Centurelli, R. Della Sala, P. Monsurrò, P. Tommasino, and A. Trifiletti, "An ultra-low-voltage class-AB OTA exploiting local CMFB and body-to-gate interface," *AEU - Int. J. Electron. Commun.*, vol. 145, Feb. 2022, Art. no. 154081.
- [20] M. Akbari, S. M. Hussein, Y. Hashim, and K. Tang, "0.4-V tail-less quasi-two-stage OTA using a novel self-biasing transconductance cell," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 69, no. 7, pp. 2805–2818, Jul. 2022.
- [21] T. Kulej, F. Khateb, D. Arbet, and V. Stopjakova, "A 0.3-V high linear rail-to-rail bulk-driven OTA in 0.13 μm CMOS," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 69, no. 4, pp. 2046–2050, Apr. 2022.
- [22] A. Ballo, A. D. D. Grasso, S. Pennisi, and G. Susinni, "A 0.3-V 8.5- μA bulk-driven OTA," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 31, no. 9, pp. 1444–1448, Sep. 2023.
- [23] M. Akbari, S. M. Hussein, Y. Hashim, and K. Tang, "An enhanced input differential pair for low-voltage bulk-driven amplifiers," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 29, no. 9, pp. 1601–1611, Sep. 2021.
- [24] P. Monsurrò, S. Pennisi, G. Scotti, and A. Trifiletti, "0.9-V CMOS cascode amplifier with body-driven gain boosting," *Int. J. Circuit Theory Appl.*, vol. 37, no. 2, pp. 193–202, Mar. 2009.
- [25] T. Kulej and F. Khateb, "A compact 0.3-V class AB bulk-driven OTA," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 28, no. 1, pp. 224–232, Jan. 2020.
- [26] R. D. Sala, F. Centurelli, P. Monsurrò, G. Scotti, and A. Trifiletti, "A 0.3V rail-to-rail three-stage OTA with high DC gain and improved robustness to PVT variations," *IEEE Access*, vol. 11, pp. 19635–19644, 2023.
- [27] A. D. Grasso, D. Marano, F. Esparza-Alfaro, A. J. Lopez-Martín, G. Palumbo, and S. Pennisi, "Self-biased dual-path push-pull output buffer amplifier for LCD column drivers," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 61, no. 3, pp. 663–670, Mar. 2014.
- [28] Z. Qin, A. Tanaka, N. Takaya, and H. Yoshizawa, "0.5-V 70-nW rail-to-rail operational amplifier using a cross-coupled output stage," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 63, no. 11, pp. 1009–1013, Nov. 2016.
- [29] A. D. Grasso, S. Pennisi, G. Scotti, and A. Trifiletti, "0.9-V class-AB Miller OTA in 0.35- μm CMOS with threshold-lowered non-tailed differential pair," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 64, no. 7, pp. 1740–1747, Jul. 2017.
- [30] M. A. Mohammed and G. W. Roberts, "Scalable multi-stage CMOS OTAs with a wide CL-drivability range using low-frequency zeros," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 70, no. 1, pp. 74–87, Jan. 2023.
- [31] H. Khorramabadi, "A CMOS line driver with 80-dB linearity for ISDN applications," *IEEE J. Solid-State Circuits*, vol. 27, no. 4, pp. 539–544, Apr. 1992.
- [32] C. Mohan and P. M. Furth, "A 16- Ω audio amplifier with 93.8-mW peak load power and 1.43-mW quiescent power consumption," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 59, no. 3, pp. 133–137, Mar. 2012.
- [33] K. N. Leung and P. K. T. Mok, "A capacitor-free CMOS low-dropout regulator with damping-factor-control frequency compensation," *IEEE J. Solid-State Circuits*, vol. 38, no. 10, pp. 1691–1702, Oct. 2003.



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