Synthesizing Step-Down Switched Capacitor Power Converter Topologies

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***Abstract*— The fast-growing development in wearable electronic devices leads to high demand for small-volume, lightweight, and high-efficiency DC-DC power converters, particularly switched capacitor (SC) DC-DC converters. In this paper, we propose a synthesis framework of step-down SC DC-DC power converters to obtain an optimum converter topology under the design constraints of the conversion ratio and a minimum number of capacitors. The proposed rule-based clustering reduction techniques have reduced the search space and sped up the conversion ratio analysis. In the case study of 8:1 converter synthesis, the run-time for conversion ratio analysis is reduced by 1.26 × 10^6. The proposed efficiency optimization method has improved the peak efficiencies of the cascaded 2:1 converter and Fibonacci converter by 4.7% and 12.8%. The proposed framework has identified new topologies and variants of conventional topologies. The variant of cascaded 2:1 converter shows an improvement of 8.2% on peak efficiency.**

***Index Terms*— Circuit synthesis, capacitors, topology, DC–DC power converters, switched-capacitor power converter.**

I. Introduction

THE development of low-power wearable and implantable devices has significantly increased the demand for DC-DC power converters with small volume, lightweight, and high efficiency [1], [2], [3]. Switched-capacitor (SC) DC–DC power converters, compared with their inductor-based or hybrid counterparts, can be fully integrated on the chip due to the readily available switches and capacitors in CMOS technologies [4], [5], [6], [7]. Hence, reconfigurable SC DC-DC converter [8], multiphase SC DC-DC converter grid [9], and multilevel SC DC-DC converter [10] have been proposed to provide multiple voltage domains and independent voltage scaling in multicore processors.

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A SC DC-DC power converter converts electricity by switching back and forth between multiple circuit topologies during different operating phases, where each circuit topology is a specific configuration of switches and capacitors that determine the ideal converter conversion ratio [11], [12], [13]. Compared with two-phase converters, converters with three or more phases demand a fewer number of capacitors and demonstrate a lower charge redistribution loss, while requiring more complicated control schemes and incurring a larger switch conduction loss [13], [14], [15]. Interestingly, SC DC-DC power converters suffer from fast efficiency degradation once the input-to-output voltage ratio deviates from the ideal conversion ratio [16], [17], [18].

To address these problems, several circuit topologies have been proposed to provide fine-grained voltage conversion ratios. Bang et al. put forward the successive-approximation SC DC-DC power converter topology that achieves a conversion ratio resolution of $V_{IN}/2^{\text{number of stages}}$ based on cascaded 2:1 SC DC-DC power converter cells (SC cells) [19], while Salem et al. proposed a recursive SC DC-DC power converter to recursively divide output charge across N 2:1 SC cells and realize N bit ratios [20]. On the other hand, negator-based SC DC-DC power converter [21] and asymmetrical shunt SC DC-DC power converter [22] introduce negative voltage feedback into N-stage cascaded 2:1 SC cells to realize p/q conversion ratios, where $0 < p < q < 2^{N+1}$. Although these binary or rational reconfigurable circuit topologies can achieve a large number of conversion ratios, they suffer from a severe power loss due to the cascaded structures [23]. Presently, various power converter circuit topologies are derived intuitively or by modifying existing topologies. It has raised the question of whether synthesizing an optimum converter topology under the constraints of conversion ratios and the number of capacitors will be a better method to overcome the aforementioned problems.

Currently, the topology synthesis methods for SC DC-DC converters can be classified into two categories. One is based on canonical forms where predefined cells, such as extracted Dickson cell and charge-path-folding cell [24], backtracking cell [25], Zeckendorf representation generation cell [26], Fibonacci and series-parallel topology canonical cell [27], are assembled to construct the topology. This method generates power converters using a larger number of capacitors, which limits its optimum performance. For example, the algorithmic voltage feed-in SC DC-DC power converter [24]

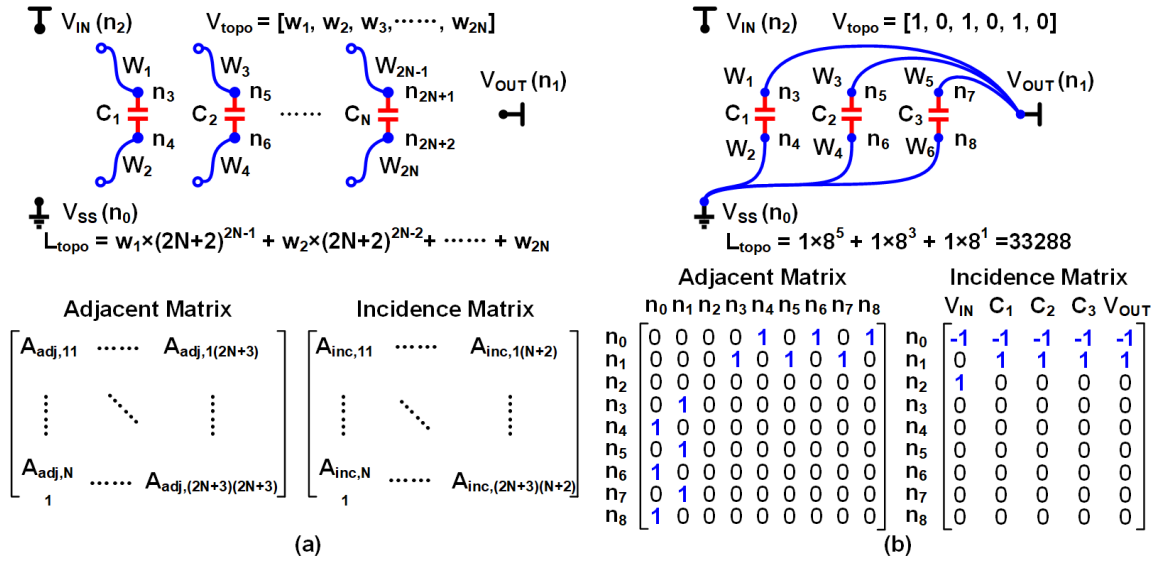


Fig. 1. SC DC-DC converter topology: (a) abstract topological model and (b) a topology example with three capacitors.

incorporates 20 cells to cover a conversion range from 2:1 to 1:7, which is unsuitable for small form factor applications. The other method is to synthesize a power converter based on a general network model [28], general wiring model [29], or through iterative algorithms like ANTZ tree generation [30] and series/parallel iteration [31]. These do not limit the topology to a predefined form but require a prohibitive amount of computation when the designed converter has a large number of capacitors. For example, the method proposed in [29] derives 5.4 $\times 10^{10}$ power converter topologies with 4 capacitors.

To overcome all the aforementioned challenges, we present a new synthesis framework of a step-down SC DC-DC power converter and our contributions are as follows:

1) We propose a step-down SC converter synthesis framework that generates and analyzes SC converters from a comprehensive pool of topologies to obtain the converter with a specified conversion ratio and number of capacitors. New topologies and topology variants for conventional topologies are generated and analyzed. The variant of cascaded 2:1 converter topology shows an improvement of 8.2% in the peak efficiency.
2) To overcome the problem of excessive computation, we propose rule-based clustering reduction techniques to remove redundant topologies during the conversion ratio analysis. In the case of synthesizing 4:1 converters and 8:1 converters, the computation on conversion ratio analysis is reduced by 3.47 $\times$ 10^4 and 1.26 $\times$ 10^6 compared with the prior works [28] and [29], respectively.
3) Furthermore, the proposed efficiency optimization method enumerates the alternative wiring methods based on the spanning tree search method to optimize the loss metrics. The efficiencies of the cascaded 2:1 converter and Fibonacci converter are improved by 4.7% and 12.8%, respectively.

The rest of this paper is organized as follows: Section II presents a model of step-down SC DC-DC power converters, the mathematical expressions for their circuit topologies, and constraints to identify invalid circuit topologies. Section III details our proposed framework for the synthesis of SC DC-DC power converters. Section IV presents a case study where 4:1 power converters are synthesized, categorized, and verified by SPICE simulation. Section V compares our framework with prior work based on a case study of synthesizing 8:1 converters. The obtained 8:1 converters are verified by SPICE simulation. Our work is concluded in Section VI.

II. Modeling of Step-Down SC DC-DC Power Converter

A. Definitions

Fig. 1(a) illustrates the abstracted topological model of step-down SC DC-DC power converters, which consists of N flying capacitors, $2N$ wires, and $2N+3$ nodes, including 3 external ports, namely, V_{IN}, V_{SS}, and V_{OUT}. For simplicity, we termed it circuit topology.

Definition 1 (Circuit Topology): Let the N flying capacitors be C_i for i=1, 2, $\cdots$ N, and the top and bottom terminals of C_i are denoted as n_{2i+1} and n_{2i+2}, respectively. The wires connected to the top and bottom terminals of C_i are denoted as W_{2i-1} and W_{2i}, respectively. Similarly, let three external ports, V_{SS}, V_{OUT}, and V_{IN} to be n_0, n_1, and n_2, respectively. Each terminal of the flying capacitor is connected either to other terminals of the flying capacitors or to one of the external ports through a wire.

Definition 2 (Topological Vector, V_{topo}): Let the topological vector, V_{topo}, be a vector representing the $2N$ wire connections in a circuit topology, where the i^{th} element in V_{topo} is assigned as j if the wire W_i is connected to n_j.

For example, as shown in Fig. 1(b), since W_1, W_3, and W_5 are connected to V_{OUT}, the first, third, and fifth elements in the topological vector are the node number of V_{OUT}. Similarly, the second, fourth, and sixth elements in the topological vector are the node number of V_{SS}, to which W_2, W_4 and W_6 are connected. Thus, the topological vector, V_{topo}, is [1, 0, 1, 0, 1, 0].

Definition 3 (Topological Label, L_{topo}): Let the topological label, L_{topo}, to be an integer representing the circuit topology of V_{topo} and it is formulated as follow:

$$L_{topo} = \sum_{i=1}^{2N} \{V_{topo}(i) \times (2N+2)^{2N-i}\}, \tag{1}$$

where $V_{topo}(t, i)$ is the i^{th} element of its topological vector. For example, as shown in Fig. 1(b), the V_{topo} [1, 0, 1, 0, 1, 0] has a N of 3 and its L_{topo} is 33288. The use of L_{topo} allows us to uniquely label each circuit topology.

B. Circuit Topology Representations

1) Adjacency Matrix, $\boldsymbol{A_{adj}}$ Representation: Given Definitions 1 and 2, for a step-down SC DC-DC power converter with N flying capacitors, there will be a total number of $(2N)^{2N}$ circuit topologies. In this work, we proposed to use the undirected graph G representation for each circuit topology, where circuit nodes and wires are regarded as vertices and edges, respectively. The adjacency matrix A_{adj} of the graph is a symmetric matrix whose element $a_{ij} = a_{ji} = 1$ if n_{i-1} is connected to n_{j-1}, and $a_{ij} = a_{ji} = 0$ if they are not connected. The number of paths between two vertices in a graph is determined using the power of its adjacency matrix. The $(i, j)^{th}$ as well as $(j, i)^{th}$ element of $(A_{adj})^k$ equal the number of paths of k wires that connect n_{i-1} to n_{j-1}. For example, the adjacency matrix for the circuit topology as shown in Fig. 1(b) is:

$$A_{adj,\,fig.1(b)} = \begin{bmatrix} 0&0&0&0&\mathbf{1}&0&\mathbf{1}&0&\mathbf{1} \\ 0&0&0&\mathbf{1}&0&\mathbf{1}&0&\mathbf{1}&0 \\ 0&0&0&0&0&0&0&0&0 \\ 0&\mathbf{1}&0&0&0&0&0&0&0 \\ \mathbf{1}&0&0&0&0&0&0&0&0 \\ 0&\mathbf{1}&0&0&0&0&0&0&0 \\ \mathbf{1}&0&0&0&0&0&0&0&0 \\ 0&\mathbf{1}&0&0&0&0&0&0&0 \\ \mathbf{1}&0&0&0&0&0&0&0&0 \end{bmatrix}, \tag{2}$$

where the i^{th} row and column of A_{adj} indicate the connections between n_{i-1} and other nodes. For example, in the first row and first column of the matrix, only the fifth, seventh, and ninth elements are nonzero, showing that n_0 is connected to n_4, n_6, and n_8 but not to other nodes.

2) Incidence Matrix, $\boldsymbol{A_{inc}}$ Representation: Besides the adjacency matrix representation, the circuit topology is represented using the incidence matrix format. The incidence matrix, A_{inc}, of a circuit topology is a matrix of order $(2N+3) \times (N+2)$, where N is the number of flying capacitors. Each row and column of A_{inc} correspond to a node and a circuit element in the circuit topology, respectively. Each entry of the incidence matrix is defined as follows:

(i) $A_{inc}(i, j)$ is 1 if the j^{th} element's positive terminal is connected to node n_{i-1};
(ii) $A_{inc}(i, j)$ is -1 if the j^{th} element's negative terminal is connected to node n_{i-1};
(iii) $A_{inc}(i, j)$ is 0 if the j^{th} element is not connected to node n_{i-1}.

For example, as presented in Fig. 1(b), the circuit topology is expressed with the following incidence matrix:

$$A_{inc,\,fig.1(b)} = \begin{array}{c} \\ n_0 \\ n_1 \\ n_2 \\ n_3 \\ n_4 \\ n_5 \\ n_6 \\ n_7 \\ n_8 \end{array} \begin{array}{c} \begin{array}{ccccc} V_{IN} & C_1 & C_2 & C_3 & V_{OUT} \end{array} \\ \begin{bmatrix} \mathbf{-1} & \mathbf{-1} & \mathbf{-1} & \mathbf{-1} & \mathbf{-1} \\ 0 & \mathbf{1} & \mathbf{1} & \mathbf{1} & \mathbf{1} \\ \mathbf{1} & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix} \end{array}, \tag{3}$$

where the first and last columns indicate the connections to the input terminal, V_{IN}, and the output terminal, V_{OUT}. The remaining columns indicate the connection to the terminals of the capacitors (C_1, C_2 and C_3).

C. Circuit Constraints

Given that the top terminal of each flying capacitor has a higher electric potential than that of the bottom terminal. Thus, the connections formed by the wires need to satisfy the following constraints to form a valid circuit topology for step-down SC DC-DC power converters:

(i) To prevent the top terminal of a capacitor having a higher electric potential than V_{IN}, wires that are connected to the bottom terminal of the capacitor must not be connected to V_{IN}.
(ii) To prevent the bottom terminal of a capacitor having a lower electric potential than V_{SS}, wires that are connected to the top terminal of the capacitor must not be connected to V_{SS}.
(iii) To prevent any short circuit, wires that are connected to the top terminal of a capacitor must not be connected to its bottom terminal.
(iv) To prevent redundant paths between any two circuit nodes, paths must not have any loops.
(v) To prevent capacitors from having zero or negative voltages, paths must not loop series-connected capacitors.

Constraints (i) and (ii) can be nullified to allow for circuit nodes with electric potential higher than V_{IN} or lower than V_{SS}. Thus, the proposed method can synthesize step-up SC converters or inverting SC converters.

Fig. 2 illustrates the four examples of invalid topologies under one or more of these constraints. Fig. 2(a) shows a topology that violates constraints (i) and (ii). The top terminal of C_1 is connected to V_{SS}, hence the electric potential of C_1's bottom terminal, which is assumed to be lower than that of the top terminal, is lower than V_{SS}. Similarly, the electric potential of C_2's top terminal is higher than V_{IN} because C_2's bottom terminal is connected to V_{IN}. Fig. 2(b) presents a topology where constraint (iii) is violated because C_1 is short-circuited by W_1, W_2, and W_3. In Fig. 2(c), the loop of wires formed by W_1, W_3, and W_5 means that there exist redundant paths between any two of the nodes in the loop, i.e., n_1, n_3, and n_5. For example, W_1 and the path formed by W_3 and W_5 both connect n_1 to n_5, thus violating constraint (iv). In Fig. 2(d),

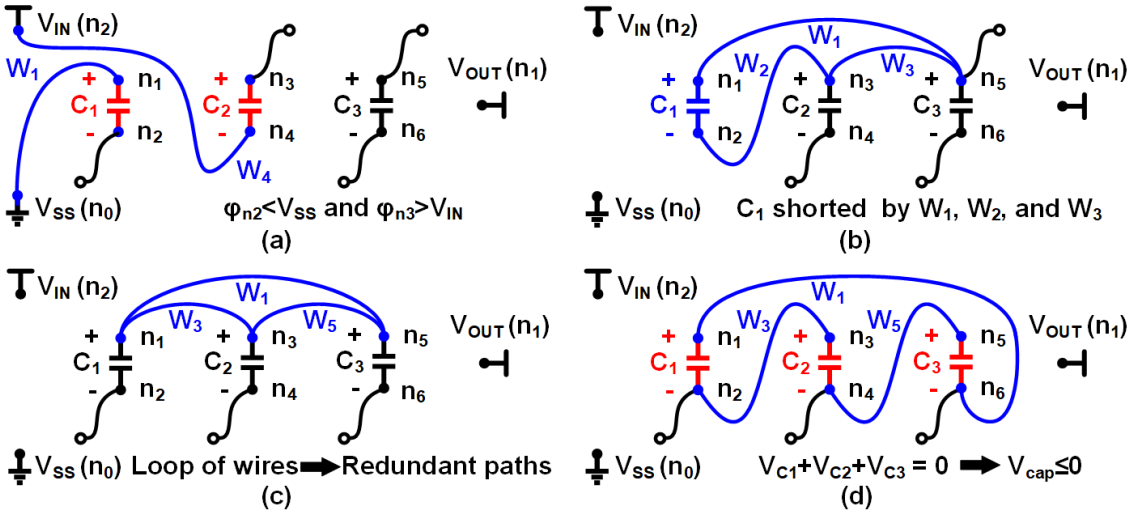


Fig. 2. Examples of invalid topologies that violate the constraints due to (a) capacitor terminals with electrical potential lower than V_{SS} or higher than V_{IN}, (b) a short-circuited capacitor, (c) redundant paths between nodes, and (d) capacitor voltage less than or equal to zero.

C_1, C_2, and C_3 are series-connected and form a loop, which violates constraint (v). Since the sum of voltages across these capacitors is zero, at least one of the capacitors must have a voltage less than or equal to zero.

D. Problem Statement

Since the two-phase step-down SC DC-DC power converter converts electricity by switching back and forth between two circuit topologies, the number of power converter circuits is given by the binomial coefficient:

$$Number\ of\ Power\ Converters = \binom{M}{2} = \frac{M^2 - M}{2}, \quad (4)$$

where M is the number of valid circuit topologies. To reduce the computation on verifying these combinations, it is desirable to reduce the number of valid topologies.

Problem 1 (Identifying the Most Optimal Step-Down SC DC-DC Power Converter Circuit Topology Problem): Given the number of capacitors, N, and the conversion ratio, R, the goal is to identify the most optimal group of power converter circuits.

III. Synthesis of Step-Down SC DC-DC Power Converter

A. Overview of the Proposed Methodology

Our proposed synthesis methodology of a step-down SC DC-DC power converter (Fig. 3) is summarized as follows:

1) Step 1 - Topology Generation: Given the number of capacitors, N, and the conversion ratio, R, as input constraints to our abstract topological model, the wire connections are enumerated to get $(2N)^{2N}$ circuit topologies.

2) Step 2 - Topology Removal Technique #1 - Invalid Topologies: Based on the circuit constraints (Section II-C), any circuit topology is expressed by the adjacency matrix, which is used to identify the invalid circuit topologies and remove them from the present topology candidates. For example, for N=4, the number of circuit topologies is reduced from 16,777,216 to 460,536, which amounts to a 36.43× reduction.

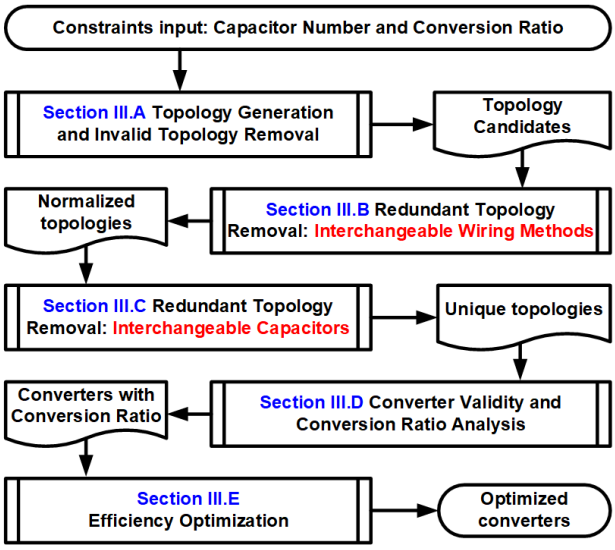


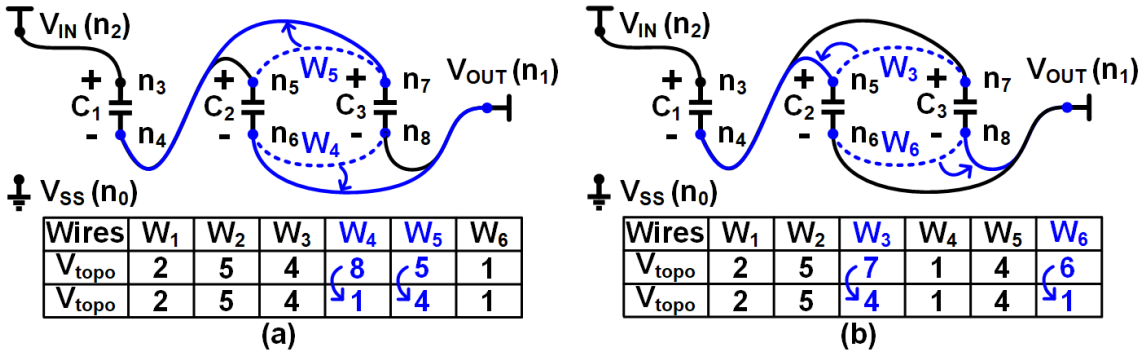
Fig. 3. Synthesis methodology of a step-down SC DC-DC power converter.

3) Step 3 - Rule-based Clustering Reduction Techniques: To overcome the problem of excessive computation and reduce the redundant permutated circuit topologies, we propose several rule-based clustering reduction techniques (Steps 3A and 3B). For example, for N=4, the number of valid circuit topologies has been further reduced from 460,536 to 458, which is a 1,006× reduction.

4) Step 3A - Topology Removal Technique #2 - Interchangeable Wiring: The connectivity of circuit components is unchanged when circuit nodes are connected by different wiring methods. Such wiring methods do not influence the conversion ratio and circuit functionality but the conduction loss. Before conversion ratio analysis, different wiring methods are normalized to reduce computation.

5) Step 3B - Topology Removal Technique #3 - Interchangeable Capacitors: Since the order of capacitors, C_i in the circuit topology are interchangeable, there exist redundant topologies in the present topology candidates.

6) Step 4 - Converter Validity and Conversion Ratio Analysis: Kirchhoff's laws formulate the circuit topology into



Wires	W_1	W_2	W_3	W_4	W_5	W_6
V_{topo}	2	5	4	8	5	1
V_{topo}	2	5	4	1	4	1

(a)

Wires	W_1	W_2	W_3	W_4	W_5	W_6
V_{topo}	2	5	7	1	4	6
V_{topo}	2	5	4	1	4	1

(b)

Fig. 4. An example of topologies with the same circuit functionality due to interchangeable wires: (a) topology 1 and (b) topology 2.

algebraic equations in terms of V_{IN}, V_{SS}, and V_{OUT}. All the valid power converters are identified by solving the algebraic equations from each pair of two circuit topologies and obtaining their conversion ratio.

7) Step 5 - Efficiency Optimization: For obtained converters with the desired conversion ratio, removed topologies with different wiring methods (Step 3A) are analyzed to optimize the conduction loss. Each power converter circuit is evaluated using the equivalent output resistance [11], which is based on the slow-switching limit (SSL) loss metric K_{SSL} and the fast-switching limit (FSL) loss metric K_{FSL}.

B. Topology Removal Technique #2: Interchangeable Wiring Methods

The wiring method of circuit nodes does not change the connectivity of circuit components, and hence it does not affect the conversion ratio and circuit functionality. However, the wiring is implemented by CMOS metal layers and on-state switches, so the wiring method determines the resistance between circuit nodes and affects the conduction loss. Before conversion ratio analysis, the wiring method of each topology is normalized so that redundant topologies that result in the same conversion ratio are eliminated. Specifically, if a group of nodes is interconnected by one or more wires, these wires are normalized to connect to the node with the minimal node number.

Thus, we can significantly reduce the number of redundant permutated circuit topologies. This is termed as topology removal technique #3: Interchange wire, which is considered a type of rule-based clustering reduction technique.

For example, as presented in Fig. 4(a), since n_4, n_5, and n_7 are interconnected, W_5, which originally connects n_7 to n_5, is re-arranged to connect n_7 to n_4. Similarly, W_4 is re-arranged to connect n_6 to n_1 without affecting the circuit functionality. The topology in Fig. 4(a) and (b) can be converted to the same topology, thus eliminating the redundancy due to interchangeable wires.

C. Topology Removal Technique #3 - Interchangeable Capacitors

Let S be the set of $s_1, s_2, \cdots, s_i, \cdots, s_m$ valid circuit topologies. There exist redundant topologies, s_i, s_j with the same circuit functionality since the order of capacitors, C_i in the circuit topology are interchangeable. For example, the topology in Figs. 5(a) and (b), denoted by s_i and s_j, are convertible to each other by swapping C_1 and C_3 and their respective wires (W_1, W_2, W_5, and W_6), and thus there exist redundant topologies.

Let the equivalence relation, topologies are convertible to each other by changing the capacitor order, be denoted by $\sim$. Let e be a topology in S and $[e]$ be its equivalence class. Their relation is expressed as follows:

$$[e] = \{s \in S \mid s \sim e\}. \tag{5}$$

The total number of circuit topologies with the same equivalence class is given by the permutation formula $P(N, N) = N!$.

Using the topological label, L_{topo}, we can simply identify the total unique number of equivalence classes in S and remove the redundant topologies. This is termed as topology removal technique #2 - Interchangeable capacitors, which is considered as a rule-based clustering reduction technique.

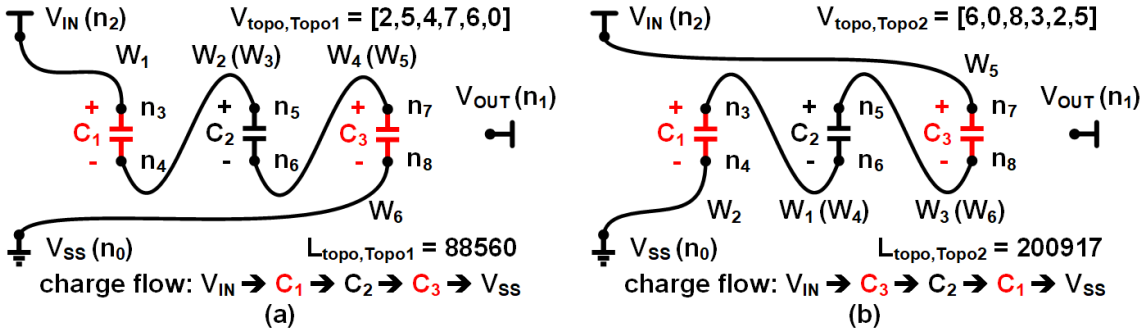
For example, the topology in Fig. 5(b) is a topology obtained in Section III-B. We obtain its equivalence class including $3! = 6$ topologies by changing the order of capacitors. Fig. 5(c) shows the topological vectors and topological labels of these topologies. The valid topology in Fig. 5(b) is then replaced by the topology with the minimal topological label, in this case, the topology in Fig. 5(a). Similarly, each of the topologies obtained in Section III-B is analyzed and replaced by the topology having minimal topological label among its equivalence class. Finally, repetitive topologies are removed for the following analysis.

D. Converter Validity and Conversion Ratio Analysis

Kirchhoff's laws are used to formulate the circuit topology into algebraic equations in terms of V_{IN}, V_{SS}, and V_{OUT}. To identify any two circuit topologies that can be used to form a valid power converter with a conversion ratio, R, we can derive their algebraic equations and obtain the R, where R is $(V_{OUT}\text{-}V_{SS})/(V_{IN}\text{-}V_{SS})$.

Let i_{elm} be the vector elements representing the current in each node. According to Kirchhoff's current law (KCL), each circuit topology is represented using the incidence matrix, A_{inc} and current vector, i_{elm}:

$$A_{inc} \times i_{elm} = 0, \tag{6}$$



Topology	V_{topo}	L_{topo}	Topology	V_{topo}	L_{topo}
Topo1	[2,5,4,7,6,0]	88560	Topo2	[6,0,8,3,2,5]	200917
Topo3	[2,7,8,0,4,5]	98341	Topo4	[8,5,4,0,2,3]	284691
Topo5	[6,7,2,3,4,0]	226538	Topo6	[8,0,2,7,6,3]	263667

(c)

Fig. 5. An example of circuit topologies with the same circuit functionality due to interchangeable capacitors: (a) topology 1, (b) topology 2, and (c) equivalence class of topologies.

where the i^{th} entry of $A_{inc}i_{elm}$ is the sum of currents leaving node i.

Matrix, B_{loop} is a loop matrix with the coefficients of Kirchhoff's voltage law (KVL) equations as its entries. It is used to calculate the conversion ratio based on its orthogonality relations with the incidence matrix, A_{inc} [32]. For example, as presented in Fig. 1(b), the reduced row echelon form with the removal of null rows, the incidence matrix, A_{inc} becomes:

$$A_{inc,ech,fig.1(b)} = \left[\begin{array}{cc|ccc} 1 & 0 & 0 & 0 & 0 \\ 0 & 1 & 1 & 1 & 1 \end{array}\right], \tag{7}$$

which is generalized as an augmented matrix:

$$A_{inc,ech,fig.1(b)} = \left[I \middle| \hat{A}_{inc,ech,fig.1(b)}\right]. \tag{8}$$

Thus, the current vector, i_{elm} is partitioned into a vector of independent current vector, $i_{elm,indep}$ and a vector of dependent current vector, $i_{elm,dep}$, and their relationship is given by:

$$i_{elm,dep} = -\hat{A}_{inc,ech} \times i_{elm,ind}. \tag{9}$$

The current vector, i_{elm} can therefore be expressed as:

$$i_{elm} = \begin{bmatrix} -\hat{A}_{inc,ech} \\ I \end{bmatrix} i_{elm,ind} = B_b^T i_{elm,ind}. \tag{10}$$

For example, the loop matrix, $B_{loop,fig.4(c)}$ of circuit topology as presented in Fig. 1(b) is:

$$B_{loop,fig.1(b)} = \begin{bmatrix} 0 & -1 & 1 & 0 & 0 \\ 0 & -1 & 0 & 1 & 0 \\ 0 & -1 & 0 & 0 & 1 \end{bmatrix}. \tag{11}$$

The conversion ratio, R can be obtained by solving the following equation:

$$\begin{bmatrix} B_{loop,topo1} \\ B_{loop,topo2} \end{bmatrix} V_{elm} = 0, \tag{12}$$

where V_{elm} is a vector containing the voltages across each circuit element, $[(V_{IN} - V_{SS}), V_{C1}, V_{C2}, \cdots, V_{CN}, (V_{OUT} - V_{SS})]^T$.

E. Efficiency Optimization

The SC DC-DC converter can be modeled as an ideal DC voltage source in series with a finite output resistance [15], which can be expressed as follows:

$$R_{OUT} \approx \sqrt{R_{SSL}^2 + R_{FSL}^2}. \tag{13}$$

R_{OUT} is the root sum square of the slow-switching-limit (SSL) resistance R_{SSL}, which represents charge redistribution loss of capacitors, and fast-switching-limit (FSL) resistance R_{FSL}, which represents conduction loss of switches. R_{SSL} and R_{FSL} are calculated as follows:

$$R_{SSL} = K_{SSL} \frac{1}{C_{fly} f_{sw}}, \tag{14}$$

$$R_{FSL} = K_{FSL} R_{ON}, \tag{15}$$

where K_{SSL} and K_{FSL} are topological loss metrics determined by the charge flow of capacitors and switches, C_{fly} is the capacitance of the flying capacitor, f_{sw} is the switching frequency, and R_{ON} is the on-resistance of switches. Thus, the capacitor charge redistribution loss and switch conduction loss can be calculated based on R_{OUT} and output current I_O:

$$P_{LOSS} = R_{OUT} I_O^2. \tag{16}$$

The parasitic effect is not considered in the proposed method. However, the obtained database of SC DC-DC converters can be the input for more comprehensive modeling methods [8], [33], [34].

1) SSL Loss Metric: The slow-switching limit metric K_{SSL} is the sum of square normalized capacitor charge flows:

$$K_{SSL} = \frac{1}{2} \sum_{j}^{2} \sum_{i}^{N} \left(\frac{Q_{Ci}^j}{Q_{OUT}}\right)^2, \tag{17}$$

where Q_{Ci}^j is the charge flow through a capacitor C_i during the j^{th} phase, and Q_{OUT} is the total output charge flow in all the phases. Based on (6), the capacitor charge flow satisfies:

$$A_{inc}^1 \times Q_{elm}^1 = 0, \quad A_{inc}^2 \times Q_{elm}^2 = 0, \tag{18}$$

where Q^j_{elm} is a vector containing the charge flowing between input and output sources and capacitors during the j^{th} phase, $[Q^j_{IN}, Q^j_{C1}, Q^j_{C2}, \cdots, Q^j_{CN}, Q^j_{OUT}]^T$. Thus, the incidence matrix and the charge flow vector are partitioned into three groups of augmented matrices, which correspond to the input source, capacitors, and output source, respectively.

$$A^j_{inc} = \left[A^j_{IN} \middle| A^j_C \middle| A^j_{OUT}\right] \tag{19}$$

$$Q^j_{elm} = \left[Q^j_{IN} \middle| Q^j_C \middle| Q^j_{OUT}\right]^T \tag{20}$$

In steady-state, the net charge flow of each capacitor in both phases must be zero:

$$Q^1_C + Q^2_C = 0. \tag{21}$$

Based on (19) to (21), the two equations in (18) is expressed as follows:

$$A_{inc,both} \times \begin{bmatrix} Q^1_{IN} \\ Q^2_{IN} \\ Q^1_C \\ Q_{DIFF} \\ Q_{OUT} \end{bmatrix} = 0, \tag{22}$$

where $A_{inc,both}$ is an integration of the incidence matrices in both phases:

$$A_{inc,both} = \begin{bmatrix} A^1_{IN} & 0 & A^1_C & A^1_{OUT} & 0 \\ 0 & A^2_{IN} & A^2_C & 0 & A^2_{OUT} \end{bmatrix} \begin{bmatrix} I & 0 \\ 0 & T \end{bmatrix}, \tag{23}$$

where T is:

$$T = \begin{bmatrix} -1/2 & 1/2 \\ 1/2 & 1/2 \end{bmatrix}, \tag{24}$$

and Q_{DIFF} and Q_{OUT} are the difference and sum of the output charge flow in the two phases:

$$Q_{DIFF} = Q^2_{OUT} - Q^1_{OUT}, \tag{25}$$

$$Q_{OUT} = Q^1_{OUT} + Q^2_{OUT}. \tag{26}$$

Thus, the slow-switching limit metric, K_{SSL}, (17) is calculated by obtaining the Q^j_{Ci} through solving (22).

2) FSL Loss Metric: The fast-switching limit metric K_{FSL} is the sum of square normalized switch charge flows:

$$K_{FSL} = \frac{1}{D} \sum_j^2 \sum_i^N \left(\frac{Q_{SW^j_i}}{Q_{OUT}}\right)^2, \tag{27}$$

where D is the duty cycle of each phase, $Q_{SW^j_i}$ is the charge flow of the switch SW^j_i (the wire W_i of the topology) in the j^{th} phase. The switch charge flows are calculated based on the charge flows of the input and output sources, and capacitors:

$$Q^1_{SW} = A^1_{SW} \times Q^1_{elm}, \quad Q^2_{SW} = A^2_{SW} \times Q^2_{elm}. \tag{28}$$

The coefficient matrix A^j_{SW} has a dimension of $2N \times N$, where N is the number of capacitors.

The calculation of K_{FSL} can be simplified when there are zero switch charge flow conditions present in the power converter circuit. Zero switch charge flow conditions occur when (i) two or more wires/switches connect to the same terminals in either phase, and (ii) one or more wires/switches connect to the same terminal in both phases. Thus, the corresponding rows in A^j_{SW} are zero rows. For the switches with non-zero charge flows, the corresponding rows are defined as follows:

(i) $A^j_{SW}(m, \lceil m/2 \rceil)$ is 1 (or -1) if W_m is connected to the positive (or negative) terminal of $C_{\lceil m/2 \rceil}$ in the j^{th} phase;

(ii) $A^j_{SW}(m, n)$ is 1 (or -1) if the terminal of $C_{\lceil m/2 \rceil}$ connected by W_m is connected by wires other than W_m to the positive (or negative) terminal of C_n in the j^{th} phase. Otherwise, $A^j_{SW}(m, n)$ is 0;

Figs. 6(a) and (b) illustrate the different conditions of switch charge flow. The two coefficient matrices A^1_{SW} and A^2_{SW} for the power converter in phase 1 (Φ1) and phase 2 (Φ2) are:

$$A^1_{SW} = \begin{array}{c} \\ SW^1_1 \\ SW^1_2 \\ SW^1_3 \\ SW^1_4 \\ SW^1_5 \\ SW^1_6 \end{array} \begin{array}{c} \begin{array}{ccc} C_1 & C_2 & C_3 \end{array} \\ \begin{bmatrix} \mathbf{0} & \mathbf{0} & \mathbf{0} \\ -1 & 0 & 0 \\ \mathbf{0} & \mathbf{0} & \mathbf{0} \\ 0 & -1 & 0 \\ 0 & 0 & 1 \\ \mathbf{0} & \mathbf{0} & \mathbf{0} \end{bmatrix} \end{array}, \tag{29}$$

$$A^2_{SW} = \begin{array}{c} \\ SW^2_1 \\ SW^2_2 \\ SW^2_3 \\ SW^2_4 \\ SW^2_5 \\ SW^2_6 \end{array} \begin{array}{c} \begin{array}{ccc} C_1 & C_2 & C_3 \end{array} \\ \begin{bmatrix} \mathbf{0} & \mathbf{0} & \mathbf{0} \\ -1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & -1 & 0 \\ \mathbf{0} & \mathbf{0} & \mathbf{0} \\ \mathbf{0} & \mathbf{0} & \mathbf{0} \end{bmatrix} \end{array}, \tag{30}$$

where SW^1_1, SW^1_3, SW^1_6, SW^2_1, SW^2_5, and SW^2_6 are zero switch charge flow conditions.

3) Identifying Optimal Circuit Topology Using Spanning Tree Search Method: As discussed in Section III-B, the topology removal technique #2 (interchangeable wires) normalizes the wiring method to reduce the computation on conversion ratio. However, the normalized wiring method is not necessarily the optimal wiring method due to the FSL loss (conduction losses from on-state switches and CMOS metal layers) during high-speed operation. A spanning-tree method is proposed to determine which wiring method has the minimal FSL loss by enumerating and identifying optimal wiring connections [35], [36].

Let a set of n nodes be vertices V in a graph G. The number of spanning trees, i.e. sub-graphs of G that traverse every vertex in V with (n-1) edges, is given by Cayley's Formula [37]:

$$T_n = n^{n-2} \tag{31}$$

For example, in the circuit topology illustrated in Fig. 4(a), node 4 is interconnected with node 5 and node 7 by two wires, W_2 (W_3) and W_5. Based on (31), there are a total of $3^{(3-2)} = 3$ different wire connections to connect the three nodes with the two wires. Subsequently, the converters with these wire connections are analyzed to identify the power converter with the most optimal K_{FSL}.

IV. Case Study: Synthesis of 4:1 Step-Down SC DC-DC Power Converters

A case study on the proposed synthesis methodology for 4:1 power converters will be discussed: The minimum number of

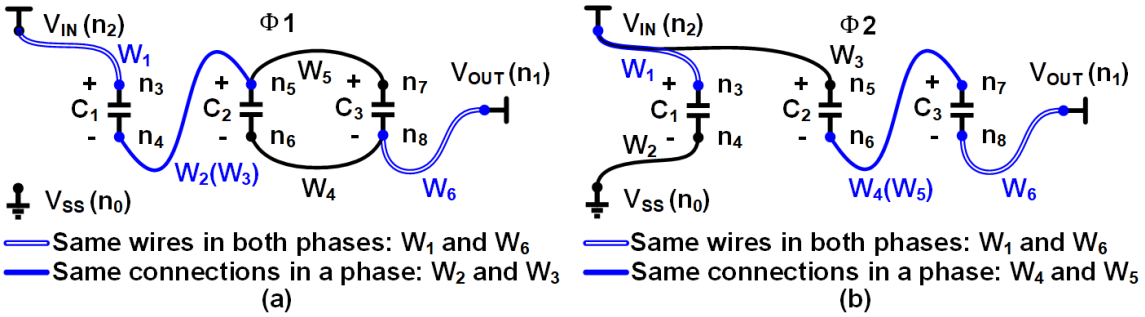


Fig. 6. An example converter with zero switch charge flow conditions: (a) the converter topology in phase 1 and (b) the converter topology in phase 2.

TABLE I
COMPUTATIONAL TASKS AND RUN-TIME OF 4:1 STEP-DOWN SC DC-DC POWER CONVERTER SYNTHESIS METHODS

Method	Number of Task-I	Number of Task-II	Number of Task-III	Number of Task-IV	Run-time of Task-I	Run-time of Task-II	Run-time of Task-III	Run-time of Task-IV	Run-time of Other Functions	Total Run-time
[28]	1,048,576	0	0	675,887,761	*10.473 s	0	0	*33516.245 s	N.A.	*33,526.245 s
Our work	46,656	329	81	19,440	0.466 s	0.080 s	0.058 s	0.964 s	1.385 s	2.953 s

* Estimated run-time based on the number of tasks. The synthesis framework is validated using NVIDIA GEFORCE RTX 3060 GPU and the run-time is tracked using a timing profiler. Task-I: Identifying valid topologies; Task-II: Topology removal technique #2: Interchangeable Wiring; Task-III: Topology removal technique #3: Interchangeable Capacitors; Task-IV: Conversion ratio analysis.

capacitors, N, required to implement a q:p two-phase power converter with a conversion ratio $R = p/q$ must satisfy:

$$F_{N+2} \geq max[p, q], \tag{32}$$

where F_i is the i^{th} Fibonacci number, and p, q are positive integers that are co-prime [41]. N is determined to be 3 to achieve the 1/4 conversion ratio. Table I compares the proposed method with the method in [28]. Compared with [28], there are a total of $(2N)^{2N} = 46,656$ topologies enumerated based on N=3, which is 22.47 × fewer. Based on our proposed rule-based clustering reduction techniques (Section III-B and III-C), a total of 81 topologies with normalized wiring methods are obtained, which is 453 × fewer than the valid topologies in [28]. As a result, 19,400 converters are analyzed. Compared with 675,887,761 converters in [28], the run-time of conversion ratio analysis is reduced from 33,516.245 s to 0.964 s, which is a 3.47 × 10^4 reduction.

Based on the proposed synthesis method, nineteen 4:1 power converters are identified. To categorize these 4:1 converters, we define the variant of any converter A as a converter A-V that generates the output voltage based on the same principle, but with a distinct equivalent circuit in each phase. Thus, among 4:1 converters, eight are based on the cascaded two 2:1 converter topology and seven variants, one has the Dickson topology, two are based on the series-parallel topology and a variant, and eight show three new topologies unrecorded in the prior works and their five variants.

Based on the efficiency optimization method (Section III-E), 675 alternative wiring methods are analyzed to find optimal wiring methods for these 4:1 converters. The topology category, topological vectors, K_{SSL} and K_{FSL} values for converters with normalized, optimal, or conventional wiring methods that have been reported are summarized in Table II. Each converter is denoted based on the topology and wiring method. For example, Cas-N, Cas-O, and Cas-C are based on the cascaded two 2:1 converter topology with the normalized, optimal, and conventional wiring methods, respectively, while Cas-V1-NO represents the converter with the first variant of the cascaded two 2:1 converter topology and the normalized wiring method, which is also the optimal wiring method.

A. Optimization of the Cascaded Two 2:1 Converter Topology

The schematic and equivalent circuit in each phase for Cas-C, Cas-N, and Cas-O are shown in Fig. 7. During phase 1 (Φ1), C_2 and C_3 are connected in series and charged by the input source, V_{IN}, resulting in a voltage of 1/2 V_{IN}, while during phase 2 (Φ2), C_2 and C_3 are connected in parallel to charge the cascaded C_1 and the output, V_{OUT}, resulting in a voltage of 1/4 V_{IN} at the output. The normalized capacitor charge flow in Φ1 and Φ2 is:

$$\left[Q^1_{C1},\ Q^1_{C2},\ Q^1_{C3}\right] = \left[-0.5,\ 0.25,\ -0.25\right] Q_{OUT}, \tag{33}$$

$$\left[Q^2_{C1},\ Q^2_{C2},\ Q^2_{C3}\right] = \left[0.5,\ -0.25,\ -0.25\right] Q_{OUT}. \tag{34}$$

During Φ2 of Cas-C, a total of Q^2_{C2} charges flow from the top terminal of C_2 to the top terminal of C_1 via two switches, $SW_{2,3}$ and $SW_{2,5}$, while during Φ2 of Cas-N, these charges only flow through $SW_{2,3}$. Thus, compared with the conventional wiring method, the normalized wiring method reduces the normalized charge flow of $SW_{2,5}$ from 0.5 to 0.25 and the K_{FSL} value from 2.5 to 2.125. Furthermore, during Φ1 of Cas-N, a total of $-Q^1_{C1}$ charges flow from the bottom terminal of C_1 to the ground, V_{SS}, via $SW_{1,2}$, while during Φ1 of Cas-O, half of these charges are recycled to the bottom terminal of C_3 via $SW_{1,6}$. Thus, compared with the normalized wiring method, the optimal wiring method reduces the normalized charge flow of $SW_{1,2}$ from 0.5 to 0.25. Meanwhile, two additional switches, $SW_{1,6}$ for the charge recycling path during Φ1 and $SW_{2,6}$ for connecting the bottom terminal of C_2 to the ground during Φ2, are introduced in the optimal wiring method, and they both have a normalized charge flow of 0.25. As a result, compared with Cas-N, the K_{FSL} value of Cas-O is slightly reduced from 2.125 to 2.

TABLE II
4:1 STEP-DOWN SC DC-DC POWER CONVERTERS

Category	Topology	Topological Vectors	K_{SSL}	K_{FSL}	Category	Topology	Topological Vectors	K_{SSL}	K_{FSL}
Cascade 2:1	**1. Cas-N**	Φ1: [1 0 2 6 6 0] Φ2: [3 1 3 0 3 0]	0.375	2.125	Unrecorded	**12. U1-V1-N**	Φ1: [1 0 2 6 6 1] Φ2: [3 1 3 1 3 0]	0.375	2.375
	1.1. Cas-C [19]	Φ1: [1 0 2 6 6 0] Φ2: [3 1 7 0 3 0]	0.375	2.5		12.1 U1-V1-O	Φ1: [1 0 2 6 6 1] Φ2: [3 1 3 4 3 0]	0.375	2
	1.2. Cas-O	Φ1: [1 0 2 6 6 4] Φ2: [3 1 3 0 3 0]	0.375	2		**13. U1-V2-NO**	Φ1: [1 0 2 6 6 1] Φ2: [3 1 3 0 1 0]	0.1875	1.25
	2. Cas-V1-NO	Φ1: [1 0 1 6 1 6] Φ2: [3 1 3 0 2 3]	0.375	2.125		**14. U1-V3-N**	Φ1: [1 0 2 6 6 1] Φ2: [3 1 3 0 3 1]	0.375	2.125
	3. Cas-V2-N	Φ1: [1 0 5 1 5 1] Φ2: [3 1 3 0 2 3]	0.375	2.375		14.1. U1-V3-O	Φ1: [1 0 2 6 6 1] Φ2: [3 1 3 0 3 4]	0.375	2
	3.1. Cas-V2-O	Φ1: [1 0 5 1 5 3] Φ2: [3 1 3 0 2 3]	0.375	1.75		**15. U1-V4-NO**	Φ1: [1 0 2 6 6 1] Φ2: [3 1 1 0 3 0]	0.1875	1.25
	4. Cas-V3-NO	Φ1: [1 0 2 6 6 0] Φ2: [3 1 2 3 2 3]	0.375	2.125		**16. U1-V5-N**	Φ1: [1 0 5 0 5 1] Φ2: [2 4 4 1 2 4]	0.375	2.375
	5. Cas-V4-N	Φ1: [1 0 5 0 5 0] Φ2: [3 1 3 0 2 3]	0.375	2.125		16.1. U1-V5-O	Φ1: [1 0 5 0 5 1] Φ2: [2 4 4 1 3 4]	0.375	2
	5.1. Cas-V4-O	Φ1: [1 0 5 4 5 0] Φ2: [3 1 3 0 2 3]	0.375	2		**17. U1-V6-N**	Φ1: [1 0 5 0 5 1] Φ2: [3 1 2 3 3 1]	0.375	2.125
	6. Cas-V5-NO	Φ1: [1 0 2 6 6 0] Φ2: [2 4 4 1 4 1]	0.375	2.375		17.1. U1-V6-O	Φ1: [1 0 5 0 5 1] Φ2: [3 1 2 3 3 4]	0.375	2
	7. Cas-V6-N	Φ1: [1 0 1 6 1 6] Φ2: [3 1 3 0 2 3]	0.375	2.375		**18. U2-N**	Φ1: [2 0 2 6 6 0] Φ2: [3 0 3 1 3 1]	0.375	2.375
	7.1. Cas-V6-O	Φ1: [1 0 3 6 1 6] Φ2: [3 1 3 0 2 3]	0.375	1.75		18.1. U2-O	Φ1: [2 1 3 6 6 0] Φ2: [3 0 3 1 3 1]	0.375	1.75
	8. Cas-V7-NO	Φ1: [1 0 5 6 5 6] Φ2: [3 1 3 0 2 3]	0.375	2.25		**19. U3-NO**	Φ1: [2 0 5 0 5 1] Φ2: [3 0 3 1 2 3]	0.375	2.375
Dickson	**9. DKS-NCO** [38]	Φ1: [1 0 5 1 5 1] Φ2: [3 1 2 1 3 0]	0.1875	1.25	Ladder	Ladder [39]	Φ1: [1 0 5 1 5 1 9 5 9 5] Φ2: [3 1 3 1 7 3 7 3 2 7]	1.1875	6.25
Series-parallel	**10. SP-NCO** [40]	Φ1: [1 0 1 0 1 0] Φ2: [3 1 5 3 2 5]	0.1875	1.25	3-phase	TP [15]	Φ1: [2 4 4 1] Φ2: [3 0 3 0] Φ3: [3 0 2 0]	0.25	1.75
	11. SP-V1-NO	Φ1: [1 0 1 0 2 1] Φ2: [3 1 5 3 5 0]	0.1875	1.25					

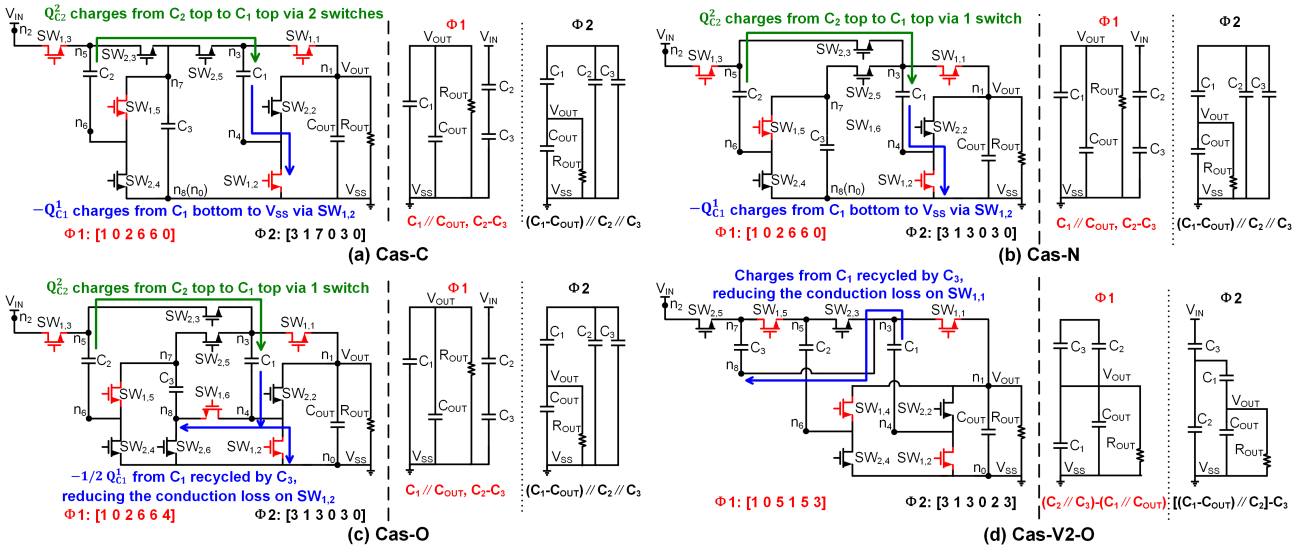


Fig. 7. 4:1 converters based on cascaded two 2:1 converter topology: (a) Cas-C, Cascaded two 2:1 converter topology with conventional wiring method; (b) Cas-N, Cascaded two 2:1 converter topology with normalized wiring method; (c) Cas-O, Cascaded two 2:1 converter topology with optimized wiring method; (d) Cas-V2-NO, the second variant of Cascaded two 2:1 converter topology with optimized wiring method.

Fig. 7(d) shows the schematic and equivalent circuit in each phase for Cas-V2-O, the second variant of cascaded two 2:1 converter topology with the optimal wiring method. During Φ1, the paralleled C_2 and C_3 are placed at the top of the paralleled C_1 and the output. Hence, C_2 and C_3 share the same voltage, as do C_1 and the output. During Φ2, C_2 and C_3 are connected in series and charged by the input source, resulting in a voltage of 1/2 V_{IN}. Meanwhile, C_1 and the output are connected in series and charged by 1/2 V_{IN}, resulting in a voltage of 1/4 V_{IN} at the output. In Cas-V2-O, a charge recycling path is formed between the bottom terminal of C_3 and the top terminal of C_1 without introducing additional switches. Therefore, it has the lowest K_{FSL} value of 1.75 among the cascaded two 2:1 converter topology categories.

B. SPICE Simulation and Topology Comparison

Cas-C, Cas-N, Cas-O, and Cas-V2-O are verified based on 55 nm technology. The switches are implemented by CMOS transmission gates each consisting of a 200μ m/60nm

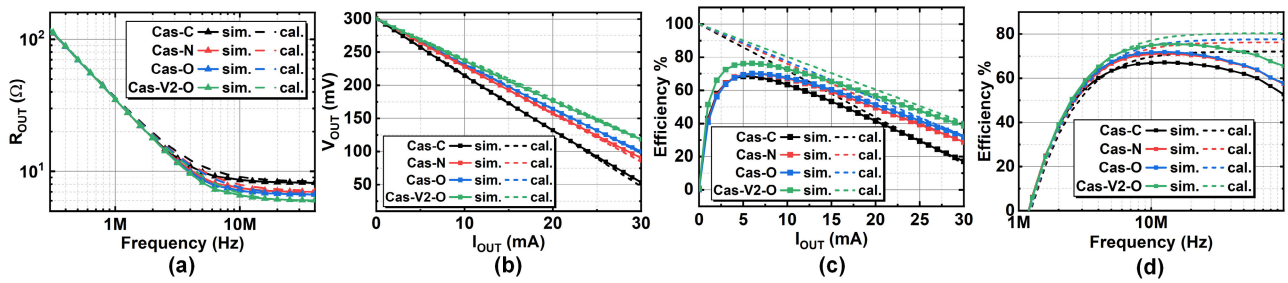


Fig. 8. Theoretical calculation and simulations for 4:1 converters based on cascaded two 2:1 converter topology: (a) equivalent output resistance; (b) output voltage versus output current; (c) efficiency versus output current at a switching frequency of 40 MHz; (d) efficiency versus frequency at an output current of 10 mA.

PMOS and 160μ m/60nm NMOS. The nominal voltages for MOSFETs are 1.2 V, and the flying capacitors are 10 nF MOM capacitors. The parasitic resistance and capacitance are extracted for post-layout simulation.

Fig. 8(a) shows the theoretical calculation and simulated output resistance versus frequency. In the low-frequency domain where R_{SSL} dominates, the calculated and simulated output resistances are the same because Cas-C, Cas-N, Cas-O, and Cas-V2-O have the same K_{SSL} values and thus the same R_{SSL} values. When R_{SSL} and R_{FSL} are close, the simulated output resistance is higher than the calculated output resistance [11]. In the high-frequency domain where R_{FSL} dominates, the calculated and simulated output resistances are consistent with K_{FSL} values. For example, Cas-V2-O has the lowest K_{FSL} value of 1.75, the lowest calculated and simulated output resistance of 5.9 Ω and 6.0 Ω, while Cas-C has the highest K_{FSL} value of 2.5, the highest calculated and simulated output resistance of 8.4 Ω and 8.2 Ω. Fig. 8(b) shows the theoretical calculation and simulated output voltage versus output current at a clock frequency of 40 MHz. Due to their output resistance, when the output current is increased from 0 to 30 mA, Cas-V2-O shows the lowest calculated and simulated output voltage drop of 180.0 mV and 181.6 mV, while Cas-C shows the highest calculated and simulated output voltage drop of 252.7 mV and 246.6 mV.

Fig. 8(c) shows the theoretical calculation and simulated efficiency versus output current at a clock frequency of 40 MHz. When the output current is low, the efficiency is dominated by the parasitic coupling loss and gate driving loss, and the calculated efficiency is higher than the simulated efficiency. At an output current of 4 mA, Cas-C, Cas-N, and Cas-O show similar simulated efficiencies of $\sim$ 68%, while Cas-V2-O shows a higher simulated efficiency of 75.2%. When the output current is high, the efficiency is dominated by the loss from output resistance, and the simulated efficiency approximates the calculated efficiency. At an output current of 20 mA, Cas-C shows the lowest calculated and simulated efficiency of 43.9% and 41.5%, Cas-O shows improved calculated and simulated efficiency of 54.9% and 51.3%, while Cas-V2-O shows the highest calculated and simulated efficiency of 60.5% and 56.7%.

Fig. 8(d) shows the theoretical calculation and simulated efficiency versus frequency at an output current of 10 mA. When the frequency is low, the efficiency is dominated by the loss from output resistance and the simulated efficiency matches with the calculated efficiency. When the frequency is high, the parasitic coupling loss and gate driving loss are notable, and the simulated efficiency is lower than the calculated efficiency. Compared with the conventional wiring method (Cas-C), the optimal wiring method (Cas-O) has improved the simulated peak efficiency from 67.2% to 71.9%, while Cas-V2-O shows the highest simulated peak efficiency of 75.4%.

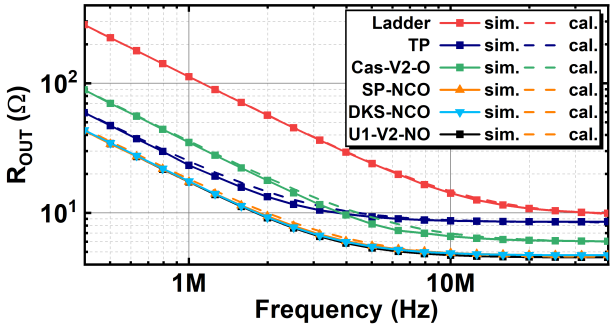


Fig. 9. Theoretical calculation and simulated equivalent output resistance for converters with the minimal K_{SSL} and K_{FSL} values in their categories.

Converters with the minimal K_{SSL} and K_{FSL} values in their categories, Cas-V2-O, DKS-NCO [38], SP-NCO [40], U1-V2-O are compared with the conventional ladder converter (Ladder) [39] and the three-phase converter (TP) proposed in [15]. These converters are simulated based on the same switching frequency. Fig. 9 shows the theoretical calculation and simulated output resistance of these converters. U1-V2-O, DKS-NCO, and SP-NCO show similar simulated output resistance and the same calculated output resistance due to the same K_{SSL} and K_{FSL} values of 0.1875 and 1.25. In lower frequencies, TP shows a lower output resistance compared to Cas-V2-O due to its K_{SSL} value of 0.25, which is lower than the K_{SSL} value of Cas-V2-O, 0.375. In higher frequencies, TP shows a larger output resistance due to its K_{FSL} value of 2.625, which is larger than the K_{FSL} value of Cas-V2-O, 1.75. TP achieves a lower K_{SSL} value because it has fewer capacitors and the output charge flow is distributed to three phases. According to (17), reducing the capacitor charge flow in each phase results in a quadratic decrease of the K_{SSL} value. On the contrary, TP has a larger K_{FSL} value because the switch charge flow is completed in a shorter phase, leading to a larger current and conduction loss. According to (27), the K_{FSL} value is in inverse proportion to the duty cycle of each phase. Thus, compared with a two-phase converter, a converter

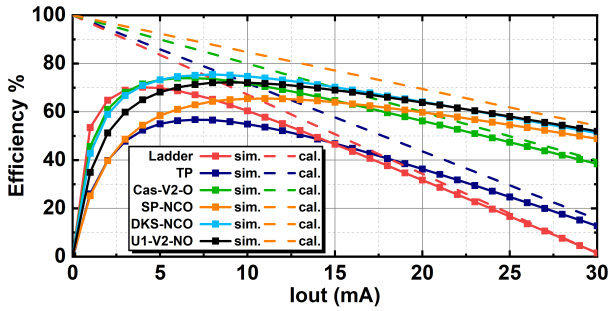


Fig. 10. Theoretical calculation and simulated efficiency versus output current at a frequency of 40 MHz for converters with the minimal K_{SSL} and K_{FSL} values in their categories.

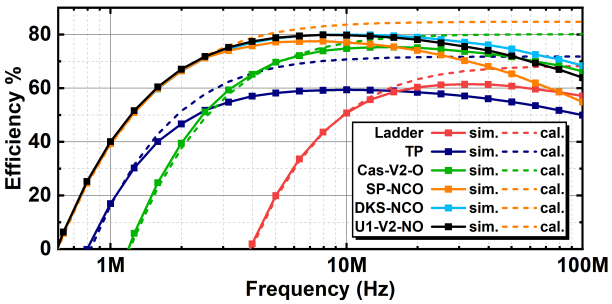


Fig. 11. Theoretical calculation and simulated efficiency versus frequency at an output current of 10 mA for converters with the minimal K_{SSL} and K_{FSL} values in their categories.

with three or more phases has a lower output resistance at low frequencies but a higher output resistance at high frequencies.

Fig. 10 shows the theoretical calculation and simulated efficiency versus output current of these converters at a frequency of 40 MHz. As the output current increases, the loss from output resistance becomes dominant, and the simulated efficiency approaches the calculated efficiency. At an output current of 30mA, U1-V2-NO, SP-NCO, and DKS-NCO show simulated efficiencies of 54.2%, 48.8%, and 51.1%, respectively, while Ladder, TP, and Cas-V2-O show simulated efficiencies of 1.5%, 12.7%, and 38.4%, respectively. Fig. 11 shows theoretical calculation and simulated efficiency versus frequency for these converters at an output current of 10 mA. As the frequency increases, the parasitic loss becomes notable, and the simulated efficiency gradually becomes lower than the calculated efficiency. U1-V2-O, SP-NCO, and DKS-NCO show similar simulated peak efficiencies of 79.9%, 77.5%, and 80.0%, respectively, while Cas-V2-O, Ladder, and TP have peak efficiencies of 75.3%, 61.5%, and 59.4%, respectively.

V. Case Study: Synthesis of 8:1 Step-Down SC DC-DC Power Converters

A case study on the proposed synthesis methodology for 8:1 power converters is discussed as follows: Based on (32), the number of capacitors N is determined to be 4 to achieve the 1/8 conversion ratio. There are a total of $(2N)^{2N} = 16,777,216$ topologies enumerated based on N=4. Based on our proposed rule-based clustering reduction techniques (Section III-B and III-C), a total of 458 topologies with normalized wiring methods are obtained, reducing the number of topologies by 36631.5×. Therefore, there a total of $((458 \times 457)/2) \times 4! = 2,511,672$ power converters being enumerated.

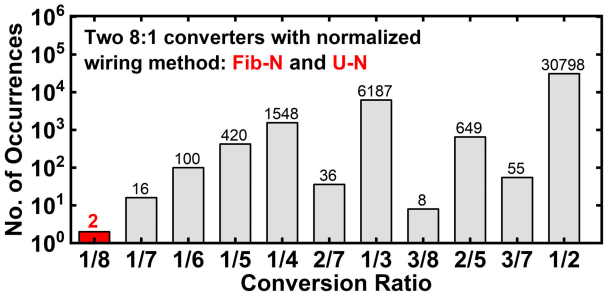


Fig. 12. Conversion ratio distribution for 4-capacitor converters with normalized wiring method.

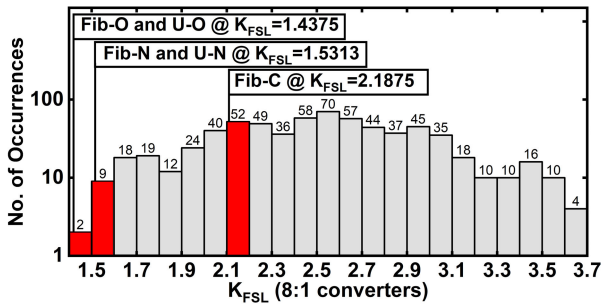


Fig. 13. Histogram of K_{FSL} values for 8:1 converters with alternative wiring methods.

After analyzing the validity of each power converter and its conversion ratio, the total number has reduced to 180,752 (13.9×).

Fig. 12 presents the distribution of conversion ratios based on 180,752 power converters. Two converters are 8:1 converters. One is based on the Fibonacci topology (FiB-N) and the other is based on a new topology unrecorded in the prior works (U-N). The alternative wiring methods for the two topologies are searched and their corresponding K_{FSL} values are shown in Fig. 13. The topologies with the optimal wiring methods are denoted as FiB-O and U-O. Additionally, the Fibonacci converter [12] is denoted as FiB-C for its conventional wiring method. The topological vectors, K_{SSL} values, and K_{FSL} values for converters with normalized, optimal, and conventional wiring methods are summarized in Table III.

Table IV compares our work with the prior work [29]. Compared with [29], our method additionally computes 460,536 iterations in Task-II to remove the redundant topology based on interchangeable wiring methods and 6,635 iterations in Task-III to remove the redundant topology based on interchangeable capacitors. These topology removal techniques reduce the number of unique topologies to 458, which in turn reduces the number of power converters from 5.4×10^{10} to 2,511,672. Thus, our method has dramatically reduced the computation on evaluating the conversion ratio of power converters (Task-IV). The additional run-times in computing Task-II and Task-III are 0.588 s and 0.405 s, respectively, which are negligible compared to the total run-time of 439.473 s. In contrast, 278.467 s are required to compute 2,511,672 iterations in Task-IV in our work. Based on the 5.4×10^{10} iterations in Task-IV that need to be computed in work [29], we estimate that their method takes 5.94×10^6 s to analyze conversion ratios, which dominates its total run-time. Therefore, by reducing the number of Task-IV that need

TABLE III
8:1 STEP-DOWN SC DC-DC POWER CONVERTERS

Category	Converter	Topological Vectors	K_{SSL}	K_{FSL}	Category	Converter	Topological Vectors	K_{SSL}	K_{FSL}
Fibonacci	FiB-N	Φ1: [1 0 2 6 6 0 6 1] Φ2: [3 1 5 0 5 3 3 0]	0.2344	1.5313	Unrecorded	U-N	Φ1: [1 0 5 0 5 0 5 1] Φ2: [3 1 5 3 2 5 3 0]	0.2344	1.5313
	FiB-C [12]	Φ1: [1 0 2 6 6 0 7 3] Φ2: [3 1 5 0 5 9 3 0]	0.2344	2.1875		U-O	Φ1: [1 0 5 0 9 0 5 1] Φ2: [3 1 5 3 2 5 3 0]	0.2344	1.4375
	FiB-O	Φ1: [1 0 2 6 9 0 6 1] Φ2: [3 1 5 0 5 3 3 0]	0.2344	1.4375					

TABLE IV
COMPUTATIONAL TASKS AND RUN-TIME OF 8:1 STEP-DOWN SC DC-DC POWER CONVERTER SYNTHESIS METHODS

Method	Number of Task-I	Number of Task-II	Number of Task-III	Number of Task-IV	Run-time of Task-I	Run-time of Task-II	Run-time of Task-III	Run-time of Task-IV	Run-time of Other Functions	Total Run-time
[29]	16,777,216	0	0	5.4×10^{10}	*141.243 s	0	0	*5.94×10^{6} s	N.A.	*5.94×10^{6} s
Our work	16,777,216	460,536	6,635	2,511,672	141.243 s	0.588 s	0.405 s	278.467 s	18.77 s	439.473 s

* Estimated run-time based on the number of tasks. The synthesis framework is validated using NVIDIA GEFORCE RTX 3060 GPU and the run-time is tracked using a timing profiler. Task-I: Identifying valid topologies; Task-II: Topology removal technique #2: Interchangeable Wiring; Task-III: Topology removal technique #3: Interchangeable Capacitors; Task-IV: Conversion ratio analysis.

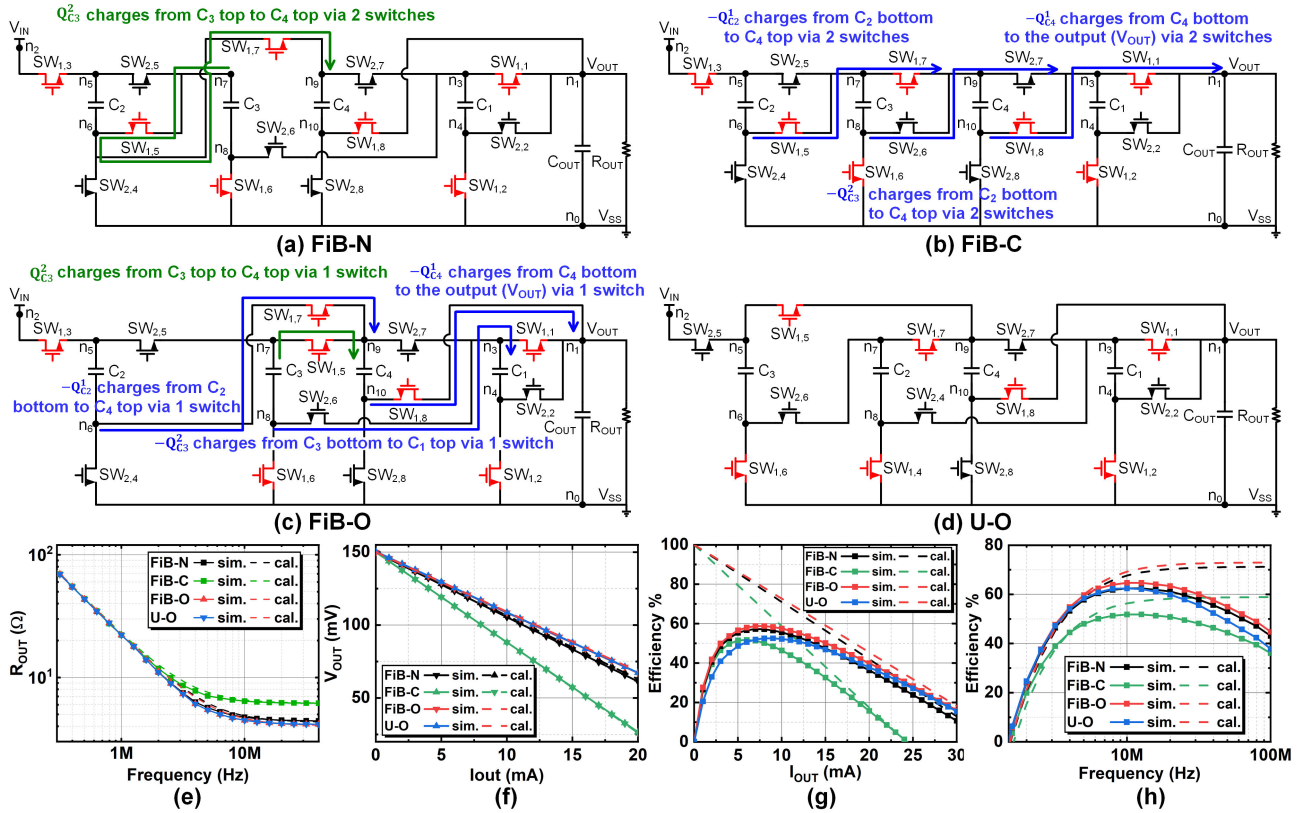


Fig. 14. 8:1 converter topologies: (a) FiB-N, Fibonacci converter with normalized wiring method; (b) FiB-C, Fibonacci converter in canonical form; (c) FiB-O, Fibonacci converter with optimized wiring method; (d) U-O, Unrecorded converter with optimized wiring method.(e) equivalent output resistance. (f) output voltage versus output current; (g) efficiency versus output current at a frequency of 40 MHz; (h) efficiency versus frequency at an output current of 10 mA.

to be computed, the topology removal techniques based on interchangeable wiring methods and interchangeable capacitors have significantly reduced the run-time.

A. Optimization of the Fibonacci Topology

The converters with Fibonacci topology, FiB-C, FiB-N, and FiB-O, are shown in Fig. 14. During Φ1, C_1 and C_4 are connected in series to provide a boosted voltage for C_3, while C_3 and C_2 are connected in series and charged by the input source, V_{IN}. During Φ2, C_1 and the output, V_{OUT}, are connected in series to provide a boosted voltage for C_4, while C_4 and C_3 are connected in series to provide a boosted voltage for C_2. Thus, the voltages of the output, C_1, C_4, C_3, C_2, and V_{IN} are proportional to numbers in the Fibonacci sequence. The normalized capacitor charge flow in Φ1 and Φ2 is:

$$[Q^1_{C1}, Q^1_{C2}, Q^1_{C3}, Q^1_{C4}] = [-0.375, 0.125, -0.125, 0.25]Q_{OUT}, \quad (35)$$

$$[Q^2_{C1}, Q^2_{C2}, Q^2_{C3}, Q^2_{C4}] = [0.375, -0.125, 0.125, -0.25]Q_{OUT}. \quad (36)$$

During Φ1 of FiB-C, a total of $-Q^1_{C2}$ charges flow from the bottom terminal of C_2 to the top terminal of C_4 via

two switches, $SW_{1,5}$ and $SW_{1,7}$, while during $\Phi 1$ of FiB-O, these charges only flow through $SW_{1,7}$. Thus, compared with the conventional wiring method, the optimal wiring method reduces the normalized charge flow of $SW_{1,5}$ from 0.25 to 0.125. Similarly, the normalized charge flow of $SW_{2,7}$ is reduced from 0.375 to 0.25, and that of $SW_{1,1}$ is reduced from 0.625 to 0.375. As a result, compared with the conventional wiring method, the optimal wiring method reduces the K_{FSL} value from 2.1875 to 1.4375. During $\Phi 1$ of FiB-N, a total of Q_{C3}^{1} charges flow from the top terminal of C_3 to the top terminal of C_4 via two switches, $SW_{1,5}$ and $SW_{1,7}$, while during $\Phi 1$ of FiB-O, these charges only need to flow through $SW_{1,5}$. Thus, compared with FiB-N, FiB-O reduces the normalized charge flow of $SW_{1,7}$ from 0.25 to 0.125 and the K_{FSL} value from 1.5313 to 1.4375.

The 8:1 converter with an unrecorded topology and the optimal wiring method, U-O, is shown in Fig. 14(d). During $\Phi 1$, C_1 and C_4 are connected in series to provide a boosted voltage to C_2 and C_3. During $\Phi 2$, C_1 and the output are connected in series to provide a boosted voltage to C_4, while C_3, C_2, C_1, and the output are cascaded and charged by the input source. Therefore, the voltage of the output, C_1, C_4, and C_2 (C_3) are proportional to numbers in the Fibonacci sequence, while C_2 and C_3 share the same voltage. Thus, compared with the Fibonacci topology, the voltage across C_2 in the unrecorded topology is reduced from 0.675 V_{IN} to 0.325 V_{IN}. The normalized charge flow of capacitors and switches in U-O is similar to that of FiB-O, and they have the same K_{SSL} value of 0.2344 and K_{FSL} value of 1.4375.

B. SPICE Simulation and Topology Comparison

The converters FiB-N, FiB-C, FiB-O, and U-O are simulated based on the same technology node and circuit implementation as those detailed in Section IV. Fig. 14(e) shows the theoretical calculation and simulated output resistance of FiB-N, FiB-C, FiB-O, and U-O. The calculated output resistance for FiB-O and U-O are the same due to their same K_{SSL} and K_{FSL} values. In the low-frequency domain where R_{SSL} dominates, the calculated and simulated output resistances for FiB-C, FiB-N, FiB-O, and U-O are the same because they have the same K_{SSL} value and thus the same R_{SSL} value. In the high-frequency domain where R_{FSL} dominates, the calculated and simulated output resistance for each converter is consistent with its K_{FSL} value. For example, FiB-O and U-O have the same K_{FSL} value of 1.4375 and similar simulated output resistances of 4.15 Ω and 4.17 Ω, respectively, while FiB-C has the highest K_{FSL} value of 2.5 and the highest simulated output resistance of 6.14 Ω. Fig. 14(f) shows theoretical calculation and simulated output voltage versus output current. Due to their output resistance, when the output current is increased from 0 to 20 mA, FiB-O and U-O show a simulated output voltage drop of 82.9 mV and 82.7 mV, respectively, while FiB-C shows the highest simulated output voltage drop of 123.4 mV.

Fig. 14(g) shows theoretical calculation and simulated efficiency versus output current at a clock frequency of 40 MHz. As the output current increases, the loss from output resistance becomes dominant, and the simulated efficiency approaches the calculated efficiency. At an output current of 15 mA, the optimal wiring method (FiB-O) has improved the simulated efficiency from 32.6% to 50.2% as compared to the conventional wiring method (FiB-C), while U-O shows a simulated efficiency of 46.8%. Fig. 14(h) shows theoretical calculation and simulated efficiency versus frequency at an output current of 10 mA. As the frequency increases, the parasitic loss becomes notable, and the simulated efficiency gradually becomes lower than the calculated efficiency. Compared with the conventional wiring method (FiB-C), the optimal wiring method (FiB-O) has improved the simulated peak efficiency from 51.8% to 64.6%, while U-O shows a simulated peak efficiency of 62.4%.

VI. Conclusion

This paper describes a framework to synthesize two-phase step-down SC DC-DC converters with a specified conversion ratio and number of capacitors. In the case study of 8:1 converter synthesis, the proposed rule-based clustering reduction techniques have significantly reduced the computation on conversion ratio analysis from 5.4 $\times 10^{10}$ iterations to 2,511,672 iterations, which in turn reduces the run-time from an estimated 5.94 $\times 10^{6}$ s to 278.467 s. Based on the proposed efficiency optimization method, the optimal wiring methods for conventional cascaded 2:1 converter and Fibonacci converter improve their peak efficiencies by 4.7% and 12.8%. The synthesis framework has identified new topologies or topology variants for conventional topologies. The variant of cascaded 2:1 converter topology improved the peak efficiency of the conventional topology by 8.2%.

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