Guest Editorial: Special Issue on Learning, Optimization, and Implementation for Circuits and Systems Driven by Artificial Intelligence

CIRCUITS and systems, such as multidimensional and nonlinear ones, large-scale integration circuits, and power networks, play a significant role in the whole spectrum of science and technology, from basic scientific theories to various real-world applications. With the increasing demand from applications, it is vital to develop circuits and systems with high accuracy, stability, flexibility, and security through efficient learning, design optimization, and integrated implementation. The rapid advancement of artificial intelligence (AI) has fostered a symbiotic relationship between circuits and systems and AI in both theory and applications. On the one hand, research in circuits and systems on efficient learning, design optimization, and integrated implementation aided by AI has recently gained a promising development, where energy-efficient circuits and systems have a very broad range of applications. On the other hand, the utilization of AI in real-world applications has become indispensable for the optimization and implementation of circuits and systems with high efficiency and low-power computation. Overall, through advanced learning, optimization, and implementation driven by AI, efficient circuits and systems running in real-time with low power can be realized for wider applications.

In view of this, the aim of this Special Issue is to present a collection of the latest research advancements focused on learning, optimization, and implementation for circuits and systems through the assistance and utilization of AI. Following a rigorous peer-review process of the submitted manuscripts, 31 articles have been chosen for inclusion in this Special Issue. A summary of these contributions, categorized into the aspects of learning, optimization, and implementation, is provided as follows.

Learning: From the view of efficient learning for circuits and systems, AI-based methods provide deeper insights into the behavior of circuits and systems, revealing complex patterns and ensuring stable and robust performance of circuits and systems. In [A1], Zhang et al. proposed an AI-based detection and countermeasure strategy to protect load frequency control (LFC) systems from false data injection attacks. The effectiveness of this strategy is illustrated through simulations of two interconnected power systems. In [A2], Lu et al. introduced two machine learning methodologies to predict simulation-based fault injection outcomes at the gate level, enabling early-stage circuit reliability analysis. Graph neural networks are employed to represent circuits as graphs, enhancing prediction performance. To learn and analyze the robustness of systems, in [A3], Zhang et al. proposed a novel, versatile, and unified robustness learning approach based on a customized graph transformer (NRL-GT). NRL-GT simultaneously accomplishes robustness curve learning, overall robustness learning, and synthetic network classification tasks. This approach efficiently handles complex networks with varying sizes for different tasks.

Optimization: The current circuit and system processes face challenges in meeting specific requirements, minimizing power consumption, and optimizing control, which underscore the importance of optimization in various aspects such as identifying optimal design parameters, designing energy-efficient circuits, developing scheduling algorithms, and making control strategies. AI-based methods offer a promising solution to automate the design process, accelerate innovation, and generate highly optimized circuits and systems that meet stringent design objectives. In [A4], Díaz-Lobo et al. propose a high-level synthesis methodology for sigma-delta modulators. This methodology integrates behavioral modeling and simulation for performance evaluation and utilizes artificial neural networks to generate high-level design variables to meet specified requirements. Experiments demonstrate that the presented approach yields more efficient design solutions in terms of performance metrics and CPU time. To mitigate process, voltage, and temperature (PVT) variations, which involve analyzing offsets of dc operating points in the design, Li et al. [A5], develop a "PVT-Transfer" framework to facilitate knowledge transfer with evolutionary design. Design knowledge is transferred through parameter migration by cross-operating the circuit parameters under variations, thus enhancing the robustness of the resultant circuit. In [A6], Gubbi et al. proposed an optimized and automated secure IC (OASIC) design flow as a defense-in-depth approach to minimize overhead while maximizing security. Their results indicate that the proposed OASIC design flow can maximize security while incurring less than 15% area overhead and maintaining a similar power footprint compared to the original design. Furthermore, in [A7], Choi et al. proposed an MA-Opt as an analog circuit optimizer using a reinforcement learning-inspired framework. MA-Opt offers multiple predictions of optimized circuit designs simultaneously and introduces a novel approach to iteratively refine previously optimized designs into further optimized ones. In [A8], Cai et al. proposed a thru-reflect-line neural network (TRL-NN) to achieve accurate calibration. The

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experimental results demonstrate that TRL-NN can effectively calibrate a transmission line spanning the entire *D*-band of 110–170 GHz. In [A9], Yi et al. proposed the Skew-CIM technique as a software-hardware co-design approach aimed at disrupting the balance between '0' and '1' states while preserving accuracy. This technique is applicable to a wide range of analog-mixed-signal compute-in-memory systems, particularly those with memories showing large on-off cell current ratios.

To optimize the processes of circuits and systems and accomplish energy-efficient applications, several approaches have been developed to compute faster with fewer memory requirements. In [A10], Chang et al., proposed a range-aware rounding (RAR) method for runtime bit-width adjustment, eliminating the need for predeployment efforts. RAR can be seamlessly integrated into a computing-in-memory accelerator to reduce the energy consumption of convolutional neural networks while maintaining accuracy. Moreover, in [A11], Jung et al. developed an energy-efficient, unified convolutional neural network accelerator for real-time, multiobject semantic segmentation in autonomous electric vehicle systems. The proposed system, integrated with a depth-fused trilateral network, achieves a throughput of 40.07 frames/s in multiobject semantic segmentation applications with high-resolution driving scene datasets. In [A12], Guella et al. proposed the framework MARLIN to deploy layerwise approximate neural networks on PULP, a microcontroller with a RISC-V core, which can leverage the genetic algorithm NSGA-II to search for the best configurations among thousands of approximate neural networks. The experimental results demonstrate a 23.9% reduction in multiplication energy while maintaining 99% accuracy compared to the exact model. To balance performance and power consumption for video rendering applications, in [A13], Zhou et al. developed a deep recurrent deterministic gradient (DRDPG) governor. The DDPG algorithm ensures fine-grained power regulation without action space explosion, while the RNN-FC network topology mitigates the partial observability issue.

AI-based optimization algorithms enable the identification of cost-effective and sustainable solutions in the allocation and utilization of available resources in circuits and systems. In [A14], Cai et al. presented two-step centralized and distributed resource allocation algorithms to address the resource allocation problem of subchannels, transmit power, and RIS coefficients in RIS-aided heterogeneous networks. Their experimental results show that the centralized algorithm achieves a higher total throughput, while the distributed algorithm significantly reduces the resource allocation time. In [A15], Zhang et al. proposed a subgraph-based hierarchical Q-learning network approach to solve the optimal resource scheduling problem for complex industrial networks. Numerical experiments simulating industrial scheduling scenarios validate the effectiveness and advantages of the proposed method. Moreover, in [A16], Zhou et al. proposed a novel fully distributed proximal alternating direction method of multipliers to address the social welfare maximization problem for optimal energy management in a smart grid. In [A17], Ju et al. introduce fixed-time neurodynamic algorithms with time-varying coefficients for composite optimization problems. Numerical experiments on image recovery and sparse logistic regression validate the superiority of the proposed algorithms. Furthermore, in [A18], Li et al. presented a distributed neurodynamic optimization algorithm to achieve an optimal energy management for networked microgrids, ensuring load requirements and stability. An illustrative example involving 3-MG NMGs is elaborated to demonstrate the validity and effectiveness of the proposed algorithm.

To facilitate optimal decision-making in circuits and systems under varying conditions, it is essential to employ appropriate control strategies that enable real-time adaptation and response to changing circumstances. To address the near-optimal control problem of discrete-time switched nonlinear systems with hysteresis, in [A19], Li et al. designed an optimal control scheme. System transformation is utilized to avoid non-causal problems, and an action-critic network is employed to offset the influence of hysteresis, ensuring system stability and minimizing the performance index of the subsystem. In [A20], Yan et al. designed a new mode-dependent RL algorithm of identifier-critic-actor architecture to address the adaptive optimized tracking control problem for strict-feedback cyclic switched nonlinear output constrained systems with average cyclic dwell time. Furthermore, in [A21], Cui et al. proposed an adaptive horizon mechanism design methodology based on deep reinforcement learning (DRL) for generalized predictive control. Simulation and experimental comparisons with other controllers demonstrate the efficacy and performance improvements. In [A22], Wang et al. presented a novel shifting function to unify initial values, along with an adaptive neural tracking control scheme, addressing a neuro-adaptive fixed-time tracking control issue for switched nonlinear systems subject to asymmetric time-varying constraints and unknown control gains. Moreover, in [A23], Geng et al. developed a unified framework for realizing prespecified-time intermittent control and theoretically analyzed to achieve prespecified-time bipartite consensus for both leaderless and leader-following multiagent systems. Numerical examples of actual circuit systems are provided to validate the theoretical results and their application.

Implementation: From the perspective of integrated implementation, both hardware and software implementation for circuits and systems need to consider utilization, adaptability, and compatibility. To make hardware suitable for the implementation of AI algorithms, it is critical to design hardware with efficient data movement, high-speed memory, flexibility, and programmability. In [A24], Chen et al. present a 50-Gb/s optical receiver (ORX) chipset, comprising a transimpedance amplifier and a clock and data recovery circuit in a 45-nm silicon-on-insulator CMOS. When integrated with a high-speed silicon photonics photodetector, the ORX achieves an input sensitivity of −7.7 dBm at 50 Gb/s with a power efficiency of 1.61 pJ/bit. It enables data recovery at a quarter rate of 12.5 Gb/s with low output jitter and phase noise. In [A25], Kumar et al. proposed a field-programmable analog machine learning processor named "ARYABHAT." ARYABHAT employs a fully reconfigurable tile-based modular analog architecture, allowing for adjustable throughput and configurable energy requirements, thus enabling its suitability for various machine-learning computations. Furthermore,

in [A26], Valente et al. present Shaheen, a 9 mm^2 200-mW SoC implemented in 22-nm FDX technology. Shaheen integrates a Linux-capable RV64 core and a fully programmable energy and area-efficient multi-core cluster of RV32 cores. Experiments across a wide range of benchmarks demonstrate the capabilities of the proposed SoC. In [A27], Shakibhamedan et al. propose a Signed Carry Disregard Multiplier for integration into Convolutional Neural Networks. Extensive experiments demonstrate that ACE-CNN outperforms other configurations, providing a favorable balance between accuracy and computational efficiency.

Integrating AI algorithms into hardware and software implementations enhances the flexibility and capabilities of circuits and systems. In [A28], Xiao et al. proposed a memristor-based brain-inspired recognition system. This system emulates the brain's information processing mechanism without requiring additional cross-modal processing, resulting in behavior more akin to human responses. In [A29], Chen et al. introduced a memristor synapse-driven ReLU-type Hopfield neural network for detecting hidden dynamics. Circuit experiments conducted on digital hardware devices confirm the dynamic effects and lossless control of the memristive neural network, as well as the physical reliability of the electronic neuron. In [A30], Li et al. propose a memristor-based neuron circuit system (MNCS) according to the microdynamics of neurons and complex neural cell structures. Both PSpice simulations and practical experiments demonstrate that MNCS can replicate 24 types of repeating biological neuronal behaviors. Moreover, Sharma et al. [A31] proposed a compute-efficient LS-augmented interpolated deep neural network (LSiDNN) based on a CE algorithm and implemented on Zynq SoC. Experiments demonstrate that LSiDNN provides reduced execution time and lower resource utilization.

We hope that 31 articles featured in this Special Issue will soon significantly contribute to the advancement of the utilization of AI in learning, optimization, and implementation for circuits and systems. We extend our sincere appreciation to the contributions of all the authors who submitted their work to this Special Issue and to the dedicated efforts of all reviewers who helped ensure the quality of the selected papers. Finally, we express our gratitude to the Editor-in-Chief, the Deputy Editor-in-Chief, and the editorial office for their timely guidance and consistent support throughout the publication process.

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APPENDIX: RELATED ARTICLES

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