A *W*-Band 2 × 2 Phased-Array Transmitter With Digital Gain-Compensation Technique

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***Abstract*— In this paper, a *W*-band 2 × 2 phased-array transmitter with digital gain compensation is proposed to minimize amplitude and angle errors of synthesized beams. The RF phase-shifting architecture is utilized for the phased-array transmitter to reduce circuit blocks and lower system complexity. The high-resolution phase shifting is achieved by a vector-sum phase shifter, which is based on a quadrature-all-pass filter (QAF) with compensation network and Gilbert-type variable gain amplifiers (VGAs) with digital-controlled current digital-to-analog converters (I-DACs). To lower the gain error introduced by the phase shifter in RF phase-shifting architecture, the variable-gain power amplifier (VGPA) is proposed. The gain of the VGPA is finely adjusted to compensate the gain variation of phase shifter in different phase states. Meanwhile, the phase variation of the VGPA under variable gain states is optimized to avoid the influence on phase errors. To verify the aforementioned mechanism, a *W*-band 2 × 2 phased-array transmitter is implemented and fabricated in a conventional 40-nm CMOS technology. Based on the digital gain-compensation technique, the phased-array transmitter exhibits a less than 1.12dB RMS gain error and less than 1.82° RMS phase error. In addition, the fabricated chip achieves 8.13dBm peak saturated output power and better than 9dB power gain with 135mW power consumption for each channel.**

***Index Terms*— Phased-array transmitter, vector-sum phase shifter, variable-gain power amplifier (VGPA), low gain/phase error, *W*-band.**

I. Introduction

With the ever-development of modern millimeter-wave wireless applications, such as long range communications, imaging systems, and detecting radar, on-chip large scale active electrically scanned phased-array systems are highly demanded [1], [2], [3], [4], [5], [6], [7], [8], [9]. Phased arrays can increase signal-to-noise ratio (SNR), channel capacity, and effective isotropic radiated power (EIRP) to overcome the performance limitation in integrated systems. Besides, for the low loss free-space electromagnetic-wave transmission window around 94GHz, *W*-band phased arrays have been developed using various techniques, especially in CMOS and SiGe technologies.

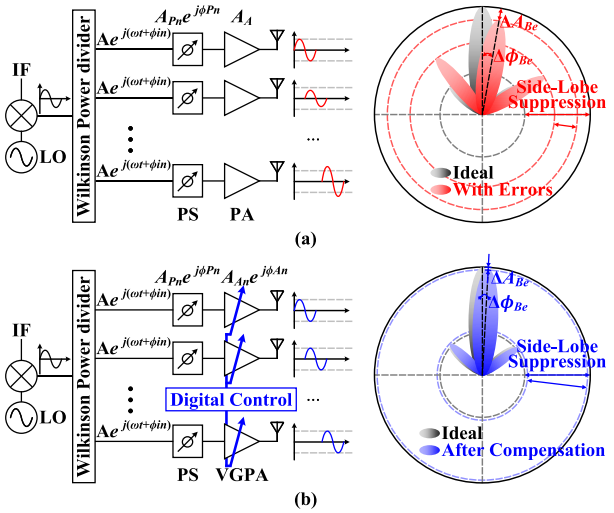

Fig. 1. (a) Simplified architecture of a N-path RF phase-shifting phased-array transmitter with PA. (b) Proposed architecture of a N-path RF phase-shifting phased-array transmitter with VGPA.

To avoid the influence of phase shifters on signal paths, LO phase-shifting architectures are widely used in phased-array systems [10], [11], [12], [13], [14]. In the LO phase-shifting architecture, phase shifters are added in each LO signal path before mixers. Thus, the nonlinearity of phase shifter, such as system linearity and amplitude variation, has a low influence on the performance of phased-array systems. However, mixers are required in each signal channel of the LO phase-shifting architecture, which increases the complexity of phased-array systems. Besides, the floorplan and routing are not easy with the increasing array size of LO phase-shifting phased arrays.

Due to minimized number of circuit blocks and low system complexity, RF phase-shifting architecture has attracted wide attentions both in academia and industry [15], [16], [17], [18], [19], [20], [21], [22], [23], [24], [25], [26], [27], [28], [29]. For such system, shown in Fig. 1(a), phase shifters are placed after mixers in RF link. Thus, many circuit

Manuscript received 13 May 2023; revised 16 September 2023 and 13 November 2023; accepted 3 January 2024. Date of publication 5 February 2024; date of current version 29 March 2024. This work was supported in part by the National Key Research and Development Program of China under Grant 2021YFE0205600, in part by the Shenzhen Science and Technology Program under Grant JCYJ20210324120004013, and in part by the National Natural Science Foundation of China under Grant 61934001 and Grant 62161160310. This article was recommended by Associate Editor M. A. Abdulaziz. *(Corresponding author: Xun Luo.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TCSI.2024.3352594.

Digital Object Identifier 10.1109/TCSI.2024.3352594

blocks can be shared, such as mixers, LO generator, and IF circuits. The array with RF phase shifting could be easily extended for large-scale active electrically scanned phased-array systems. However, the output signal of RF phase shifters is directly amplified by next-stage power amplifiers. Thus, the non-ideality of the RF phase shifter deteriorates the amplitude/angle error and side-lobe suppression of synthesized beams.

For on-chip RF phase shifters, many techniques have been introduced and developed, including switch-type, reflective-type, and vector-sum phase shifter topologies. The passive phase shifters based on switch-type topology are widely used in RF phase-shifting phased-array systems, due to its high linearity and zero power consumption [30], [31], [32], [33]. However, limited by the cutoff frequency of silicon-based technologies, the loss of MOSFET-based switches is large at millimeter wave, especially at *W*-band. Besides, the number of series cell is limited to reduce the insertion loss. Thus, the phase resolution is low and no phase calibration is required. A 4-bit switch-type phase shifter exhibits more than 20-dB insertion loss at *W*-band [30]. Compared to the switch-type phase shifters, reflective-type phase shifters can achieve phase-shifting with a low insertion loss and a relatively small chip size [34], [35], [36], [37], [38], [39], [40]. The trade-off for reflective-type phase shifters exists among phase tuning range, operational bandwidth, and insertion loss. Meanwhile, the phase error is reduced by carefully setting the impedance of tunable reflective loads. A 4-bit reflective-type phase shifter with insertion loss of 7.4dB and phase tuning range of 180° over 88–96GHz is proposed in [35]. Active vector-sum phase shifters are another approach to generate high-resolution phase shifting at millimeter wave [41], [42], [43], [44], [45], [46]. In addition, due to the variable gain amplifier (VGA) in vector-sum phase shifters, the insertion loss is relatively low. For example, better than 0.8-dB power gain is achieved at millimeter wave [43]. A digital-to-analog converter (DAC) for bias current control is widely used in VGA. The current ratios are accomplished by carefully presetting the width of MOSFET in DAC. Thus, digital calibration cannot be performed in traditional analog vector-sum phase shifter. Another challenge of vector-sum phase shifters is the gain variation under different phase states. The gain variation is dramatically increased at millimeter wave, due to the nonlinearity of VGA and large amplitude/phase mismatch of quadrature signals within a wideband. A phase shifter with phase error of 11.2° and gain error of 1.46dB at 89.2GHz is reported in [43].

To show the influence of non-ideality of phase shifters on the phased-array system, the beam patterns are synthesized with and without phase/gain errors. Fig. 2 depicts the synthesized beam patterns for 4- and 64-element phased-array systems under an ideal omnidirectional antenna. Note that the phase and gain errors ($\Delta\phi_{e\_n}$ and ΔA_{e_n}) for each channels are assumed by the Gaussian distribution.

$$\Delta\phi_{e\_n} \sim N(\phi_{avg}, \Delta\phi^2_{e,rms}), \tag{1}$$

$$\Delta A_{e\_n} \sim N(A_{avg}, \Delta A^2_{e,rms}). \tag{2}$$

Both the mean values of phase and gain errors (ϕ_{avg} and A_{avg}) are 0. Besides, the RMS values of phase and gain errors ($\Delta\phi_{e,rms}$ and $\Delta A_{e,rms}$) are 5° and 1.5dB, respectively. For small-scale phased-array system, the non-ideality of phase shifter mainly deteriorates the amplitude/angle error of beam. Meanwhile, for large-scale phased-array system, the non-ideality mainly deteriorates the side-lobe suppression of beam. As shown in Fig. 2, the beam becomes narrower with the increasing scale of phased-array systems. Besides, the scanning resolution θ of beam is determined by the phase resolution ϕ of phase shifter [47], which is expressed as

$$\theta = \sin^{-1}\left(\frac{\lambda\phi}{2\pi d}\right) \tag{3}$$

where d is the distance between two adjacent antennas. For 64-element phased-array system, the 3-dB bandwidth of beam is about 1.6°. When d is $\lambda/2$, less than 5° phase resolution, i.e., larger than 6-bit phase resolution, is required. Thus, for a large-scale phased-array system, high-resolution phase shifters are necessary. Phase shifter with high resolution usually features a low RMS phase error, which leads to a good beam performance. However, increasing the resolution of phase shifter cannot decrease RMS gain error directly. Therefore, the design of high-resolution RF phase-shifting phased-array systems with low phase and gain errors is still a great challenge.

In this paper, phased-array transmitter architecture with variable-gain power amplifiers (VGPAs) is proposed for improved phase and gain errors, as shown in Fig. 1(b). The proposed phased-array transmitter consists of Wilkinson power dividers, vector-sum phase shifters, and VGPAs. The high-resolution phase-shifting characteristic is performed by the vector-sum phase shifter with digital pre-distortion techniques. The VGPAs are proposed to compensate the gain variation generated by the vector-sum phase shifters. With low phase and gain errors, the angle and amplitude errors of synthesized beams are reduced. Besides, after gain compensation, the side-lobe suppression of the beams is improved. To verify the mechanisms mentioned above, a 2 × 2 phased-array transmitter operating from 90 to 98GHz is implemented and fabricated based on a conventional 40-nm CMOS technology [48]. It exhibits a RMS phase error of 1.35°–1.82° and RMS gain error of 0.64–1.12dB. The minimal gain error is reduced from 0.71 to 0.64dB by the digital gain-compensation techniques. Meanwhile, the saturated output power is 8.13dBm for each channel with 135 mW power consumption.

This paper is organized as follows. In Section II, the architecture and operation of digital gain-compensation techniques are introduced. Section III describes the detailed circuit implementation of the phased-array systems. Experimental results and comparison with the state-of-the-arts are discussed in Section IV. Finally, a conclusion is given in Section V.

II. Architecture and Operation

The block diagram of the proposed *W*-band phased-array transmitter with digital gain-compensation techniques is shown in Fig. 3. The transmitter utilizes a 2 × 2 array topology. Each channel is composed of a high-resolution phase shifter and a

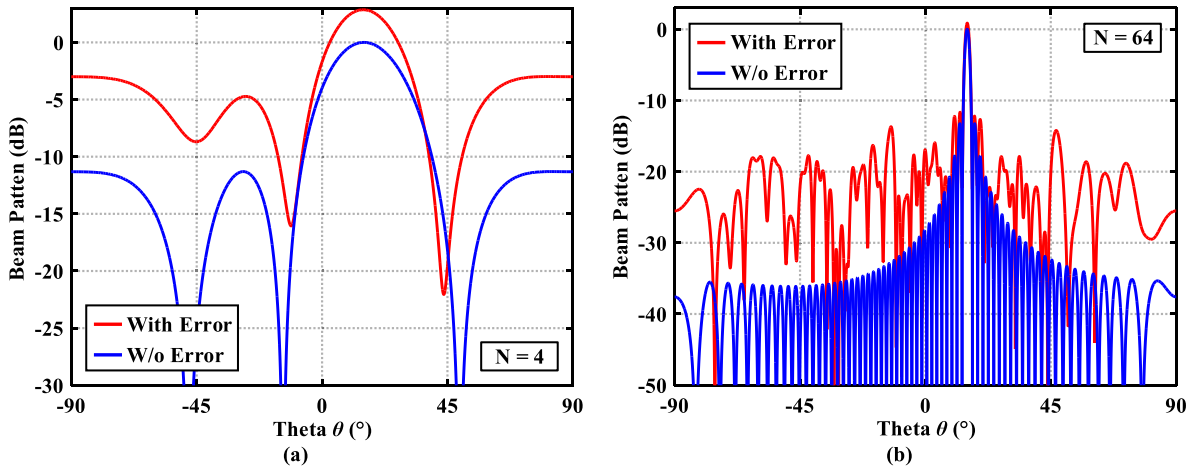


Fig. 2. Synthesized beam patterns with and without errors for (a) 4- and (b) 64-path phased-array transmitter.

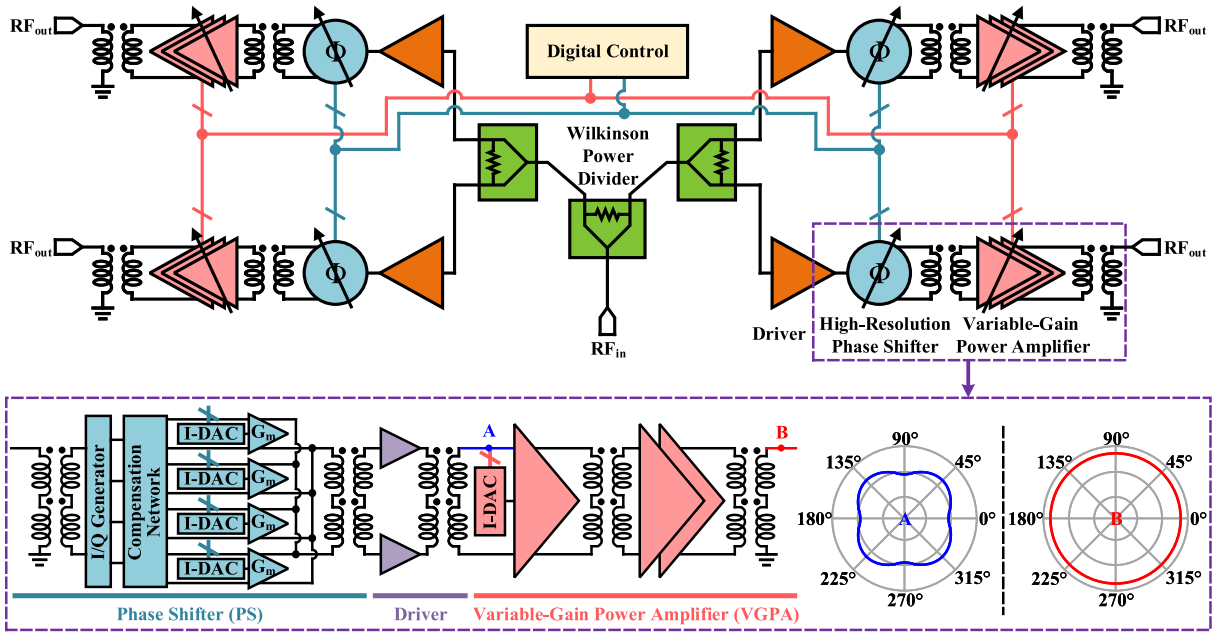


Fig. 3. Block diagram of proposed *W*-band phased-array transmitter with digital gain-compensation technique.

VGPA. Meanwhile, the feed-forward mechanism is utilized to achieve synchronized gain control of VPGA, according to the phase states of phase shifter.

The active phase shifter is implemented based on a quadrature all-pass filter (QAF) for quadrature vectors generation and four VGAs with current digital-to-analog converters (I-DACs) for high-resolution vector modulation. A compensation network is proposed between QAF and VGA circuits to reduce the phase and amplitude mismatches of quadrature signals. Meanwhile, the digital pre-distortion (DPD) technique is utilized for low phase error [49]. To minimize the gain error of whole systems, the three-stage VGPA is introduced. A current source array (CSA) based topology is utilized in the first stage for gain adjustment. Then, the gain variation of output RF signals from phase shifter is compensated by adjusting the gain properly.

In a conventional RF phase-shifting phased-array transmitter, the gain and phase errors are mainly generated from RF phase shifters. Since the gain and phase errors of the reported phase shifters in CMOS technology are large at *W*-band [43], [44], [45], [46], the gain compensation with proper gain tuning range is needed. In addition, with the increasing array size, the bandwidth of the beam becomes narrow. To ensure sufficient beam-steering resolution for good SNR performance, the phase-shifting resolution is also needed to be improved. With improved phase-shifting resolution, the RMS phase error can be decreased simultaneously. However, increasing phase-shifting resolution has little benefit on RMS gain error.

Fig. 4 shows the operation of the proposed gain compensation techniques. The input signal after driver (i.e., node A) is defined as

$$Signal_A = \text{real}(Ae^{j(\omega t+\phi_{in})}) \tag{4}$$

where ω and ϕ_{in} are the frequency and original phase of the input signals, respectively. Then, the RF signal is phase rotated by the phase shifter (i.e., node B), which can be expressed as

$$Signal_B = \text{real}(AG_{PS\_i}e^{j(\omega t+\phi_{in})}e^{j\phi_{PS\_i}}) \tag{5}$$

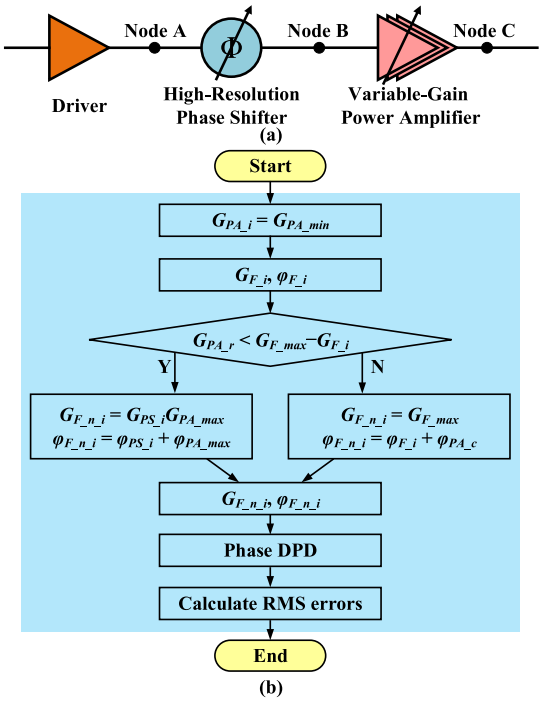


Fig. 4. (a) signal nodes in the transmission channel. (b) Flowchart of the digital gain-compensation techniques.

where G_{PS_i} and ϕ_{PS_i} are the signal gain and phase shifting under i^{th} phase state of the phase shifter, respectively. In general, the signal gain G_{PS_i} is different under various phase states. Next, VGPA is utilized to amplify the signal and compensate the gain variation. Then, the RF signal after VGPA (i.e., node C) can be expressed as

$$Signal_C = \text{real}(AG_{PS\_i}G_{PA\_i}e^{j(\omega t+\phi_{in})}e^{j(\phi_{PS\_i}+\phi_{PA\_i})}) \quad (6)$$

where G_{PA_i} represents the variable gain and ϕ_{PA_i} represents the phase variation of VGPA to compensate the i^{th} gain states. Thus, the final amplitude gain G_{F_i} and phase shifting ϕ_{F_i} of the output signals are

$$G_{F\_i} = G_{PS\_i}G_{PA\_i}, \quad (7)$$

$$\phi_{F\_i} = \phi_{PS\_i} + \phi_{PA\_i}. \quad (8)$$

To reduce the amplitude and phase errors of whole phased-array systems, the amplitude gain G_{F_i} needs to keep constant and the phase shifting ϕ_{F_i} needs to be equal to ideal phase $i \times \phi_{res}$ (ϕ_{res} represents the phase resolution).

Fig. 4(b) illustrates the detailed flowchart of the proposed gain-compensation techniques. Firstly, obtain the amplitude gain G_{F_i} and phase shifting ϕ_{F_i}, when the VGPA is operated at the lowest gain state (i.e., G_{PA_min}). Then, once the difference between amplitude gain G_{F_i} and the maximum amplitude gain G_{F_max} is larger than the gain tuning range of VGPA (i.e., G_{PA_r}), the VGPA is working on maximum gain state (i.e., G_{PA_max}). Meanwhile, the corresponding compensated amplitude gain $G_{F\_n\_i}$ is $G_{PS\_i}G_{PA\_max}$ and phase $\phi_{F\_n\_i}$ is updated as $\phi_{PS\_i} + \phi_{PA\_max}$. On the contrary, once the difference between amplitude gain G_{F_i} and the maximum amplitude gain G_{F_max} is smaller than the gain tuning range G_{PA_r}, the output amplitude gain $G_{F\_n\_i}$ is compensated to be identical (i.e., G_{F_max}). Besides, the phase $\phi_{F\_n\_i}$ is updated as $\phi_{F\_i} + \phi_{PA\_c}$. ϕ_{PA_c} is the phase variation of VGPA under compensation state. Finally, the DPD [49] is employed to choose the optimum results from the compensated phase and amplitude states (i.e., $\phi_{F\_n\_i}$ and $G_{F\_n\_i}$).

III. Circuit Implementation

A. Variable-Gain Power Amplifier

As shown in Fig. 5, the VGPA is composed of three stages for high output power and power gain. The first stage is implemented using a Gilbert-cell type amplifier with CSA, while the rest two stages are implemented using a common-source topology for high output power and linearity. To improve the current tolerance, the transistor is constructed using parallel nMOSs. Three transformers with an output capacitor are utilized for inter-stage and output matching networks.

The detailed schematic of the first stage is shown in Fig. 6(a), where the feed-forward digital-controlled CSA circuit is introduced for gain control. MOSFET M_0 with bias voltage V_b is utilized to ensure the prime power gain, while the six MOSFETs $M_{<1>}$–$M_{<6>}$ with digital control voltages V_{c1}–V_{c6} are used for gain adjustment. Besides, to simplify the layout and digital routing for lower parasitics, the ratio of width and length (i.e., W/L) for the CSA circuit is designed in binary weighted (i.e., ×1, ×2, ×4, …, ×32). The gain control is achieved by turning on/off the MOSFETs in the CSA circuits. To decrease the influence of the VGPA on the phase-shifting characteristic, the phase response is investigated. The phase variation is mainly determined by the imaginary parts of the input impedance at transformer output terminal (i.e., Z_1). The simulated input impedance versus variable gain states is depicted in Fig. 6(b). It is notable that the range of imaginary parts of Z_1 is from 68.27Ω to 68.85Ω. The variation of imaginary part could be optimized by tuning the width of the CSA. Besides, a symmetric configuration for the CSA circuits is introduced for better gain continuity, as shown in Fig. 7(a). The asymmetric configuration, depicted in Fig. 7(b), is utilized for comparison. The post-simulated gain control and phase variation for symmetric and asymmetric configurations are compared, as depicted in Fig. 7(c)-(e). The simulated results exhibit the symmetric configuration features three merits. Firstly, the differential gain continuity for the symmetric configuration are better than the asymmetric one, which is more suitable for gain compensation. Then, the common-mode rejection of symmetric configuration is better than asymmetric configuration. Finally, the phase variation is decreased, when the symmetric configuration is used.

A 1.5-dB gain control range with 6-bit gain resolution and 3.6° phase variation is implemented by the VGPA with symmetric CSA circuits. Note that the gain control range is mainly determined considering the follow aspects: 1) The output phase variation of the VGPA increases with the increasing of gain control range. Thus, to reduce the influence of the VGPA on the phase characteristic of the transmitter, the gain control range of the VGPA is limited. 2) The variable gain of the VGPA is performed to compensate

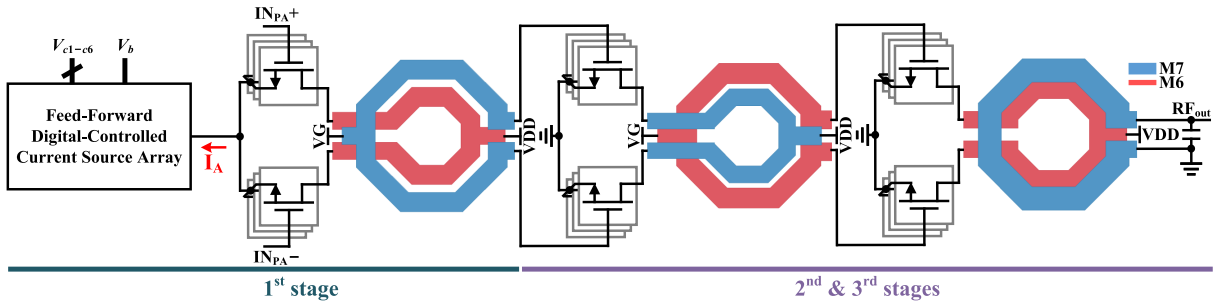


Fig. 5. Schematic of the proposed VGPA.

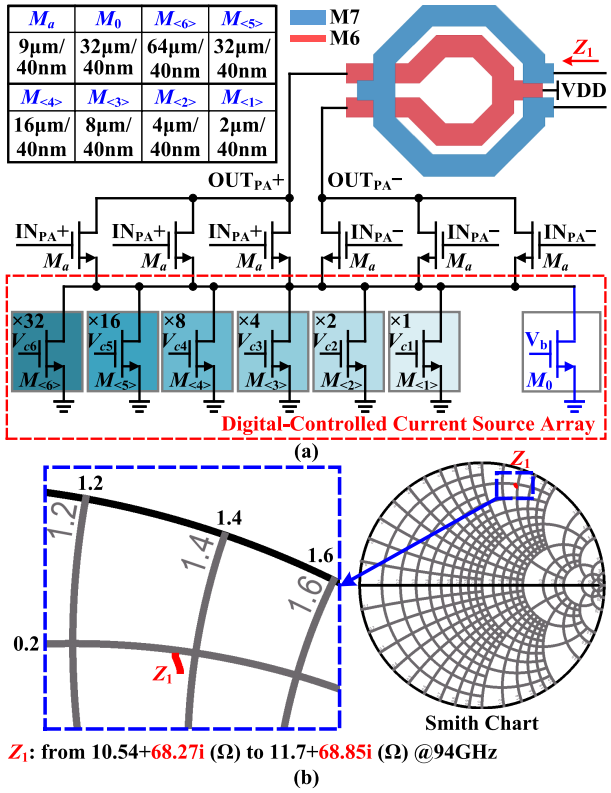


Fig. 6. (a) Schematic of the first-stage power amplifier with CSA circuit. (b) Simulated Z_1 under different gain states.

the gain variation of the vector-sum phase shifter. Thus, the gain control range covers the majority of gain states of the phase shifter. 3) The efficiency of the VGPA decreases with the reduction of power gain. A large gain control range can further compensate the gain error. However, it leads to a poor efficiency. Thus, there is a trade-off between RMS gain error and system efficiency. 4) The gain resolution of the VGPA is a key value for gain-compensation techniques. Under the same gain resolution, a larger gain control range means a larger gain control step, which leads to a worse gain error after gain compensation.

Fig. 8(a) shows the post-simulated power gain and power added efficiency (PAE) of the three-stage VGPA. At 94GHz, the proposed VGPA features a 14.1dB power gain, when the whole digital-control CSA circuits are turned on. Besides, the corresponding PAE is 8%. When all MOSFETs in the CSA circuits are turned off, the power gain decreases to be 12.6dB and the VGPA has a 1.5% efficiency reduction. Fig. 8(b) exhibits the small-signal S-parameters and the Rollet stability factor K. From 90 to 98GHz, the Rollet stability factor K of the proposed VGPA is better than 4.

B. High-Resolution Phase Shifter

To obtain a high-resolution phase-shifting characteristic with low phase error and insertion loss, the vector-sum topology is utilized in phase shifter implementation [50]. Fig. 9(a) illustrates the schematic of the proposed high-resolution phase shifter, which is composed of three parts: QAF, compensation network, and four VGAs. The relative phase shiftings are generated by modulating and synthesizing four quadrature vectors with variable amplitudes, which are produced by VGAs.

The QAF circuit is utilized to generate the quadrature signals. Compared to the traditional two-stage RC poly-phase filter, QAF circuit features a low insertion loss and wide operational bandwidth. However, due to the large parasitics of MOSFET, large amplitude and phase errors of quadrature signals are obtained at W-band. To reduce the influence of the parasitics, an inductor-based compensation network is introduced. The inductor is adopted to counteract the parasitics capacitance of next stage, i.e., the gate terminals of the MOSFET in VGAs. Meanwhile, the parameters of the components (i.e., inductor, capacitor, and resistor) in the QAF circuits are optimized for low phase and amplitude errors within a wideband. Fig. 10 presents the post-simulated phase and amplitude mismatches of the QAF circuits. It is notable that the phase and amplitude mismatches of the QAF circuits are below 5° and 2.2dB from 90 to 98GHz, respectively.

To achieve high-resolution gain modulation, the Gilbert-cell type amplifier with high-resolution I-DAC circuits is proposed for VGA. Considering the polarity of the quadrature vectors, there are four quadrants, i.e., I+/Q+, I–/Q+, I–/Q–, and I+/Q–, which means a 2-bit quadrant-selection resolution. Four pairs of Gilbert-cell type amplifiers are utilized with two turned-on and two turned-off to implement quadrant selection for 360° phase-shifting range. As shown in Fig. 9(b), for quadrants 1 (i.e., I+/Q+), the differential pairs a and b are turning on, while the rest differential pairs c and d are turning off. Such method avoids additional switch circuit in the signal path for polarity selection, which leads to a low loss deterioration characteristic. The gain of the VGA

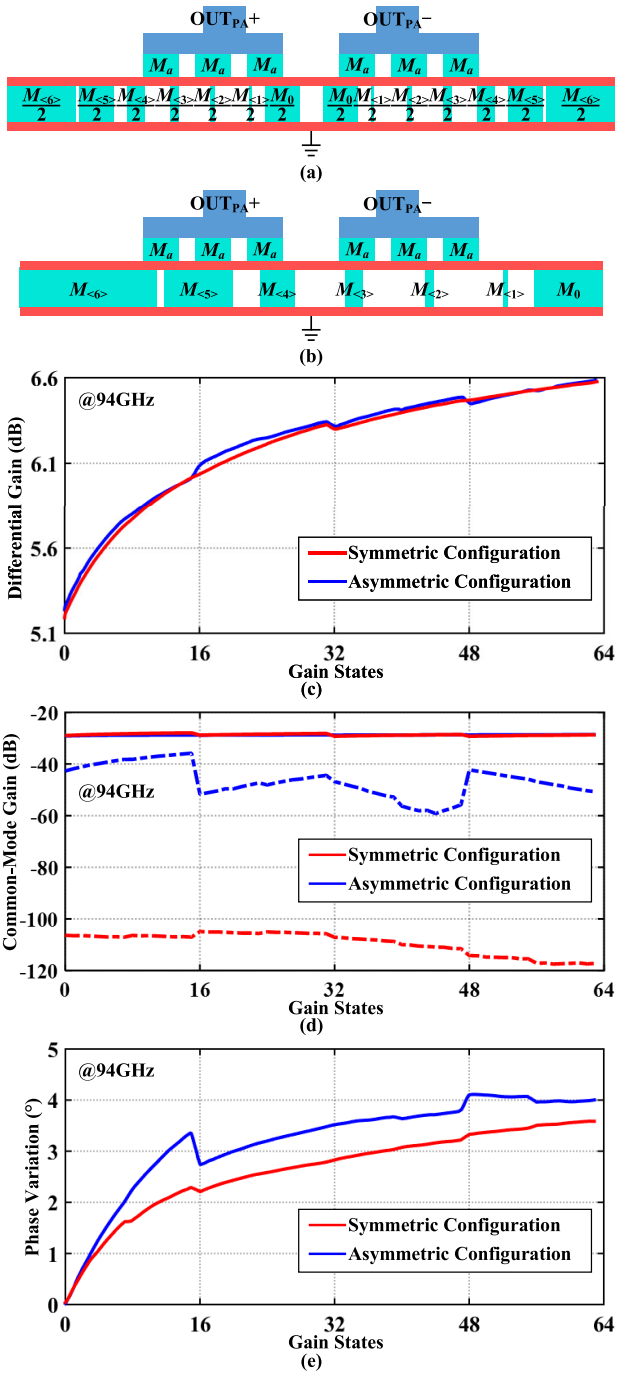


Fig. 7. (a) symmetric and (b) asymmetric configurations of the first stage. Post-simulated (c) differential gain, (d) common-mode gain (dotted line: with ideal transformer, solid line: with practical transformer), and (e) phase variations between symmetric and asymmetric configurations at 94GHz.

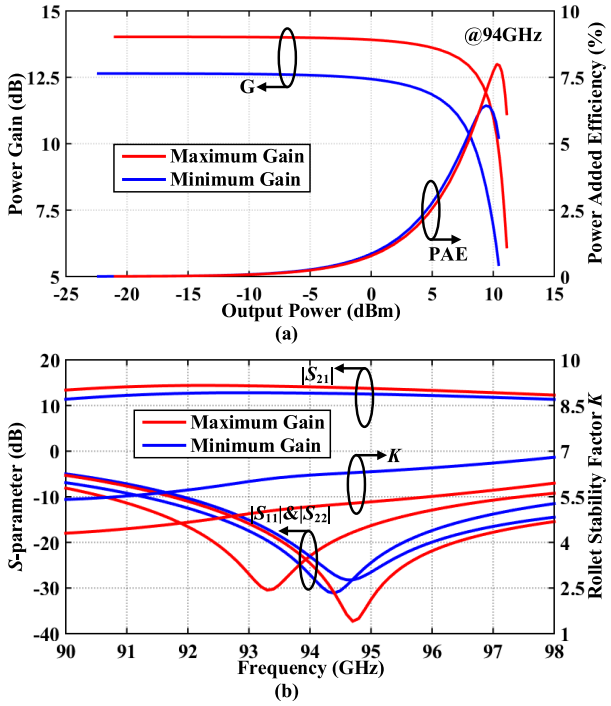
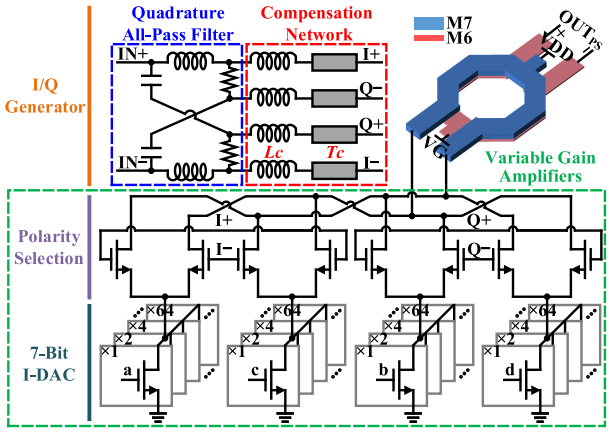


Fig. 8. (a) Simulated power gain and power added efficiency of the proposed VGPA. (b) Simulated *S*-parameter and Rollet stability factor *K*.



OPERATIONAL PRINCIPLE OF PHASE SHIFTER

Quadrant	a	b	c	d
1 (0°~90°)	Code	2^7−Code	0	0
2 (90°~180°)	0	Code	2^7−Code	0
3 (180°~270°)	0	0	Code	2^7−Code
4 (270°~360°)	2^7−Code	0	0	Code

(b)

Fig. 9. (a) Schematic and (b) operational principle of the proposed vector-sum high-resolution phase shifter.

is controlled by turning on or off the MOSFETs in the I-DAC circuits. Meanwhile, to decrease complexity of layout and digital control, the ratio of width and length (i.e., W/L) for the I-DAC circuit is designed in binary weighted (i.e., $\times 1$, $\times 2$, $\times 4$, …, $\times 64$). Adopting this method, only seven MOSFETs are utilized in the I-DAC circuit for a 7-bit gain adjustment. Besides, to simplify control operation, the control code for I and Q paths are complementary, i.e., a(c) + b(d) = 2^7. Then, a 9-bit phase-shifting resolution, i.e., 2-bit quadrant selection and 7-bit gain adjustment, is achieved. Meanwhile, a current limited vector-sum method is adopted to achieve low phase error, gain error, and power consumption [49], simultaneously.

C. Gain-Compensated Transmitter Channel

By combining the high-resolution phase shifter and VGPA, the digital gain-compensated transmitter channel is proposed. Fig. 11 shows the microphotograph of the fabricated gain-compensated transmitter channel. A driver circuit is utilized

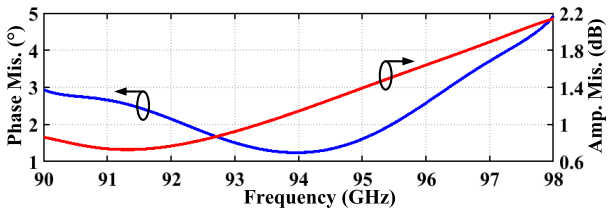


Fig. 10. Simulated phase and amplitude mismatches after compensation.

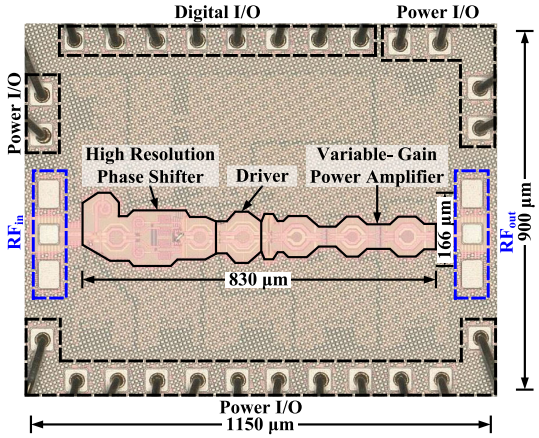


Fig. 11. Chip microphotograph of the *W*-band single channel.

TABLE I
PERFORMANCE SUMMARY OF THE *W*-BAND SINGLE CHANNEL

Parameter	Value	Parameter	Value
Frequency	90–98GHz	Gain Tuning Range	1.5dB
Peak Gain	17.7dB	Phase Variation	3.6°
Input P_{1dB}	–9.7dBm	RMS Gain Error	<1.11dB
Output Power	8.3dBm	RMS Phase Error	<1.79°
Gain Resolution	6-bit	Power Consumption	126mW
Phase Resolution	9-bit	Core size	0.138mm^2

to connect the phase shifter and VGPA. The performance of the single channel is measured by a vector network analyzer with on-chip probing method. Besides, the key measured parameters of the single channel are summarized in Table I. A 1.5-dB gain tuning range and less than 3.6° phase variation are achieved. Besides, after digital gain compensation, the transmitter channel features less than 1.11dB RMS gain error and 1.79° RMS phase error.

D. Wilkinson Power Divider

To construct phased-array systems by the transmitter channels, high-isolation power dividers are required. Due to the high isolation and low loss, three 2-path Wilkinson power dividers, shown in Fig. 12(a), are utilized for four-way power distribution. The 3-D layout of the Wilkinson power divider is shown in Fig. 12(b). The Wilkinson power divider is implemented with 3.3-μm ultra-thick top metal layer (i.e., M7) to reduce the transmission loss. Besides, to minimize the chip size, the coplanar waveguide (CPW) structures are

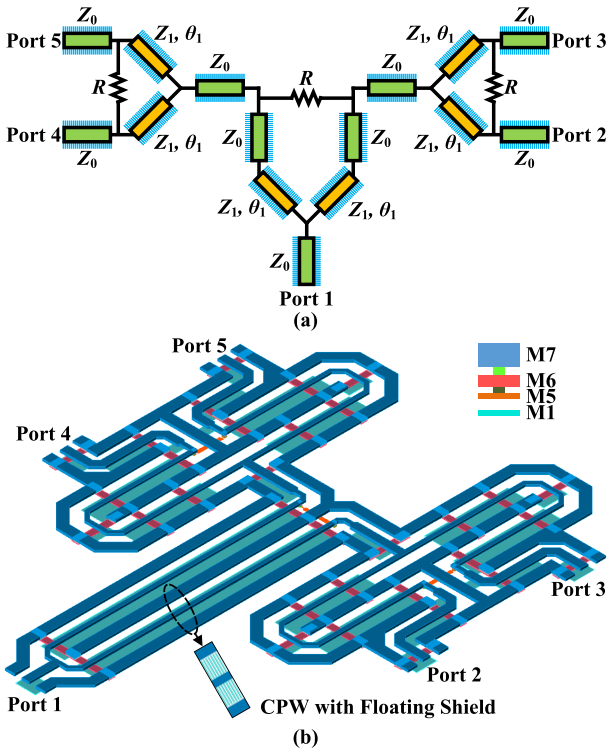


Fig. 12. (a) Circuit model and (b) 3-D layout of the Wilkinson power divider.

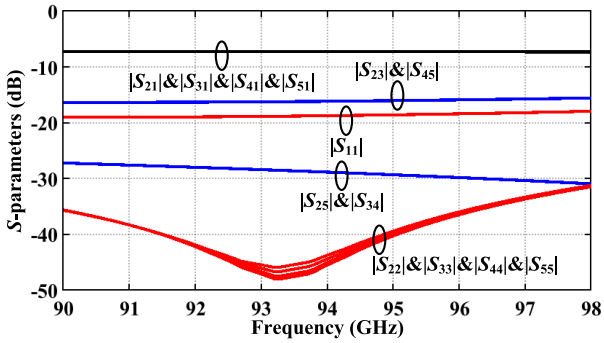


Fig. 13. Simulated *S*-parameters of the Wilkinson power divider.

folded. The width and gap are precisely optimized to design the characteristic impedance Z_1 of 70.7Ω, while the length is optimized for electrical length θ_1 of 90° at 94GHz. Meanwhile, a folded metal resistor with resistance of 100Ω is placed between the two output branches to enhance the isolation performance. A floating shield using the bottom metal (i.e., M1) is introduced with design rule compatible smallest width and gap under the signal path, which would further minimize the loss from the silicon substrate and substrate coupling effects. The 2.5-D electromagnetic (EM) solver environment of ADS momentum is utilized for layout simulation. As shown in Fig. 13, the post-layout insertion loss, excluding 6-dB dividing power, is less than 1.2dB from 90 to 98GHz. Meanwhile, the return losses of five input/output ports and the isolation between the output ports are better than 18dB and 16dB, respectively. The core chip size of the power divider is only 0.33mm^2.

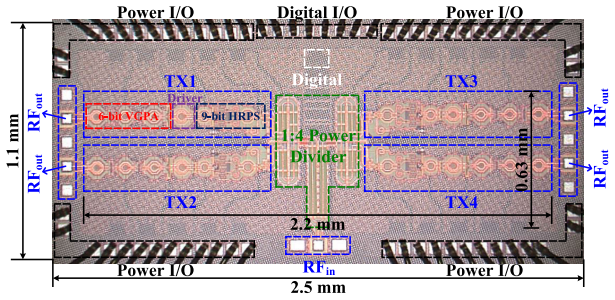


Fig. 14. Chip microphotograph of the *W*-band phased-array transmitter.

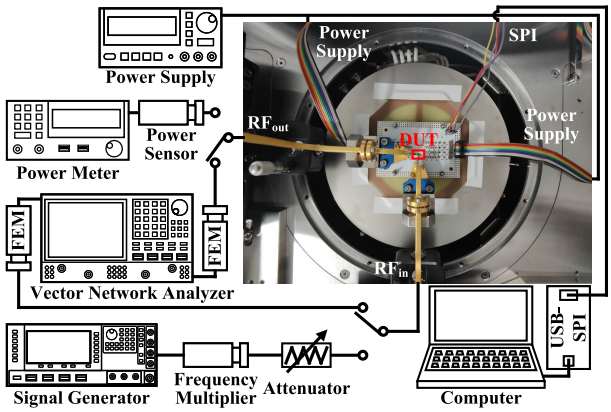


Fig. 15. Measurement setup for single-channel characterizations.

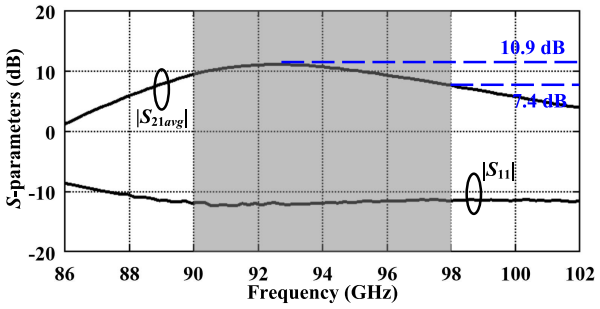


Fig. 16. The average $|S_{21avg}|$ (under 512 phase-states) and typical $|S_{11}|$ of the proposed phased-array transmitter.

IV. Fabrication and Measurement

Based on the mechanisms mentioned above, a 2 × 2 *W*-band phased-array transmitter with high-resolution phase shifter and digital gain-compensated VGPA is implemented and fabricated in a conventional 40-nm CMOS technology. The chip microphotograph is shown in Fig. 14. The total chip size is 2.5 × 1.1 mm^2 including all pads, while the core size is only 2.2 × 0.63 mm^2. Meanwhile, the supply voltage is 1.2V.

A. Single Channel Characterizations

Fig. 15 shows the measurement setup for each single channel. The chip is mounted on a printed circuit board (PCB) without any off-chip matching networks. For the channel test, the input and output signals are fed and measured with two ground-signal-ground (GSG) probes connecting to the input and output pads. The vector network analyzer with 75–110 GHz frequency extension modules (FEMs) after on-chip standard TRL calibration is utilized to measure the small signal *S*-parameters and insertion phases. A signal generator with frequency multiplier and a power meter with power sensor are used to measure the output power, power linearity, and power gain of the proposed phased-array transmitter. The input power is adjusted by a tunable attenuator. All the losses, including waveguide and probe loss, are calibrated out. Note that the phase and gain control codes are generated from an USB-SPI adaptor controlled by a computer.

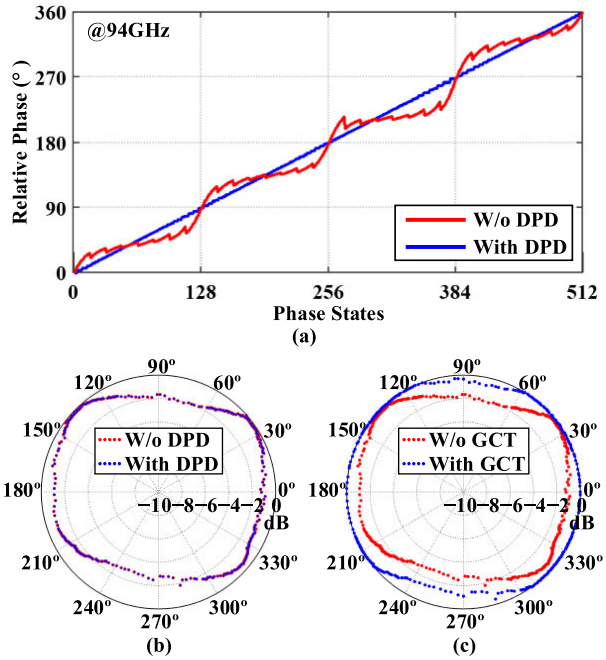


Fig. 17. (a) Relative phase shift before and after DPD at 94GHz. Polar diagrams showing measured phase/power variation at 94GHz (b) with and without DPD and (c) with and without gain-compensation techniques (GCT).

The measured average insertion loss (i.e., $|S_{21avg}|$) under various phase states and typical return loss of the input port (i.e., $|S_{11}|$) are depicted in Fig. 16. The average small-signal gain is from 7.4 to 10.9dB over 90–98GHz, while the return loss is below –10dB. Note that the VGPA is setting under maximum power gain and the power loss of power dividers is included. Fig. 17(a) shows the relative phase shifts versus phase control codes at 94GHz before and after DPD, respectively. It is seen that the phase linearity of relative phase shift is improved by the DPD, which leads to a low phase error. Note that the DPD for phase is performed as follow [49].

1) Measure all output phases after gain compensation under different phase control codes. In the implemented phased-array transmitter, output phases under 512 codes are measured. Here, due to the non-linearity of VGA in phase shifter, n^{th} phase state is not equal to n/512 × 360°, n = 0, 1, 2, …, 511. Therefore, the phase response is non-linear with phase state, as shown in Fig. 17(a, read line).

2) Select the most approximate output phase for each desired phase. For example, the desired phase of 32nd state is 32/512 × 360° = 22.5°. However, the measured phase under

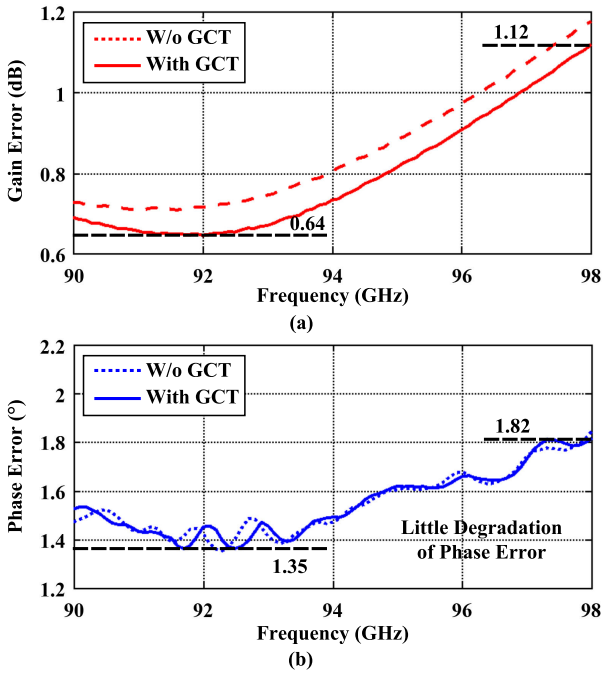


Fig. 18. RMS (a) gain and (b) phase errors with and without gain-compensation technique.

32^{nd} code is 32.2°. There is a large phase error. Then, select the most approximate phase (the measured phase under 10^{th} code is 22.3°) from all 512 measured phases as the updated 32^{nd} phase state. Repeat this procedure for each desired phase. Fig. 17(a, blue line) exhibits the updated phase response versus phase state, which approaches a straight line. A look-up table is used to pre-map the phase code for each desired phase.

The DPD is performed by selecting the most proximate phase compared to the ideal phase shifts. Thus, the phase constellation plot with and without DPD is similar, as show in Fig. 17(b). The DPD has little effectiveness to reduce the gain variation. Then, gain compensation is performed. Fig. 17(c) exhibits the polar diagram of measured phase/power with and without gain-compensation techniques. The power variation is reduced after gain compensation. Besides, the RMS phase and gain errors are calculated by

$$\varphi_{\Delta,RMS} = \sqrt{\frac{1}{2^9-1} \times \sum_{i=1}^{2^9-1} (\varphi_{mea\_i} - \varphi_{ideal\_i})^2}, \quad (9)$$

$$G_{\Delta,RMS} = \sqrt{\frac{1}{2^9} \times \sum_{i=1}^{2^9} (G_{mea\_i} - G_{ideal\_i})^2}, \quad (10)$$

where $\varphi_{mea\_i,ideal\_i}$ and $G_{mea\_i,ideal\_i}$ are the measured/ideal phase and gain of the i^{th} selected state, respectively.

Fig. 18 illustrates the calculated RMS gain and phase errors with/without digital gain-compensation technique. The RMS gain error is 0.64–1.12dB, and RMS phase error is 1.35°–1.82° from 90 to 98GHz after digital gain compensation. Note that an obvious gain error reduction is achieved, while the RMS phase error almost remains unchanged after gain compensation. The reduction of RMS gain error is from 0.81 to

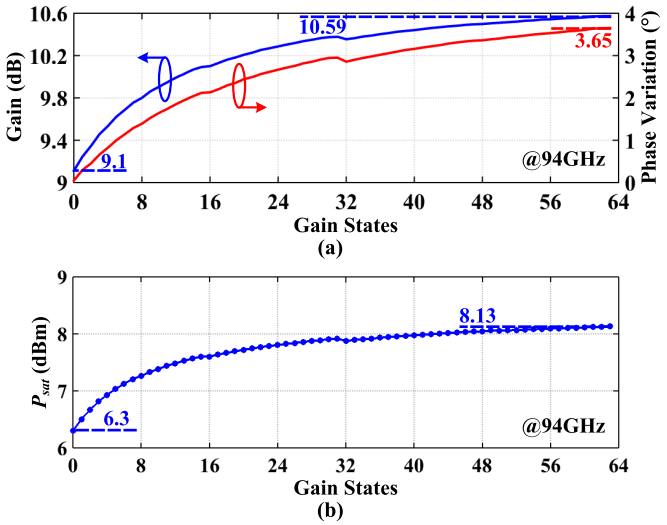


Fig. 19. (a) The gain and phase variations versus 64 gain states at 94GHz. (b) The saturated output power versus 64 gain states at 94GHz.

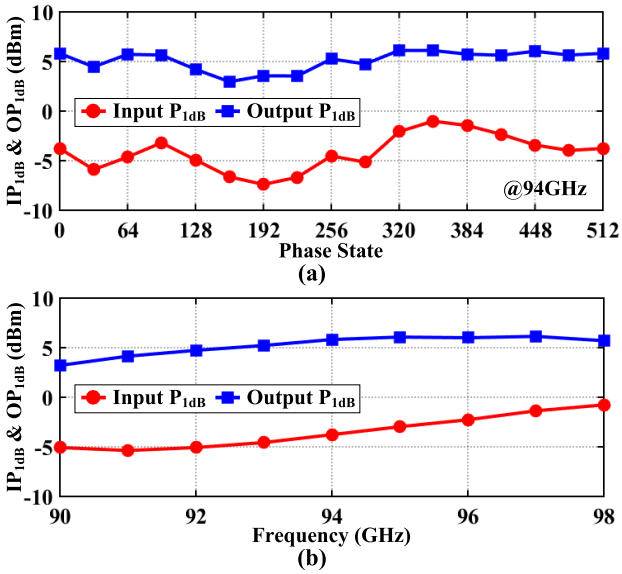


Fig. 20. (a) The input and output 1-dB compression points at 94GHz under different phase states (at maximum power gain). (b) The input and output 1-dB compression points from 90 to 98GHz (at 0° phase state).

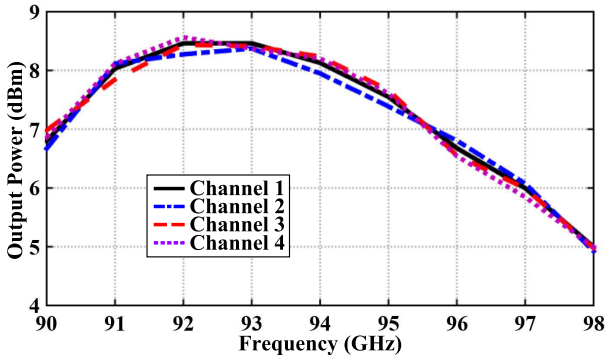


Fig. 21. Output power for four channels.

0.73dB at 94GHz. Note that a better gain error reduction can be achieved by increasing the gain tuning range of the VGPA. In the proposed phased-array transmitter, the RMS

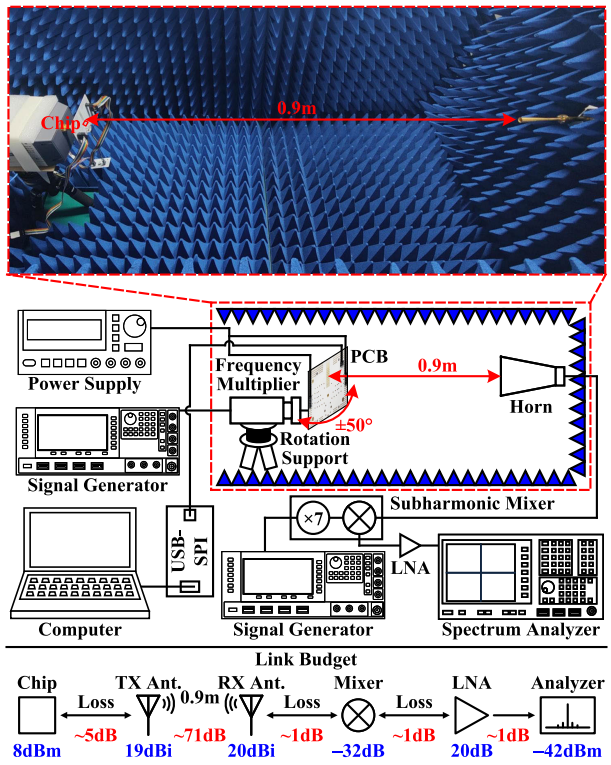


Fig. 22. Measurement setup for beam patterns.

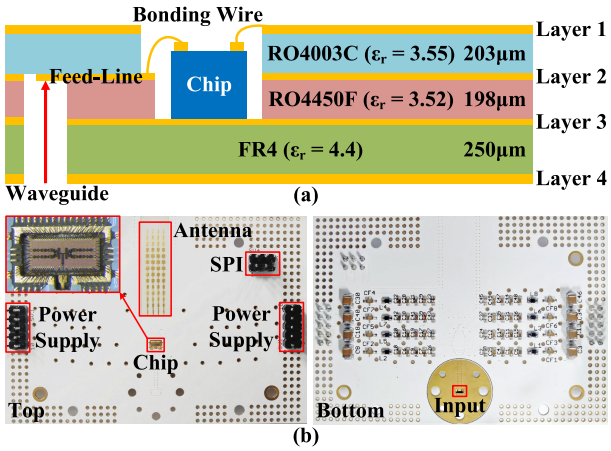


Fig. 23. (a) Low-cost substrate cross sections. (b) Photograph of the fabricated PCB for array characterizations measurement.

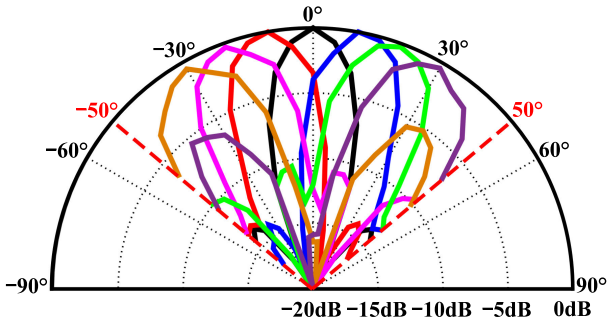


Fig. 24. Measured 4-element radiation results of the normalized beam patterns at 94GHz.

phase error is less than 1.82°, which is smaller than the half of 5.625°. Thus, the effective bit of the phase shifter is regarded as 6 bit, which is sufficient for a *W*-band phased-array system. Fig. 19(a) depicts the gain tuning range and phase variation versus gain control codes. The gain tuning range is 9.1–10.59dB, while the phase variation is less than 3.65° at 94GHz. Meanwhile, the saturated output power versus gain states is shown in Fig. 19(b). The phased-array transmitter exhibits 6.3–8.13dBm saturated output power at 94GHz. Note that the power consumption at the peak gain of each channel is 135mW. The input and output 1-dB compression points at 94GHz are shown in Fig. 20(a). The input and output P_{1dB} are from –7.41 to –1.02dBm and from 2.96 to 6.12dBm, respectively. Note that the VGPA is operated at the maximum power gain. The input and output 1-dB compression points from 90 to 98GHz are shown in Fig. 20(b). The input and output P_{1dB} versus frequency are from –5.37 to –0.77dBm and from 3.21 to 6.14dBm, respectively.

B. Array Characterizations

To show the array characterizations, the output power for four channels are shown in Fig. 21. During the measurement, the four channels are simultaneously turned on. The variation of output power is less than 0.31dBm from 90 to 98GHz, which is caused by layout asymmetry and measurement uncertainties from cable, probe, etc. To further validate the array level performance of the proposed phased-array transmitter, measurements with antennas are carried out under the measurement setup in Fig. 22. A three-layer dielectric substrate (i.e, substrate-1 RO4003C with 0.203mm thickness, substrate-2 RO4450F with 0.198mm thickness, and substrate-3 FR4 with 0.25mm thickness) is used due to its high performance at millimeter wave, as shown in Fig. 23(a). The fabricated PCB for array characterizations measurement is shown in Fig. 23(b). The series-fed microstrip patch antenna arrays are utilized at millimeter wave [51], which features a 13dBi antenna gain at 94GHz. Besides, a *W*-band waveguide-to-microstrip transition is used to transmit the signals into the chip [52]. The detailed information of the waveguide-to-microstrip transition is provided in Appendix. To avoid insertion loss of vias, feed-lines from chip to antennas are placed on the top layer (i.e, layer 1), while DC and control lines are placed on bottom layer (i.e, layer 4). Meanwhile, the top two-layer substrates (i.e, substrate-1 and 2) are removed to place chip for reduced length of bonding-wire.

Under a $\lambda/2$ spacing between two adjacent antennas at 94GHz, the radiated beam patterns are measured. Normalized to the peak power, the measured beam patterns after digital gain compensation at 94GHz are depicted in Fig. 24. Note that only ±50° radiation range with 5° step is obtained, due to the measurement limitation. To further verify the gain-compensation operation on beam patterns, the measured beam patterns with/without gain-compensation technique at 94GHz are normalized and shown in Fig. 25. With gain-compensation technique, there is about 2.8-dB

TABLE II
COMPARISONS WITH THE STATE-OF-THE-ART *W*-BAND PHASED-ARRAY TRANSMITTERS

Ref.	**This Work**	[21]	[24]	[12]	[35]	[25]	[3]	[29]
Architecture	**RF Phase-Shifting with Digital Gain Compensation**	RF Phase-Shifting	RF Phase-Shifting	RF Phase-Shifting	RF Phase-Shifting	RF Phase-Shifting	RF Phase-Shifting	RF Phase-Shifting
Frequency (GHz)	**90∼98**	87.8∼98.9	92∼98	94	88∼96	70∼100	80∼100	93
Element	**4**	4	1	4	2	16	16	4
Average Gain (dB)	**7.4∼10.9**	—	7.5∼12	—	>25	—	—	26
OP_{1dB} (dBm)	**3.21∼6.14**	—	1.5∼2.6	—	0∼3[#]	—	—	11
P_{sat} (dBm)	**6.3∼8.13**	—	6∼7.2	6.4	2.2∼4.7[#]	<8.8[#]	6–8	14
Phase Resolution (bit)	**9(6⋆)**	7	4	5.3⋆	5	5	5	6
Gain Compensation	**Yes**	No	No	No	No	No	No	No
RMS Gain Error (dB)	**0.64∼1.12**	0.73∼0.78[#]	1.1∼1.3[#]	<1.4	0.6∼2.4[#]	—	—	0.45
RMS Phase Error (°)	**1.35∼1.82**	0.9∼2.3[#]	1.5∼6[#]	<9	2∼9[#]	<1	—	0.39
Side-Lobe Suppression Improvement (dB)	**2.8**	—	—	—	—	—	—	—
Data Rate (Gb/s)	**2**	—	—	—	—	30	>10	1.6
Supply Voltage (V)	**1.2**	1.2	2.5	1.8	2.7	1.5/2.5	1.5/2.5	3.3
P_{DC}/Element (mW)	**135**	150	26	71	116	300	275	320
FOM	**184**	—	100	26	8	—	—	1088
Technology	**40-nm CMOS**	65-nm CMOS	130-nm SiGe	130-nm SiGe	120-nm SiGe	180-nm SiGe	180-nm SiGe	130-nm SiGe
Chip/Core Size (mm^2)	**2.75/1.39**	7.56/—*	—/0.77	7.4/—*	—/1.9*	24.5/—*	36.5/—*	4/—

⋆Effective phase resolution; *The whole TRX; [#]Estimated from the figures.

$$\text{FOM} = \frac{P_{sat}\ (\text{mW}) \times \text{Phase Resolution (bit)}}{\text{RMS Gain Error (lin.)} \times \text{RMS Phase Error (°)} \times P_{DC}/\text{Element (W)}}.$$

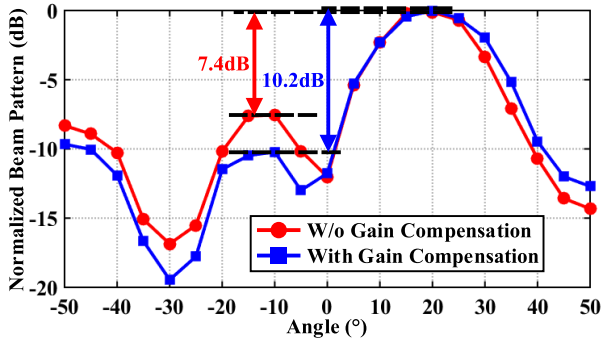


Fig. 25. Normalized beam patterns of the phased-array transmitter with and without digital gain-compensation techniques at 94GHz.

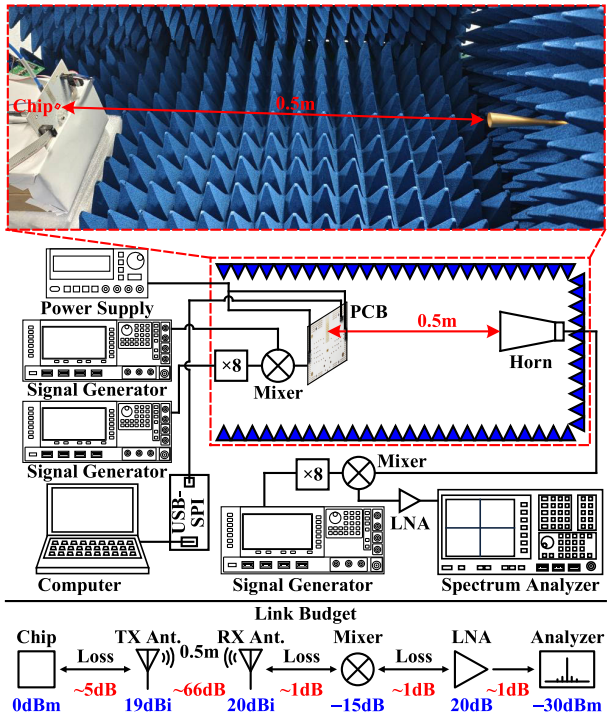


Fig. 26. Measurement setup for over-the-air transmission.

improvement of side-lobe suppression for a typical 20° beam steering.

The measured setup for over-the-air (OTA) transmission is similar as that for beam pattern. As shown in Fig. 26, an up-conversion mixer is placed between the frequency multiplier and PCB. Besides, the modulated IF signals for the mixer is provided by a signal generator. Fig. 27 exhibits the measured constellations of 500MHz 16-QAM with and without gain-compensation techniques at 94GHz. A 0.7-dB EVM improvement is obtained. The measured data rate is 2Gb/s, which may be limited by the following issues. Firstly, the manual wire-bonding process introduces amplitude and phase errors between each elements, which leads to the EVM and SNR degradation. Secondly, the test instruments, e.g., the up-/down-conversion mixers, cannot support high-order modulation. The noise introduced by the mixers leads

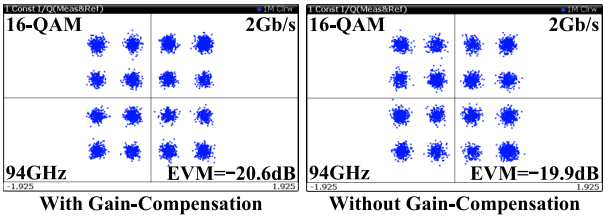


Fig. 27. Measured constellations of 500MHz 16-QAM with and without gain-compensation techniques at 94GHz.

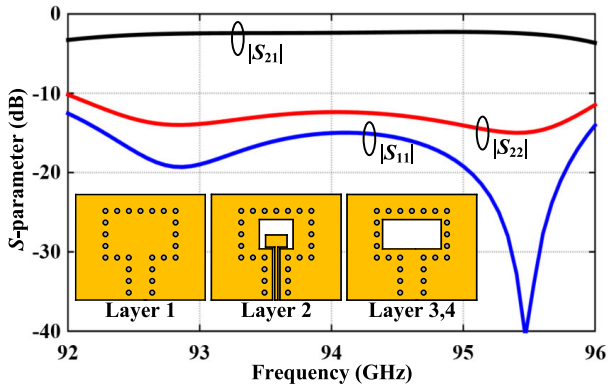


Fig. 28. Layout configuration and simulated *S*-parameters (Port 1: waveguide input, Port 2: microstrip output) of the waveguide-to-microstrip transition.

to a poor EVM performance. Thirdly, the IF frequency of up-/down-conversion mixers is 1GHz, which limits the available signal bandwidth. The data rates might be improved using the robust approaches (e.g., AiP, CoWoS) and mixers with better performance.

Table II summarizes and compares performances with the state-of-the-art millimeter-wave phased-array transmitters. It is notable that the proposed phased-array transmitter features the highest phase resolution of 9-bit. Besides, our phased-array transmitter achieves better RMS phase and gain errors, due to the digital gain-compensation techniques. The chip with concise architecture also occupies a compact size.

V. Conclusion

In this paper, a *W*-band 2 × 2 phased-array transmitter with digital gain-compensation technique is proposed. To obtain a high-resolution phase-shifting characteristic, a digital vector-sum phase shifter based on QAF with compensation network and VGAs with high-bit I-DAC is introduced. Besides, a VGPA is utilized to decrease the gain error of the transmitter channel. With proper gain adjustment, the gain error of the phased-array transmitter could be decreased without sacrificing the phase error from 90 to 98GHz. Based on a conventional 40-nm COMS technology, the proposed phased-array transmitter is implemented with a maximum RMS amplitude error of 1.12dB and maximum RMS phase error of 1.82° from 90 to 98GHz. Meanwhile, the RMS gain error at 94GHz is reduced from 0.81 to 0.73dB by the proposed digital gain-compensation technique. With such good performances, the proposed *W*-band phased-array transmitter is attractive in the wireless communication and radar systems.

Appendix

To measure the phased-array system with antenna arrays at *W*-band, the waveguide-to-microstrip transition is utilized to feed the input signals. The transition is directly implemented in the three-layer dielectric substrate PCB. The configuration of the proposed transition is shown in Fig. 28. Note that the input feed-line is placed on layer 2 to avoid connection between signal and ground. The simulated insertion loss of the waveguide-to-microstrip transition is about 2.4dB at 94 GHz with return loss better than 12dB.

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