Enhanced Jitter Analysis and Minimization for Digital PLLs With Mid-Rise TDCs and its Impact on Output Phase Noise

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***Abstract*— Bang-bang digital phase locked loops (BBDPLL's) use a binary phase detector (BPD) to limit the complexity and consumption of area and power of the time-to-digital converter (TDC), which inevitably introduces more quantization errors (QE's) than a conventional high-resolution TDC. Coarse-resolution TDCs with a few more bits than the BPD can help to mitigate the TDC-induced output jitter and phase noise (PN). This paper derives estimates of the RMS input and output jitters of such digital phase locked loops (DPLL's) with mid-rise TDCs, including BBDPLLs, based on a multi-rate discrete-time model. A comprehensive jitter minimization strategy is provided. The impact of this type of jitter minimization on the enhancement of the output PN performance is studied for the first time. Behavioral simulations verify our analysis. Finally, we conclude with design rules of thumb and a design procedure that helps to mitigate the system jitter and to achieve an output PN spectrum that is dominated by the noises contributed by the reference and digitally controlled oscillator (DCO).**

***Index Terms*— Bang-bang, digital PLL, jitter, phase noise, frequency synthesizer, quantization error, jitter minimization, discrete-time, multi-rate, phase detector, TDC, DCO, PLL.**

I. Introduction

DIGITAL phase locked loops (DPLL's), as shown in Fig. 1, incorporating a multi-bit time-to-digital converter (TDC) as the phase detector (PD) can outperform analog phase locked loops (PLL's) that use a phase-frequency detector followed by a charge pump (CP) [1] in design simplicity and power/area consumption, thanks to the full digitization of the PD and loop filter. Hence, the DPLL has become a popular design option to serve as the frequency synthesizer for wireless communication and clocking purposes. A major breakthrough for advanced DPLLs has been the adoption of a one-bit binary (or bang-bang) phase detector (BPD) to limit the complexity and power/area consumption of the TDC and to achieve a promising trade-off between jitter/noise and power for bang-bang DPLLs (BBDPLL's) at the system level [2].

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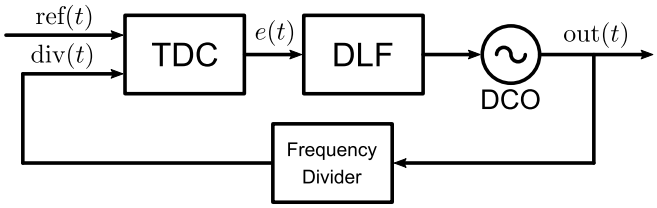


Fig. 1. DPLL system model.

In the locked state, the sources of random time jitter, i.e., reference clock jitter, TDC quantization error (QE), and DCO period jitter, can be referred to the input of the TDC, where they can be approximated by a Gaussian distribution, which can be characterized using the root-mean-square (RMS) value of the absolute jitter [2], [3], [4], [5]. In a BBDPLL, this input jitter interacting with the coarse resolution of the BPD inevitably induces a greater QE compared with multi-bit TDCs. The contribution of the BPD QE can therefore dominate the system's output phase noise (PN) at close-in frequencies (see [3] for example). Recently, Avallone et al. [4] have demonstrated that using a TDC with one or two extra bits and an optimized time resolution in place of the BPD can reduce the power of the TDC QE and hence the input-referred jitter, with only a modest increase in the complexity and power consumption.

This paper first considers DPLLs with coarse-resolution TDCs and provides an enhanced jitter analysis and a minimization strategy that outperform those in [4]. The latter is an extension of [3] that focused only on BBDPLLs. The prediction of the input jitter contributed by the TDC QE (or the jitter arising from the "limit-cycle regime") in those works is derived using the method introduced in [6]. We will show that they lack prediction accuracy, which in turn leads to incorrect jitter minimization. This motivates us to find an alternative method to perform a more accurate input jitter analysis. To date, [7] provides the most accurate jitter analysis framework for a BBDPLL, which originates from the discrete-time method used in [8]. Instead of integrating the power spectrum using a continuous-time system model [3], [4], [5], the analysis framework in [7] derives the RMS input jitter by solving its difference equation using a multi-rate discrete-time BBDPLL model. We extend this analysis to the multi-bit-TDC case and verify the prediction accuracy with behavioral simulations.

Furthermore, the works on jitter minimization, such as [3] and [4], aim to minimize the DPLL's input jitter that is

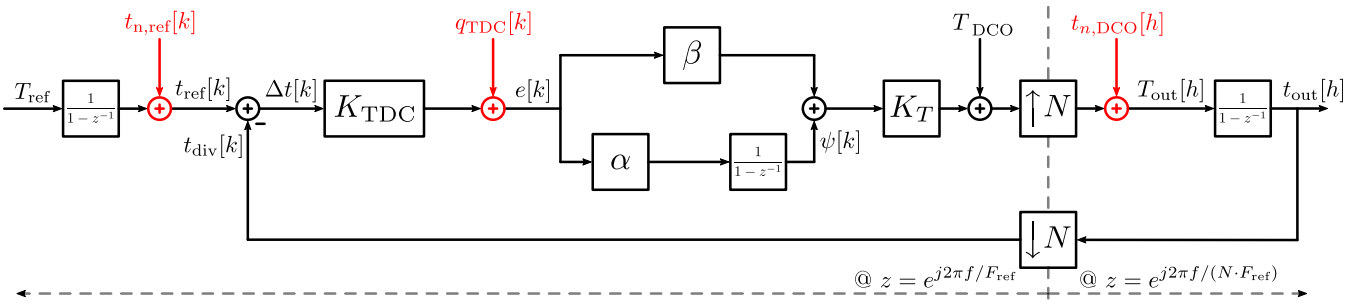


Fig. 2. z-domain model for a multi-rate discrete-time DPLL system, where injections of the jitter/noise sources are marked in red.

assumed to be equivalent to the output jitter as the reference jitter is omitted in their derivations. Our framework allows us to derive the DPLL output jitter as well, based on which we introduce a comprehensive jitter minimization procedure for the output jitter of DPLLs.

Finally, despite the jitter minimization described in [4], its influence on the system's output PN, which is a more relevant performance metric for DPLLs used as frequency synthesizers, is as yet not studied. This paper addresses this impact analytically for the first time. We provide accurate predictions for the output PN components that are verified against behavioral simulation results to confirm our analysis. We conclude that, after jitter minimization, TDCs with more bits can significantly reduce the PN components induced by the TDC and digitally controlled oscillator (DCO). A methodology designed to *mask* the output PN induced by the TDC by that induced by the reference jitter using a minimum number of TDC bits is provided, the result of which is that the system's output PN is dominated by the contributions from the reference and DCO jitters only.

The paper is arranged as follows. Sec. II presents a multi-rate discrete-time model for the DPLL incorporating a multi-bit TDC that is used to derive accurate expressions for the system's input and output jitters. The RMS value measured from the simulated jitter confirms that the accuracy of our prediction outperforms the counterpart predicted by [4]. Sec. III proposes our minimization strategy for the derived jitter by optimizing the loop parameters and the time resolution of the TDC. Sec. IV provides the noise transfer functions (NTF's) that relate the contributions from the inherent jitter/noise sources to the power spectral density (PSD) of the output PN. Inspecting these, we discuss the impact of the proposed jitter minimization strategy on the system's output PN and summarize with a jitter-minimization-oriented design procedure. The methodology is verified by prediction vs. simulation results in Sec. V. Finally, conclusions are drawn in Sec. VI.

II. Jitter Analysis

The multi-rate discrete-time model for a DPLL is shown in Fig. 2, which exploits the timestamps of the rising edges (or positive zero-crossing events) to represent the signals within the loop. In transient analysis, the phase locking ability of the system can be examined by inspecting the variation of the timestamps of the input signals; in the steady state, the jitter and PN performances are associated with the variation of the phases of the signals as well. The timestamping

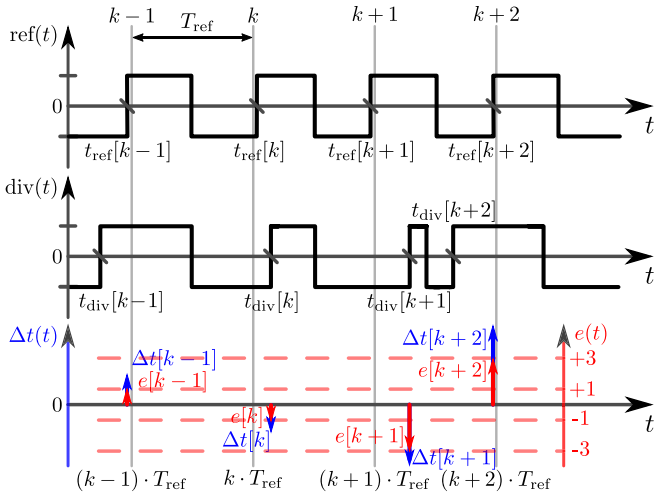


Fig. 3. Example timing diagram illustrating ref(t), div(t), $t_{\mathrm{ref}}[k]$, $t_{\mathrm{div}}[k]$, $\Delta t[k]$, and $e[k]$; where $t_{\mathrm{ref}}[k]$, $t_{\mathrm{div}}[k]$ are the "timestamps" taken for ref(t) and div(t), whose difference $\Delta t[k]$ is recorded for each kth sample, which is quantized by $e[k]$.

notation [7], [9], [10] is explained with Fig. 3, which illustrates the signals associated with the TDC block as an example. As shown at the input of Fig. 1, the TDC takes as input the reference clock and divided output signals, denoted ref(t) and div(t) respectively, that are pulse sequences as functions of t, the "wall time", as shown in Fig. 3. For the kth reference clock cycle, the TDC detects the time difference, $\Delta t[k]$, between the kth rising edges of ref(t)[1] and div(t). We represent their timestamps by $t_{\mathrm{ref}}[k]$ and $t_{\mathrm{div}}[k]$. Thus,

$$\Delta t[k] = t_{\mathrm{ref}}[k] - t_{\mathrm{div}}[k]. \tag{1}$$

Thereafter, the TDC behaves like an N_b-bit analog-to-digital converter that produces a quantized error signal, $e[k]$. Note that, in the discrete-time domain, $\Delta t[k]$ and $e[k]$ record the heights of the kth samples of the impulse sequences $\Delta t(t)$ and $e(t)$.

The system model in Fig. 2 is partitioned into two parts as per the corresponding signal rates. On the input side, the signals operating at the reference frequency ($F_{\mathrm{ref}} = 1/T_{\mathrm{ref}}$) are indexed with k; and on the output side, the signals operating at the output frequency ($F_{\mathrm{out}} = 1/T_{\mathrm{out}}$) are indexed with h. The DPLL as a negative feedback system guarantees that, in the

[1]Notice that the rising edges of ref(t) do not necessarily appear at exact integer multiples of T_{ref}, $t = k \cdot T_{\mathrm{ref}}$, $k \in \mathbb{Z}_{\geq 0}$, where T_{ref} is the nominal period of the reference lock, because of the inevitable reference clock jitter.

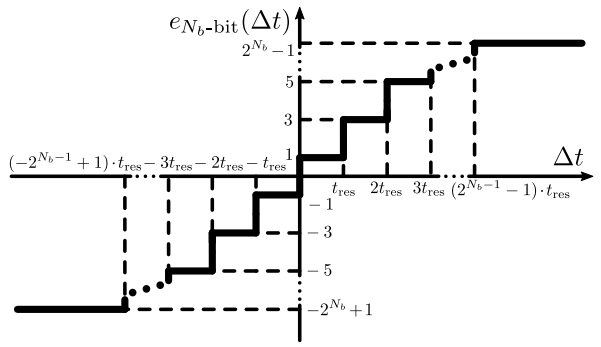


Fig. 4. Transfer characteristic of a generic N_b-bit mid-rise TDC with equidistant quantization thresholds.

locked state, $F_{\text{out}} = N \cdot F_{\text{ref}}$. This paper considers integer-N operation, where N is the integer divide ratio of the feedback frequency divider.

In the slow-rate region, the quantization characteristic of a generic N_b-bit TDC is shown in Fig. 4. To make a fair comparison with a BPD that outputs ± 1s with an output spacing of 2, the N_b-bit TDC's quantization levels are $\pm 1, \pm 3, \pm 5, \ldots, \pm 2^{N_b} - 1$. The quantizer can be modeled as a linear gain element with gain K_{TDC} to whose output is added the QE as follows:

$$e[k] = K_{\text{TDC}} \cdot \Delta t[k] + q_{\text{TDC}}[k]. \tag{2}$$

Adopting a minimum-mean-square-error (MMSE) estimator [11], the linearized gain and the variance of the QE of the TDC, considering the probability distribution of the input jitter being zero-mean Gaussian in the integer-N case, are [10]

$$K_{\text{TDC}} = \sqrt{\frac{2}{\pi}} \cdot \frac{1}{\sigma_{\Delta t}} \cdot \left(1 + 2 \cdot \sum_{k=1}^{2^{(N_b-1)}-1} e^{-\frac{k^2\gamma^2}{2}}\right), \tag{3}$$

in bit/s, and

$$\sigma^2_{Q_{\text{TDC}}} = \left[(2^{N_b}-1)^2 - 8 \cdot \sum_{k=1}^{2^{(N_b-1)}-1} k \cdot \text{erf}\left(\frac{k\cdot\gamma}{\sqrt{2}}\right)\right] - \frac{2}{\pi} \cdot \left(1 + 2 \cdot \sum_{k=1}^{2^{(N_b-1)}-1} e^{-\frac{k^2\gamma^2}{2}}\right)^2, \tag{4}$$

in bit^2, where $\sigma_{\Delta t}$ is the standard deviation (or RMS value) of the input jitter; and

$$\text{erf}\left(\frac{x}{\sqrt{2}\sigma_{\Delta t}}\right) = 2 \cdot F_{\Delta t}(x) - 1 = \sqrt{\frac{2}{\pi}} \cdot \frac{1}{\sigma_{\Delta t}} \int_0^x e^{-\frac{a^2}{2\sigma^2_{\Delta t}}}\, \text{d}a,$$

where $F_{\Delta t}(x)$ is the cumulative distribution function of the random variable Δt that represents the ensemble of the input jitter. To simplify the analysis, we normalize the TDC time resolution to the RMS input jitter as in [4]

$$\gamma = \frac{t_{\text{res}}}{\sigma_{\Delta t}}. \tag{5}$$

Note that, in principle, when γ is large, i.e., $t_{\text{res}} \gg \sigma_{\Delta t}$, most of the input jitter will be accommodated by the two middlemost quantization levels; in this case, the outputs will be mostly ± 1s, which approximates to the behavior of a BPD. In the limit, as $\gamma \to \infty$ and $N_b = 1$ in (3) and (4), the effective gain and power of the QE of the BPD can be calculated as

$$K_{\text{BPD}} = \sqrt{\frac{2}{\pi}} \cdot \frac{1}{\sigma_{\Delta t}} \text{ and } \sigma^2_{Q_{\text{BPD}}} = \frac{\pi - 2}{\pi},$$

which are the same expressions that have been derived in the literature analyzing BBDPLLs [5], [7].

After the TDC detection, $e[k]$ is lowpass filtered by the digital loop filter (DLF), which is a proportional–integral (PI) controller that has a proportional path with the coefficient, β, and an integral path with the coefficient, α. The filtered signal drives the DCO, which is modeled as an upsampler by N that operates with a center frequency, $F_{\text{DCO}} = 1/T_{\text{DCO}}$, and period gain, K_T, to produce the output signal, $t_{\text{out}}[h]$, at the high rate. In the feedback path, the divider downsamples the output by N to produce the divided signal, $t_{\text{div}}[k]$.

In the remainder of this section, we will perform jitter analysis based on this multi-rate discrete-time system model. In Sec. II-B, the RMS input jitter, $\sigma_{\Delta t}$, of the DPLL with a multi-bit TDC will be derived as an explicit function of the parameter γ in (5). Notice that, at first glance, the relationship between γ and $\sigma_{\Delta t}$ might seem recursive in the sense that the normalized TDC resolution (γ) is set with respect to a known RMS jitter ($\sigma_{\Delta t}$), yet setting a particular value for γ varies the linearized gain and power of the QE of the TDC which, in turn, can change the value of $\sigma_{\Delta t}$. However, we will show in Sec. II-C that, starting with a specified γ value, together with some known loop parameters, the corresponding $\sigma_{\Delta t}$ value can be predicted (calculated). Then, substituting γ and $\sigma_{\Delta t}$ into (5), the absolute TDC resolution (t_{res}) can be set; using this in the behavioral simulation, the DPLL will achieve a simulated system jitter that precisely matches the prediction.

Furthermore, we will prove in Sec. III that, to minimize the overall system jitter, there exists an optimal value of γ for each value of $N_b = 1, 2, 3, \ldots$. The optimal γ values will be derived and tabulated in Sec. III-B. Finally, the jitter-minimization-oriented design procedure which also takes into account the optimization of the PN performance, will be summarized in Sec. IV-E.

A. Classification of Oscillator Jitters in DPLL Analysis

Apart from the TDC QE discussed above, there are two inevitable jitter/noise sources that contribute to the jitter and PN performance of the DPLL, namely, the reference clock jitter ($t_{\text{n,ref}}[k]$) and the DCO random jitter ($t_{\text{n,DCO}}[h]$). Their injection points are marked in red in Fig. 2. In DPLL jitter analysis, these two intrinsic oscillator jitters can be classified by two canonical types.

1) Reference Synchronous Jitter: DPLL frequency synthesizers typically uses a crystal oscillator to provide the reference frequency, which displays a flat PN profile beyond an offset of about one kilohertz [12], [13], [14]. The white PN approximation conforms to the characteristic of a clock source that generates *synchronous* jitter that is directly affiliated with each timestamp of the transition events and does not move the center frequency of the clock [15], [16]. The timestamp of the kth cycle of the reference clock can be expressed as

$$t_{\text{ref}}[k] = k \cdot T_{\text{ref}} + t_{n,\text{ref}}[k], \tag{6}$$

whose jitter term, $t_{n,\mathrm{ref}}[k]$, is synchronous with the current cycle with no memory of the previous jitter samples. The variance of the jitter is expressed as $\sigma^2_{t_{n,\mathrm{ref}}}$. From (6), the kth period of the reference can be obtained as

$$T_{\mathrm{ref}}[k] = t_{\mathrm{ref}}[k] - t_{\mathrm{ref}}[k-1] = T_{\mathrm{ref}} + t_{n,\mathrm{ref}}[k] - t_{n,\mathrm{ref}}[k-1], \tag{7}$$

which is implicitly modeled in [7].

2) DCO Accumulating Jitter: a free-running DCO generates an output transition referring to its previous transition with a jitter representing the uncertainty in the time difference between two consecutive transition events. Thus, the time-stamp of a particular transition contains an accumulation of all the jitters in previous cycles, in which case the jitter is termed *accumulating* [16], random-walk [3], [4], [7], or period [17] jitter. For the DCO with accumulating jitter, the clock period of the hth cycle is represented as

$$T_{\mathrm{DCO}}[h] = T_{\mathrm{DCO}} + t_{n,\mathrm{DCO}}[h]. \tag{8}$$

The variance of the period jitter is expressed as $\sigma^2_{t_{n,\mathrm{DCO}}}$. Based on (8), the timestamp of the hth cycle is

$$t_{\mathrm{DCO}}[h] = \sum_{i=1}^{h} T_{\mathrm{DCO}}[h] = h \cdot T_{\mathrm{DCO}} + \sum_{i=1}^{h} t_{n,\mathrm{DCO}}[h].$$

Using the above models, we provide an analysis of the time jitter referred to the system's input and output.

B. Input Jitter

Following the model in Fig. 2, a recurrent equation for the timestamp of the divided signal can be expressed as

$$t_{\mathrm{div}}[k+1] = t_{\mathrm{div}}[k] + \sum_{h=N\cdot k+1}^{N\cdot(k+1)} \Bigg\{ \underbrace{K_T\left(\beta \cdot e[k] + \psi[k]\right)}_{\text{control via DLF}} + \underbrace{T_{\mathrm{DCO}} + t_{n,\mathrm{DCO}}[h]}_{\text{DCO period with jitter in (8)}} \Bigg\}, \tag{9}$$

where $\psi[k] = \psi[k-1] + \alpha \cdot e[k]$ is the output of the integral path of the DLF. As the DPLL's stability requires that $\alpha \ll \beta$ [9], [18], $\psi[k]$ in (9) can be neglected without sacrificing the accuracy of the jitter transfer analysis.

Substituting (1) and (2) into (9), one can derive the difference equation of the input time difference (jitter) shown in (10), bottom of the page.

In integer-N mode, the divide ratio N is a constant integer. Therefore, the sum operator in (10) can be replaced by multiplication by N for the terms in the sum that are independent of the index h. Substituting the definition of synchronous reference jitter in (7) and recalling that $T_{\mathrm{ref}} = N \cdot T_{\mathrm{DCO}}$ in the locked state, (10) can be simplified and rearranged as

$$\Delta t[k+1] = (1-X)\cdot\Delta t[k] + \left(t_{n,\mathrm{ref}}[k+1] - t_{n,\mathrm{ref}}[k]\right) - \left\{ \frac{X}{K_{\mathrm{TDC}}} \cdot q_{\mathrm{TDC}}[k] + \sum_{h=N\cdot k+1}^{N\cdot(k+1)} t_{n,\mathrm{DCO}}[h] \right\}, \tag{11}$$

where we use the shorthand notation,

$$X = K_{\mathrm{TDC}} \cdot \beta \cdot K_T \cdot N. \tag{12}$$

Solving the difference equation (11) yields (13), shown at the bottom of the next page. For a stable loop, $0 < X < 2$ is always satisfied [7]. Therefore, in the steady state, where $k \to \infty$, the first term on the right-hand side vanishes, which reflects the ability of a DPLL to close an arbitrary initial phase/time gap at the input.

The noise sources are assumed to be zero-mean, ergodic, and uncorrelated from each other [7], [19]. In particular, the uncorrelatedness between the predicted TDC QE and the other sources is guaranteed by the MMSE estimation [11]. Ergodicity allows one to take (time-domain) variances on both sides of (13), whilst noticing that the last term on the right-hand side represents a sum of N independent DCO period jitters, to calculate the (ensemble) input jitter power as a sum of the powers of the noise/jitter sources, which is

$$\sigma^2_{\Delta t} = \sigma^2_{t_{n,\mathrm{ref}}} + \sum_{i=0}^{k} (1-X)^{2(k-i)} \left\{ X^2 \sigma^2_{t_{n,\mathrm{ref}}} + \frac{X^2}{K^2_{\mathrm{TDC}}} \cdot \sigma^2_{Q_{\mathrm{TDC}}} + N \cdot \sigma^2_{t_{n,\mathrm{DCO}}} \right\}. \tag{14}$$

Approaching the steady state, $0 < X < 2$ guarantees the convergence of the geometric series in (14), hence $\lim_{k\to\infty} \sum_{i=0}^{k} (1-X)^{2(k-i)} = \frac{1}{X(2-X)}$ which, when substituted into (14), yields

$$\sigma^2_{\Delta t} = \frac{2}{2-X} \cdot \sigma^2_{t_{n,\mathrm{ref}}} + \frac{X}{2-X} \cdot \frac{\sigma^2_{Q_{\mathrm{TDC}}}}{K^2_{\mathrm{TDC}}} + \frac{N}{X(2-X)} \cdot \sigma^2_{t_{n,\mathrm{DCO}}}. \tag{15}$$

To simplify the analysis, let

$$Y = \sqrt{\frac{2}{\pi}} \cdot \left(1 + 2 \cdot \sum_{k=1}^{2^{(N_b-1)}-1} e^{-\frac{k^2\gamma^2}{2}} \right),$$

and

$$Z = (2^{N_b}-1)^2 - 8 \cdot \sum_{k=1}^{2^{(N_b-1)}-1} k \cdot \mathrm{erf}\left(\frac{k\cdot\gamma}{\sqrt{2}} \right).$$

$$\Delta t[k+1] = \Delta t[k] + (t_{\mathrm{ref}}[k+1] - t_{\mathrm{ref}}[k]) - \sum_{h=N\cdot k+1}^{N\cdot(k+1)} \left\{ K_{\mathrm{TDC}} \cdot \beta \cdot K_T \cdot \Delta t[k] + \beta \cdot K_T \cdot q_{\mathrm{TDC}}[k] + T_{\mathrm{DCO}} + t_{n,\mathrm{DCO}}[h] \right\}. \tag{10}$$

Equations (3) and (4) then become

$$K_{\text{TDC}} = \frac{Y}{\sigma_{\Delta t}}, \tag{16}$$

and

$$\sigma^2_{Q_{\text{TDC}}} = Z - Y^2, \tag{17}$$

which simplify the variance of the input-referred TDC QE in (15) as

$$\sigma^2_{Q_{\text{in,TDC}}} \equiv \frac{\sigma^2_{Q_{\text{TDC}}}}{K^2_{\text{TDC}}} = \left(\frac{Z}{Y^2} - 1\right) \cdot \sigma^2_{\Delta t}. \tag{18}$$

Note that Y has a dimension of bit, and that the Z has a dimension of bit^2.

Substituting (16) into (12), together with (18) into (15), yields a quadratic equation for the RMS input jitter as

$$\sigma^2_{\Delta t} - \left(\frac{N\beta K_T \cdot Z}{2 \cdot Y} + \frac{\sigma^2_{t_{n,\text{DCO}}}}{2 \cdot \beta K_T \cdot Y}\right) \cdot \sigma_{\Delta t} - \sigma^2_{t_{n,\text{ref}}} = 0,$$

the positive root of which can be represented as

$$\sigma_{\Delta t} = \frac{\eta}{2} + \sqrt{\left(\frac{\eta}{2}\right)^2 + \sigma^2_{t_{n,\text{ref}}}}, \tag{19}$$

where

$$\eta = \underbrace{\frac{N\beta K_T \cdot Z}{2 \cdot Y}}_{\text{From TDC QE}} + \underbrace{\frac{\sigma^2_{t_{n,\text{DCO}}}}{2 \cdot \beta K_T \cdot Y}}_{\text{From DCO jitter}}. \tag{20}$$

Note that, in the special case of a BPD, $N_b = 1$ and $\gamma = \infty$, giving $Y = \sqrt{\frac{2}{\pi}}$ and $Z = 1$, which, when substituted into (20), yield

$$\eta_{\text{BPD}} = \sqrt{\frac{\pi}{2}} \cdot \left(\frac{N\beta K_T}{2} + \frac{\sigma^2_{t_{n,\text{DCO}}}}{2 \cdot \beta K_T}\right). \tag{21}$$

The prediction for η in (20) as a general case for DPLLs using generic N_b-bit TDCs is a new result. The special case, η_{BPD} in (21), corresponds to the most accurate prediction to date in [7], which focuses exclusively on the analysis of BBDPLLs.

C. Comparison of η Predicted in This Work Vs. That in [4]

As introduced in Sec. I, the input jitter analysis for DPLLs with multi-bit TDCs conducted in [4] omits the contribution from the reference jitter. Hence, its derived input jitter is limited to the prediction of the value of η, which contains only the contributions from the TDC QE and DCO jitter, or, using the language of [4], the jitters derived in the "limit-cycle" and "random-noise" regimes. Nevertheless, we can compare the accuracy of its prediction of η against that of ours. Using the terminology of this work, [4] predicts that

$$\eta_{\,[4]} = \frac{N\beta K_T}{\sqrt{3}} \cdot \left[(2^{N_b} - 1) - 2 \cdot \sum_{k=1}^{2^{(N_b-1)}-1} \text{erf}\left(\frac{k \cdot \gamma}{\sqrt{2}}\right)\right] + \frac{\sigma^2_{t_{n,\text{DCO}}}}{2 \cdot \beta K_T \cdot Y}, \tag{22}$$

whose prediction of the contribution from the DCO jitter (the second term) is the same as its counterpart in (20), yet its prediction of the TDC QE's contribution is fundamentally different from (20).

To compare and contrast the predictions in this work and that in [4], we perform closed-loop behavioral simulations for DPLLs parameterized with the loop and noise settings used in [7, Sec. III], which are tabulated in Table I. For a fair comparison with [4], what is different from Table I is that the reference source is assumed to be free of jitter, and hence the PSD of the reference jitter $S_{\phi_{\text{ref}}} = -\infty$ and $\sigma_{t_{n,\text{ref}}} = 0$. We simulate the cases where BPD, 2-bit, and 3-bit TDCs are used as the PD for the DPLLs. For the latter two cases, $\gamma = 1.08$ and 0.66 are chosen, as suggested by [4], to mitigate the input jitter. Substituting the γ value, (20) and (22) predict the values of η for the two methods, which is equivalent to $\sigma_{\Delta t}$ without reference jitter. The values of γ and $\sigma_{\Delta t}$ are substituted into (5) to select the absolute TDC resolution used in the simulations.

We measure the standard deviation of the sequence of the TDC input samples. The comparisons tabulated in Table II show that, for all three TDC cases, the input jitters predicted by this work using (20) outperform their counterparts by [4] in the sense that the predictions using the former match the simulated results much better. The reason that the prediction in the latter lacks accuracy is that the jitter component contributed from the TDC QE is underestimated in (22) of [4]. To verify further the accuracy of our prediction using (19), we extend the analysis to the cases where (i) the DCO is jitter-free, hence $S_{\phi_{\text{DCO}}} = -\infty$ and $\sigma_{t_{n,\text{DCO}}} = 0$, and (ii) the reference and DCO both exhibit jitter as parameterized in Table I. The results

TABLE I
DPLL LOOP AND NOISE PARAMETERIZATION

Parameter	Value
F_{ref}	100 MHz
N	24
F_{DCO}	$N \cdot F_{\text{ref}}$
β	70
α	$2^{-8} \cdot \beta$
K_T	0.145 fs/bit
$S_{\phi_{\text{ref}}}$ [a]	-155 dBc/Hz ($\sigma_{t_{n,\text{ref}}} = 283$ fs)
$S_{\phi_{\text{DCO}}}(1\text{ MHz})$ [b]	-108 dBc/Hz ($\sigma_{t_{n,\text{DCO}}} = 33.9$ fs)

[a, b] The relationships between $S_{\phi_{\text{ref}}}$ & $\sigma_{t_{n,\text{ref}}}$ and $S_{\phi_{\text{DCO}}}(\Delta f)$ & $\sigma_{t_{n,\text{DCO}}}$ are derived in (36) and (38).

$$\Delta t[k+1] = (1-X)^{k+1} \cdot \Delta t[0] + t_{n,\text{ref}}[k+1] - \sum_{i=0}^{k} (1-X)^{(k-i)} \left\{ X \cdot t_{n,\text{ref}}[i] + \frac{X}{K_{\text{TDC}}} \cdot q_{\text{TDC}}[i] + \sum_{h=Ni+1}^{N(i+1)} t_{n,\text{DCO}}[h] \right\}. \tag{13}$$

TABLE II

COMPARISON OF η PREDICTED BY [4] VS. THIS WORK AND MEASURED FROM SIMULATIONS ASSUMING A JITTER-FREE REFERENCE

TDC	[4] by (22)	This work by (20)	Simulation
BPD	211 fs	223 fs	222 fs
2-bit	252 fs	267 fs	267 fs
3-bit	368 fs	396 fs	399 fs

TABLE III

COMPARISON OF PREDICTED AND SIMULATED $\sigma_{\Delta t}$

TDC	No DCO jitter		Reference & DCO jitters	
	Prediction	Simulation	Prediction	Simulation
BPD	369 fs	369 fs	416 fs	416 fs
2-bit	423 fs	423 fs	446 fs	447 fs
3-bit	528 fs	529 fs	543 fs	544 fs

tabulated in Table III verify our prediction accuracy for these cases.[2]

Accurate prediction of RMS input jitter is crucial in terms of ascribing the correct linearized gain and power of the QE to the TDC. In particular, note that (3) and (4) include $\sigma_{\Delta t}$. These will be used directly for linearized analysis of DPLLs at the system level. As simulations confirm the accuracy of our prediction of the input jitter in all the cases of reference and DCO jitter combinations and with all the tested types of TDCs, the output jitter analysis and jitter minimization in the following sections will be performed based on the expressions (19) and (20).

D. Output Jitter

The RMS *output* jitter of the DPLL that functions as a frequency synthesizer is typically of more interest than the DPLL's *input* one. In general, the output jitter is the one that ought to be minimized. References [3] and [4] ignore the reference jitter in their jitter derivation. In particular, the output jitter is claimed to be quantitatively equivalent to the TDC-input jitter. However, as reference jitter is indeed inevitable, the relationship between the system's input and output jitters, both of which are statistically dependent on the reference jitter, may not be that straightforward. In this subsection, we perform the analysis of the output jitter to reveal its relationship with the input one.

We begin by noticing that the variance of the jitter of the divided signal ($t_{\text{div}}[k]$) is the same as that of the output signal ($t_{\text{out}}[h]$). By inspecting Fig. 2, assuming the divider *per se* does not add jitter to the transitions, the former sequence is just a decimated and compressed version of the latter that is uniformly sampled for every N elements. Hence, the RMS jitter of $t_{\text{div}}[k]$ is equivalent to the RMS output jitter. We define the cycle-wise jitter associated with the $t_{\text{div}}[k]$ sequence as the deviation of the kth sample from the expected value as

$$t_{\text{n,div}}[k] = t_{\text{div}}[k] - \mathbb{E}\left[t_{\text{div}}[k]\right] = t_{\text{div}}[k] - k \cdot T_{\text{ref}}, \tag{23}$$

[2]Readers should not be confused by the increase of RMS input jitter in Tables II and III, when extra numbers of bits are used in the TDC. This is because, in these comparisons, the loop parameterization is not yet optimized corresponding to the TDC change. The loop optimization will be performed in the next section.

as the DPLL locks the divided frequency to the reference frequency.

Substituting (1), (6), and (23) into (11), after some manipulations, yields a difference equation of $t_{\text{n,div}}[k]$ as

$$t_{\text{n,div}}[k+1] = (1-X)\cdot t_{\text{n,div}}[k] + X \cdot t_{n,\text{ref}}[k] + \frac{X}{K_{\text{TDC}}}\cdot q_{\text{TDC}}[k] + \sum_{h=N\cdot k+1}^{N\cdot(k+1)} t_{n,\text{DCO}}[h],$$

solving which and taking variances of both sides following the procedure detailed in Sec. II-B, the variance of the jitter of the divided signal is given by

$$\sigma^2_{t_{\text{n,div}}} = \frac{X}{2-X}\cdot\sigma^2_{t_{n,\text{ref}}} + \frac{X}{2-X}\cdot\frac{\sigma^2_{Q_{\text{TDC}}}}{K^2_{\text{TDC}}} + \frac{N}{X(2-X)}\cdot\sigma^2_{t_{n,\text{DCO}}}. \tag{24}$$

Substituting (24) into (15) yields

$$\sigma^2_{\Delta t} = \sigma^2_{t_{\text{n,div}}} + \sigma^2_{t_{n,\text{ref}}}. \tag{25}$$

Although the random varying divided signal (represented by the first term on the right-hand side) is dependent on the reference jitter (represented by the second term on the right-hand side) as it contains the latter transferred to its position, these two variables on the right-hand side are statistically uncorrelated when referred to the input of the DPLL as the variance of the sum of these variables equals the sum of the variances of the variables. The RMS output jitter can then be expressed as

$$\sigma_{t_{\text{n,out}}} = \sqrt{\sigma^2_{\Delta t} - \sigma^2_{t_{n,\text{ref}}}} = \sqrt{\frac{\eta^2}{2} + \eta\sqrt{\left(\frac{\eta}{2}\right)^2 + \sigma^2_{t_{n,\text{ref}}}}}. \tag{26}$$

Hereinafter, we will perform the jitter minimization directly on $\sigma_{t_{\text{n,out}}}$.

III. JITTER MINIMIZATION

Avallone et al. [4] proposed two input jitter minimization schemes that scale the normalized TDC resolution, γ, to find the best resolution that minimizes the target quantities. The first of these is a "local optimization" that aims to minimize the power of the TDC QE, whilst the other is a "global optimization" that aims to minimize the RMS system jitter directly. This section provides an enhanced jitter minimization strategy for the DPLL based on the jitter expressions derived in the previous section. We will demonstrate that the difference that existed between the two minimization schemes in [4] is due to its flawed prediction of the input jitter that is discussed in Sec. II-C. In fact, the two schemes in [4] are substantially identical, in the sense that, if the correct expressions are used, the quantities to be minimized by them are the same.

A. Loop Dynamic Optimization

To minimize $\sigma_{t_{\text{n,out}}}$ represented in (26), we first determine the optimal loop parameterization, namely, the optimal setting of the DLF proportional gain β. A necessary condition for the optimal value, $\hat{\beta}$, is when it makes the first-order partial derivative of the $\sigma_{t_{\text{n,out}}}$ with respect to β equal to zero, that is

$$\frac{\partial\sigma_{t_{\text{n,out}}}}{\partial\beta} = 0. \tag{27}$$

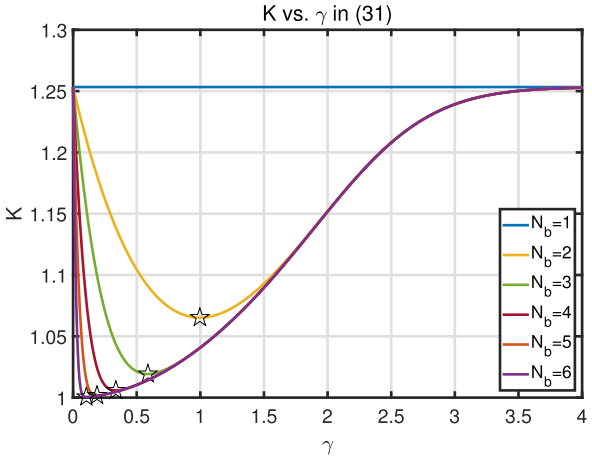


Fig. 5. Calculated K with swept γ by (31) for $N_b = 1, 2, \ldots, 6$. Stars represent the optimal value of γ, denoted $\hat{\gamma}$, and its corresponding $\hat{K}$ for each case that are tabulated in Table IV.

Substituting (20) and (26) into (27) yields

$$\left[\eta + \sqrt{\left(\frac{\eta}{2}\right)^2 + \sigma_{t_{n,\text{ref}}}^2} + \frac{\eta^2}{4}\left(\left(\frac{\eta}{2}\right)^2 + \sigma_{t_{n,\text{ref}}}^2\right)^{-\frac{1}{2}}\right] \cdot \left(\frac{\eta^2}{2} + \eta\sqrt{\left(\frac{\eta}{2}\right)^2 + \sigma_{t_{n,\text{ref}}}^2}\right)^{-\frac{1}{2}} \cdot \frac{\partial \eta}{\partial \beta} = 0.$$

As all the preceding terms are positive, the only real-valued solution can be found when

$$\frac{\partial \eta}{\partial \beta} = 0, \tag{28}$$

with which the second-order derivative $\frac{\partial^2 \sigma_{t_{\text{n,out}}}}{\partial \beta^2}$ can be proven to be positive. Altogether, these yield the necessary and sufficient condition for $\hat{\beta}$ that makes $\frac{\partial \eta}{\partial \beta} = 0$ to minimize the output jitter. Similarly, it is trivial to show that the value $\hat{\beta}$ also minimizes the input jitter expressed in (19).

Substituting (20) to solve (28), the optimal loop setting can be found as

$$\hat{\beta} = \frac{\sigma_{t_{n,\text{DCO}}}}{K_T\sqrt{N \cdot Z}}. \tag{29}$$

This value, substituted into (20), in fact equalizes the amounts of jitter contributed by the TDC QE and the DCO period jitter. This is the sufficient condition for the stochastic resonance operation that randomizes limit-cycle behavior of the TDC in locked state [19], which also yields a spur-free output PN spectrum, as will be shown in Sec. V. The optimal value $\hat{\eta}$ is thus expressed as

$$\hat{\eta} = \sqrt{\frac{Z}{Y^2}} \cdot \sqrt{N} \cdot \sigma_{t_{n,\text{DCO}}}. \tag{30}$$

B. TDC Time Resolution Optimization

To reduce the input and output jitters further, one can vary the time resolution, γ, of the N_b-bit TDC so that $\hat{\eta}$ in (30), that is readily optimized with respect to the loop dynamics, will be ultimately minimized. Therefore, with $\sqrt{N}$ and $\sigma_{t_{n,\text{DCO}}}$ fixed, the expression $\sqrt{Z/Y^2}$ needs to be minimized, to represent which we assign a dimensionless variable K as

$$K = \sqrt{\frac{Z}{Y^2}} \tag{31a}$$

$$= \sqrt{\frac{\pi}{2}} \cdot \sqrt{\frac{(2^{N_b}-1)^2 - 8\sum_{k=1}^{2^{(N_b-1)}-1} k \cdot \text{erf}\left(\frac{k\gamma}{\sqrt{2}}\right)}{\left(1 + 2 \cdot \sum_{k=1}^{2^{(N_b-1)}-1} e^{-\frac{k^2\gamma^2}{2}}\right)^2}}. \tag{31b}$$

The multiplicand following $\sqrt{\frac{\pi}{2}}$ in (31b) consists of complicated functions that cannot be easily differentiated with respect to γ to find the minima explicitly. Therefore, we use numerical methods to find the optimal $\hat{\gamma}$ values for TDCs with different numbers of bits, N_b.

It is worth noticing that, for TDCs with different numbers of bits $N_b = 1, 2, 3, \ldots$, calculating K in (31) as a function of γ with extreme γ settings yields the maximum value as

$$K_{\max} = \lim_{\gamma \to 0} K(\gamma) = \lim_{\gamma \to \infty} K(\gamma) = \sqrt{\frac{\pi}{2}}.$$

Meanwhile, notice that using a large number of bits for the TDC can reduce the TDC QE referred to its input, which theoretically reduces the latter to zero as the number of bits approaches infinity. This implies that, expressing K as a function of N_b and the corresponding optimal $\hat{\gamma}$, the non-negative $\sigma_{Q_{\text{in,TDC}}}^2$ in (18) can be minimized with

$$K_{\min} = \lim_{N_b \to \infty} K\left(N_b, \hat{\gamma}\right) = 1.$$

Moderate values of $0 < \gamma < \infty$ and N_b keep the value of K within the range $(1, \sqrt{\pi/2}]$, which in turn minimize the values of $\hat{\eta}$, $\sigma_{\Delta t}$, and $\sigma_{t_{\text{n,out}}}$.

A numerical search for the optimal $\hat{\gamma}$ and $\hat{K}$ pairs by sweeping γ in (31) was performed for $N_b = 1, 2, \ldots, 6$ as shown in Fig. 5. A BPD, where $N_b = 1$, does not have an explicit γ, but $K = \sqrt{\pi/2}$ in this case, which is represented by the horizontal line at the top of the figure. The plots are consistent with our analytical predictions for $K_{\max}$ and $K_{\min}$. The optimal $\hat{\gamma}$ and $\hat{K}$ pairs are tabulated in Table IV, from which we can see that, with more bits used by the TDC, the optimal $\hat{K}$ is reduced from $\sqrt{\pi/2}$ towards 1, where $N_b = 2$ or 3 already reduces $\hat{K}$ to a level that is close to 1, which is the theoretical ideal case for a "linear" TDC that generates no QE.

It is interesting to note that when $K = \sqrt{Z/Y^2}$ is minimized by $\hat{\gamma}$, the quantities $\left(Z - Y^2\right)$ and $\left(Z/Y^2 - 1\right)$ are also minimized exactly, which are the expression in (17) and the coefficient in (18) respectively. This implies that, the global optimization result, $\hat{\gamma}$, that minimizes the system jitters is effectively the same as the local optimization result that

TABLE IV
RECORDED OPTIMAL $\hat{\gamma}$, $\hat{K}$, AND $\hat{Z}$ FOR $N_b = 1, 2, \ldots, 6$

N_b	$\hat{\gamma}$	$\hat{K}$	$\hat{Z}$
1	N/A	1.253	1
2	0.996	1.065	3.554
3	0.588	1.019	11.151
4	0.336	1.006	35.036
5	0.188	1.002	112.772
6	0.104	1.001	369.432

minimizes the TDC QE. In other words, the optimal TDC resolution $\hat{\gamma}$ should be the one that simultaneously minimizes the DPLL's input jitter in (19), output jitter in (26), TDC QE in (17), and TDC-input-referred QE in (18). On the other hand, although [4] defines the TDC QE term, "K_q", to be the same as $\left(Z/Y^2-1\right)$ using our terminology, the system jitter represented by "K_J" in that work is derived from the flawed prediction in (22). This results in the global optimization—"K_J vs. γ" and the local optimization—"K_q vs. γ" performed in [4] being fundamentally different, which we now know is incorrect.

Furthermore, as introduced in Sec. III-A, the optimal loop parameter $\hat{\beta}$ balances the values of the TDC QE and DCO terms within Eq. (20), which can be ultimately minimized by the optimal $\hat{\gamma}$ as discussed in this subsection. However, these jitter minimization practices cannot alter the jitter contributed by the reference jitter, i.e., the $\sigma^2_{t_{n,\text{ref}}}$ term in the expressions of the system input and output jitters, (19) and (26). This fact limits the jitter minimization effect when the reference clock is the dominant contributor to the jitter.

Finally, substituting the optimal $\hat{Z}$ values in Table IV into (29) yields the optimal setting for the loop dynamics, $\hat{\beta}$, in which case the minimized values for the DPLL's input and output jitters can be derived by substituting $\hat{\gamma}$ and $\hat{K}$ in Table IV into (30), that is used to evaluate (19) and (26).

IV. Impacts of Jitter Minimization on Phase Noise

The jitter minimization strategy described in this work varies (i) the loop dynamics, i.e., β in (29), (ii) the estimated TDC linearized gain, K_{TDC} in (16), and (iii) the TDC QE, e.g., $\sigma^2_{Q_{\text{in,TDC}}}$ in (18). Together these affect the DPLL's output PN performance. This section comprehensively analyzes the impacts of the jitter minimization on the contributions to the output PN from the reference jitter, the TDC QE, and the DCO jitter separately, considering which we provide some design rules of thumb for efficient PN mitigation. Finally, we conclude this section with a design procedure to achieve low-jitter and low-PN DPLL systems.

A. Phase Noise Transfer Functions

The multi-rate system model shown in Fig. 2 can be linearized using a linear time-invariant (LTI) model as shown in Fig. 6, where $z = e^{j2\pi f/(N\cdot F_{\text{ref}})}$.[3] The phase perturbations injected by the reference jitter, TDC QE, and DCO jitter are marked in red, and these are transferred to the overall output PN level via their respective NTFs. Unlike Fig. 2 that refers the white Gaussian DCO period jitter to the DCO input, Fig. 6 models the DCO jitter referred to its output for simplicity of analysis, in which way the DCO-output-referred PN has a -20 dB/dec slope in its close-in power spectrum.

[3]A *time-variant* model that takes into account the downsampling operation of the feedback divider, which, in principle, imposes a folding effect to the out-of-band PN has been reported in [7]. This modeling approach is more accurate, yet complicates the DPLL model and analysis. As pointed out in [20], the slight increase in the far-off PN level is negligible for most DPLL systems. Therefore, we model the feedback divider as an LTI divide-by-N module in this section to simplify our analysis. The feedback division operation inherently contributes a unit delay as well, as shown in Fig. 6, according to [7, Fig. 5].

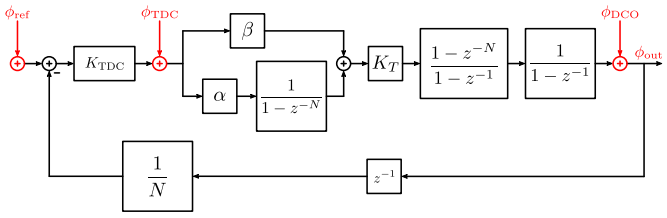


Fig. 6. Phase-domain LTI model of a DPLL system for PN analysis.

For the conciseness of presentation, we represent the feed-forward (or open-loop) gain of the system as

$$G_{\text{FF}}(z) = K_{\text{TDC}} \cdot \left(\beta + \frac{\alpha}{1-z^{-N}}\right) \cdot K_T \cdot \frac{1-z^{-N}}{1-z^{-1}} \cdot \frac{1}{1-z^{-1}}, \tag{32}$$

and the feedback gain as

$$G_{\text{FB}}(z) = \frac{1}{N} \cdot z^{-1}. \tag{33}$$

Hence, the loop gain of the system is

$$G_{\text{loop}}(z) = G_{\text{FF}}(z) \cdot G_{\text{FB}}(z). \tag{34}$$

1) $S_{\phi_{out}}$ Due to Reference Jitter: the system output PN PSD due to the (assumed) white reference PN is

$$S_{\phi_{\text{out,ref}}}(f) = \left|\frac{G_{\text{FF}}(z)}{1+G_{\text{loop}}(z)}\right|^2 \cdot S_{\phi_{\text{ref}}}, \tag{35}$$

where f in this section represents the offset frequency in relation to the center output frequency, the PSD of the PN of the reference jitter is related to the RMS reference jitter via

$$S_{\phi_{\text{ref}}} = (2\pi)^2 F_{\text{ref}} \cdot \sigma^2_{t_{n,\text{ref}}}. \tag{36}$$

2) $S_{\phi_{out}}$ Due to TDC QE: the system output PN PSD contributed by the TDC QE can be expressed as

$$S_{\phi_{\text{out,TDC}}}(f) = \left|\frac{1}{K_{\text{TDC}}} \cdot \frac{G_{\text{FF}}(z)}{1+G_{\text{loop}}(z)}\right|^2 \cdot S_{\phi_{\text{TDC}}},$$

where $S_{\phi_{\text{TDC}}} = (2\pi F_{\text{ref}})^2 \cdot S_{Q_{\text{TDC}}}$ is the phase-domain PSD of the TDC QE transferred from the PSD of TDC QE, which is $S_{Q_{\text{TDC}}} = \sigma^2_{Q_{\text{TDC}}}/F_{\text{ref}}$ as the TDC QE is randomized in the stochastic resonance regime so that it has a white power spectrum and its noise power is uniformly distributed in the bandwidth, F_{ref} [7]. $\sigma^2_{Q_{\text{TDC}}}$ is presented in (17). Together, we can rewrite

$$S_{\phi_{\text{out,TDC}}}(f) = (2\pi)^2 F_{\text{ref}} \cdot \left|\frac{G_{\text{FF}}(z)}{1+G_{\text{loop}}(z)}\right|^2 \cdot \sigma^2_{Q_{\text{in,TDC}}}, \tag{37}$$

where the variance of TDC-input-referred QE, $\sigma^2_{Q_{\text{in,TDC}}}$, is expressed in (18).

3) $S_{\phi_{out}}$ Due to DCO Jitter: the -20 dB/dec PSD of the DCO-output-referred PN due to the DCO jitter is expressed as

$$S_{\phi_{\text{DCO}}}(f) = S_{\phi_{\text{DCO}}}(\Delta f) \cdot \left(\frac{2\pi(\Delta f)}{N \cdot F_{\text{ref}}}\right)^2 \cdot \frac{1}{\left|1-z^{-1}\right|^2},$$

where the parameterization, $S_{\phi_{\text{DCO}}}(\Delta f)$, represents the value of the PSD referred to a specific offset frequency Δf [7]. For

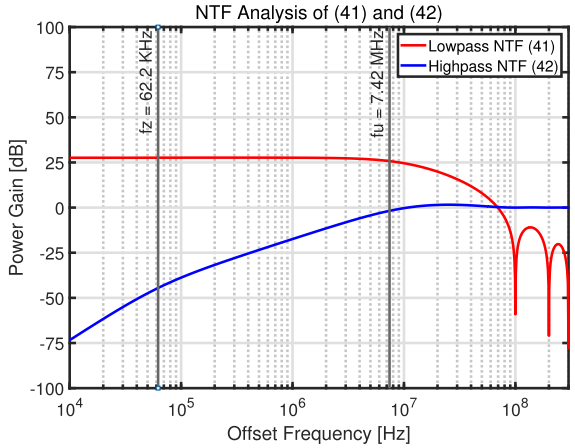


Fig. 7. PN NTFs in (41) and (42) for the system modeled in Sec. II-C.

example, $S_{\phi_{\text{DCO}}}(1\text{ MHz}) = -108$ dBc/Hz specified in Table I. $S_{\phi_{\text{DCO}}}(\Delta f)$ can be calculated by

$$S_{\phi_{\text{DCO}}}(\Delta f) = \frac{(N \cdot F_{\text{ref}})^3}{(\Delta f)^2} \cdot \sigma^2_{t_{n,\text{DCO}}}, \tag{38}$$

The system output PN PSD due to the DCO period jitter can be expressed as

$$S_{\phi_{\text{out,DCO}}}(f) = \left| \frac{1}{1 + G_{\text{loop}}(z)} \right|^2 \cdot S_{\phi_{\text{DCO}}}(f). \tag{39}$$

Finally, the PSD of the DPLL's output PN is a linear combination of the PSDs contributed by the uncorrelated noise sources in (35), (37), and (39), which is

$$S_{\phi_{\text{out}}}(f) = S_{\phi_{\text{out,ref}}}(f) + S_{\phi_{\text{out,TDC}}}(f) + S_{\phi_{\text{out,DCO}}}(f). \tag{40}$$

The above NTFs are used to predict the DPLL's output PN in the next section, which is then compared with the behaviorally simulated counterpart.

B. Loop Bandwidth

Notice that the NTFs for the reference jitter and TDC QE are defined by

$$\left| \frac{G_{\text{FF}}(z)}{1 + G_{\text{loop}}(z)} \right|^2, \tag{41}$$

whilst that for the DCO jitter is defined by

$$\left| \frac{1}{1 + G_{\text{loop}}(z)} \right|^2. \tag{42}$$

Plots of (41) and (42) are shown in Fig. 7.

To facilitate the frequency-domain analysis for the NTFs, we consider the narrowband approximation, where $f \ll F_{\text{ref}}$, which yields $z^{-1} \approx 1 - j2\pi f/(N \cdot F_{\text{ref}})$ and $z^{-N} \approx 1 - j2\pi f/F_{\text{ref}}$. In this way, the zero frequency contributed by the PI-based DLF with a transfer function, $\beta + \alpha/\left(1 - z^{-N}\right)$, can be simplified as

$$f_z \approx \frac{F_{\text{ref}}}{2\pi} \cdot \frac{\alpha}{\beta}. \tag{43}$$

Moreover, the term associated with α in (32) can be neglected as $\alpha \ll \beta$. As $2\pi f/(N \cdot F_{\text{ref}}) \ll 1$, we can further approximate $z^{-1} \approx 1$ in (33) for the feedback path [21]. With these approximations, the NTFs in (32)–(34) can be simplified in the frequency domain as

$$G_{\text{FF}}(f) \approx \frac{K_{\text{TDC}} \cdot \beta \cdot K_T \cdot N^2 \cdot F_{\text{ref}}}{j2\pi f}, \tag{44}$$

$$G_{\text{FB}}(f) \approx \frac{1}{N},$$

$$G_{\text{loop}}(f) \approx \frac{K_{\text{TDC}} \cdot \beta \cdot K_T \cdot N \cdot F_{\text{ref}}}{j2\pi f}. \tag{45}$$

The corner frequency can be found by calculating the unity-gain frequency, where $\left|G_{\text{loop}}(f_u)\right| = 1$, as it indeed manifests as the pole in the denominators of (41) and (42). Here,

$$f_u \approx \frac{K_{\text{TDC}} \cdot \beta \cdot K_T \cdot N \cdot F_{\text{ref}}}{2\pi}, \tag{46}$$

which is commonly referred to as the "loop bandwidth" of the DPLL.

Substituting (44) and (45) into (41), the lowpass NTFs for the PNs of the reference and TDC become a lowpass filter with a DC gain of N^2, and a -20 dB/dec roll-off beyond f_u. On the other hand, Substituting (43) and (45) into (42) yields the NTF for the DCO PN as a highpass filter with a +40 dB/dec slope below f_z, +20 dB/dec slope between f_z and f_u, and a unity highpass gain. The plotted z-domain NTFs using (41) and (42) for the system modeled in Table I are shown in Fig. 7, where the DC gain of (41) is $10\log(24^2) = 27.6$ dB and $f_z = 62.2$ kHz and $f_u = 7.42$ MHz as per (43) and (46). Note that, due to the discrete-time nature of the lowpass NTF in (41), high-frequency lobes are present in the out-of-band spectrum instead of a constant-slope roll-off.

C. PN Performance Impacted by Jitter Minimization

Our jitter minimization strategy optimizes the values of the TDC linearized gain and the DLF proportional gain, which alter the loop dynamics simultaneously. In particular, the change of the loop bandwidth is critical. Substituting the expressions for K_{TDC} and $\hat{\beta}$ in (16) and (29) into (46) yields

$$f_u = \sqrt{\frac{Y^2}{Z}} \cdot \frac{\sigma_{t_{n,\text{DCO}}}}{\sigma_{\Delta t}} \cdot \frac{\sqrt{N}}{2\pi} \cdot F_{\text{ref}}. \tag{47}$$

Since all the fractions on the right-hand side are dimensionless, the dimension of (47) is defined by F_{ref}, and hence is Hz, as expected. After jitter minimization, we observe that, within (47),

- the RMS input-referred jitter, $\sigma_{\Delta t}$, in the denominator was minimized;
- as the factor $K = \sqrt{Z/Y^2}$ in (31a) was minimized from the maximum value of $K = \sqrt{\pi/2}$ for the BPD case toward 1 for $N_b \to \infty$, interestingly, the term $\sqrt{Y^2/Z}$ must be maximized from $\sqrt{2/\pi} \approx 0.8$ toward 1;
- all the other terms remain unchanged.

Altogether, we conclude that, compared to a BBDPLL system with β optimized for the BBDPLL case, our jitter minimization via (i) increasing N_b, (ii) optimizing β for the new N_b case, and (iii) optimizing γ increases the loop bandwidth, but only slightly. In general, when the overall output jitter is guaranteed to be minimized, a broadened loop bandwidth is a desirable feature in terms of tracking speed, loop stability, etc.

To analyze the impact of our strategy on the contributions to the output PN from each of the noise/jitter sources individually, we observe that, compared to before jitter minimization,

1) For Reference-Jitter-Induced PN: our strategy does not change the power of the reference jitter represented by the white PSD, $S_{\phi_{\text{ref}}}$, or the DC gain of the NTF in (35). Therefore, the magnitude of the close-in PN level of $S_{\phi_{\text{out,ref}}}(f)$ will remain unchanged. The bandwidth of the close-in PN level is larger. However, as introduced above, the change in the bandwidth is insignificant and can be neglected;

2) For TDC-QE-Induced PN: same as the reference analysis above, the lowpass NTF's DC gain is unchanged, whilst its bandwidth is changed slightly. Referring to (37), as the white power of TDC-input-referred QE as expressed in (18) is minimized, the entire level of the PN contributed by the TDC QE will be reduced. Because the more TDC bits are used, the closer the Z/Y^2 is pushed to 1, and hence the less is the power of the TDC QE. Substituting (18) into (37), we can extrapolate that, in the limit, a TDC with an infinite number of bits contributes effectively zero PN, which corresponds to a conceptually linear TDC that does not generate quantization noise.

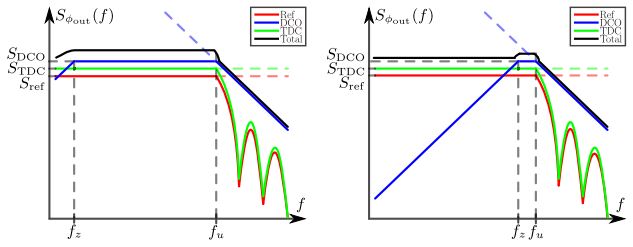
3) For DCO-Jitter-Induced PN: jitter minimization does not change the intrinsic power of the DCO jitter that is represented by the $S_{\phi_{\text{DCO}}}(f)$ with a -20 dB/dec slope in (39). In the meantime, as the corner frequency of the highpass filtering NTF is pushed higher, the PN contributed by the DCO will be better suppressed.

Finally, we conclude that jitter minimization performed in this work can increase the loop bandwidth modestly, which is desirable when the overall output jitter is guaranteed to be minimized. The optimized bandwidth rebalances slightly the PN contributions from the reference and DCO jitters, in the sense that the reference-induced PN is changed insignificantly, whilst the DCO-induced PN is better suppressed. The overall PN level contributed by the TDC QE is reduced by using extra TDC bits if the loop dynamics and TDC resolution are optimized accordingly.

D. Rules of Thumb for N_b Choices

As increasing the number of bits used by the TDC reduces its contributed output PN level, it is useful to derive a criterion that determines how many bits should be used to best mitigate the TDC-QE-induced PN. Conventionally, in the PN power spectrum, once the magnitude of the TDC-induced PN contribution is overwhelmed by those of the other noise-induced levels, the TDC-induced level will be *spectrally masked* by the latter, in which case one can argue that the TDC-induced PN has been *"canceled completely"*. In this subsection, we derive some design rules of thumb considering two separate scenarios, i.e., when $f_z \ll f_u$ and when $f_z < f_u$.

The intrinsic PN contributors of the reference jitter and TDC QE are both assumed white, and the NTFs for them are both defined by the same lowpass filter in (41). Therefore, the output PNs contributed by them have the same lowpass filtered shape. On the other hand, the intrinsic DCO-output-referred PN has a -20 dB/dec slope which, when passed through the highpass NTF of the type-II DPLL as discussed in Sec. IV-B, yields an output PN spectrum that has +20 dB/dec, flat, −20 dB/dec slopes in the three regions separated by f_z and f_u.



(a) $f_z \ll f_u$. (b) $f_z < f_u$.

Fig. 8. Illustration of the output PN power spectra in the two scenarios. Ref (red), DCO (blue), and TDC (green) curves represent the output PNs contributed by the reference jitter, DCO jitter, and TDC QE. Total (black) represents the overall PN.

Loop stability requires that $f_z < f_u$ [5]. We observe that, due to different settings of the α/β ratio, the distance between f_z and f_u varies. In some of the reported systems, e.g., [22] and [7, Fig. 6], $f_z \ll f_u$. In this case, the DCO-induced output PN has a broad flat level at close-in frequencies, which contributes to the overall in-band PN level together with the reference and TDC PNs. Note that the overall output PN in this case is similar to that of a type-I DPLL that does not have an integral path in the DLF, and hence $f_z = 0$ [23]. Meanwhile, some other systems, e.g., [2] and [3], push f_z close to f_u. In this way, the DCO-induced PN is much more suppressed and exhibits peaking near the corner frequency. Hence, the close-in phase noise level is only determined by the reference and TDC PNs in this case. We call the former configuration the "$f_z \ll f_u$" case and the latter the "$f_z < f_u$" case.

The output PN power spectra together with the breakdown of the PN contributions in these two cases as per the above analysis are illustrated in Fig. 8. To simplify the analysis, we represent the levels of the flat regions in the power spectrum induced by the reference jitter, DCO jitter, and TDC QE as S_{ref}, S_{DCO}, and S_{TDC}. We quantitatively derive their magnitudes using the RMS jitters elaborated in the previous sections as follows

- substitute (36) into (35) and recall that the DC gain of the NTF expressed by (41) is N^2, the PSD value of the flat region of the output PN induced by the reference jitter can be derived as
$$S_{\text{ref}} = (2\pi)^2 \cdot N^2 \cdot F_{\text{ref}} \cdot \sigma^2_{t_{n,\text{ref}}}; \tag{48}$$
- similarly, recall (37), the level of the flat region induced by the TDC QE is
$$S_{\text{TDC}} = (2\pi)^2 \cdot N^2 \cdot F_{\text{ref}} \cdot \sigma^2_{Q_{\text{in,TDC}}}, \tag{49}$$
which is equivalent to, as per (18),
$$S_{\text{TDC}} = (2\pi)^2 \cdot N^2 \cdot F_{\text{ref}} \cdot \left(K^2 - 1\right) \cdot \sigma^2_{\Delta t}, \tag{50}$$
where K is defined in (31).
- notice that between f_z and f_u, $\left|\frac{1}{1+G_{\text{loop}}(z)}\right|^2 \approx (f/f_u)^2$, substituting which, together with (47) and (38), into (39) yields the level of the flat region induced by the DCO jitter as
$$S_{\text{DCO}} = (2\pi)^2 \cdot N^2 \cdot F_{\text{ref}} \cdot K^2 \cdot \sigma^2_{\Delta t}. \tag{51}$$

Note that we can discard the common coefficient $(2\pi)^2 \cdot N^2 \cdot F_{\text{ref}}$ that appears in all the expressions, (48)–(51), when comparing their magnitudes.

1) When $f_z \ll f_u$: as illustrated in Fig. 8, in this case, the output close-in PN level is determined by the contributions from all the three PN sources. We observe that

- for S_{TDC} vs. S_{DCO}: interestingly, comparing (50) and (51), as the inequality of $\left(K^2-1\right)\cdot\sigma_{\Delta t}^2 < K^2\cdot\sigma_{\Delta t}^2$ always holds, this implies that the DCO-induced output PN always exceeds that induced by the TDC, as long as the jitter minimization is performed correctly. Note that this relationship is true for TDCs with any number of bits, and is even true for the BPD that generates the worst-case QE;
- for S_{TDC} vs. $S_{\text{DCO}}+S_{\text{ref}}$: taking into account the reference jitter in (48), we can see that the PN level contributed by the TDC QE must be masked by that contributed by both the reference and DCO jitters as $\left(K^2-1\right)\cdot\sigma_{\Delta t}^2 < K^2\cdot\sigma_{\Delta t}^2+\sigma_{t_{n,\text{ref}}}^2$ is always satisfied;
- for S_{TDC}, S_{DCO}, and S_{ref}: by our jitter minimization, K^2 and $\sigma_{\Delta t}^2$ are minimized, which lowers the output PN level contributed by the DCO and TDC simultaneously, yet has no effect on that from the reference jitter. Interestingly, one can interpret that the jitter minimization has an impact on the PN level that is *very similar* to that on the input/output jitters. As discussed in Sec. III-B, jitter minimization minimizes the jitters contributed by the DCO and TDC, but has no effect on the reference-induced jitter. Explicitly, the close-in output PN level is defined by (48), (50), and (51) as $(2\pi)^2\cdot N^2\cdot F_{\text{ref}}\left[\left(2\cdot K^2-1\right)\cdot\sigma_{\Delta t}^2+\sigma_{t_{n,\text{ref}}}^2\right]$;
- for S_{ref} vs. S_{DCO}: furthermore, recall (25) that $\sigma_{\Delta t}^2=\sigma_{t_{\text{n,out}}}^2+\sigma_{t_{n,\text{ref}}}^2$, hence $\sigma_{\Delta t}^2 > \sigma_{t_{n,\text{ref}}}^2$ always stands. As K^2 is minimized within the range of $(1,\pi/2]$, comparing (48) and (51), we can see that $\sigma_{t_{n,\text{ref}}}^2 < K^2\cdot\sigma_{\Delta t}^2$ is always satisfied. Therefore, no matter how much the DCO-induced PN is minimized, its magnitude is reduced towards the reference-induced level and can never be lower than the latter. In an extremely jitter-minimized case using a large number of bits, the magnitude of the overall close-in PN level will be determined by about twice S_{ref}.

2) When $f_z < f_u$: in this case, the close-in output PN level is only contributed by the PNs induced by the reference and TDC, which, as discussed already, have the same shape. As the DCO-induced output PN is much suppressed by just relocating the f_z position, this configuration is considered a better solution for enhanced PN performance. Note that the relationship of S_{ref} vs. S_{DCO} discussed in the last item in the above case still exists, which implies that the peaking in the DCO PN contribution will always exceed the reference-induced PN level. In order to have the TDC-induced PN *masked* by the reference-induced one, we come up with a useful inequality as a design criterion. By comparing (48) and (49), we need to ensure that

$$\sigma_{Q_{\text{in,TDC}}}^2 < \sigma_{t_{n,\text{ref}}}^2, \tag{52}$$

which can be accomplished by adopting more bits for the TDC followed by a correct jitter minimization. The inequality indicates that, as long as the power of the TDC-input-referred jitter is less than that of the reference jitter, the close-in PN will be dominated solely by the reference PN, as if the TDC is *"ideal"* and contributes no noise. Note that this PN minimization can be achieved by using a relatively small number of bits for the TDC, where we can already almost *"completely cancel"* the TDC-QE-induced PN from the output spectrum. This gives an advantage for using a DPLL in place of an analog CP-PLL, whose CP exhibits inevitable physical noises that cannot be easily mitigated [1]. Using additional bits for the TDC beyond this point is meaningless, as it only consumes more area and power.

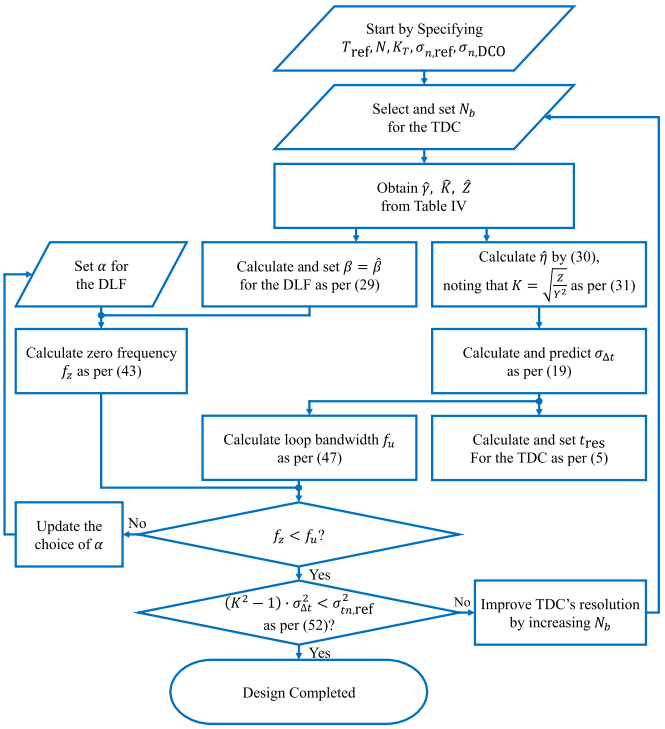


Fig. 9. Proposed jitter-minimization-oriented design procedure for a type-II DPLL whose output PN is dominated by the reference and DCO noises only.

E. Jitter-Minimization-Oriented Design Procedure

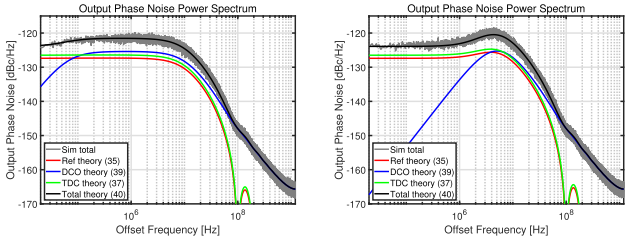
In order to achieve this optimal PN performance, insight into the inequality (52) can be gained by rewriting it as $\left(K^2-1\right)\cdot\sigma_{\Delta t}^2 < \sigma_{t_{n,\text{ref}}}^2$. The value of the optimal $\hat{K}$ can be obtained from Table IV, $\sigma_{\Delta t}^2$ is derived in the step for (19), and $\sigma_{t_{n,\text{ref}}}^2$ is a known characteristic of the reference source. The design procedure proposed in this work is summarized in the flowchart shown in Fig. 9; one can follow this procedure to achieve a type-II DPLL that has a minimized system jitter and an optimized PN performance that is dominated by the contributions from the reference and DCO jitters only, whilst using a minimum number of bits in the TDC.

V. Verification Results

To verify our analysis and predictions, we first model a multi-rate discrete-time DPLL system using the parameters presented in Table I that are extracted from [7, Sec. III]. We start with a BBDPLL with $\beta = 70$ and $\alpha = 2^{-8}\cdot\beta$. The PSD of the output PN is plotted in Fig. 10(a), which is the same as [7, Fig. 6 (c), right]. In this case, the resultant bandwidths are $f_z = 62.2$ kHz and $f_u = 7.42$ MHz. Note that this β value, and hence f_u, is not optimized for jitter minimization purposes. The relationship between f_z and f_u

TABLE V
PREDICTED VALUES AND SIMULATED INPUT JITTER FOR THE DPLLS OF FIGS. 10 AND 11

Case	TDC	$\sigma_{Q_{\text{TDC}}}$ [bit]	$\sigma_{Q_{\text{in,TDC}}}$ [fs]	K_{TDC} [bit/s]	β	f_u [MHz]	$\sigma_{\Delta t_{\text{prediction}}}$ [fs]	$\sigma_{\Delta t_{\text{simulation}}}$ [fs]
(a)	BPD [7] (with $\beta = 70$)	0.603	314	$1.92{\cdot}10^{12}$	70	7.42	416	416
(b)	BPD (with $\hat{\beta}$)	0.603	306	$1.97{\cdot}10^{12}$	47.8	5.20	405	407
(c)	2-bit (with $\hat{\beta}$)	0.650	141	$4.60{\cdot}10^{12}$	25.3	6.44	385	385
(d)	3-bit (with $\hat{\beta}$)	0.646	74.9	$8.62{\cdot}10^{12}$	14.3	6.82	380	380
(e)	3-bit (with $\beta = 90\% \cdot \hat{\beta}$)	0.646	75.0	$8.61{\cdot}10^{12}$	12.9	6.13	381	381
(f)	3-bit (with $\beta = 110\% \cdot \hat{\beta}$)	0.646	75.0	$8.61{\cdot}10^{12}$	15.7	7.49	381	381



(a) $f_z \ll f_u$. (b) $f_z < f_u$.

Fig. 10. Simulated vs. predicted PN PSDs for a BBDPLL before jitter minimization. Sim total (gray) is the simulated output PN; Ref theory (red), DCO theory (blue), TDC theory (green) are the analytically predicted PNs contributed by reference and DCO jitters, and TDC QE; Total theory (black) is the sum of all the predicted.

corresponds to the $f_z \ll f_u$ case discussed. To configure the $f_z < f_u$ case, we keep the other parameters unchanged and set $\alpha = 40 \cdot 2^{-8} \cdot \beta$, which yields $f_z = 2.49$ MHz that is much closer to f_u. The reconfigured output PN is shown in Fig. 10(b). Fig. 10 demonstrates the representative cases classified in Sec. IV-D. Case (a) of Table V shows the key system values that are predicted and then simulated.

A. Analysis of Effect of Jitter and PN Mitigation

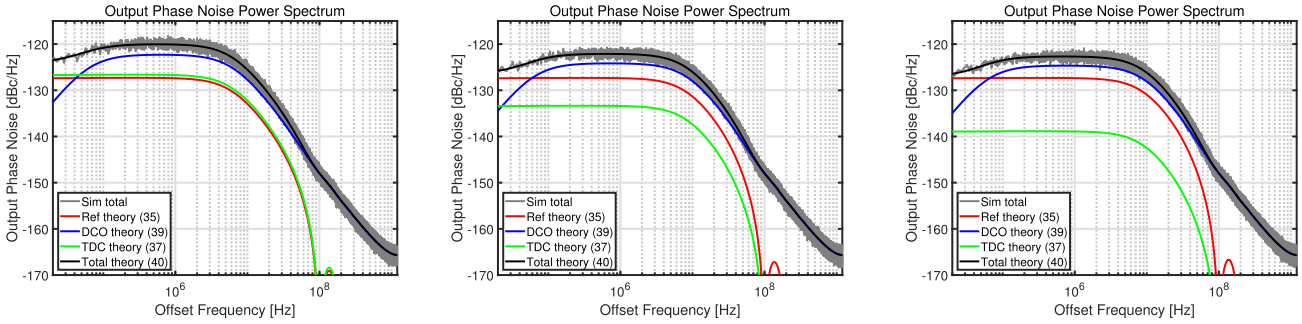
For the two cases shown in Fig. 10, we perform jitter minimization by setting the optimal loop bandwidth using $\hat{\beta}$ calculated with (29) and increasing TDC $N_b = 2, 3$ with the optimal values of $\hat{\gamma}$ in Table IV. The first and second rows of Fig. 11 show the output PNs after the jitter minimization process for representative $f_z \ll f_u$ and $f_z < f_u$ cases respectively. The key values are tabulated in Cases (b)–(d) in Table V. We observe that

- comparing the BPD cases before and after jitter minimization: as recorded in Cases (a) and (b) of Table V, jitter minimization by optimizing the loop bandwidth helps to reduce the system jitter from 416 to 405 fs;
- considering increased N_b with jitter minimization: in terms of jitter minimization, we can see that our strategy reduces the RMS TDC-input-referred QE, $\sigma_{Q_{\text{in,TDC}}}$, and the RMS input jitter, $\sigma_{\Delta t}$, simultaneously. In terms of PN performance, our strategy increases the loop bandwidth modestly, as expected. The TDC-QE-induced PN level is reduced from above to below the reference-induced level. Note that the reference-induced noise level is determined by $\sigma_{t_{n,\text{ref}}} = 283$ fs. Referring to the fourth column of Table V, we see that $N_b \geq 2$ makes $\sigma_{Q_{\text{in,TDC}}} < \sigma_{t_{n,\text{ref}}}$. As per (52), this in turn brings the TDC-induced level below the reference-induced level. The higher the number of bits, the lower is the TDC-induced PN level. With jitter minimization, the flat region of the DCO-induced PN level decreases as well, yet, as predicted in Sec. IV-D, it cannot be reduced to be lower than the reference-induced level. Hence, for the $f_z \ll f_u$ case with jitter minimization, the overall close-in PN level is determined by the PN contributed by the DCO and reference;
- considering the $f_z < f_u$ case: in terms of the key values, the only difference from the $f_z \ll f_u$ case is that $f_z = 2.49$ MHz now. In this case, our strategy successfully minimizes the TDC QE and system jitters as well. The close-in output PN level is only determined by the reference and TDC PNs, which is lower compared with the $f_z \ll f_u$ case. Increasing N_b together with a correct jitter minimization, the TDC-QE-induced level can be reduced significantly. In Fig. 11(d), the TDC-induced level contributes more to the overall PN level than the reference one, whereas in Fig. 11(f), the TDC-PN is overwhelmingly masked by the reference-PN so that the close-in level is dominated by the reference PN *per se*. Similar to the previous observation, $N_b \geq 2$ satisfies the inequality in (52) that ensures that the reference-induced PN level is dominant. Notice that, as predicted in Sec. IV-D, the DCO-induced PN always has a narrow flat region whose magnitude can be reduced, yet can never by lower than the reference-induced level;
- finally, as discussed in Sec. III-A, the output spectra are free of spurs due to the fact that the TDC is operating in the stochastic resonance regime.

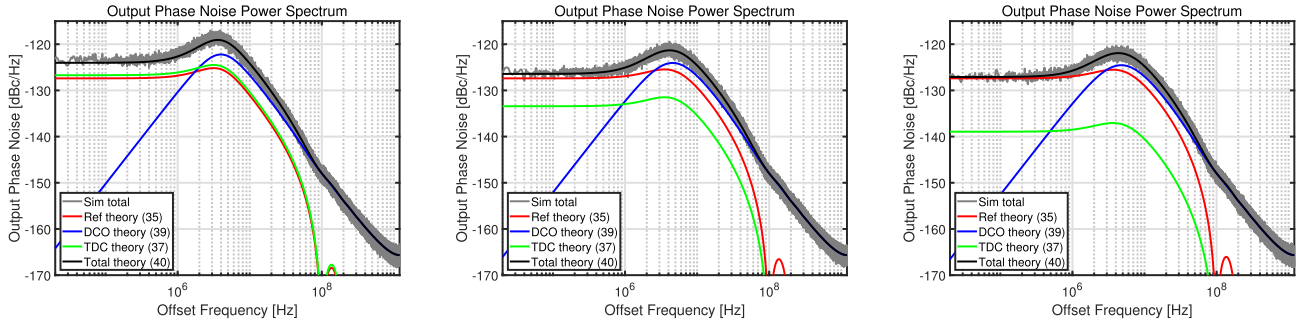
Quantitatively, our predicted RMS input jitters match the simulated counterparts for all the cases presented, which confirms the accuracy and effectiveness of our albeit idealized analysis.

B. Sensitivity of the Optimized Designs to Variations, Mismatch, and Nonlinearity

To assess the optimality of the loop bandwidth set by applying $\hat{\beta}$, recalling (46), we predicted and simulated the DPLLs with a 3-bit TDC where the loop bandwidth is slightly increased (or reduced) by setting a value for β that is 10% greater (or less) than $\hat{\beta}$. The predicted and simulated key values of these cases are tabulated in Cases (e) and (f) of Table V. Compared with Case (d), which describes the 3-bit-TDC DPLL that is optimized as per our jitter minimization strategy, we observe that making the loop bandwidth slightly narrower or wider in fact degrades the TDC-input-referred QE and the system jitter but only slightly. This indicates that the loop bandwidth set by $\hat{\beta}$ derived in this work is indeed an optimized one. It also confirms that the value of β is insensitive to

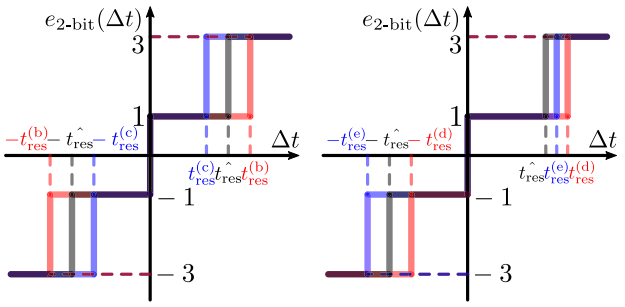


(a) $f_z \ll f_u$, BPD. (b) $f_z \ll f_u$, 2-bit. (c) $f_z \ll f_u$, 3-bit.



(d) $f_z < f_u$, BPD. (e) $f_z < f_u$, 2-bit. (f) $f_z < f_u$, 3-bit.

Fig. 11. Simulated vs. predicted PN PSDs for DPLLs after jitter minimization. Sim total (gray) is the simulated output PN; Ref theory (red), DCO theory (blue), TDC theory (green) are the analytically predicted PNs contributed by reference and DCO jitters, and TDC QE; Total theory (black) is the sum of all the predicted.



(a) Symmetric mismatch. (b) Asymmetric mismatch.

Fig. 12. Illustration of 2-bit TDCs with nonideal thresholds described in Cases (b)–(e) in Table VI.

small variations in the sense that having a value of β slightly deviated from $\hat{\beta}$ only degrades the system jitter marginally (by 1 fs in our simulations).

We also assessed the sensitivity of the derived optimal setting to the TDC's nonlinearity, for which we simulated the two typical cases using a 2-bit TDC as examples. Table VI tabulates the simulated system jitters. The TDCs in the simulations have zero as the center threshold and positive and negative quantization thresholds that symmetrically or asymmetrically mismatch the optimal resolution as shown in Fig. V-A. Symmetrically mismatched thresholds are 10% wider ($\pm t_{\text{res}}^{(b)}$ in Fig. V-A(a)) or narrower ($\pm t_{\text{res}}^{(c)}$ in Fig. V-A(a)) than the optimal. Asymmetrically mismatched positive and negative thresholds in Case (d) of Table VI are 10% right offset from the optimal ($\pm t_{\text{res}}^{(d)}$ in Fig. V-A(b)); those in Case (e) are 5% right and 10% left offset from the optimal ($\pm t_{\text{res}}^{(e)}$ in Fig. V-A(b)). The asymmetric mismatch can also

TABLE VI

SIMULATED INPUT JITTER OF 2-BIT-TDC DPLLS WITH $\hat{\beta}$ AND IDEAL (OPTIMIZED) OR NONIDEAL TDC THRESHOLDS

Case	Feature of γ	t_{res}	$\sigma_{\Delta t_{\text{simulation}}}$ [fs]
(a)	Optimum	$\hat{t_{\text{res}}} = \hat{\gamma}/\sigma_{\Delta t}$	384.9
(b)	Symmetric Mismatch	$110\% \cdot \hat{t_{\text{res}}}$	385.4
(c)		$90\% \cdot \hat{t_{\text{res}}}$	385.9
(d)	Asymmetric Mismatch (Nonlinearity)	$\hat{t_{\text{res}}} + 10\% \lvert\hat{t_{\text{res}}}\rvert$	385.3
(e)		$-\hat{t_{\text{res}}} - 10\%\lvert\hat{t_{\text{res}}}\rvert$ & $\hat{t_{\text{res}}} + 5\%\lvert\hat{t_{\text{res}}}\rvert$	385.2

be regarded as the TDC exhibiting a static nonlinearity. The mismatched cases once again confirm the optimality of our optimized TDC's resolution, whilst the slightly degraded jitter performances show that our proposed TDC setting is relatively intensive to mismatch and the TDC's nonlinearity.

VI. CONCLUSION

In this paper, we performed a comprehensive analysis of the input and output jitters of DPLLs with mid-rise TDCs with an accuracy which outperforms that of the most recent analysis of this architecture in [4]. A complete jitter minimization strategy is provided based on our jitter prediction, which can minimize the power of the TDC QE and system jitters simultaneously. The impact of jitter minimization on the DPLL's output PN performance is studied, considering the characteristics of the loop's NTFs and bandwidth that are changed by jitter minimization. As per the case studies for different loop dynamics, we provide insights, design rules of thumb and a detailed procedure that assists efficient jitter and PN mitigation for DPLLs used as frequency synthesizers.

The analysis and predictions in this work are confirmed with closed-loop behavioral simulations.

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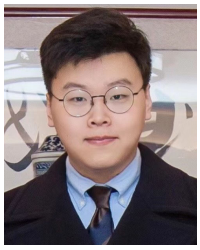

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