APCCAS 2022 Guest Editorial Special Issue Based on the 18th Asia Pacific Conference on Circuits and Systems

THE IEEE Asia Pacific Conference on Circuits and Systems (APCCAS) is the regional flagship conference of the IEEE Circuits and Systems Society (CASS) in Asia. This conference is a major international forum established by the IEEE Circuits and Systems Society for researchers to exchange their latest findings in circuits and systems. It covers a wide range of topics, including analog, mixed-signal, digital, communication, sensory, biomedical, power/energy, nonlinear, and artificial intelligence circuits and systems.

The 18th APCCAS was held in Shenzhen, China, on November 11–13, 2022, which was a hybrid event due to the COVID-19 pandemic in China. Among all the accepted contributions, 15 articles were selected and invited for this Special Issue, and seven articles went through the peer-review process consisting of world-renowned reviewers in the related fields. A brief description of the accepted articles is provided as follows.

In [A1], Shi et al. propose a spatio-temporal video denoising co-processor to suppress an image sequence's spatial and temporal noise. Temporal denoising is achieved by merging the current and previous frames at the pixel level in which the current frame is processed by a spatial filter. After exploiting noise estimation and motion detection, the Wiener filter calculates the merge ratio. Rather than buffering the entire previous frame, the JPEG-like codec can dynamically adjust the compression ratio through a predefined quantization table to satisfy the designed on-chip storage. The experimental results demonstrate that the spatio-temporal denoising co-processor can effectively eliminate the fluctuation of the grayscale value of the noise in videos. Simultaneously, the adaptive codec can reduce the storage space consumption for the frame buffer by at least 80% of the original size.

In [A2], Zhang et al. propose a low-power high-accuracy keyword spotting (KWS) system based on analog passive switched capacitor (SC) bandpass filters (BPF). The proposed system innovatively extracts the Mel-frequency cepstrum coefficient (MFCC) features with all-analog circuits, providing a better spotting performance than the present analog short-time amplitude or energy features under the same condition. The size of the fully connected neural network (FCNN) classifier in the proposed KWS system is thereby reduced. A high-order and fully differential BPF is also proposed, achieving ultra-low power and high dynamic range by combining zero and pole generation stages rather than building stages separately. The total power consumption of the feature extractor is 661.7 nW, achieving an accuracy of 96.6% in two-keyword spotting by an FPGA-based, 15k bit parameter FCNN with a 9.6 μs latency.

In [A3], Chen et al. propose a full-custom eight-transistor (8T) SRAM-based Processing-in-Memory (PIM) architecture to realize a pixel-parallel array processor for energy-efficient vision chips. The proposed PIM architecture is constructed by embroidering each dual port 8T SRAM cell with multiplexer-based lightweight computing circuits, to form a PIM PE array. A full custom physical layout of a 128 $\times$ 128 prototyping PIM PE array is designed and simulated using a 65-nm CMOS technology. The simulation results demonstrate 200 MHz operation at 1.0 V, an energy efficiency of 512 GOPS/W, and an area efficiency of 29 GOPS/mm^2 of the PIM PE array.

In [A4], Long et al. present a novel approach to improve the efficiency of the neural Radiance Field (NeRF) rendering by adopting precision-scalable computation. The idea of scene-dependent quantization is first analyzed and validated for NeRF. Based on that, the authors further propose look-up table (LUT) processing element (PE)-based precision-scalable computation unit designs. The comparison results show that energy efficiency can be significantly improved using precision-scalable computation for NeRF.

In [A5], Chen et al. design a 50-Gb/s optical receiver (ORX) chipset consisting of a transimpedance amplifier (TIA) and a clock and data recovery (CDR) circuit in a 45-nm silicon-on-insulator CMOS. A complete optical-to-electrical (OE) link is built by integrating the proposed ORX with a high-speed Silicon Photonics (SiP) photodetector (PD). The measurements show that the proposed TIA has a transimpedance gain of 53 dBΩ and a BW of 27 GHz. By integrating it with the SiP PD, the OE frontend (PD+TIA) achieves an input sensitivity of -7.7 dBm at 50 Gb/s. It features a power efficiency of 1.61 pJ/bit at a data rate of 64 Gb/s. The complete 50 Gb/s ORX achieves data recovery at a quarter rate of 12.5 Gb/s with an output jitter of 1.6 psrms, and has a 3.125 GHz clock with phase noise of -115.22 dBc/Hz at an offset frequency of 1 MHz.

In [A6], Yan et al. propose a top-down design strategy for approximate floating-point (FP) FFT, which includes a mantissa bit-width adjustment algorithm and a step-by-step multiplier approximation algorithm. With the mantissa bit-width

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adjustment algorithm, the approximate 64 FP FFT achieved 50% area reduction and 70% power-delay product (PDP) reduction compared to the exact design with a 60dB Signal Noise Ratio (SNR) requirement, which is also at least 52% and 33% better than the previous approximate FP FFT. After using the step-by-step multiplier approximation algorithm, the approximate mantissa multiplier with an 8-bit fractional part reduced the area and PDP by 81.15% and 93.70%, respectively. The feasibility of the proposed approximate FFT design is verified in the channel estimation module of a wireless communication system, spectrum analysis, and image processing system.

In [A7], Luo et al. propose an NoC-based scalable multi-die FPGA architecture and a corresponding floorplanning framework, namely, Hierarchical and Recursive Floorplanning Framework (HRFF). First, from the architecture side, an interconnection architecture with a class of scalable hierarchical topology is introduced. Second, from the algorithm side, the generic floorplanning problem for NoC-based architectures is formulated as a multi-objective Mixed Integer Linear Programming (MILP) problem, balancing the design timing and interconnection workload. Third, a novel recursive approximate method is developed to efficiently solve the multi-objective MILP formulation over the proposed architecture, with a configurable trade-off between solution quality and solver run time. Experimental results show that the scalability of the proposed technique is at least 1.5× on all and 3× on certain benchmarks as that of the state-of-the-art solutions with no loss of design throughput.

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APPENDIX: RELATED ARTICLES

[A1] G. Shi et al., "A spatio-temporal video denoising co-processor with adaptive codec," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 70, no. 11, pp. 4223–4234, Nov. 2023.

[A2] S. Zhang, F. Su, Y. Wang, S. Mai, K. P. Pun, and X. Tang, "A low-power keyword spotting system with high-order passive switched-capacitor bandpass filters for analog-MFCC feature extraction," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 70, no. 11, pp. 4235–4248, Nov. 2023.

[A3] L. Chen et al., "An 8-T processing-in-memory SRAM cell-based pixel-parallel array processor for vision chips," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 70, no. 11, pp. 4249–4259, Nov. 2023.

[A4] K. Long et al., "Analysis and design of precision-scalable computation array for efficient neural radiance field rendering," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 70, no. 11, pp. 4260–4270, Nov. 2023.

[A5] S. Chen et al., "A 50 Gb/s CMOS optical receiver with Si-photonics PD for high-speed low-latency chiplet I/O," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 70, no. 11, pp. 4271–4282, Nov. 2023.

[A6] C. Yan, X. Zhao, T. Zhang, J. Ge, C. Wang, and W. Liu, "Design of high hardware efficiency approximate floating-point FFT processor," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 70, no. 11, pp. 4283–4294, Nov. 2023.

[A7] J. Luo, X. Liu, F. Chen, and Y. Ha, "HRFF: Hierarchical and recursive floorplanning framework for NoC-based scalable multi-die FPGAs," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 70, no. 11, pp. 4295–4308, Nov. 2023.