The Hidden Behavior of a D-Latch

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***Abstract*— For clock and data transitions in close temporal proximity, synchronous memory elements potentially enter metastability, which leads to unintended output behavior. Although respective analyses in literature have already derived suitable explanations, almost all of them modeled the control (clock) signal transition with negligible rise/fall time. In modern circuits this assumption is, however, not reasonable any more. In fact, due to a finite slope, intermediate clock signal values have to be considered during a large share of the storage process, while their concrete impact is not yet sufficiently explored. In this paper we thus use static and dynamic considerations to thoroughly investigate the behavior of a latch for arbitrary analog control, data and output values, i.e., during the storage process. Basic circuit considerations allow us to derive a unified model which identifies the latch as a Schmitt Trigger with vastly varying hysteresis. We verify the correctness of our predictions by comparison to analog SPICE simulations. Finally we are able to generalize our findings and thus provide explanations for yet unexplained behavior reported in literature.**

***Index Terms*— Memory loop, latch, Schmitt trigger, buffer, metastability.**

I. Introduction

MANY stateful digital circuit elements, like the D-latch (further called `Latch`) and SR-latch [1], the Mutex [2], or the Muller C-element [3], rely on the same fundamental storage primitive. While there are important differences, e.g., in regard to the input stack, the most popular implementations all comprise a "memory loop" of two inverting gates that constitutes the actual storage, when the element is *opaque*, i.e., in "hold mode". Among these circuit elements, the `Latch` is the only one with a dedicated enable input (*en*) that directly determines whether the storage capability is enabled or disabled; in the other circuit elements the data inputs control this implicitly.

Analyses of such stateful digital circuit elements in literature have also primarily focused on the `Latch`, especially on describing its switching behavior. This is easily explainable by the fact, that combining two such devices results in a flip flop, which is, with distinction, the most popular storage element in synchronous circuit designs.

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Since the seminal work by Kinniment and Edwards [4], Chaney and Molnar [5], and Veendrick [6] it is understood that the `Latch` exhibits, besides the two desired stable states `HI` and `LO` also a *metastable* state in between. In general the latter quickly resolves to a stable one. Nevertheless, the `Latch` may, in principle, remain metastable for an arbitrary amount of time. Careful analyses led to a statistical estimate of the Mean Time Between Upset (MTBU) [6], which scales exponentially with the time t_{res} allowed for metastability resolution, i.e., MTBU$\sim \exp(t_{res}/\tau)$, where τ denotes a time constant tied to a specific `Latch` implementation.

The calculation of the MTBU consists of two parts: 1) the chance of the `Latch` getting metastable and 2) its resolution speed out of metastability. The former is represented by the probability of *sampling* the data signal while it is transitioning, i.e., at an intermediate value. The sampling itself is realized by activating the hold mode (switching signal *en*),[1] where the respective transition on *en* is assumed perfect, i.e., having negligible rise/fall time. For 2) the output trajectory of an opaque `Latch`, initialized near its metastable state, is computed and the rate of convergence towards a stable value extracted.

Interestingly, the assumption of a perfect *en* signal has rarely been questioned in past investigations of latch and flip flop. Although signal transitions in the GHz clock regime are far from ideal, the clock signal was completely neglected in various studies focused, for example, on the impact of process variations [7], [8], [9] or aging effects [10]. Nevertheless, there are also exceptions: Larsson and Svensson [11], Alioto et al. [12], and Pandey et al. [13] investigated the delay variations of flip flops due to differing clock slopes. Ma et al. [14] did a very similar analysis for the supply current, which they then used for side-channel attack protection. Additionally, Hayasaka and Kobayashi [15] focused on the sampling time error induced by finite clock slope. However, the overall behavior of a `Latch` for intermediate *en* values has not yet been thoroughly investigated, which we are going to complement in the sequel.

The main contribution of this paper is, therefore, a thorough analysis of all possible `Latch` behaviors when controlled by a "non digital" or slowly rising *en* signal. In detail we investigate the observable changes when maneuvering in between transparent mode, i.e., where the input is directly forwarded to the output, and hold mode. Using basic circuit analysis methods we develop a simplified model that is capable of describing the behavior over the whole range of analog in- and output voltages. This enables us, for the first time,

[1] In some earlier publications the `Latch` was denoted as flip flop, and *en* as *clk*.

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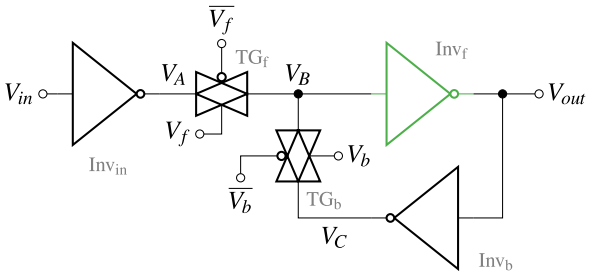


Fig. 1. Gate-level implementation of a TG-controlled memory loop.

to retrace the behavior of storage elements during transition that was inexplicable in previous publications. We want to emphasize that, due to the static nature and universality of our model, only qualitative statements can be made; for accurate quantitative results about a specific circuit in a specific layout analog simulations are still mandatory.

In a nutshell our analysis reveals that a Latch can actually be modeled by a Schmitt-Trigger (S/T) [16] with gradually varying input-output hysteresis width. Analog SPICE simulations confirm our predictions and even reveal additional behavior, such as a tri-stable memory element. Finally we discuss the consequences of our findings on other storage elements and provide possible applications.

This paper is organized in the following fashion: In Section II we summarize the available behavioral analyses of the Latch, which already allow us to derive prognoses for yet unknown regimes. Using a low-level representation we develop a simplified model in Section III that correctly depicts the continuous characteristic change from a buffer over an S/T like behavior to a memory loop with changing en. We verify our analytic considerations in Section IV by extensive analog simulations and discuss general implications of our results. In Section V we highlight possible future benefits of our gained insights while a short conclusion and an outlook on future work in Section VI finally closes the paper.

II. Background

In this section we first present already known Latch behaviors and, based on these, extrapolate still unexplored operating conditions. For this purpose we will investigate the circuit shown in Fig. 1, which consists of a loop of forward (Inv$_f$) and backward (Inv$_b$) inverter. Its operation mode is controlled by a forward (TG$_f$) and backward (TG$_b$) Transmission Gate (TG). A high value on the inputs V_f and V_b causes the respective TG to be conducting while a low one corresponds to an open wire.[2] In an actual Latch the two TGs are coupled such that $\overline{V_f} = V_b$ and $V_f = \overline{V_b}$ (we will introduce this in Section III), but for the sake of the desired generalization we consider them separated for now.

We decided to use an implementation with two TGs to simplify our explanations and thus make them easier retraceable. In general, any Latch must contain a storage loop and the possibility to either propagate the state of the storage loop or the input value itself to the gate output. For this selection, V_b and V_f could be viewed as abstract values qualifying the contributions of storage loop and input, respectively. With this abstraction in mind, we believe that our analysis covers all common static implementations of a Latch, like those using gated inverters [1] or only one TG. In our opinion, these will only differ in the specific mapping of their control input V_{en} on the two values V_f and V_b. Even the removal of the input inverter (Inv$_{in}$), which allows to neglect the unknown strength of the source driving V_{in} in the analysis, would only result in a modified mapping of V_{en} on V_f. In this case the maximum value of V_f would be limited to model the output resistance of the assumed V_{in} source. In fact, our chosen Latch model represents an even larger set of circuits, e.g., the (S/T) implementation used in [17], making our results more generally applicable.

[2]For simplicity we assume $\overline{V_f} = V_{DD} - V_f$ and $\overline{V_b} = V_{DD} - V_b$ here. Simulations with more general setups revealed qualitatively equal results.

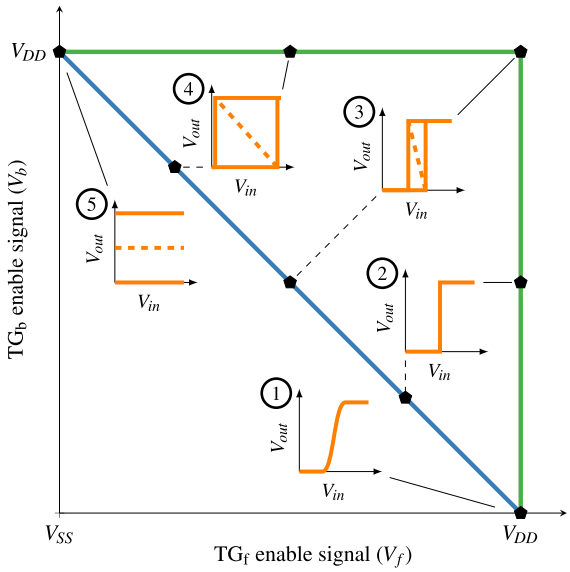


Fig. 2. Known and predicted behaviors over V_f and V_b.

Fig. 2 visualizes the static behavior of the Latch obtained for independent variations of V_f and V_b. For case ① ($V_f = V_{DD}$ and $V_b = V_{SS}$) the backward inverter is completely cut off, such that the input and forward inverter in series determine the overall characteristic, namely a buffer. In this setup we obtain an unambiguous one-to-one mapping from input to output value, which renders metastability impossible. In the reverse situation ⑤ ($V_f = V_{SS}$ and $V_b = V_{DD}$) the input inverter is completely cut off and thus the well known behavior of a memory loop can be observed: Irrespective of the input voltage, there are two stable output values at V_{DD} and V_{SS} (solid lines), while the actual output value at any given point in time naturally depends on past input trajectory. Inevitably, this stateful behavior also entails one metastable state in between the stable ones (dashed line) [18].

Another well known configuration is ③ ($V_f = V_b = V_{DD}$), where both TGs are transparent: Here we obtain a competition between the state fed back by TG$_b$ and the input conveyed by TG$_f$, which resembles the behavior of a non-inverting S/T [16].

At a first glance the operation of a Schmitt-Trigger appears fundamentally different from that of a `Latch`: While the latter captures the input on the falling transition of *en* and then stores the value, the former does not even have a control input. Even more, as shown in Fig. 3, it implies an input hysteresis, meaning that the output stays constant until a threshold value (V_L or V_H depending on the input direction) has been passed. In ③ the relative conductivity of the TGs determine the balance between backward and forward paths, and hence the hysteresis width $W = V_H - V_L$: Increasing the strength of TG_b leads to an increased W as more driving force from TG_f is required (V_{in} closer to V_{DD}/V_{SS}) to flip the memory loop.

Such an input-output hysteresis (indicated by dashed lines in Fig. 3) is often used to create clean (fast and full range) output transitions by filtering small fluctuations around $V_{DD}/2$ or uniquely assigning an intermediate voltage (like one resulting from a metastable `Latch`) to a defined logic `LO` or `HI`. This makes the S/T attractive for many areas of application, such as reliable circuits [19], oscillators [20] or SRAM [21].

But then again, it has been shown by Marino [18] and recently further elaborated by Steininger et al. [22] that S/Ts can become metastable as well. Even worse: in contrast to the `Latch`, which solely has two stable and one metastable output values (red crosses in Fig. 3), the S/T may propagate a whole range of undesired voltages. In detail the metastable γ_2 connects the stable γ_3 at V_L and γ_1 at V_H, leading to the characteristic S-shape (respectively Z-shape for inverting S/Ts). This stateful behavior again points to a possible relation between `Latch` and S/T.

We can use these insights to predict the yet unknown behavior at the intermediate positions ② and ④. In this regard it is important to note that a TG essentially limits the current that is delivered per unit voltage drop. Thus moving from ③ towards ⑤ increasingly weakens the input path. This is equivalent to strengthening the backward path, leading to a growing hysteresis width W, as is shown at ④. It becomes apparent that mainly the relative driving strength of input and backward path are of concern, not their absolute values. At some point the voltage range of V_{in} is insufficient to flip the state, meaning that the unit works as a memory loop. Note, however, that this situation is still different from the fully opaque `Latch`, since the metastable line (dashed line) is not yet horizontal, implying a residual dependence on the input. Only when the threshold points of the hysteresis move to the theoretical $\pm\infty$, the metastable line becomes horizontal (and hence the metastable voltage input independent), which is depicted at ⑤.

Similarly when going from ③ towards ① one reduces the current from the backward TG and thus weakens its influence. In this case the hysteresis width W gets smaller and smaller until finally $V_L = V_H$ is achieved. From this point onward the behavior changes to an amplifier with a unique mapping from V_{in} to V_{out}. Therefore, no metastability can occur in this region. To achieve a consistent representation we define in this mode of operation V_L resp. V_H as the input values V_{in} where V_{out} starts to deviate from V_{SS} resp. V_{DD}, even though the hysteresis $W = V_L - V_H$ formally becomes negative then. In summary we thus experience a declining hysteresis width

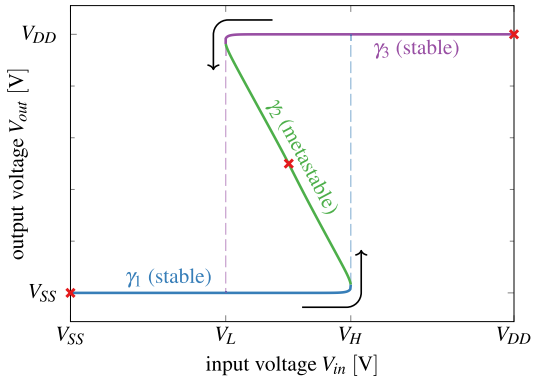


Fig. 3. (Meta)stable states of a memory loop (crosses) and an S/T (lines), V_{in} and V_{out} representing the nodes in the loop. Inspired by [17].

W when traversing along the green line, from $W = \infty$ at ⑤ to $W < 0$ at ①.

Defining the TG enable signals by $V_f = V_{DD} - V_b$, which corresponds to the blue line shown in Fig. 2, allows us to apply our former analysis to the `Latch`. Start- ① and endpoint ⑤ are still the same, however, now the TG_f will be strengthened (increasing V_f) while TG_b is simultaneously weakened (decreasing V_b). Recalling our observation that the *relative* drive strength of the TGs determines the hysteresis, and assuming continuous behavior of real circuits,[3] we can conclude that also along the blue path from ① to ⑤ every relation of drive strengths and hence every hysteresis width W can be observed. Be advised that the dynamic properties, e.g., the metastability resolution speed, most likely will change due to the much higher power dissipation for higher values of V_f and V_b. A more fine grained analysis of this topic is scheduled for future research.

Although these statements hold true for many paths in the plane, it is not generally applicable. For example for those coming too close to the origin $V_f = V_b = 0$, both TGs become weak and potentially stop conducting altogether, as also pointed out in [23]. This would not only compromise the dynamic behavior but also lead to a direct transition from memory loop to buffer operation, with a floating internal node in between. For these reasons, overall a very interesting design space is opened up.

III. Extended Latch Model

To show that the intuitive description given so far is indeed correct we will investigate in the sequel the electrical properties of the `Latch`. For this purpose we have to set $V_{en} = V_b = \overline{V_f}$ in Fig. 1, where the inversion is approximated by $\overline{V_{en}} = V_{DD} - V_{en}$. Recall that the storage loop is formed by the forward (Inv_f) and backward (Inv_b) inverter, while the input voltage V_{in} is supplied via the input inverter (Inv_in). The two TGs connecting V_A with V_B, and V_C with V_B, respectively, are used to switch between transparent and hold mode. The `Latch` is thus opaque (holds its current value) for $V_{en} = V_{DD}$ while for $V_{en} = V_{SS}$ it is transparent (behaves like a buffer).

[3]This would of course not be justified if we had to consider quantum mechanical aspects.

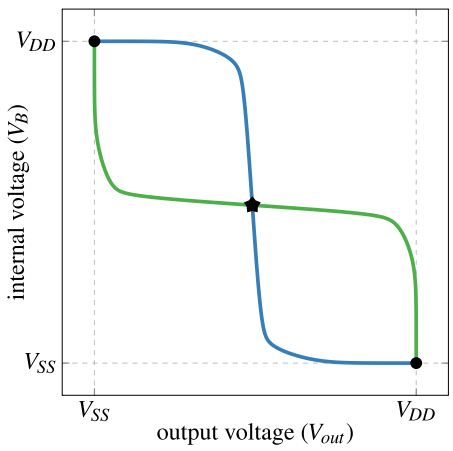


Fig. 4. Stable (dots) and metastable (star) states of the opaque `Latch` obtained by intersecting the inverter characteristics ($V_{en} = V_{DD}$).

In the sequel we are going to determine the static (meta)stable states based on the values of V_{in} and V_{en}, which will allow us to retrace the changes in the `Latch` behavior. Note that these static considerations even enable a qualitative estimation of the dynamic behavior, as the `Latch` tries to escape metastable configurations towards stable ones.

We want to emphasize that an analytic evaluation of this circuit, i.e., one that considers the actual transistor characteristics, would be very challenging. In fact it is too complicated to be presented properly at this point. To put the focus on the key idea we thus limit ourselves to a very simplified explanation, which is, nevertheless, capable to derive the general shape. Our evaluations will be confirmed in Section IV by SPICE simulations that reflect the transistor behavior very accurately.

A. Determining (Meta)Stable Points

(Meta)stable states share the characteristic property that the voltages and currents within the circuit are perfectly balanced. Here, this corresponds to the case that the internal voltage V_B leads to an output value V_{out} which, in combination with V_{en} and V_{in}, exactly recreates V_B. Thus our task is, based on a given tuple of input voltages (V_{in}, V_{en}), to identify the values of V_B and V_{out} that result in such a balanced configuration.

A very efficient solution for this problem is a graphical representation. Fig. 4 shows an appropriate overlay of the static transfer characteristics $V_o = f(V_i)$ for the forward (f_f; drawn in green) and backward inverter (f_b; drawn in blue) in the hold mode ($V_{en} = V_{DD}$). The crossing points mark the two stable configurations (dots) and the metastable one (star). Generating this graphic for various combinations of V_{in} and V_{en} then allows to depict the general behavior, i.e., the number of (meta)stable states and their relative values.

Within the storage loop, the forward path, i.e., the mapping from V_B to V_{out}, is solely determined by Inv_f (green inverter in Fig. 1) and thus independent of V_{en} and V_{in}. So its characteristics remains unchanged when altering V_{in} respectively V_{en}. Consequently the only remaining task is to evaluate the static characteristic of the backward path from V_{out} to V_B. It consists of the backward inverter with its static characteristic f_b, followed by the control block formed by the TGs.

To simplify the description of the latter, we model each TG as a voltage controlled resistor with a resistance in the range $[0, R]$ for some arbitrary R. This is possible since we are only interested in the static value of V_B and in this case, the TGs form a voltage divider. Consequently, the ratio of the resistances has to continuously change from 0 to ∞ and vice versa. Since the actual mapping is not important for our calculations we resorted to a simple linear approach, i.e., $R \cdot (1 - \frac{V_{en}}{V_{DD}})$ for the backward TG and $R \cdot \frac{V_{en}}{V_{DD}}$ for the forward one. The simulations in Section IV then, of course, use the real TG behavior and thus a more evolved dependency on V_{en}.

In the case of $V_{en} = V_{DD}$ the storage loop closes completely and disconnects the input, while the `Latch` becomes fully transparent for $V_{en} = V_{SS}$. For intermediate values of V_{en} we obtain a voltage divider that is characterized by

$$V_B = \frac{\overline{V_{en}}}{V_{DD}} \cdot V_A + \frac{V_{en}}{V_{DD}} \cdot V_C. \tag{1}$$

The first part of this sum constitutes an offset of V_B imposed by V_{in} (via V_A) and scaled by $\overline{V_{en}}$, while the second term expresses a compression of V_C based on V_{en}. Considering that $V_C = f_b(V_{out})$ is the output voltage of Inv_b, we can apply this scaling directly to f_b, resulting in a modified f_b'. Put simply, the backward path can be described by vertically scaling f_b and adding a voltage offset dictated by V_{in}. Both transformations are moderated by V_{en}.

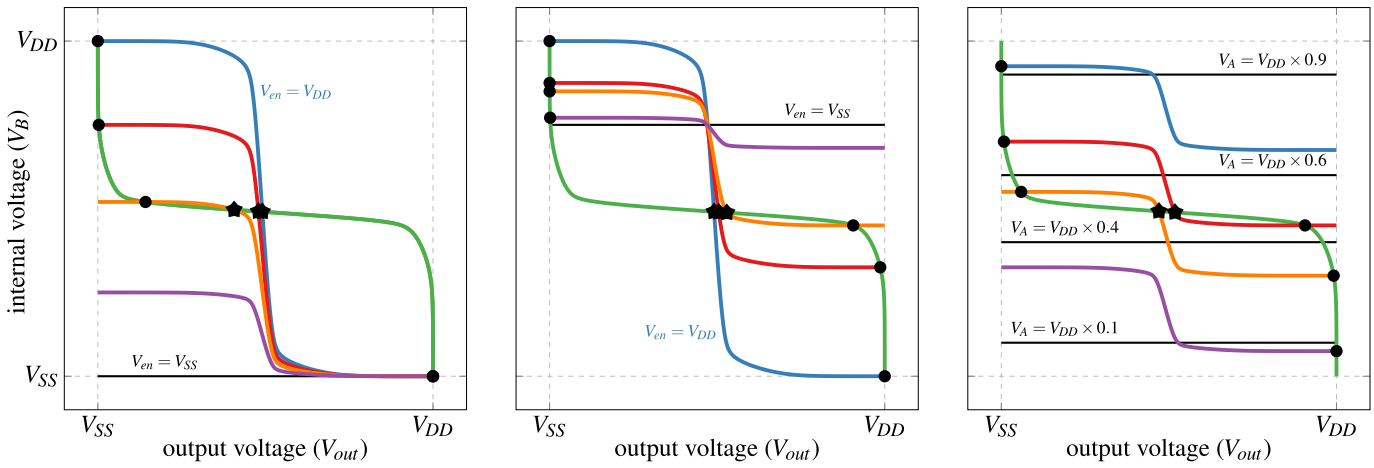
Based on this model we can now return to the graphical analysis and determine the (meta)stable points, this time using f_f and f_b', the transformed version of f_b. Theoretically, two observations are possible: (i) If f_f and f_b' cross only once then there is a single, stable configuration and thus a one-to-one mapping between in- and output. (ii) Otherwise exactly three crossings are observed. Interpreting the outer, stable ones as energy minima it becomes obvious that the inner one has to be metastable (energy maximum), due to the continuous properties of energy [18].

In the sequel we either pin V_{in} or V_{en} to a defined value, vary the other and observe the impact.

B. Varying V_{en}

Varying the enable signal effectively changes the amount of current Inv_in and Inv_b are able to propagate from/to V_B, where a rising value weakens the former and strengthens the latter. For our initial observations we set $V_A = V_{SS}$ and $V_{en} = V_{DD}$, in which case the `Latch` is in hold mode and the already known shape for f_b (blue line in Fig. 5a) is achieved. How does this situation change when V_{en} is reduced?

As stated before, a dropping V_{en} strengthens TG_f which, due to an internal value of $V_A = V_{SS}$, thrives to pull V_B low. Depending on the value of V_{out} (especially for low values) this leads to a driving conflict, as input and backward inverter are pulling in different directions. V_{en} simply spoken regulates the relative strengths and thus determines whether V_B is pulled more towards the one or the other direction. According to our findings above we model this behavior by compressing f_b in



(a) $V_A = V_{SS}$ (b) $V_A = \frac{3}{4}V_{DD}$ (c) $V_{en} = \frac{1}{4}V_{DD}$

Fig. 5. Intersections of the static characteristics for forward and backward path to identify (meta-)stable states for varying enable voltages (V_{en}) for two constant output values of the input inverter (V_A) in (a) and (b), as well as for varying input voltage (V_{in}) for constant V_{en} (c).

the y-direction. Note that for high values of V_{out} (for this particular V_A) both inverters pull towards the same value so no change can be observed there. Overall, the stable point at $V_{out} = V_{DD}$ remains fixed, while possible further crossing points are altered. Traces of f_b' for varying values of V_{en} are shown in Fig. 5a.

More specifically, the second stable point (initial value $V_{out} = V_{SS}$) increases with a decreasing V_{en}, while the metastable one decreases, i.e., they are approaching each other. As both coincide they vanish and thus eliminate the possibility for metastability altogether. From here onward we can observe the buffer-like behavior where V_{in} alone determines the (single) stable value of V_{out}: Further decreasing V_{en} compresses f_b even more until a horizontal line at $V_B = V_{SS}$ is achieved. Overall, reducing V_{en} thus causes one stable and the metastable state to merge leaving finally only a single stable configuration.

For internal values $V_A > V_{SS}$ a similar behavior can be observed. The main difference is that now both ends of f_b are compressed around the fixed point V_A. In detail both stable points are pulled towards V_A (since $V_{en} = V_{SS}$ results in a straight line) which causes the part with less distance to be compressed slower. As can be observed in Fig. 5b the overall behavior stays the same, with the difference that all (meta)stable points are altered. Nevertheless, still a stable and the metastable point merge for some V_{en}. For one very specific configuration of V_{in} and V_{en} all three states merge to a single stable value, which is equal to the initially metastable one.

C. Varying V_{in}

We can reuse the observations from varying V_{en} to analyze the behavior for a constant V_{en} and varying V_{in}: We saw that V_{en} governs the vertical compression of f_b, while V_{in} determines the fixed point and hence the vertical offset. For a constant V_{en} we thus get a unique f_b' moving up and down dependent on V_{in}, which is shown in Fig. 5c. By this movement different crossing points are achieved. For rather high/low values of V_A only one stable configuration is possible, while for intermediate values two stable and one metastable states are achieved.

For the shown compression we thus get properties known from an S/T: For input voltages close to V_{DD} or V_{SS} there is only a single stable solution for V_{out} with, hence, no potential for metastability. For the range in between, however, a memory loop behavior with three intersections, one of them being metastable, can be observed. For less compressed versions of f_b, always three crossings are assured and consequently, for all input values a memory loop behavior is shown. In contrast, strongly compressed versions always end up in a single crossing, which corresponds to a buffer.

This actually confirms the predictions we achieved in Section II. Decreasing V_{en} from V_{DD} to V_{SS} causes the memory loop to transform into an S/T and finally to a buffer, as we predicted. Consequently, we can deduce the surprising fact that a `Latch` can actually behave in three different fashions, solely depending on the value of V_{en}.

D. Calculating the Crossing Points

Although the described approach provides good explanations, concrete values are hard to extract from compressing and shifting graphical representations derived from SPICE simulations. For calculations, an analytic description of the inverter characteristics would be necessary, which is, due to varying operation regions of the transistors, not easily possible. Since we are only interested in a qualitative illustration of the `Latch` behavior we empirically fitted the static characteristic of an in inverter in our library by the function

$$V_{out}(V_{in}) = 0.5 \cdot (1 - \tanh(8 \cdot (2 \cdot V_{in} - 1))) \quad (2)$$

which we then used as approximation for f_f and f_b. The results achieved in this fashion (see Fig. 6) are not only very reasonable but, in general, confirm our observations presented

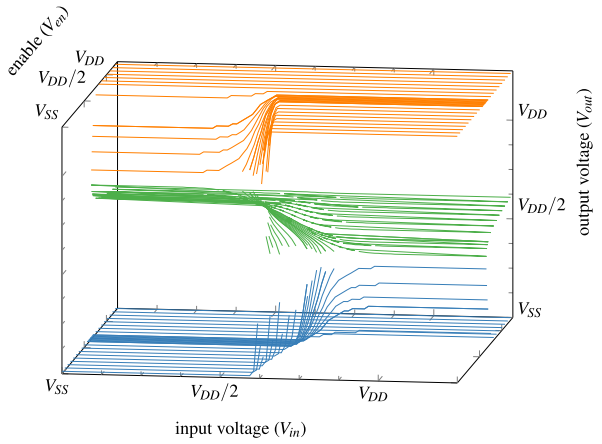


Fig. 6. 3D representation of the simple model showing (meta)stable lines for constant values of the enable voltage (V_{en}).

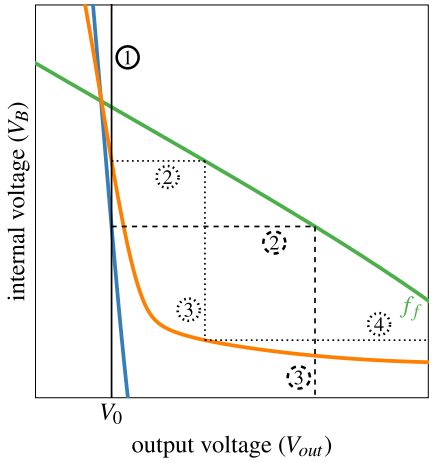


Fig. 7. Predicting the responsiveness r based on f_f and f_b.

so far. In fact, they only deviate marginally from the ground truth that will be derived through SPICE analysis in the following section.

E. Responsiveness r

In the introduction we already stated that the Mean Time Between Upset (MTBU) of a `Latch` follows an exponential curve MTBU$\sim \exp(t_{res}/\tau)$. This is based on the assumption that the metastable voltage resolves with the time constant τ in an exponential fashion. Maier et al. [17], however, recently reported that in real-world S/Ts the trajectories deviate slightly from an ideal exponential, making it impossible to determine a unique τ. Therefore the authors introduced the responsiveness $r(V_{in}(t), V_{out}(t))$, which allows to model the output voltage for a fixed input voltage as $V_{out}(t) = V_M \pm \exp(r(t) \cdot t)$ with V_M denoting the metastable voltage. Based on simulated output trajectories for $V_{in}(t) = V_1$ they calculated

$$r(V_1, V_{out}(t_0)) = \ln'\left(\left|V'_{out}(t)\right|\right)\Big|_{t=t_0} = \frac{V''_{out}(t)}{V'_{out}(t)}\Big|_{t=t_0}.$$

Note that we obtain $r = 1/\tau$ for a perfectly exponential trajectory with time constant τ.

In this paper we want to answer the question how the responsiveness changes during the metastability resolution of a `Latch`. To this end, let us recall that according to [6] the time constant τ, and thus also r, corresponds to (the inverse of) the gain/bandwidth product of the storage loop. While our static analysis cannot assess the bandwidth, whose impact will be analyzed during the discussion of the results in Section IV, we can observe the gain and draw some conclusions from that. Linearizing f_f and f_b around the metastable configuration $V_{out,m} = f_f(V_{B,m}) = f_f(f_b(V_{out,m}))$ as shown in Fig. 7 yields

$$V_{out}[n] = V_{out,m} - p \cdot (V_B[n-1] - V_{B,m})$$
$$V_B[n] = V_{B,m} - q \cdot (V_{out}[n] - V_{out,m})$$

to describe the trajectories of the signals as a sequence of steps. Note that the loop gain corresponds to $p \cdot q$ where both coefficients are, due to the amplification of the inverter, bigger than one. From the figure these values are hard to determine so a more straight forward figure of merit is the angle α in between the linearizations, which can be calculated as

$$\alpha = \arctan(q) - \arctan\left(\frac{1}{p}\right).$$

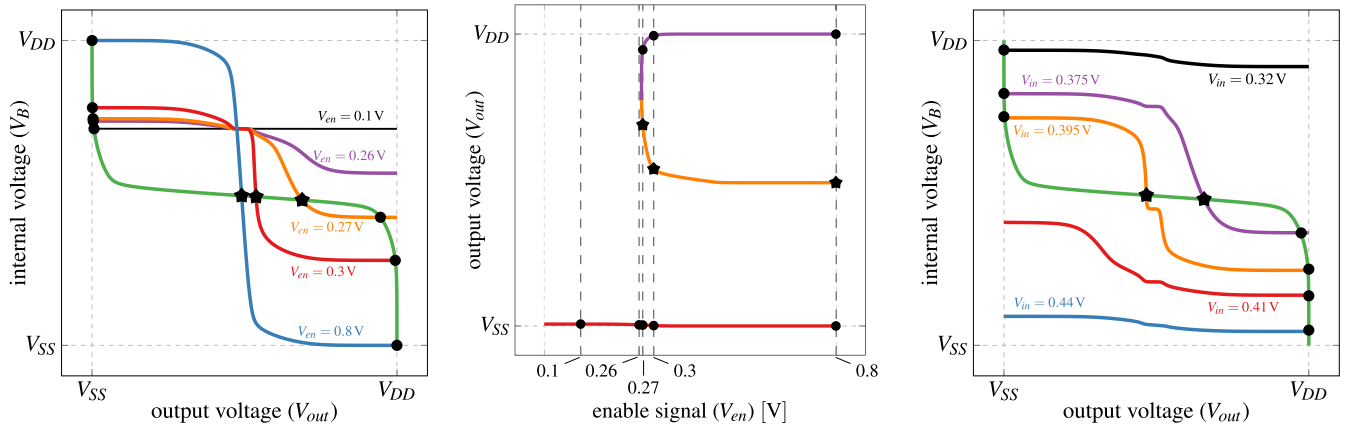
The bigger the angle the more voltage is gained in a single iteration, corresponding to a higher gain, higher responsiveness r and hence faster resolution.

Fig. 7 provides a graphical explanation. In this configuration we assume $V_{out}(0) = V_0$ to be slightly off the metastable point. This is the typical situation when metastability is resolving. With V_0 at its input the backward inverter sets V_B to a value which is determined by f_b. Here we evaluate a steep (▬) and shallow (▬) version. For the latter the slight deviation on V_{out} causes small but noticeable change on V_B relative to the metastable point (see 2 and dotted lines). Plugging this new V_B value into f_f finally results in a more pronounced increase in V_{out}, marked by 3. This value forms the starting point for the next round, yielding 4 and 5 (not shown). This process continues until V_{out} saturates.

For the steep version of f_b, and thus a higher responsiveness r, it can be seen that already the initial voltage change is much larger (see 2 and dashed lines) yielding a faster progress of the resolution towards saturation.

Clearly, this figure just serves as an illustration, making our prediction plausible, while assuming that the bandwidth will not change as significantly. Further note, that for simplicity our explanation has been focused on the slope of f_b: The more vertical f_b is, the better, since the vertical projections of V_{out} rapidly move to lower V_B. A similar argument can be made for f_f: The more horizontal f_f is, the faster the projections of a decreasing V_B to the right move towards increasing V_{out}.

Based on the previously presented estimations of f_b for varying V_{en} and V_{in} we receive the following predictions for r: In the case of constant input voltage but varying V_{en} (cf. Fig. 5a) the angle between f_b and f_f in the metastable point gets shallower with decreasing V_{en}. Thus we also expect a



(a) $V_{in} = 0.38\,\mathrm{V}$ (b) $V_{in} = 0.38\,\mathrm{V}$ (c) $V_{en} = 0.3\,\mathrm{V}$

Fig. 8. Analog simulation results for varying enable (V_{en}) and input voltage (V_{in}).

decreasing value of r. For constant enable input and varying V_{in} (cf. Fig. 5c) the angle is shallow for the first metastable states, then increases, and finally decreases again. Therefore a peak at around $V_{DD}/2$ is expected.

IV. Verification by Simulation

To verify the predictions presented in Section III we resort to analog SPICE simulations of a 15 nm Nangate Open Cell Library with FreePDK15™ FinFET models [24] ($V_{DD} = 0.8$ V) using Synopsys HSPICE (Version 2018.09-SP1). Note that we also ran our analysis for an older standard UMC 65 nm technology, which showed qualitatively the same results. Thus we limit ourselves to the smaller technology node here. Due to the very high precision demands of metastability investigations we refrained ourselves from measurements and instead fully focused on simulations.

We want to emphasize that simple `DC` simulations are sufficient to gather most of the required data. While this is trivially the case for f_f and f_b, Maier et al. [17] have shown that even the (meta)stable values of the S/T, and thus the `Latch`, can be derived this way. This is based on the key insight that for both stable and metastable states the internal electric currents have to perfectly compensate, since both can be maintained forever. Thus for initial values close to the desired states the *Newton-Raphson* algorithm, which is utilized in HSPICE to find valid `DC` configurations, automatically delivers very accurate results.

Naturally, the dynamic behavior of the `Latch` can not be covered well based on these static results. Running a characterization using transient simulations is, however, a near impossible task as the parameter space extends to the point where our choices would become somewhat arbitrary, very much dependent on specific circuit properties like parasitic capacitances, the input slope and even the past trajectories. Thus, multiple simulations for a single point in the 3D space would be necessary, whereat each would deliver differing results. Since our intention was to elaborate on the generic behavior – without claim for high (quantitative) accuracy, but instead with an intuition of the underlying effects – we restrict ourselves to the analysis of the responsiveness r.

A. Varying V_{en}

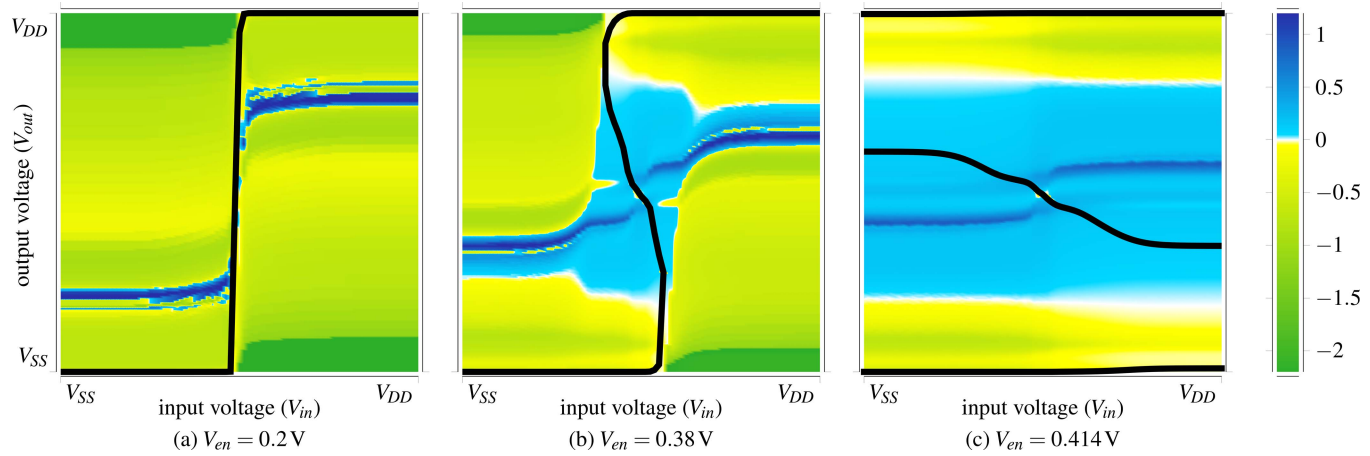
To compare model predictions and simulation results directly we start by determining the static characteristic f_b' and its crossing points with f_f as shown in Fig. 8a. Although we get qualitatively similar results (cf. Fig. 5b) there are some interesting deviations. Overall f_b is not merely compressed for $V_{en} < V_{DD}$ but actually deformed quite significantly. This is most pronounced around the value of V_A which corresponds to the chosen input value. In detail a short, almost horizontal segment can be observed which was not visible in the simplified model. On closer examination we were able to identify the nMOS transistor in $\mathrm{TG_b}$ on the feedback path as the main culprit: Thereby this small horizontal part marks the onset of conductance of the nMOS transistor. Since it operates in its saturation region, and so the delivered current is almost independent of the drain-source voltage, altering V_{out} does neither change the current through the TG nor, in consequence, the voltage at V_B. Similar disadvantageous effects due to the near-threshold operation of TGs have been reported in [23].

The flat part suggests another oddity: By an appropriate vertical movement it could be possible to achieve three intersections of f_b' and f_f in that region. Indeed we succeeded in finding such a constellation for $V_{in} = 0.39265$ V and $V_{en} = 0.2$ V. The achieved three (!) stable states are approximately at $(V_B, V_{out}) \in [(0.374, 0.633), (0.392, 0.403), (0.412, 0.149)]$ volts and the two (!) metastable ones approximately at $(V_B, V_{out}) \in [(0.391, 0.421), (0.398, 0.322)]$ volts. Even though setting up this situation required careful tweaking of the parameters, which suggests that it is unlikely to be encountered in practice, it is a very notable behavior for a "bi-stable" storage element that is generally assumed to have two stable states and one metastable state only.

Fig. 8b finally shows continuous traces for the (meta)stable states over V_{en}. The vertical lines mark the configurations that are shown in Fig. 8a. As predicted, the metastable and one stable state merge, leaving only the other stable configuration for low values of V_{en}.

B. Varying V_{in}

Pinning V_{en} to 0.3 V and varying V_{in} leads to the simulation results shown in Fig. 8c. Once again, a good qualitative



(a) $V_{en} = 0.2\,\mathrm{V}$ (b) $V_{en} = 0.38\,\mathrm{V}$ (c) $V_{en} = 0.414\,\mathrm{V}$

Fig. 9. Analog simulation results showing the (meta)stable line(s) (▬) and the responsiveness $f(r) = \mathrm{sgn}(r)\log_{10}(|r/A|+1)$.

agreement to our predictions from Section III can be observed, although f_b' shows significant variations among various values of V_{in}: For $V_{in} < 0.32\ V$ it is almost flat and sticks close to V_{DD}. Increasing V_{in}, and consequently decreasing V_A, eventually leads to an expansion, i.e., $V_B(V_{DD})$ drops quicker than $V_B(V_{SS})$, such that three crossing points are observed (one metastable and two stable configurations). The bigger V_{en}, the more pronounced this expansion becomes. Finally, f_b' gets flatter again, and consequently f_f is crossed only once. Considering the (meta)stable values when sweeping V_{in} clearly a Schmitt-Trigger like behavior can be recognized.

The significantly varying characteristic of the `Latch` for three values of V_{en} is also shown in Fig. 9. In contrast to earlier simulations, we resorted to determining a heatmap of the responsiveness r (a detailed discussion follows in Section IV-C) using the MEtastability Analysis Tool (MEAT)[4] here. The black lines thereby mark the (meta)stable states.

In Fig. 9a a nearly vertical trajectory is visible, i.e., a comparator-like behavior (we predicted this behavior in Section II at position ②). In this setup only stable configurations are possible. Further increasing V_{en} also increases the hysteresis width W resulting in an S/T as is shown in Fig. 9b.

Finally Fig. 9c shows the case where W got so big that the supply voltages are both already covered. By looking at the stable states only, this case could barely be distinguished from any other closed loop setup. However, the non-horizontal metastable line clearly reveals the intermediate value of V_{en} (cf. position ④ in Section II).

C. Responsiveness r

The simulation results for r shown in Fig. 9 were extracted from transient simulations. For a fixed V_{in} the initial configuration was chosen as far away as possible from the stable state, i.e., close to the metastable state resp. V_{SS} or V_{DD}. The responsiveness is then determined for equidistant output values as they are "passed by" the analog trajectory (for further details refer to [17]). This is a very delicate task, which explains the noisy looking data and occasional outliers. We also reused the scaling function $f(r) = \mathrm{sgn}(r)\log_{10}(|r/A|+1)$, with $A \approx 0.5\ \mathrm{ps}^{-1}$. This is necessary to increase the expressiveness of the plotted data, since r varies in a wide range. Nevertheless, the sign is an instrumental indicator and thus has to be preserved.

For regions with a single stable value (Fig. 9a and Fig. 9b outside the hysteresis) and far away from the latter, large negative numbers can be observed, which indicate that the waveform is already slowing down there. This corresponds to a trajectory that is the fastest at its beginning. As expected, moving towards the stable value increases r gradually, i.e., the trajectory slows down even further. In contrast to an exponential, however, a massive speed-up (dark blue bands) can be observed before reaching the stable value. The cause for this effect is $\mathrm{TG_b}$ on the feedback path, which stops conducting and thus allows for a much quicker change.

Within the hysteresis a totally different situation can be observed. There, actually, a positive r is dominant, meaning that V_{out} is thriving to escape the metastable state. Only rather close to the final stable value the trajectory starts to slow down ($r < 0$) and gradually approaches V_{DD} resp. V_{SS}. Note that even within the hysteresis a short significant increase of r is observable. In this case, however, it is caused by $\mathrm{TG_f}$ in the forward path, which stops conducting and thus allows a quick resolution of the memory loop.

From these results we can also verify that our theoretical predictions from Section III-E, which totally neglected the dynamic bandwidth of the circuit, were quite accurate. Indeed, the responsiveness is increasing with increasing V_{en}, which we already inferred from the higher derivatives of f_f and f_b' near the metastable state and thus higher angle α at which they cross. In general, the responsiveness inside the hysteresis is significantly higher (> 0) than outside (< 0). This represents the fact that in the first case the output trajectory escapes the metastable voltage while in the latter solely the final value is approached.

D. Unified Model

Probably the most comprehensive and insightful view on every aspect of the `Latch` behavior can be achieved by assembling all gathered data in a three dimensional plot of the $V_{in} - V_{out} - V_{en}$ space. The angle chosen in Fig. 10 clearly

[4] `https://github.com/jmaier0/meat`

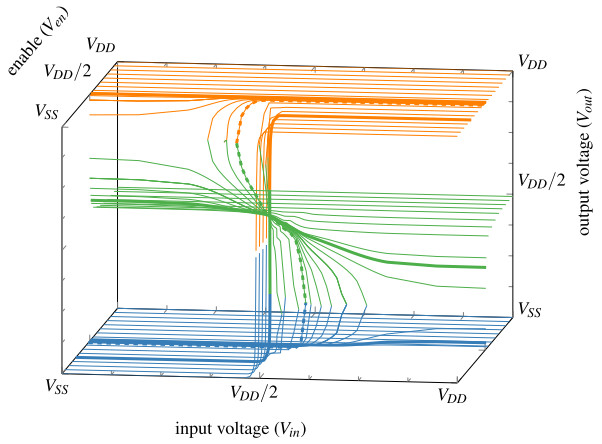


Fig. 10. 3D representation of the unified model showing (meta)stable lines for constant values of V_{en}. Bold lines mark the situations analyzed in Fig. 9.

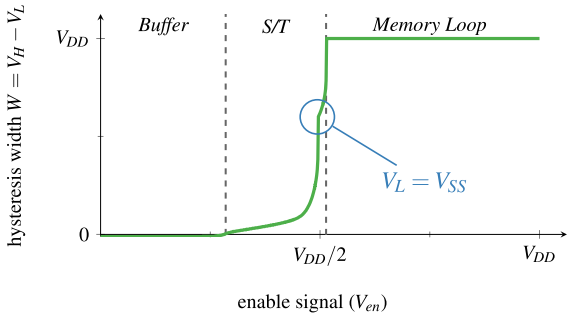


Fig. 11. Hysteresis width W with changing V_{en} indicating the different input-output behaviors of the Latch.

reveals the change of the hysteresis with V_{en}. Since a comprehensive understanding can only be gained by investigating the problem from various viewpoints we decided to provide the simulation results, in combination with a Python script for visualization, on the web [25]. The possibility to rotate and zoom on your own is essential to fully comprehend the partly very subtle effects.

Yet another illustration of the different Latch behaviors is shown in Fig. 11, where the hysteresis width $W = V_H - V_L$ over V_{en} can be observed. We extracted the data from DC simulations by starting at $(V_{in}, V_{out}) \in [(V_{SS}, V_{SS}), (V_{DD}, V_{DD})]$, and increasing/decreasing V_{in} until V_{out} differed from its initial value by at least $0.05 \times V_{DD}$. The corresponding value of V_{in} was then chosen as V_L respectively V_H. For low values of V_{en} a slightly negative W is visible, which represents the positive amplification of the buffer, whereat small (absolute) values correspond to high gain. In these cases a direct input-output mapping exists and thus excludes metastable states.

Increasing V_{en} eventually causes the hysteresis width to become zero (comparator) and then positive, marking the onset of S/T behavior. While, at first, a moderate increase is observable, W starts to change significantly faster around $V_{en} = V_{DD}/2$. This shows the high sensitivity of the transistor current with varying gate voltage in this range. Eventually $W = V_{DD}$ is achieved, meaning that the memory loop region is entered. Albeit the hysteresis width appears to stay constant for further increasing V_{en}, it actually gets even larger. Given that V_{in} has to stay within the supply rails, this does, however, not have any practical relevance, apart from the fact that the metastable voltage becomes more and more independent from V_{in} with increasing V_{en} (note carefully, e.g., that the metastable line is still not horizontal in Fig. 9c, as is often assumed for a bi-stable element).

We want to emphasize that V_L and V_H may grow at differing speed resulting in the unexpected situation that, for example, the memory loop can be set but not reset any more. More specifically in this case V_L has already reached a value $\leq V_{SS}$ while $V_H \leq V_{DD}$ still holds. Since we only simulated the range $[V_{SS}, V_{DD}]$ we pinned V_L in such a case to V_{SS}. In consequence the increase of the hysteresis is slowed down (see Fig. 11) as from there onward only V_H appears to be changing.

E. Generalization

The simulation results presented in this section have revealed that during its transition from transparent to hold mode the TG based Latch passes through an S/T operation region. We can use these insights do derive a very general conjecture: Every transition of a storage element from a combinational to a state-holding mode must be gradual. Consequently, it will experience an "intermediate" area of operation with a certain trend towards state holding combined with a trend towards following the input. This conflict introduces a hysteresis, i.e., S/T behavior, such that the state will only flip if the input change is large enough. Otherwise it will be retained.

The TG based Latch represents a special case since it has a separate input for controlling the driving strength ratio between forward an backward path. For all other storage elements this ratio is implicitly determined by the transistor sizings, e.g., in the case of the semi-static Muller C-element with staticizer [3]. This balance is well understood and a design parameter; in essence the sizing selects a vertical plane in Fig. 10 (one for constant V_{en}) that fits the task at hand.

V. Use Cases

We are optimistic that the insights gained in our analysis, i.e., that buffer, Latch and Schmitt-Trigger are actually tightly interconnected, can help to explain observed physical behavior and enable further improvements in the future. In this section we want to discuss some of our ideas in this regard.

A. Metastability Analysis

For past analyses of the Latch/flip flop the clock input was assumed to be controlled by a perfect transition with zero rise time. This is equivalent to jumping from the buffer directly to the memory loop behavior. Considering that the clock is typically the highest frequency signal in a system, with a signal shape that is often far from rectangular, the assumption of a perfect clock is highly optimistic. Our results, which provide a much more fine grained description of the Latch behavior especially in between transparent and hold mode,

could thus be a first step towards improving the metastability characterization and MTBU estimation.

The observed very tight connection between Latch and S/T makes us also optimistic that some of the rich research results from the former regarding metastability could be transferred to the latter.

Overall, our analyses enable a proper investigation regarding the consequences of imperfect clock transitions and answer questions like: What impact does the clock slope have on metastability in general and on the MTBU in particular? How does the resolution time depend on the shape of the clock signal? What is the impact of a pulse on the clock signal that does not reach full height? Here, e.g., our model gives insight to how such a pulse could make a Latch metastable, even if the data input is perfectly stable. Nevertheless, for a quantitative analysis, additional information, such as the specific trajectory of input and enable signal, are indispensable.

B. Behavioral Analysis

In our opinion, having this unified view of Latch, S/T and buffer has a beauty of its own. There has, e.g., always been some misconception around whether an S/T can actually become metastable. Our unified model presents an intuitive explanation that an S/T is a stateful element and hence metastability is an issue.

This also becomes obvious when comparing the input ranges leading to a metastable output. While the memory loop potentially experiences metastability for arbitrary input values, a buffer can only serve as a propagator, i.e., the input has to be metastable to observe malicious values at the output. The S/T is, once again, in between these extremes: While output metastability is still only possible for metastable inputs, and thus only metastability propagation is possible, the actual output value can not be determined based on the input value alone. Increasing the hysteresis width gradually changes this situation until eventually also input values considered as clearly HI or LO lead to a metastable output.

Another very important corollary we can derive from our analysis is that a single Latch is very versatile. It can either store a value, map the input directly to the output or imply a hysteresis with variable width. The behavior that is used at a specific point in time can thereby be controlled by a single terminal voltage. This enables the designer to adapt the circuit to the operation conditions at hand. A possible application is a communication channel. Depending on the noise level the hysteresis can be configured to achieve a clean signal. Such a device even outperforms adjustable hysteresis S/Ts, e.g., the one presented in [26], as it is also possible to switch to an amplifier mode or completely shut off the input signal, which might be beneficial in certain circumstances. Furthermore a Latch, or at least a flip flop, is a standard cell in each logic library and thus can be used out of the box. This renders complicated transistor sizing procedures unnecessary.

C. Behavioral Explanations

One major corollary of the analyses presented in this paper is a detailed description of the Latch while opening and closing. This enables us to analyze and explain already observed, yet not fully understood, behavior.

The analyses by Reiher and Greenstreet [23], which focused on the resolution behavior of a synchronizer (four Latches in succession), provide such an example. In a nutshell, the authors discovered that the responsiveness r, denoted as the *instantaneous gain* $\lambda(t)$ in their paper, decreases during a clock transition, i.e., that the metastable state is resolved slower. This can be well explained by the simulation results shown in this paper, more specifically by the reduced r for intermediate values of V_{en}. On the foundation of our model one might even be able to calculate, in a next step, *how much* the resolution time changes for a given non-perfect clock slope.

VI. Conclusion and Future Work

In this paper we thoroughly investigated the behavior of a D-latch for analog data and enable input values. We were able to qualitatively predict the behavior uniformly based on static DC considerations which we later confirmed by analog SPICE simulations. Overall the D-latch can either act as a buffer, mapping input values directly to the output, a Schmitt-Trigger, whose hysteresis is continuously adjustable (even a zero hysteresis comparator is possible), or a storage loop. The gradual change in behavior is thereby controlled by the enable input voltage.We have elaborated a unified model for D-latch and Schmitt-Trigger that reflects this property. Notably, we did not use an exotic circuit for this analysis but essentially a simple inverter loop controlled by transmission gates, and we have argued that the observed behavior is, in principle, implementation-independent.

In our future work we will extend our results to different D-latch implementations and observe the qualitative as well as quantitative changes. A very interesting avenue would also be to look into how non-zero transition times of the enable signal impact the Mean Time Between Upset, given that the generally used prediction model does not consider this imperfection. Furthermore we are planning to investigate for which value ranges of the signals controlling the transmission gates (when they are not complementary), our evaluations are still valid. At a certain point, all the inverters would only be operating in their sub-threshold region. What behavior can be expected in these situations and could it be leveraged for certain purposes?

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