Ultra-Low-Power Sub-1 V 29 ppm/°C Voltage Reference and Shared-Resistive Current Reference

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***Abstract*— This paper presents a curvature-compensated sub-1V voltage reference (VR) and a shared-resistive nanoampere current reference (CR) in a 130 nm CMOS process. The CR is used to generate a bipolar junction transistor complementary-to-absolute-temperature voltage, which is summed up with a proportional-to-absolute-temperature voltage generated using a summing network of PMOS gate-coupled pairs. The measured output voltage and current references from 10 chips (V_{REF} and I_{REF}) at room temperature are 469 mV and 1.86 nA, respectively. The measured average temperature coefficient of V_{REF} and I_{REF} are 29 ppm/°C and 822 ppm/°C over a temperature range from −40°C to 120°C. The minimum supply voltage of the voltage-current reference is 0.95 V, and the total power consumption is 30 nW.**

***Index Terms*— Voltage reference, curvature compensation, temperature compensation, high-precision, sub-1V, current reference, sub-threshold CMOS design, ultra-low-power, voltage-current reference.**

I. Introduction

ULTRA-LOW-POWER solutions are required in order to sustain the ever-increasing demand for wireless sensor nodes. The vast network of battery-operated low-power wireless sensor nodes is constrained by the battery usage [1], [2], [3]. The battery usage can be reduced by a radiofrequency (RF) powered wake-up receiver (WuRx). It ensures that the wireless sensor node stays in a deep-sleep state unless activated by a wake-up signal [4], thus increasing the lifetime of the battery.

Fig. 1 shows the architecture of an RF-powered WuRx. The analog frontend of the WuRx consists of an RF-DC converter, which harvests the incoming RF energy to DC energy [5]. The signal processing system includes an envelope detector, a comparator, an oscillator, and a digital processor, which operate in a low-voltage domain to reduce the power consumption. The power management system consists of a voltage reference (VR), a current reference (CR), a power-on reset (POR), and a low-dropout regulator (LDO) [4]. The strict performance requirements of the signal processing system in a WuRx demand an accurate low-power temperature-compensated voltage-current reference (VCR) with a low supply voltage startup [6], [7]. The nanowatt power budget adds to the challenge of designing a robust and accurate VCR. This work presents an ultra-low-power VCR shown in Fig. 2, which is an integral part of a WuRx.

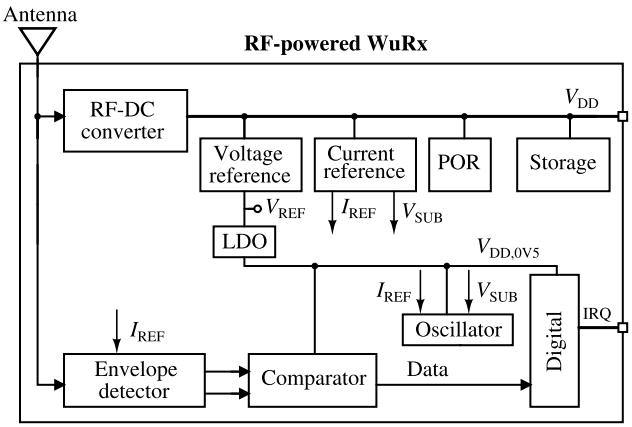

Fig. 1. RF-powered WuRx including an RF-DC converter supplying a nanowatt voltage reference and current reference.

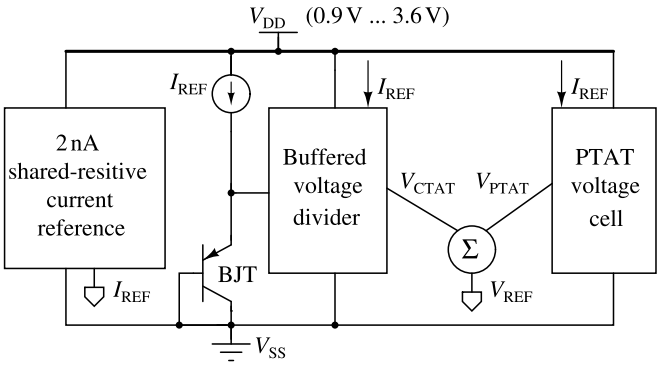

Fig. 2. Architecture of the proposed voltage-current reference VCR [8].

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A classical approach to achieving a temperature-compensated VR is by combining a proportional-to-absolute-temperature (PTAT) voltage and complementary-to-absolute-temperature (CTAT) voltage circuits [8], [9], [10]. VR circuits can be broadly categorized into bandgap-based references, CMOS-based references, and hybrid references, which combine bandgap-based and CMOS-based reference circuits. The bandgap reference (BGR) is a conventional VR with a highly accurate reference voltage and low process corner and temperature variation [11]. Sub-BGR designs have achieved a sub-1V VR for a low power consumption and a considerable accuracy [11], [12], [13]. The BGR-based VRs have a minimum supply voltage of roughly 0.9 V owing to the forward bias voltage of a bipolar junction transistor (BJT) [14].

Recently, sub-threshold CMOS-based VRs have received much attention because of their low supply voltage operation and ultra-low-power consumption [10], [14], [15], [16], [17]. The ultra-low-power CMOS-based VRs employ native MOS devices where the leakage current determines the output voltage V_{REF}. The dependence on the threshold voltage V_{TH} of a MOS transistor in this topology results in an inevitable sensitivity to process corner variations [15], [16], [17]. Therefore, BGR-based designs are still the first choice to generate high-precision VRs for energy harvesting systems.

A temperature-compensated CR is also a fundamental building block of an RF-powered WuRx (see Fig. 1). Recent works [18], [19], [20], [21], [22], [23], [24], [25], [26], and [27] have presented nanowatt CRs where the circuits make use of the sub-threshold operation of the transistors. They are broadly grouped into three categories: β-multiplier based CRs [18], [19], [20], zero-temperature coefficient (ZTC) voltage-based CRs [23], [24], [25], and CRs obtained by dividing a PTAT or CTAT voltage reference by a PTAT or CTAT resistance [26], [27]. The β-multiplier CR is the simplest CR with a well-defined bias current. Modified versions of β-multiplier CRs in [18] a nd [19] achieve a good temperature coefficient (TC) with a requirement of large resistors to generate nanoampere current. On the other hand, the ZTC voltage-based CRs are highly prone to process variations [24], [25]. The third category CRs in [26] and [27] generate a nanoampere output current at the cost of a high minimum supply voltage of 1.3 V. Overall, area-optimized versions of β-multiplier CRs are advantageous for due to the design simplicity and good performance for ultra-low-power designs.

This paper introduces a novel curvature-compensated sub-1V VR and a shared-resistive nanoampere CR with an overall power consumption of 30 nW. The proposed VCR shown in Fig. 2 includes a standalone 1.86 nA CR which supplies the bias current I_{REF} required to generate the CTAT and PTAT voltage components. The CTAT and the PTAT voltage components are summed up to generate the curvature-compensated output V_{REF}.

This paper is an extended version of [8], with an improved VCR which works for a wider temperature range from −40°C to 120°C and a higher supply voltage range from 0.95 V to 3.6 V. The extended paper addresses the curvature compensation of V_{REF} for the wide temperature range using design parameters. The paper additionally includes a trimming circuit built to optimize the TC of the VR and minimize the spread of the CR, analysis of the supply voltage fluctuations, overall power consumption, chip-measurement results, and a comparison with the latest published results. The paper is organized as follows: Section II describes the operation principle and the design of the CR. Section III describes the design procedure of the curvature-compensated VR. Section IV presents the measurement results and the comparison with the state of the art. Section V concludes the work.

II. Shared-Resistive Current Reference

The proposed VCR has been designed in an in-house modified 130 nm CMOS technology. The initial design, however, was done in a primitive n-well 130 nm CMOS process where the NMOS transistors have no possibility of a buried p-well. For the sake of backward compatibility, most of the NMOS transistors in the VCR design have a bulk connection to ground.

The low-voltage CR is built for an RF-powered WuRx with strict requirements for low power consumption and a reliable startup [2]. The CR exploits an improved version of a beta-multiplier current reference by combining PTAT and CTAT currents to generate a temperature-compensated reference current. Specific contribution of this CR is the design of a shared-resistive design which generates an additional sub-50 mV voltage reference V_{SUB}. The transistors are biased to operate in the sub-threshold region to ensure the low-power operation. The drain-source current I_{DS} in the sub-threshold region [28] and the drain-source resistance R_{DS} in the sub-threshold region can be written as:

$$I_{\mathrm{DS}} = \frac{W}{L}\mu_{\mathrm{n}} C_{\mathrm{OX}} (n-1) V_{\mathrm{T}}^2 \, \mathrm{e}^{\frac{V_{\mathrm{GS}}-V_{\mathrm{TH}}}{nV_{\mathrm{T}}}} \left(1 - \mathrm{e}^{\frac{-V_{\mathrm{DS}}}{V_{\mathrm{T}}}}\right) \quad (1)$$

$$R_{\mathrm{DS}} = 1/(\partial I_{\mathrm{DS}}/\partial V_{\mathrm{DS}}) = \frac{V_{\mathrm{T}} \left(\mathrm{e}^{\frac{V_{\mathrm{DS}}}{V_{\mathrm{T}}}} - 1\right)}{I_{\mathrm{DS}}} \quad (2)$$

where W/L is the transistor aspect ratio, μ_{n} is the mobility, C_{OX} is the oxide capacitance, n is the sub-threshold slope, V_{T} is the thermal voltage, V_{GS} is the gate-source voltage, V_{TH} is the threshold voltage, and V_{DS} is the drain-source voltage of the transistor. The dependence of R_{DS} on I_{DS} in (2) highlights the high-nonlinearity of a MOS transistor operating in the sub-threshold region.

A conventional temperature-compensated nanoampere CR combines a PTAT current β-multiplier circuit [28], [29] (see Fig. 3a, Fig. 3b) and a V_{GS}/R circuit [30] to generate a CTAT current I_{CTAT} (see Fig. 3c). The area-effective resistorless β-multiplier in Fig. 3a is widely used in microampere CRs, where the MOS transistor is biased in the linear region. However, the deployment of the MOS transistor in the sub-threshold region as a resistor brings a non-linear temperature dependence (see (2)). Unlike [30], the proposed CTAT circuit in Fig. 3c uses the PTAT current (see Fig. 4b) as a bias current for the transistor MN_2. The temperature dependence is highlighted in the schematic simulation results in Fig. 3d, which show the generated current I_{PTAT} versus temperature for the resistorless β-multiplier and the standard β-multiplier. The standard β-multiplier requires a poly-resistor

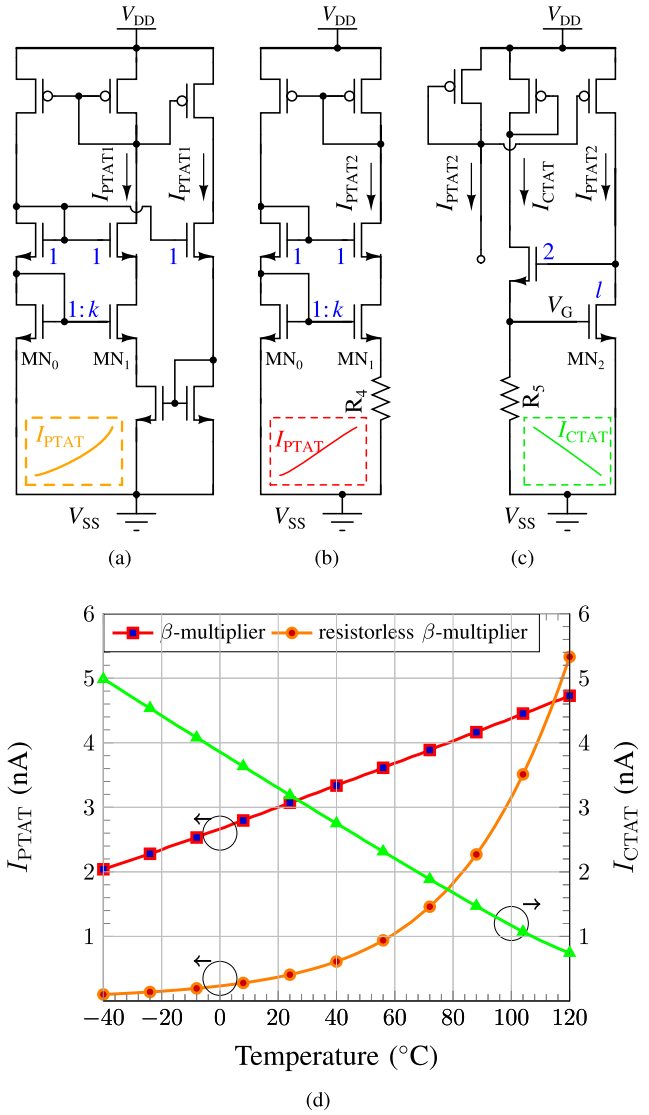


Fig. 3. (a) Resistorless β-multiplier CR [28], (b) β-multiplier CR [29], (c) V_{GS}/R CR [30] to generate I_{CTAT}, and the (d) simulated current versus temperature for the topologies (k = 6, l = 22).

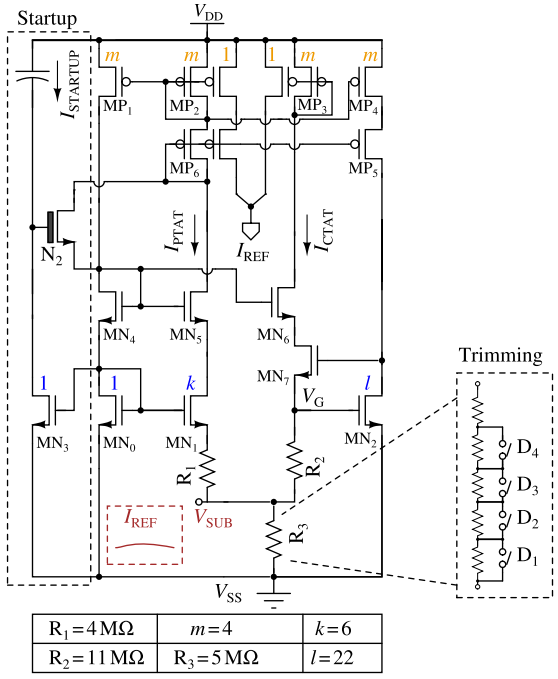
which occupies a significant area for a nanoampere I_{PTAT} generation. The generated current I_{CTAT} in the V_{GS}/R circuit is plotted alongside in Fig. 3d.

The proposed CR is based on a combination of the I_{PTAT} generator in Fig. 3b and the I_{CTAT} generator in Fig. 3c. The temperature compensation of the CR is done by the mutual compensation of the temperature dependence of I_{PTAT} ($\partial I_{PTAT}/\partial T$) and I_{CTAT} ($\partial I_{CTAT}/\partial T$). The PTAT current generator in Fig. 3b has equal currents flowing through the transistors MN_0 and MN_1. As a result, one can write the following expression connecting MN_0 and MN_1 [18]:

$$\Delta V_{GS} - \Delta V_{TH} \approx n V_T \ln(k) \tag{3}$$

where ΔV_{TH} is the difference between the threshold voltages of MN_0 and MN_1 arising because of the body effect, and k is the transistor multiplier ratio between the transistors MN_1 and MN_0. ΔV_{TH} can be expressed as [31]:

$$\Delta V_{TH} = \gamma\left(\sqrt{(\phi_S)} - \sqrt{(\phi_S + V_{S1})}\right) \approx \frac{\gamma}{2\sqrt{\phi_S}} \Delta V_{GS} \tag{4}$$



$R_1 = 4\,M\Omega$	$m = 4$	$k = 6$
$R_2 = 11\,M\Omega$	$R_3 = 5\,M\Omega$	$l = 22$

Fig. 4. Schematic of the nanoampere shared resitive CR including the startup circuit. The CR also generates a sub-50 mV reference voltage V_{SUB}.

where γ is the body bias coefficient, ϕ_S is the surface potential, and V_{S1} is the source voltage of MN_1. The resistor R_4 connected between V_{S1} and V_{SS} generates a PTAT current I_{PTAT}. I_{PTAT}, derived from (3) and (4), and it's first-order temperature coefficient $\partial I_{PTAT}/\partial T$ can be simplified and expressed as:

$$I_{PTAT} = \frac{n V_T \ln(k)}{R_4} \frac{1}{1 - (\frac{\gamma}{2\sqrt{\phi_S}})} \tag{5}$$

$$\frac{\partial I_{PTAT}}{\partial T} = \frac{1}{1 - (\frac{\gamma}{2\sqrt{\phi_S}})} \frac{n \ln(k)}{R_4} \frac{\partial V_T}{\partial T} - \frac{I_{PTAT}}{R_4} \frac{\partial R_4}{\partial T}$$

$$= I_{PTAT}\left(\frac{1}{T} - \frac{1}{R_4} \frac{\partial R_4}{\partial T}\right) \tag{6}$$

I_{CTAT} flows through R_5 across the voltage V_G. The CTAT current I_{CTAT} and it's first-order temperature coefficient $\partial I_{CTAT}/\partial T$ are [30]:

$$I_{CTAT} = \frac{V_G}{R_5} \tag{7}$$

$$\frac{\partial I_{CTAT}}{\partial T} = \frac{1}{R_5} \frac{\partial V_G}{\partial T} - \frac{I_{CTAT}}{R_5} \frac{\partial R_5}{\partial T} \tag{8}$$

A poly-resistor is chosen instead of a diffusion resistor due to its higher sheet resistance. The p+ poly-resistor R_4 in the design has a typical PTAT behavior of less than 500 ppm/°C [31]. As a result, the dominant terms in (6) and (8) are the first terms $I_{PTAT}/T \approx \frac{n V_T \ln(k)}{T * R_4}$ and $(1/R_5)(\partial V_G/\partial T)$, respectively. $\frac{\partial V_G}{\partial T}$ can be written from (1) as:

$$\frac{\partial V_G}{\partial T} = \frac{\partial V_{TH}}{\partial T} + \frac{\partial (n V_T \ln \frac{I_{PTAT2}}{K1\ V_T^2})}{\partial T}$$

$$= \frac{\partial V_{TH}}{\partial T} + \frac{nV_T \ln\frac{I_{PTAT2}}{K1\ V_T^2}}{T} + \frac{nV_T}{I_{PTAT2}}\frac{\partial I_{PTAT2}}{\partial T} - \frac{n\,V_T}{2\,T}$$
$$= \frac{\partial V_{TH}}{\partial T} + \frac{nV_T \ln(\frac{I_{PTAT2}}{K1\ V_T^2} - 0.5)}{T} + \frac{nV_T}{I_{PTAT2}}\frac{\partial I_{PTAT2}}{\partial T} \quad (9)$$

where $K1 = \frac{W}{L}\mu_n C_{OX}(n-1)$, and I_{PTAT2} is the drain-source current of MN_2. Combining (8) and (9), $\partial I_{CTAT}/\partial T$ can be rewritten as:

$$\frac{\partial I_{CTAT}}{\partial T} = \frac{1}{R_5}\frac{\partial V_{TH}}{\partial T} - \frac{I_{CTAT}}{R_5}\frac{\partial R_5}{\partial T} + \frac{nV_T \ln(\frac{I_{PTAT}}{K1\ V_T^2} - 0.5)}{R_5\ T} + \frac{nV_T}{R_5\ I_{PTAT}}\frac{\partial I_{PTAT}}{\partial T} \quad (10)$$

Depending on the substrate doping level and the oxide thickness of a transistor, $\partial V_{TH}/\partial T$ is between $-3\,\text{mV/°C}$ and $-0.5\ \text{mV/°C}$ [32], resulting in a strong CTAT behavior of the first term $\frac{1}{R_5}\frac{\partial V_{TH}}{\partial T}$ in (10). The third and fourth terms of $\partial I_{CTAT}/\partial T$ in (10) contribute to a small PTAT behavior. The second term $\frac{-I_{CTAT}}{R_5}\frac{\partial R_5}{\partial T}$ in (10) has a CTAT behavior that reduces with increasing temperature due to the dependence on the term I_{CTAT}. This causes a mild slope reduction of the I_{CTAT} curve at higher temperatures as seen in Fig. 3d. Overall, I_{PTAT} and I_{CTAT} temperature curves have a strong linear behavior (see Fig. 3d). This is attributed to the dominant first-order temperature coefficients $I_{PTAT}/T \approx \frac{nV_T\ln(k)}{T*R_4}$ in (6) and $\frac{1}{R_5}\frac{\partial V_{TH}}{\partial T}$ in (10). The proposed CR is designed by combining the PTAT and CTAT sub-circuits and matching the dominant first-order temperature coefficients.

The reference current I_{REF} is generated by combining a fraction of the reference current I_{PTAT} and I_{CTAT}, and mutually compensating $\partial I_{PTAT}/\partial T$ and $\partial I_{CTAT}/\partial T$. The fractional summing of the currents is achieved using a current mirror ratio of 4 (see Fig. 4).The overall temperature dependence of $I_{REF} = (I_{PTAT} + I_{CTAT})/4$ from (6) and (10) depends on technology parameters such as V_{TH}, the sub-threshold slope factor n, the poly-resistors R_4 and R_5, and the drain-source current of MN_2 (I_{PTAT}). The most significant contributing factor of $\frac{\partial I_{CTAT}}{\partial T}$ is $\frac{1}{R_5}\frac{\partial V_{TH}}{\partial T}$ and of $\frac{\partial I_{PTAT}}{\partial T}$ is $\frac{nV_T\ln(k)/T}{R_4}$. For the given design, the first-order temperature compensation of I_{REF} requires a ratio $R_5/R_4 = 2.75$. I_{PTAT} is adjusted to fine-tune the overall temperature dependence of I_{REF}. For a poly-resistor width of 300 nm, this implementation would require a large $0.02\,\text{mm}^2$ area for $R_5/R_4 = 39\,\text{M}\Omega/13\,\text{M}\Omega$ to generate a 2 nA [33]. A $0.02\ \text{mm}^2$ resistive area has an associated bottom-plate parasitic capacitance with respect to the substrate in the order of $60\,\text{aF}/\mu\text{m}^2 * 0.02\ \text{mm}^2 = 1\,\text{pF}$ [34]. The CR is designed for an RF-powered WuRx whose harvested output voltage has fast transients at high input RF power levels ($\Delta V_{DD}/\Delta t = 10^5\,\text{V/s}$) [2]. This fast transient at V_{DD} causes a false startup wherein the bias current is determined by the low-impedance path of the parasitic bottom-plate capacitance of the poly-resistor. Hence, it is critical to minimize the overall resistive area and its associated parasitic capacitance.

The proposed CR in Fig. 4 addresses the limitation of the large resistive area by combining I_{PTAT} and I_{CTAT} across a shared resistor R_3. The shared-resistive path for the currents also generates a first-order temperature-compensated voltage drop $V_{SUB} = (I_{PTAT} + I_{CTAT})R_3$. Equations (3) and (7) can be rewritten for Fig. 4 as:

$$nV_T \ln(k) = I_{PTAT}R_1 + V_{SUB} \quad (11)$$
$$V_G = I_{CTAT}R_2 + V_{SUB} \quad (12)$$

By maintaining the same resistor ratio, the resistors in Fig. 4 are now $R_2/R_1 = 11\,\text{M}\Omega/4\,\text{M}\Omega$. The improved design in Fig. 4 compared to the combined circuits in Fig. 3b and Fig. 3c helps achieve a $0.012\ \text{mm}^2$ area with a 60% reduction of the overall resistive-network area for a similar performance. Furthermore, the CTAT current V_{GS}/R circuit is dependent on the absolute value of V_{TH} of MN_2 in Fig. 4. The 4-bit digital trimming circuit shown in Fig. 4 helps compensate for the variation of V_{TH} (MN_2) and poly-resistors across process corners by shunting the bank resistors. The single trim-resistors' exact value was found during the design optimization process in the Cadence Virtuoso environment. The CR is designed for a supply voltage range from 1 V to 4 V. Cascode transistors in the current mirrors help to increase the output resistance and reduce the channel length modulation effect of the current mirror transistors. It helps to increase the line sensitivity of the CR against supply voltage variations at the cost of an increased voltage headroom for the cascode transistors.

The beta-multiplier PTAT circuit is self-biasing and has two stable operating points: the desired one and the unwanted one, where no current flows [29]. The implementation of the required startup circuit is shown in Fig. 4. The medium-volt thicker gate-oxide transistor N_2 with a $V_{TH} > 0.6\,\text{V}$ has been used in the startup circuit. It turns on as soon as there is sufficient gate-source voltage, resulting in the gate node of MP_6 being pulled down to start the flow of current through the CR. This turns on the transistor MN_3, which eventually pulls down the gate node of N_2 towards the ground V_{SS}. The medium-volt startup transistor N_2 is dimensioned such that the worst-case leakage current during the off state is in pA range. The low leakage current helps to ensure that the startup circuit is completely turned off once the CR is operational.

A. Simulation Results

The output current $I_{REF} = (I_{PTAT} + I_{CTAT})/4$ was set to 2 nA at 27°C. Fig. 5 shows the output I_{REF} and the normalized sub-50 mV reference voltage V_{SUB} over temperature variation, as seen in post-layout simulation results. The output I_{CTAT} decreases with increasing temperature. It reaches a minimum saturation value at 60°C. At this point, the regulation loop of MN_2 and MN_7 (see Fig. 4) ensure that a minimum I_{CTAT} flows through the transistor MN_7. As a result, the output I_{REF} starts to increase at temperatures higher than 60°C. The Monte-Carlo distribution of I_{REF} is shown in Fig. 6. The 2 nA output current I_{REF} has an average TC-I_{REF} of 530 ppm/°C. The I_{REF} σ/μ spread of 11% as seen in Fig. 6a can be attributed to the variation of the poly-resistors and the dependence on the threshold voltage of transistor MN_2 (see Fig. 4) to generate the CTAT current I_{CTAT}. The poly-resistors suffer from a typical

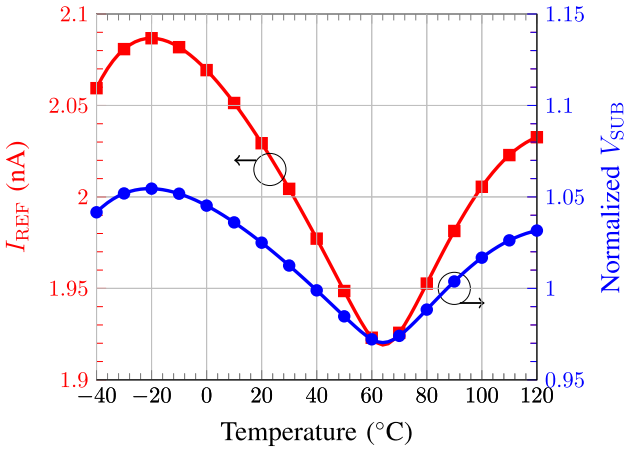


Fig. 5. Post-layout simulated output current I_{REF} and normalized sub-50 mV reference voltage V_{SUB} versus temperature (simulation details: corner = nom).

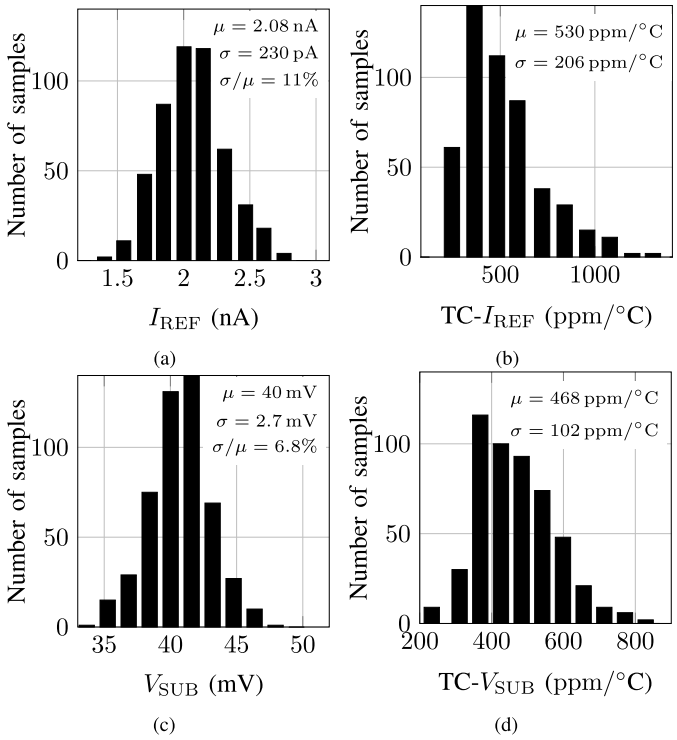


Fig. 6. Monte-Carlo post-layout simulation of (a) I_{REF}, (b) TC-I_{REF}, (c) sub-50 mV reference voltage V_{SUB}, and (d) TC-V_{SUB} (simulation details: trimming code = 0010, runs = 500).

3σ variation of +/- 20%. The output V_{SUB} with a μ of 40 mV and σ of 2.7 mV has a good mean-TC of 468 ppm/°C, as seen in Fig. 6. The reference voltage V_{SUB} is used as a reference input for the relaxation oscillator in the RF-powered WuRx in Fig. 1.

III. Sub-1 V Voltage Reference

The RF-powered WuRx in Fig. 1 requires a sub-1 V VR which is critical for the analog/mixed-signal circuits operating in a 0.5 V low-voltage domain. The proposed curvature-compensated sub-1 V VR generates an output V_{REF} by summing a CTAT voltage V_{CTAT} and a PTAT voltage V_{PTAT}, as shown in Fig. 7. The 2 nA reference current I_{REF}, presented in Sec. II is used for the generation of V_{CTAT} and V_{PTAT}. This VR mainly targets on optimizing the TC by proposing a second-order effect analysis of V_{CTAT} and V_{PTAT}. Specific contributions of this work are: 1) Design of a VR whose temperature compensation is predominantly dependent on design parameters, which helps to easily port the VR design to other CMOS technology nodes; 2) A low power sub-threshold design approach wherein the PTAT generator cells [36] are connected in a unique current and voltage summing series formation; 3) The VR design has a very high robustness against fluctuations in the bias current and process corner variations. The temperature compensation of V_{REF} is done by the mutual compensation of the first-order temperature dependence terms ($\partial V_{CTAT}/\partial T$, $\partial V_{PTAT}/\partial T$) and the second-order temperature dependence terms ($\partial^2 V_{CTAT}/\partial T^2$, $\partial^2 V_{PTAT}/\partial T^2$).

The CTAT voltage $V_{CTAT} = V_{BE}/3$ is generated by the base-emitter voltage V_{BE} of the vertical PNP-transistor Q_1, connected to a triple-well NMOS-diode voltage divider [11]. The output $V_{BE}/3$ of the voltage divider is connected to a unity gain buffer to avoid loading the node. The current consumption of the unity gain buffer is 2 nA. A 100 fF capacitor C_C improves the stability of the unity gain buffer. The CTAT voltage V_{CTAT}, it's first-order temperature dependence term $\partial V_{CTAT}/\partial T$, and it's second-order temperature dependence term $\partial^2 V_{CTAT}/\partial T^2$ can be modeled as [35]:

$$V_{CTAT} = \frac{V_{BE}}{3} = \frac{1}{3}(V_{BGR} + V_T \ln[\frac{I_C}{T^\alpha}\frac{E}{}]) \quad (13)$$

$$\left.\frac{\partial V_{CTAT}}{\partial T}\right|_{I_C} = \frac{1}{3}\left.\frac{\partial V_{BE}}{\partial T}\right|_{I_C} = \frac{V_{BE} - V_{BGR} - \alpha V_T}{3T} \quad (14)$$

$$\left.\frac{\partial^2 V_{CTAT}}{\partial T^2}\right|_{I_C} = \frac{1}{3}\left.\frac{\partial^2 V_{BE}}{\partial T^2}\right|_{I_C} = \frac{1}{3}(\frac{1}{T}\frac{\partial V_{BE}}{\partial T} - \frac{V_{BE}}{T^2}) \quad (15)$$

where E is a technology constant parameter, $\alpha = 4 - n$, $V_{BGR} = 1.205$ is the bandgap voltage of silicon at 0 K, and I_C is the temperature-compensated BJT collector current. Assuming a typical $V_{BE} = 600$ mV, $\alpha = 3.2$, and $T = 300$ K, (14) can be approximated as:

$$\left.\frac{\partial V_{CTAT}}{\partial T}\right|_{I_C} = -0.75\,\text{mV/K} \quad (16)$$

$\partial V_{CTAT}/\partial T$ as shown in (14) and (16) has a typical-negative value, and it depends on the technology parameters α and V_{BE}. $\partial V_{CTAT}/\partial T$ can be modified by adjusting the current I_C dependent term V_{BE} (see (1)). The second-order term $\partial^2 V_{CTAT}/\partial T^2 \approx -4\,\mu\text{V/K}^2$ depends on the absolute value of V_{BE} (see (15) and (16)).

The compensation of both first-order and second-order temperature dependences of V_{CTAT} is achieved using a PTAT voltage reference V_{PTAT}. The PTAT voltage in conventional BGR-based circuits is generated using bipolar PNP transistors and resistors [31]. However, the nanoampere power budget of the VR requires the usage of large resistors. As an alternative, gate-coupled PTAT generator cells [36] are used in a series connection formation to achieve a low-power V_{PTAT}. The PTAT cells include unit-cell transistors with multiplier ratio m. Every gate-coupled PTAT cell in Fig. 7 generates a drain-to-source voltage $V_{DS,i}$ across transistor N_i ($i = 1, 2, 3, 4, 5, 6$).

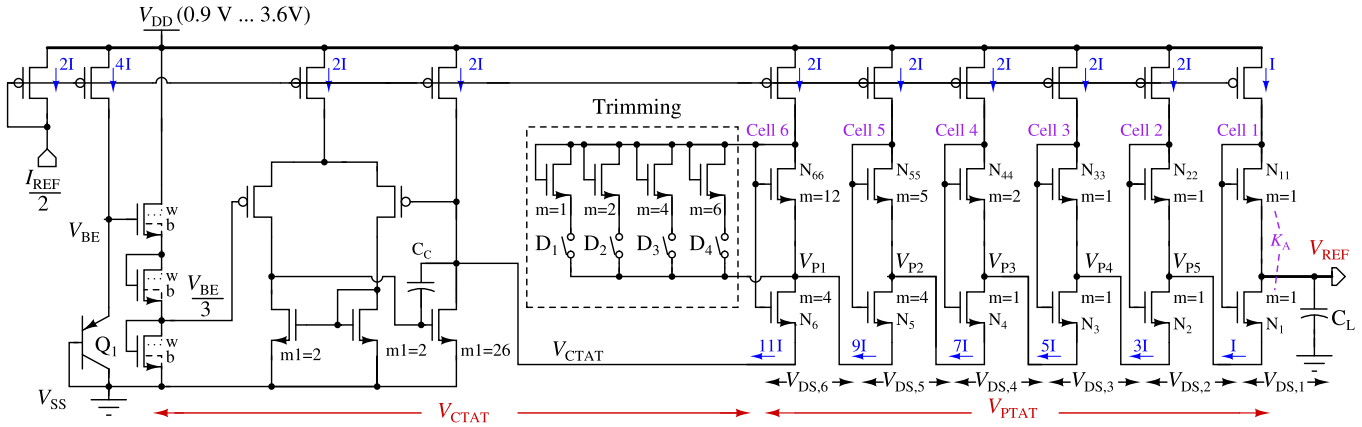


Fig. 7. Overall schematic of the proposed sub-1V voltage reference with transistor multiplier ratio m.

The output voltage $V_{DS,i}$ for the PTAT cell (N_i, N_{ii}) can be modeled as:

$$V_{DS,i} = V_{GS,i} - V_{GS,ii} = \frac{nV_T \ln(K_{A,i}K_{I,i})}{1-e^{\frac{-V_{DS,i}}{V_T}}} + \Delta V_{TH}$$
$$= \frac{nV_T \ln(K_{A,i}K_{I,i})}{1-e^{\frac{-V_{DS,i}}{V_T}}} \frac{1}{1-(\frac{\gamma}{2\sqrt{\phi_f}})} \approx \frac{nV_T \ln(K_{A,i}K_{I,i})}{1-e^{\frac{-V_{DS,i}}{V_T}}} \quad (17)$$

where $K_{A,i}$ is the ratio of the aspect ratio of the transistors N_{ii} and N_i, $K_{I,i}$ is the drain-current ratio between the transistors N_{ii} and N_i, and ϕ_f is the Fermi-potential ($\phi_f \propto T$). The aspect ratio K_A and the drain-current ratio K_I are the design parameters that define the voltage drop V_{DS} across the PTAT cell. The PTAT cell 6 in Fig. 7 has a high $K_{I,6} = 5.5$ and $K_{A,6} = 3$. The voltage drop in PTAT cell 6 is large enough to ignore the channel-length modulation term $1/(1 - e^{\frac{-V_{DS}}{V_T}})$ in (17). The channel-length modulation term cannot be ignored for the PTAT cell 1 where $K_{I,1} = 1$ and $K_{A,1} = 1$ (see Fig. 7). The first-order temperature dependence ($\partial V_{DS}/\partial T$) and the second-order temperature dependence ($\partial^2 V_{DS}/\partial T^2$) of the individual PTAT cell can be derived from (17):

$$\frac{\partial V_{DS,i}}{\partial T} = \frac{nV_T \ln(K_{A,i}K_{I,i})}{T} \frac{1}{1-e^{\frac{-V_{DS,i}}{V_T}}}$$
$$\approx \frac{nV_T \ln(K_{A,i}K_{I,i})}{T} \quad (18)$$
$$\frac{\partial^2 V_{DS,i}}{\partial T^2} \approx \frac{\partial V_{DS,i}}{\partial T} e^{\frac{-V_{DS,i}}{V_T}} \frac{V_{DS,i}}{V_T T} \quad (19)$$

The PTAT cell has a first-order positive temperature dependence as seen in (18). Iterative design of tunable design parameters K_I and K_A helps to adjust $\partial V_{PTAT}/\partial T$ and compensate $\partial V_{CTAT}/\partial T$. An additional positive second-order temperature dependence of $\partial^2 V_{DS,i}\partial T^2$ arises from the channel-length modulation term $(1 - e^{\frac{-V_{DS}}{V_T}})$ as seen in (17) and (19). The series connected PTAT cell design differs from the parallel connection topology of the PTAT cells in [11]. The series connection helps reuse the drain current in the PTAT cells and achieve a high K_I factor.

The total V_{PTAT} generated from summing up the six cells and V_{REF} can thus be written as:

$$V_{PTAT} = \sum_{i=1}^{6} V_{DS,i} \approx \sum_{i=1}^{6} \frac{nV_T \ln(K_{A,i}K_{I,i})}{1-e^{\frac{-V_{DS,i}}{V_T}}} \quad (20)$$
$$V_{REF} \approx \frac{V_{BE}}{3} + \sum_{i=1}^{6} \frac{nV_T \ln(K_{A,i}K_{I,i})}{1-e^{\frac{-V_{DS,i}}{V_T}}} \quad (21)$$

The first-order temperature compensation of $V_{REF} = V_{PTAT} + V_{CTAT}$ requires the compensation of $\partial V_{PTAT}/\partial T$ and $\partial V_{CTAT}/\partial T$. As shown in (16), the target for $\partial V_{PTAT}/\partial T$ is 0.75 mV/K. Equation (18) shows that $\partial V_{PTAT}/\partial T = \sum_{i=1}^{6} n V_T \ln(K_A * K_I)/T \approx 0.1\,\text{mV/K} * \ln(K_A * K_I)$. The equation highlights the need to design a PTAT component that has a high K_A and K_I. Choosing a high K_A is the easier design option, but it results in an extremely low pA bias current through the unit transistor in the PTAT unit cell. Low bias currents are an issue in fast corners as well as high temperatures where the leakage current is also in pA range. On the other hand, a high K_I factor is beneficial to increase the $\partial V_{PTAT}/\partial T$ term and match $\partial V_{CTAT}/\partial T$. As a trade-off between overall power consumption and minimum current through the unit-transistor cells in cell 1, the VR is designed with a series 6-stage PTAT cell formation to provide a high current-gain K_I and a realistic value of K_A. An iterative design optimization of K_I, K_A, and the current mirror ratios are done to achieve a second order temperature compensation of V_{REF} (see (14), (15), (18), and (19)).

Transistors operating in the sub-threshold region are prone to process variations and modelling error of the sub-threshold slope factor. As a result, the VR in Fig. 7 includes a 4-bit trimming circuit in cell 6 to change the aspect ratio term $K_{A,6}$. It helps to compensate the variation and mismatch effects by increasing or decreasing the PTAT slope factor through a digital control. The unit-cell design with a multiplier ratio m helps achieve a compact layout with a good matching between the transistors. The bulk nodes of the PTAT cell transistors N_i and N_{ii} ($i = 1,2,3,4,5,6$) are connected to the ground V_{SS}. As result, high ohmic p-wells at various intermediate potential

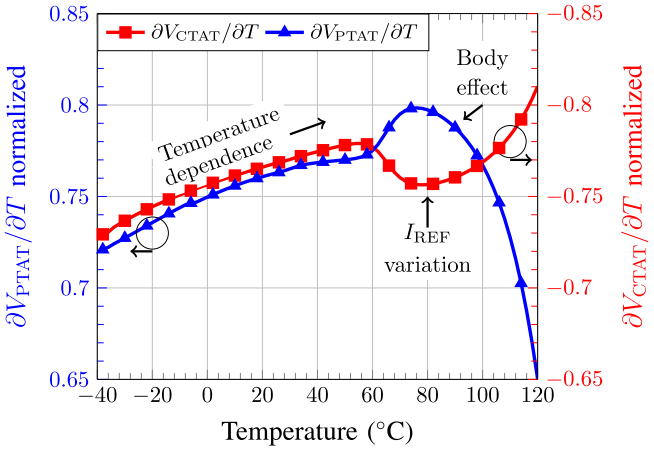


Fig. 8. Simulated normalized $\partial V_{CTAT}/\partial T$ and $\partial V_{PTAT}/\partial T$ versus temperature (simulation details: corner = nom, $V_{DD} = 1$ V).

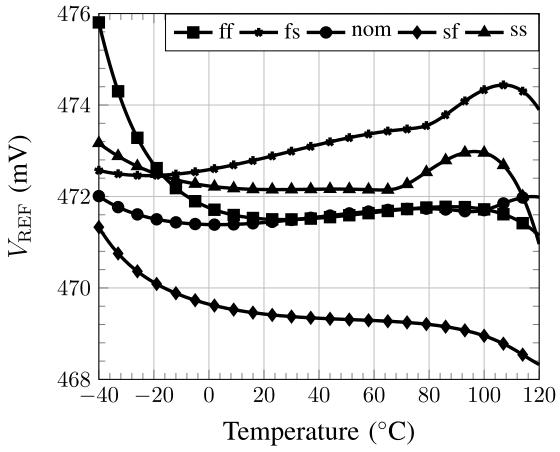


Fig. 9. Post-layout simulated output voltage V_{REF} versus temperature at different process corners.

levels are avoided. It improves the latch-up immunity and reduces the risk of startup issues.

A. Simulation Results

The DC post-layout simulation results in Fig. 8 show the temperature dependence of V_{CTAT} and V_{PTAT} to design a V_{REF}. The normalized plots highlight that $\partial V_{PTAT}/\partial T$ cancels out $\partial V_{CTAT}/\partial T$ over the temperature range from −40°C to 120°C. The second-order temperature dependence in (19) is positive, resulting in an increasing $\partial V_{PTAT}/\partial T$ over temperature until 80°C. Since the bulk of the PTAT-cell NMOS transistors (see Fig. 7) are connected to V_{SS}, the ΔV_{TH} term in (17) becomes more significant for increasing $V_{DS,i}$ at higher temperatures. The increasing ΔV_{TH} results in a reduction of $\partial V_{PTAT}/\partial T$ at higher temperatures, as shown in Fig. 8. On the other hand, V_{CTAT} has a negative first-order and second-order temperature dependence as shown in (14) and (15). Thus, the $\partial V_{CTAT}/\partial T$ curve has a similar behavior as the $\partial V_{PTAT}/\partial T$ curve. As highlighted in Fig. 8, the $\partial V_{CTAT}/\partial T$ shows a mild dependence on the bias current I_{REF} which generates the voltage drop across the BJT Q1. Across the temperature range, the output V_{REF} is first-order and second-order temperature-compensated.

Fig. 9 quantifies the effect of process variation on the output voltage V_{REF}. V_{PTAT} is dependent mainly on design parameters, and has little variation across process corners. On the other hand, V_{CTAT} generated using a vertical PNP-transistor is prone to process variations. It is slightly compensated by the variation of the bias current I_{REF}, which is generated using poly-resistors. In the fast corner, I_{REF} is 30% higher due to the lower resistance of the poly-resistors [31]. The higher output bias current I_{REF} helps to generate a higher V_{CTAT} and compensate the lowering of V_{BE} of the vertical PNP-transistor (see (13)). Similarly, the decrease of I_{REF} helps to compensate the increase of the V_{BE} in the slow process corner. It results in a highly robust V_{REF} with +/− 0.8% variation across process corners, as shown in Fig. 9.

The Monte-Carlo post-layout simulations of 500 runs for V_{REF} in Fig. 10 show a mean μ V_{REF} of 473.5 mV, and a sigma σ of 4.5 mV (+/- 2.7%) for a trimming code of 0100.

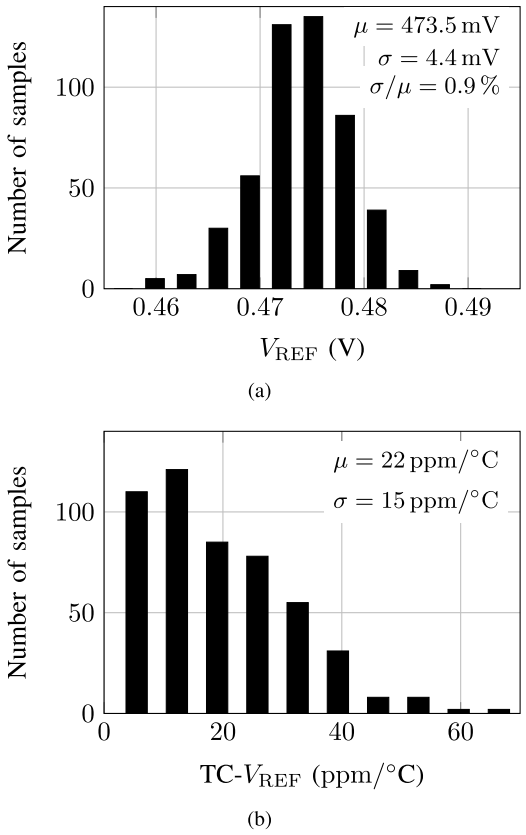


Fig. 10. Monte-Carlo post-layout simulation of (a) V_{REF} and (b) TC-V_{REF} (simulation details: trimming code = 0100, runs = 500).

V_{REF} predominantly depends on the current multiplier ratio used and the design variables (see (21)). The CTAT voltage $V_{BE}/3$ on the other hand has a logarithmic dependence on I_{REF} (see (13)). A 10% drift of I_{REF} across the temperature range would change V_{CTAT} by only $V_T/3 * \ln(1.1) \approx 1$ mV. As a result, small temperature drifts of I_{REF} have a low impact on the TC of the designed V_{REF}. It results in a mean TC-V_{REF} of 22 ppm/°C and an excellent σ of 15 ppm/°C. The contributors to the σ of the output V_{REF} are the BJT output voltage V_{BE}, the offset of the nanowatt unity-gain buffer, and the

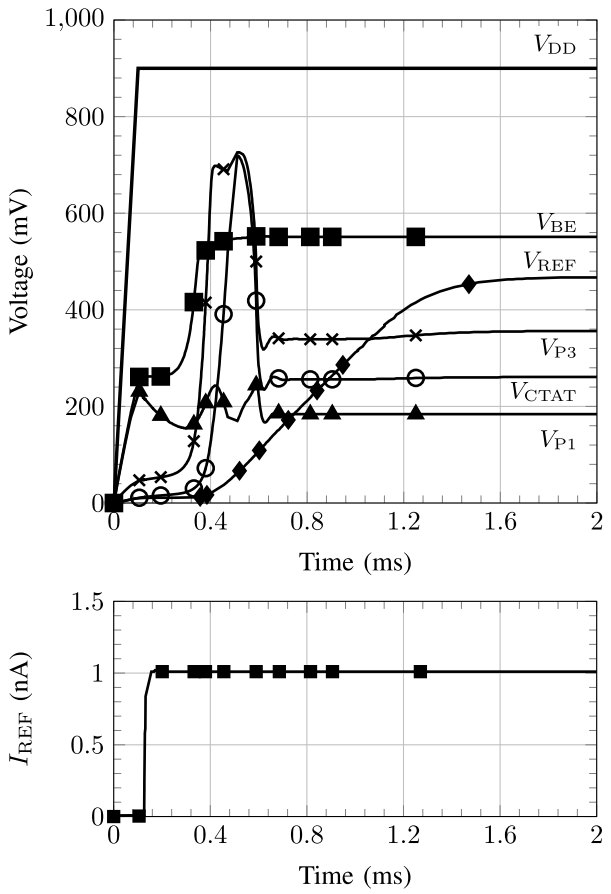


Fig. 11. Post-layout transient simulation of the startup of the voltage-current reference. An ideal voltage source is attached to the supply node V_{DD} (simulation details: corner=nom, T=27°C).

variation of I_{REF}. The compact design and layout of the PTAT cells mitigate the transistor mismatch effects. The output V_{REF} predominantly depends on design variables and technology constants, which help achieve a low TC value.

B. Supply Voltage

The minimum supply voltage V_{DD} of the sub-1V VR is defined by the emitter-base voltage and an overdrive voltage V_{OV} of the current mirror, presented by $V_{DD} > V_{BE} + V_{OV}$. The output node V_{REF} at the PTAT cell 1 output also presents a requirement for the minimum V_{DD}, where $V_{DD} > V_{REF} + V_{GS,N11} + V_{OV}$. Assuming typical values of $V_{BE}=600\,\text{mV}$, $V_{GS,N11}=250\,\text{mV}$ and $V_{OV}=200\,\text{mV}$, the minimum supply voltage $V_{DD} > V_{REF} + V_{GS,N11} + V_{OV}$ is roughly 900 mV. For other bandgap-based VR designs, a minimum supply voltage of $V_{BE}+V_{OV}=800\,\text{mV}$ is expected due to the voltage overhead of the bipolar PNP transistor.

The low-power nature of the current mirror in the design presents a challenge to ensure a correct startup at lower levels of V_{DD}. The post-layout transient simulation in Fig. 11 shows that the V_{BE} is generated as soon as the CR is operational. The output voltage V_{CTAT} generation is dependent on the startup time of the nanowatt unity-gain buffer. The current mirror in the VR gets biased at this time, resulting in the drain nodes of the current mirror transistors getting pulled up to $V_{DD}-V_{OV}$. The effect is seen in the simulation curves of the intermediate PTAT nodes V_{P1} and V_{P3}, which are pulled to this voltage level before starting to find the right operation point at 0.7 ms. The PTAT cells start from the left-most cell 6 until cell 1 because of the series nature of the design. The ramp-up of the PTAT cells of the VCR is considerably slower in a slow corner and cold temperatures. A 1 pF MOS capacitor C_L with an area of 100 μm^2 connected at the output V_{REF} helps to reduce the output ripple.

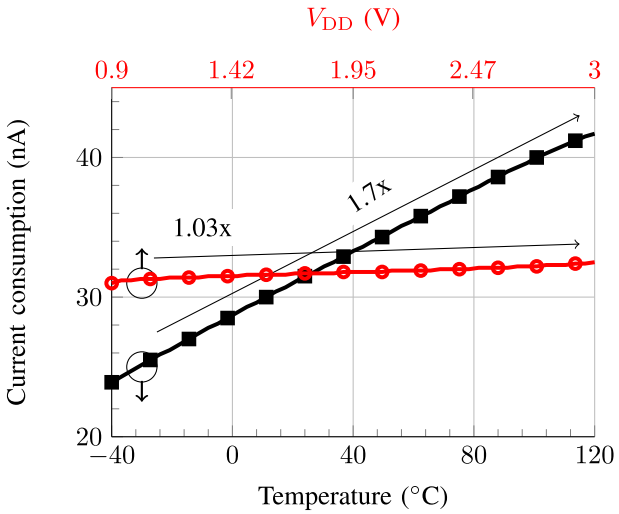


Fig. 12. Post-layout simulated power consumption of the VCR versus changes in supply voltage V_{DD} and temperature.

The line regulation (LS) and PSRR are DC and AC supply sensitivity indicators. As seen in (21), the output V_{REF} has an inherent low dependence on the supply voltage. Accordingly, we have,

$$\text{PSRR}(s) = \frac{v_{dd}(s)}{v_{ref}(s)} \approx \frac{v_{dd}(s)}{i_{ref}(s)} \frac{i_{ref}(s)}{v_{ref}(s)} \approx \frac{v_{dd}(s)}{i_{ref}(s)} g_{m,N_{11}} \qquad (22)$$

where $g_{m,N_{11}}$ is the transconductance of the PTAT cell 1 transistor N_{11} in Fig. 7. The source-follower design structure of the PTAT cell limits the output resistance and, thus, improves the PSRR, as seen in (22). The PSRR of the VR is also dependent on the PSRR of the CR (see (22)).

C. Current Consumption

Fig. 12 shows the post-layout simulated power consumption of the VCR. It consumes 32 nW at 20°C for $V_{DD}=2\,\text{V}$. Fig. 12 shows that the total current consumption is almost unaffected by changes in V_{DD}. It is because of the fixed bias current used in current mirror branches in CR (see Fig. 4) and VR (see Fig. 7). The bias current has a low dependence on supply voltage variation. The NMOS voltage divider is an exception which does not have a fix bias current. The threshold voltage of the NMOS transistors in the divider varies across the temperature range from −40°C to 120°C. As a result, the total current consumption changes by a factor of 1.7x across the temperature range.

IV. Measurement Results

The proof-of-concept voltage-current reference VCR as a part of a testchip was designed in an in-house 130 nm CMOS technology. The initial design was done in an n-well CMOS

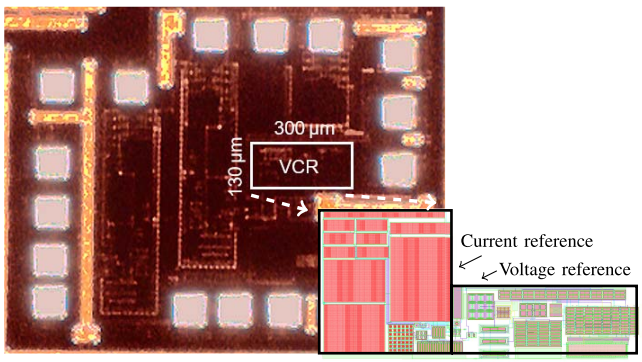


Fig. 13. Microphotograph and the layout inset of the proposed voltage-current reference.

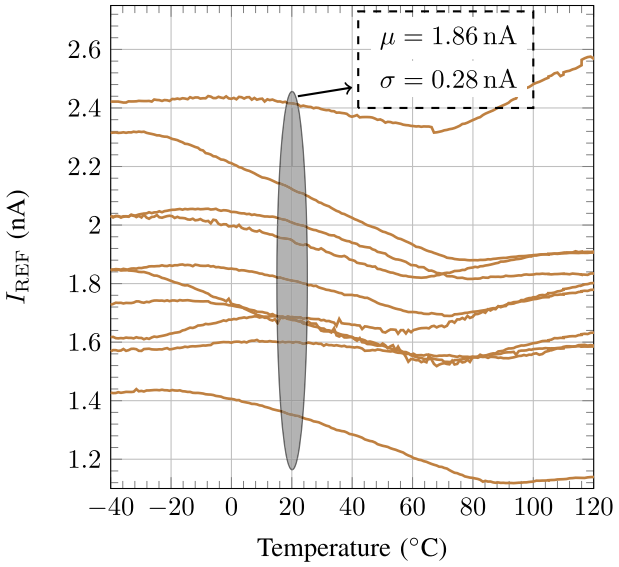


Fig. 14. Measured results of the CR: temperature dependence of the output current I_{REF} (measurement details: samples = 10, trimming code = 0010, $V_{\text{DD}} = 2.5\,\text{V}$).

process where the NMOS transistors had no possibility of a buried p-well. As a result, most of the NMOS transistors in the design have a bulk connection to ground. The VCR occupies a chip area of $0.04\,\text{mm}^2$ as shown in the chip microphotograph and the layout inset in Fig. 13. A total of 10 bare-die samples from a nominal process lot were directly bonded onto an FR4 PCB and measured. The PMOS gate-coupled pairs have a common-centroid layout to minimize mismatch effects. The poly-resistors used in the CR are the most significant contributors to the overall area of the VCR. The unit-cell design approach of the transistors in the CR and the VR helps to build compact layout structures with common-centroid topology.

The chips have been characterized in the temperature range from −40°C to 120°C. The output current I_{REF} is measured at the input of Keithley 2400 source meter using the current measurement function with a resolution of 50 pA. The measurement results of the CR are shown in Fig. 14. Measurements across ten samples reveal a mean TC-I_{REF} of 822 ppm/°C. The spread of the output I_{REF} at 20°C shows a mean $\mu = 1.86\,\text{nA}$ and a standard deviation $\sigma = 290\,\text{pA}$. The wide spread of the mean of I_{REF} can be attributed to the dependence on the

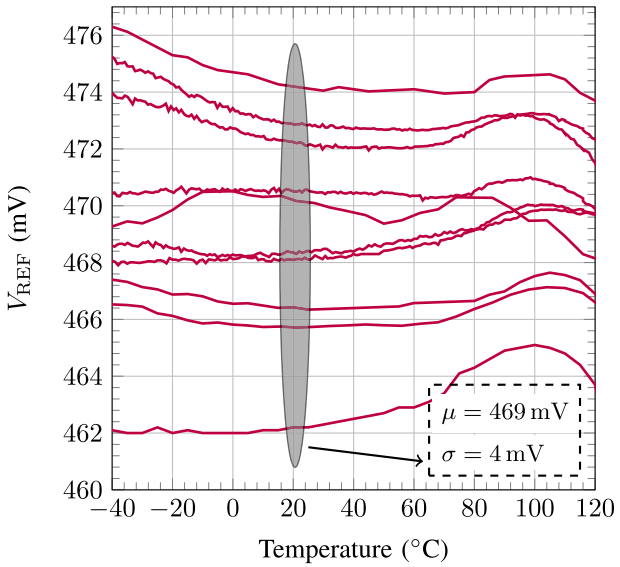
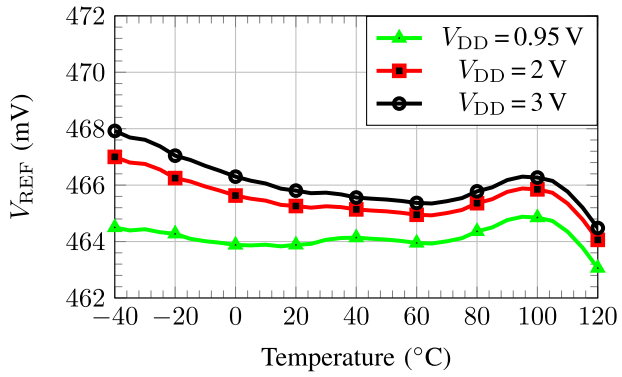


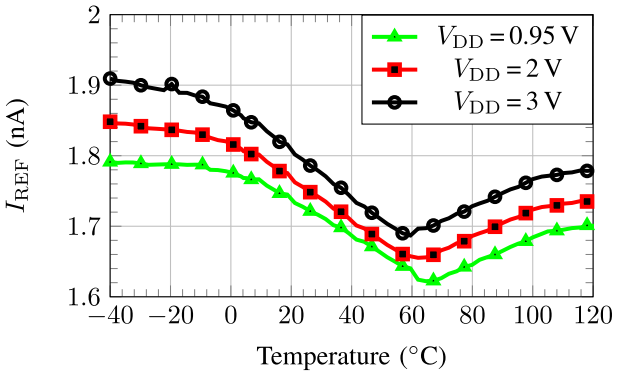
Fig. 15. Measured results of the VR temperature dependence of the output voltage V_{REF} (measurement details: samples = 10, trimming code = 0010, $V_{\text{DD}} = 2.5\,\text{V}$).

absolute value of the poly-resistors (see (5) and (7)) and the V_{TH} variation of the transistor MN_2 (see Fig. 4). Additionally, the V_{TH} variation of MN_2 has a direct impact on the first-order temperature coefficient of I_{CTAT} (see (7) and (8)). The V_{TH} variation, thus, causes a few CR samples to have a clear CTAT or PTAT behavior, as seen in Fig. 14. The CR trimming circuit has been designed to compensate process corner variations and reduce the spread of the output I_{REF} with minimal impact on the TC. Thus, CR measurements done with an individual trimming for every sample reduces the σ/μ spread of I_{REF} from 0.29 nA/1.9 nA to 0.2 nA/2 nA. Measurement results of I_{REF} reveal a bigger σ spread compared to the post-layout simulations ($\sigma = 0.23\,\text{nA}$). It arises from the usage of the minimum width poly-resistors which are highly prone to mismatch [33].

The output voltage of the VR has been connected to an on-chip unity-gain buffer to increase the output drive strength and connect to a Keysigt 34470A digital multimeter. Fig. 15 shows the measured results of the VR across the ten samples for a fixed trim setting of 0010. The curvature compensation of the VR ensures that the output V_{REF} achieves an excellent mean TC of 29 ppm/°C. For the ten measured samples, the spread of the output V_{REF} at 20°C shows a mean $\mu = 469.5\,\text{mV}$ and a standard deviation $\sigma = 4\,\text{mV}$. The measurements have been done on a nominal wafer lot. As a result, the σ spread of V_{REF} in the measurement results (4 mV) are better than the post-layout simulations results ($\sigma = 4.5\,\text{mV}$). The VR trimming has been designed to optimize the TC by changing the PTAT slope. As a result, VR measurements with an individual trimming for every sample reduces the mean TC-V_{REF} from 29 ppm/°C to 22 ppm/°C. The smaller σ/μ spread of V_{REF} compared to I_{REF} highlights the robustness of the VR design with respect to variations in the bias current I_{REF}. Fig. 16 shows the measured temperature of V_{REF} and I_{REF} for different supply voltage levels for one sample. The TC of the output current I_{REF} and output voltage V_{REF} have little



(a)



(b)

Fig. 16. Measured temperature dependence of (a) V_{REF} and (b) I_{REF} at different V_{DD} for one sample.

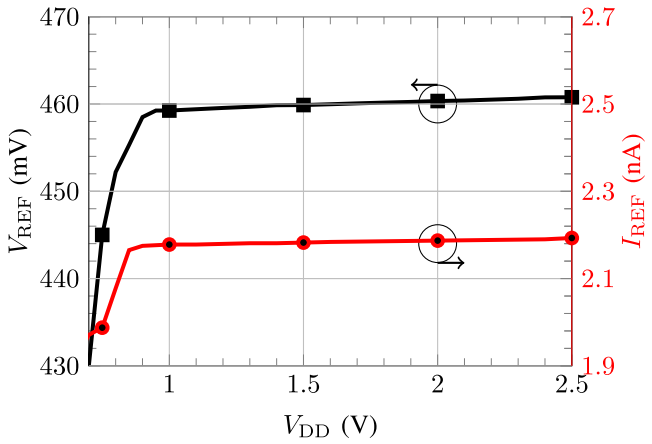


Fig. 17. Measured output voltage V_{REF} and output current I_{REF} versus the supply voltage V_{DD} (measurement details: T = 27°C).

dependence on the supply voltage variation. V_{REF} has a mild dependence on V_{DD} at cold temperatures and higher supply voltage level of 3 V. It arises from a technology dependent bulk effect in the NMOS voltage divider (see Fig. 7) built using triple-well transistors.

The minimum supply voltage V_{DD} of the sub-1V VR is defined by the emitter-base voltage of the bipolar transistor and an overdrive voltage of the current mirror (see Fig. 7). As seen in Fig. 17, the VR starts up at a minimum V_{DD} of 0.95 V. With increasing V_{DD}, the VR achieves a line sensitivity of 0.2%.

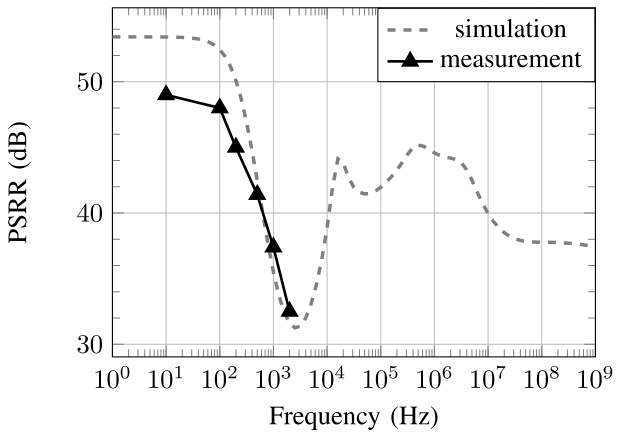


Fig. 18. Post-layout simulated and measured PSRR of V_{REF} without load capactior (T = 27°C).

It can be attributed to the low dependence of the output V_{REF} on V_{DD} (see (22)). On the other hand, the minimum V_{DD} of the CR is only limited by the voltage drop across the transistors in the PTAT current reference sub-circuit (see Fig. 4). The CR requires a minimum V_{DD} of 0.85 V (see Fig. 17). A line sensitivity of 4% is achieved from a supply voltage V_{DD} range from 0.95 V to 2.5 V. Fig. 18 shows the post-layout simulated and the measured PSRR of the output voltage V_{REF} versus frequency. As seen in the measurement results in Fig. 18, the VR has a PSRR of 49 dB at 10 Hz, which is an indicator of the line regulation. It highlights the low dependence of V_{REF} on supply voltage as also shown in (21). The PSRR has been measured only up to 2 kHz in order to exclude the effect of the output buffer amplifier connected at the output node V_{REF}. At 868 MHz which is the input frequency of the RF-powered WuRx, the VR achieves a PSRR of 37.6 dB, as seen in simulations. A typical 2 mV_{P-P} V_{DD} ripple at this frequency affects V_{REF} by only 0.03 mV_{P-P} making the VR highly suitable for RF energy harvesting applications.

V. Comparison With Related Works

In order to compare the performance of the proposed VR with the related works, a Figure of Merit (FoM) that considers the temperature range (T_{RANGE}), the TC, the power consumption, and the silicon area, can be expressed as [16]:

$$\text{FoM} = \frac{T_{RANGE}^2}{\text{TC} \cdot \text{Power} \cdot \text{Area}} \frac{1}{10^{18}} \tag{23}$$

The FoM, as seen in (23), is higher for wide-temperature range VRs. The second-order temperature compensation of the VR helps to achieve a good performance over an extended temperature range from −40°C to 120°C. Fig. 19 shows the FoM of the recent voltage references (VRs and VCRs) with respect to the power consumption. As far as the performance of the voltage reference is concerned, the designed VCR has the best FoM number compared to other VCRs in [14], [37], and [38].

As far as the performance of the standalone VR is concerned, Fig. 19 highlights three distinct groups of VRs. The high-power BGR-based VR in [39] is designed for a high

TABLE I
PERFORMANCE COMPARISON WITH RELATED WORK

		This work†	**TCAS I-19†** [37]	**ISSCC-17†** [38]	**TCAS I-19†** [14]	**JSSC-19** [10]	**ISSCC-19** [39]	**TCAS I-20** [12]	**JSSC-17** [15]	**JSSC-21** [17]
CMOS node		**130 nm**	180 nm	180 nm	130 nm	180 nm	12 nm	65 nm	180 nm	180 nm
Type		**Hybrid VR & CR**	CMOS VR & CR	BGR VR & CR	CMOS VR & CR	Hybrid VR	Sub-BGR VR	Hybrid VR	CMOS VR	CMOS VR
$V_{DD,MIN}$ (V)		**0.95**	0.7	1.4	0.5	1	0.7	0.5	0.5	0.9
Power (nW)		**30**	28	9.3	1300	0.192	5880	36	0.03	2
Temp. range (°C)		**-40 to 120**	-40 to 125	0 to 110	-40 to 80	-20 to 100	-20 to 125	-40 to 120	0 to 100	-40 to 130
Output (mV, nA)	VR	**469**	1238	1500	355	207	230	495	120	260
	CR	**1.85**	10	6.6	6000	N/A	N/A	N/A	N/A	N/A
Mean TC (ppm/°C)	VR	**29**	43	26	126	33	40	42	35	70
	CR	**822**	150	680	106	N/A	N/A	N/A	N/A	N/A
σ/μ (%)	VR	**0.85 / 0.9**^{S}	5	0.24	1.5	0.54	0.75	3	0.8	7^{S}
	CR	**15 / 11**^{S}	6	8	8	N/A	N/A	N/A	N/A	N/A
LS (%/V)	VR	**0.2**	0.027	0.1	5	0.02	0.78	0.63	0.3	0.02
	CR	**4**	6	8	5	N/A	N/A	N/A	N/A	N/A
Trimming		**Yes-4bit**	No	Yes	No	No	No	Yes-3bit	Yes-4bit	No
PSRR (dB)		**49 @ 10 Hz**	50 @ 1 Hz	46 @ 10 Hz	43 @ 1 Hz	55 @ 1 Hz	-	50 @ 1 Hz	41 @ 1 kHz	74 @ 1 Hz
No. of chips		**10**	5	5	10	45	5	7	60	15
Area (mm^2)		**0.04**	0.055	0.055	0.03	0.005	0.065	0.05	0.025	0.006

† Voltage-current reference; ^{S} calculated for 500 Monte-Carlo runs; LS = line sensitivity

accuracy at the cost of higher power consumption, achieving a smaller FoM. The ultra-low-power CMOS-based VRs in [10], [15], [16], and [17] achieve a higher FoM. They do not have an inbuilt CR and employ native MOS devices where the leakage current determines the output voltage V_{REF}. The leakage current based CMOS VRs are not suitable for energy harvesting sub-systems which typically have a significant high frequency 2 mV_{P-P} output ripple on the harvested supply voltage (f = 868 MHz) [2]. The high frequency ripple on the supple voltage causes an inrush current through the low-impedance path of the parasitic capacitors. If the inrush current is higher than the bias current, it can trigger a wrong operation point in the ultra-low-power leakage current-based CMOS VRs. On the other hand, the designed VR and the nanowatt VRs in [11], [12], [37], and [38] achieve a good tradeoff between accuracy and power consumption. They are less susceptible to process corner variations and high-frequency supply voltage ripples. They achieve a very good FoM for a low-power consumption, as seen in Fig. 19.

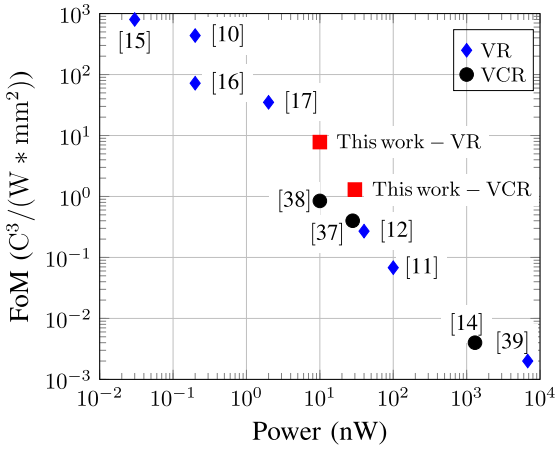


Fig. 19. Ultra-low-power state of the art voltage references FoM performance with respect to power consumption.

Table I shows the comparison of the performance of the designed VCR with the previously reported VCRs and VRs. As far as the listed VCRs are concerned, the designed VCR achieves a superior TC-V_{REF} of 29 ppm/°C and a good TC-I_{REF} of 822 ppm/°C over a wide temperature range of 160 °C. The performance of the CR is inferior to the related works because of the dependence of the output I_{REF} on the process-corner sensitive V_{TH} of the NMOS transistor and the resistance of the poly-resistors. The output voltage V_{REF} with a mean μ of 469 mV and sigma over mean σ/μ of 0.85% is well balanced among the reported works. The design area, line sensitivity, and the PSRR of the VCR are comparable to the other listed VRs in Table I. The works in [10], [15], and [38] report a lower power consumption at room temperature, but their power consumption increases by a factor of more than 50x over the temperature range. The minimum supply voltage V_{DD} of 0.95 V satisfies the requirement of RF-powered WuRx applications. The designed VCR additionally includes a sub-50 mV VR unlike the other listed VCRs.

VI. CONCLUSION

This paper presents a novel nanowatt voltage-current reference fabricated in a 130 nm CMOS process. The core of the

design lies in a shared-resistive nanoampere CR with output current I_{REF}, used as a bias current for the generation of the curvature-compensated sub-1V VR. The VR includes a hybrid architecture combining BGR and CMOS-based references. An iterative approach of optimizing the design parameters was done to achieve a second-order temperature-compensated output voltage V_{REF}. Measurement results from 10 chips show that the high-precision output 469 mV V_{REF} achieves an excellent mean TC-V_{REF} of 29 ppm/°C and σ/μ of 1.1% with an overall power consumption of 30 nW. The inbuilt current reference generates a 1.86 nA I_{REF} with a TC-I_{REF} of 822 ppm/°C.

The design methodology of the VCR temperature compensation mainly depends on the design parameters and it has a low dependence on the technology parameters. As a result, the VCR design can be easily implemented in other bipolar CMOS processes. The novel design of the CR results in the generation of an additional sub-50 mV voltage reference which can be used as a low-voltage reference for analog/mixed-signal blocks. The proposed voltage-current reference is highly suitable for RF-powered wake-up receivers and ultra-low-power IoT nodes.

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