A Detailed Model of Cyclostationary Noise in Switched-Resistor Circuits

Alessandro Fava, Francesco Centurelli, *Senior Member, IEEE*, and Giuseppe Scotti, *Senior Member, IEEE*

***Abstract*— The Switched-Resistor (S-R) technique is becoming more and more interesting to implement low-voltage low-power active-*RC* filters with high tuning range and front-end amplifiers for biomedical circuits and systems. This approach exploits MOS switches driven by a duty-cycle-controlled clock signal to achieve tunability of the equivalent resistance and, hence, of the RC time constant. Since S-R circuits can be considered as linear periodically time variant (LPTV) systems with sampled outputs, we exploit the theory of the adjoint (inter-reciprocal) network in order to develop a detailed model of the cyclostationary noise involved in this kind of circuits. The proposed model allows to gain insight into the different noise sources and transfer functions involved, highlighting the circuit parameters on which the cyclostationary noise depends. Validation of the proposed model has been carried out by comparing analytical results against periodic noise simulations referring to a commercial 130nm CMOS process. The validation activity has confirmed the good accuracy of the proposed noise model and provided some useful design guidelines to optimize the noise performance of S-R circuits.**

***Index Terms*— Biomedical applications, large time constants, integrated circuits, Switched-Resistor, noise modeling, LPTV systems, cyclostationary noise.**

I. Introduction

NOWADAYS, an ever-increasing number of integrated devices for biomedical applications requires high resistance values to implement very large time constant with a small area footprint and low input noise. In fact, biological signals, characterized by a dc component due to electrode–skin contact, require analog front-end amplifiers based on AC coupling with very low cut-off frequencies (below 1Hz) in order to remove the dc offset and properly process the signal itself. The implementation of these very large time constants on a CMOS integrated circuit is severely limited by the area requirements both of capacitors and of resistors. In fact, the capacitance per area is limited to a few fF/μm^2, if extra technological steps to exploit special dielectric materials are not implemented. Large physical resistors also require a huge Silicon area, hence alternative approaches such as Switched-Capacitor (S-C) or pseudo-resistor have been proposed to minimize the area footprint.

High resistance values are required also in new generation neural recording multi-electrodes systems, which exploit multiplexing techniques and implement front-ends based on transimpedance amplifiers (TIAs) [1]. TIAs for biomedical applications often require high-valued feedback resistances which can be tuned over a wide range of transimpedance gains and exhibit low input referred noise [2].

Designers of CMOS integrated circuits for biomedical applications typically exploit the Switched-Capacitor [3] or the pseudo-resistor [4], [5] approaches to implement large resistance values in order to handle the tradeoff between tuning range, noise and linearity. Nevertheless, it has to be pointed out that, in order to tune the resistance value of Switched-Capacitor resistors, the clock frequency has to be varied, thus changing the sample rate of the system, and this can be a disadvantage in many applications. Furthermore, the noise generated in Switched-Capacitor circuits is inversely proportional to the capacitance value, resulting in a further tradeoff between area and noise minimization [6]. Coming to pseudo-resistor implementations, their resistance value is typically tuned over a wide range by changing the gate-source voltage. However, when using this technique, the value of the equivalent resistance is strongly non-linear and also very sensitive to the common mode voltage and to process, supply voltage and temperature (PVT) variations. To mitigate these issues, many pseudo resistor topologies have been recently proposed [5], [6], [7], [8] which, however, result in worse noise performance and higher power consumption. Furthermore, the noise contributions in pseudo-resistors strongly depend on MOS devices sizing and operating points, but typically an active device generates more noise than a passive element such as a polysilicon resistor due to flicker and shot contributions [8].

In the latest years, the Switched-Resistor (S-R) approach has become more and more popular within the community of integrated circuits designers [9], [10], [11], because it allows implementing very high equivalent resistances with excellent tuning capability and good linearity performance. In fact, the S-R approach allows to boost up the value of a physical resistor through the adjustment of the duty cycle of the clock signal that drives the switch in series with it, without modifying the sample rate of the system. Another interesting characteristic of the S-R technique resides in the fact that, in S-R circuits, the output voltage is already sampled, and this allows to simplify the ADC design without considering

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The authors are with the Dipartimento di Ingegneria dell'Informazione, Elettronica e Telecomunicazioni, Universitá degli Studi di Roma La Sapienza, 00185 Rome, Italy (e-mail: giuseppe.scotti@uniroma1.it).

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an additional sample-and-hold block. All these characteristics make the S-R approach a valid alternative solution to Switched-Capacitor and pseudo-resistor approaches, especially in biomedical applications. In fact, the S-R approach has been successfully exploited in [12], [13], and [14] to implement tunable filters, TIAs and analog front-ends for biomedical integrated circuits.

Designers of biomedical integrated circuits need accurate noise models in order to satisfy constrains in term of area occupation and power consumption while achieving the target performances for their circuits. Nowadays many noise models are available for Switched-Capacitor [15], [16] and pseudo-resistor circuits [4], [17], which are able to handle analog tradeoffs in front-ends design. To the authors' knowledge, no accurate model has been presented so far for the S-R approach, and noise is typically modeled as the thermal noise related to the equivalent (average) resistance [11].

The derivation of an accurate noise model of S-R circuits is not trivial due to the cyclostationary nature of noise in these circuits. In fact, the noise analysis of LPTV (linear periodically time-variant) circuits, such as S-R systems, has to be carried out by determining the time variant frequency transfer functions for each noise source of the circuit. For this purpose, many theoretical contributions have been proposed in the literature starting from the '50s, simplifying every time the complicated analysis [18], [19], [20].

Recently, some novel theoretical contributions have been proposed in the literature to solve LPTV circuits [21], [22], [23] such as S-C circuits, mixers, and samplers. A simple method proposed by Pavan for the analysis of N-path passive filters [24], [25], [26] exploits the adjoint network theory [21], [27] to build a LTI (Linear Time-Invariant) equivalent circuit that shows a transfer function equivalent to the one of the sampled LPTV system.

In this paper we demonstrate that the conventional noise model adopted for the S-R [9], [28] is inaccurate for values of duty cycle below 1%. We then propose a new analytic noise model of S-R circuits, based on the approach proposed by Pavan, which is able to describe in an accurate way all the main noise sources that involve MOS switches and polysilicon resistors. The proposed model has been validated varying devices parameters and duty cycle values, highlighting a high accuracy in predicting the white noise components with average errors below 1%.

The paper is structured as follows: section II reviews the basics of cyclostationary noise in LPTV systems. The proposed detailed noise model is introduced and explained in section III; firstly, the adjoint network related to the S-R circuit under analysis is derived and then the equivalent transfer function for each noise source is analytically evaluated. The validation of the model is presented in section IV, highlighting the accuracy of the model and providing noise optimization guidelines. Conclusions are finally drawn in section V,

II. Review of Cyclostationary Noise in LPTV Systems

A linear periodically time-varying system can be characterized by an impulse response $h(t, \tau)$ in which the input signal $x(u)$ is applied at the instant of time $u = t - \tau$, whereby t represents the observation time and τ is the difference between the observation time and the time of application of the impulse itself. Since the system is causal, $h(t, \tau) = 0 \; for \; t < \tau$. In such a system, the excitation time plays the role of explorer of different system conditions that distinguish the time-varying nature. For a generic time-varying system the output response can be expressed as follows:

$$y(t) = \int_{-\infty}^{\infty} h(t, \tau)\, x(u)\, d\tau \tag{1}$$

Now considering a complex exponential input signal $x(u) = e^{j2\pi f u}$, (a generic input signal can be expressed as sum of infinite complex exponentials) the output $y(t)$ of the system can be rewritten as:

$$\begin{aligned} y(t) &= \int_{-\infty}^{\infty} h(t, \tau)\, e^{j2\pi f u} d\tau \\ &= e^{j2\pi f t} \int_{-\infty}^{\infty} h(t, \tau)\, e^{-j2\pi f \tau} d\tau \\ &= e^{j2\pi f t} H(t, j2\pi f) \end{aligned} \tag{2}$$

The above equation leads us to define the time-varying transfer function $H(t, j2\pi f)$ that links the time-domain response of the system with the single-frequency input signal:

$$H(t, j2\pi f) = \int_{-\infty}^{\infty} h(t, \tau)\, e^{-j2\pi f \tau} d\tau \tag{3}$$

If we assume that the system is periodic with period T_s, then the impulse response is also periodic, and the following property holds:

$$h(t, \tau) = h(t + nT_S, \tau) \tag{4}$$

In a similar way, the above property holds also for the time-varying transfer function, which can therefore be expanded in Fourier series referring to the time t. This last assumption allows us to express the frequency response (3) as:

$$H(t, j2\pi f) = \sum_{k=-\infty}^{\infty} H_k(j2\pi f)\, e^{\frac{j2\pi k}{T_s} t} \tag{5}$$

where

$$H_k(j2\pi f) = \frac{1}{T_s} \int_0^{T_s} H(t, j2\pi f)\, e^{-j\frac{2\pi k t}{T_s}} dt \tag{6}$$

are the coefficients of the Fourier series expansion of the time-varying transfer function (3). Hence, the time-varying impulse response can be seen as a sum of time-shifted nonperiodic impulse responses; then, in frequency, a sum of the harmonic transfer functions $H_k(j2\pi f)$ multiplied by the different complex exponentials related to the time-shifts.

If we consider the sampled output $y(nT_s)$, combining (2) and (5) we obtain a discrete sequence of samples which can be considered as the output of an equivalent LTI system:

$$y[n] = y(nT_s) = H_{eq}(j2\pi f)\, e^{j2\pi f (nT_s)} \tag{7}$$

$$\begin{aligned} H_{eq}(j2\pi f) &= H(nT_s, j2\pi f) \\ &= \sum_{k=-\infty}^{\infty} H_k(j2\pi f) \end{aligned} \tag{8}$$

The above considerations show that, due to the periodicity property, the output samples of a generic LPTV system are

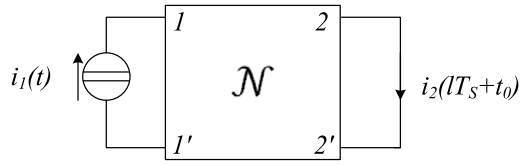

Fig. 1. An LPTV network varying with sample period T_s, whose output $i_2(t)$ is periodically sampled at T_s, with a time offset t_0.

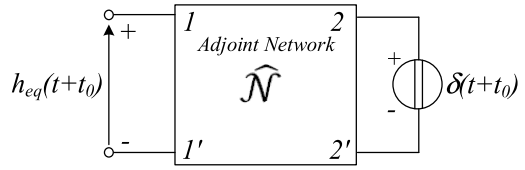

Fig. 2. Determining the impulse response $h_{eq}(t)$ of the equivalent LTI system using the adjoint network. An impulse voltage is injected into the "output" port of the adjoint network, and the open circuit voltage in the input port is $h_{eq}(t)$.

equal to the output samples of an equivalent LTI system built using as equivalent frequency response the sum of harmonic transfer functions of the LPTV system itself.

An interesting approach to derive the equivalent frequency response $H_{eq}(f)$ has been proposed by Pavan in [24] and [25], where the adjoint network theory is exploited to compute the equivalent impulse response $h_{eq}(t)$ (i.e., the inverse transform of (8)) in a few simple steps.

As thoroughly descripted in [21], given a network N, the related adjoint network $\hat{N}$ has the same graph as N and can be built from it by applying the following substitutions rules:

1) The electrical passive elements (linear resistors, capacitors, and inductors) do not change in the equivalent domain $\hat{N}$;
2) Each switch driven by a waveform $\phi(t)$ has to be replaced with a switch driven by a waveform $\phi(-t)$;
3) Linear controlled sources in the LPTV system are replaced by the symmetrical (dual) linear controlled sources in the adjoint network. For instance, a voltage-controlled voltage source has to be replaced with a current-controlled current source with exchanged ports.

Let us consider the 2-port LPTV network (N) shown in Fig. 1, excited by the current source $i_1(t)$ at the port 1, and whose output short circuit current $i_2(t)$ is sampled with period T_s at the port 2. The corresponding adjoint network $\hat{N}$ is shown in Fig.2, and when excited with an impulse voltage source $\delta(t)$ at port 2 the open-circuit voltage taken at the port 1 of $\hat{N}$ gives $h_{eq}(t)$.

By generalizing the above considerations to the multi-input case, as shown in Fig. 3, the output of interest in a generic multi-port LPTV network is assumed to be $v_o(t)$, while r generic sources are applied to the input ports. Working in the adjoint domain, the equivalent LTI system of the LPTV network can be obtained by applying an impulse voltage source at the output port of interest, while r open-circuit voltages or short-circuit currents are picked up at the respective r input ports [21], providing the equivalent impulse responses $h_{eq,i}(t)$, $i = 1, 2, \ldots r$. These functions can then be exploited to calculate the sampled output of the original network as the sum of the input sources filtered by the respective equivalent

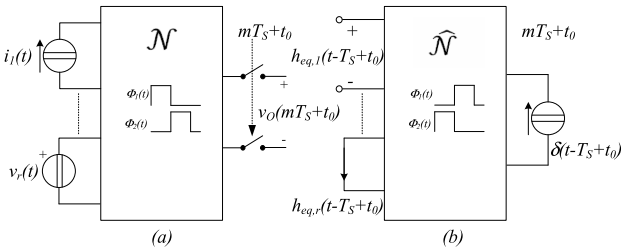

Fig. 3. (a) Original network with multiple inputs and one output, sampled at a timing offset t_o. (b) Determination of $h_{eq}, 1 \ldots, r(t)$ using the adjoint network.

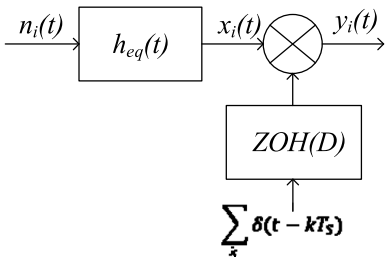

Fig. 4. Block scheme of the i-th noise source filtered by h_{eq} and sampled though a zero-order hold (ZOH) block.

impulse functions. Fig. 4 details this process for a single input, highlighting also the sampling of the output with a zero-order hold (ZOH) block, that models the fact that sampling is performed by a square-wave clock with a given duty cycle D and not by a train of ideal pulses.

If the r input sources are assumed to be the noise sources $n_i(t)$ of the network, then, referring to the block scheme in Fig. 4, this procedure allows to derive the output noise power spectral density (PSD), taking into account its cyclostationary nature and output sampling. In fact, once the equivalent impulse responses, or the equivalent transfer functions (8), have been determined, the PSD of the output $S_o(f)$ can be determined starting from the PSD S_{in} of $n_i(t)$ as follows:

$$S_o(f) = S_{in}(f) \left|H_{eq}(f)\right|^2 * |ZOH(D, f)|^2 \tag{9}$$

where

$$|ZOH(D, f)|^2 = \sum_{k-\infty}^{\infty} D^2 sinc^2\left(\frac{Dk}{T_s}\right) \delta\left(f - \frac{k}{T_s}\right) \tag{10}$$

and D is the duty cycle of the zero-order hold block, and then rewritten as:

$$S_o(f) = \sum_{k-\infty}^{\infty} S_{in}\left(f - \frac{k}{T_s}\right) \left|H_{eq}\left(f - \frac{k}{T_s}\right)\right|^2 \times D^2 sinc^2\left(\frac{Dk}{T_s}\right) \tag{11}$$

($sinc(x)$ denotes the function $sin(\pi x)/\pi x$, as usual).

This approach will be applied in the next section to develop, for the first time in the literature, a detailed model of noise in S-R circuits, that takes into account its cyclostationary nature to achieve good precision even for very low duty cycles.

III. Switched-Resistor Noise Model Based on Adjoint Network Theory

The scheme of an ideal S-R is depicted in Fig. 5. The conventional S-R model [9], [11] is based on a MOSFET

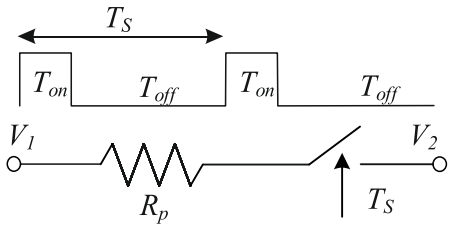

Fig. 5. Switched-Resistor ideal circuit.

Transmission Gate (TG) switch, characterized by its on-resistance r_{on}, in series with an ideal poly resistor R_p (the off-state resistance of the switch r_{off} is assumed to be infinite). A duty-cycle-controlled clock is applied to the TG switch to set the average current that flows in the series. A detailed model of the S-R technique accounting also for parasitic capacitances and off-state resistances has been recently presented in [29] by the authors to accurately predict the equivalent resistance R_{eq} of a S-R.

If the noise behaviour of a S-R circuit has to be described, the only model available in the literature [9], [28] is the one based on the thermal noise generated by the equivalent resistance:

$$S_{S-R} = \frac{4KT}{R_{eq}} \tag{12}$$

It can be easily shown that the model in eq. (12) gives a reasonable accuracy only for duty cycle values higher than about 1 to 10%, even when the equivalent resistance obtained by the model in [29] is used.

Integrated filters for biomedical and IoT devices often require high resistance values to implement the very large time constants needed to process the low frequency biological signals [30]. By using the S-R technique, the value of a reference resistor is multiplied by a factor dependent on the duty cycle of the clock signal. Since the silicon area occupied by a physical resistor is related to the desired resistance value, chip area can be strongly reduced if a small physical resistor is used and the equivalent resistance is boosted through the S-R technique. To achieve resistance multiplication factors higher than 100, the value of the duty cycle has to be reduced below 1%, and in all these cases the above noise model is not enough accurate.

When using a polysilicon resistor, the resistance value R_p is changed by varying the length L_R of the physical resistor, according to [31] ($R_p = rL_R$, where r is the resistance per unit length of the polysilicon strip), and the associated parasitic capacitance results $C_{Rp} = \frac{1}{3}\frac{c}{r}R_p$, (where c is the parasitic capacitance to substrate per unit length of the polysilicon strip).

Since the SR approach is interesting to implement very high resistance values with small silicon area, we have chosen the resistor type with the highest resistivity among the available resistors in the target 130nm process.

The main difference when using other kind of resistors is in the value of the associated parasitic capacitance, but the model is able to handle any kind of resistor.

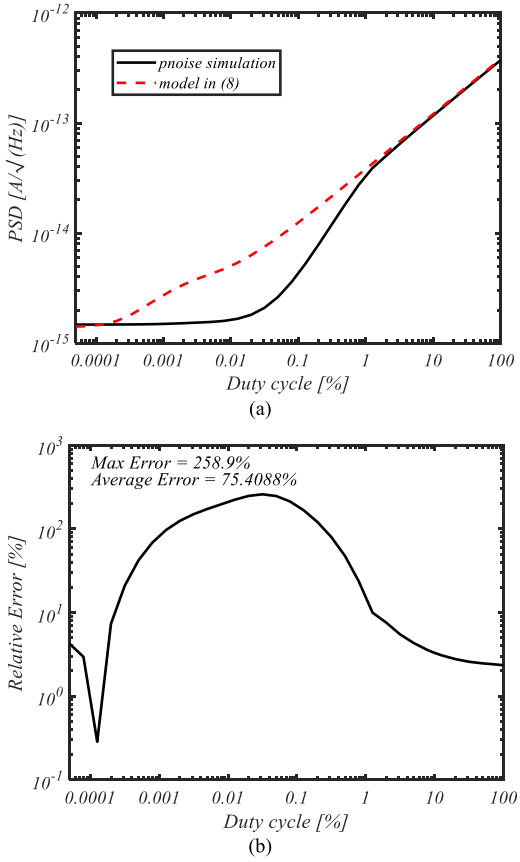

Fig. 6. S-R conventional noise model: (a) comparison of the S-R noise PSD estimated by the model in (8) (dashed line) with the results of *Pnoise* simulations (solid line); (b) relative error between the conventional model in (8) with respect to the *Pnoise* simulations.

To quantify the accuracy of the conventional S-R noise model we refer to a commercial 130nm CMOS technology and consider the power spectral density (PSD) of the S-R circuit in Fig. 5 for $R_p = 100k\Omega$ and a transmission gate (TG) switch with minimum sized MOS transistors. Periodic steady state (*PSS*), periodic *AC* (*PAC*) and periodic noise (*Pnoise*) simulations within the Cadence Virtuoso™ environment have been exploited to estimate the equivalent resistance R_{eq} and the noise PSD as a function of the duty cycle D.

Fig. 6a shows the S-R noise PSD for different values of the duty-cycle D, highlighting how the conventional model in eq. (12) (dashed line) is different from the *Pnoise* simulation result (solid line) especially at low duty cycle values. To better quantify the accuracy, we report in Fig. 6b the relative error of the conventional model in (12) with respect to *Pnoise* simulations for different duty cycles.

The values of both the maximum (259%) and average (75%) relative error confirm that the conventional model in (12) is not able to adequately describe the cyclostationary noise in S-R circuits for duty cycle values lower than about 1%.

This is due to the fact that the conventional model in (12) does not take into account the effective noise sources and how noise propagates to the output. As an additional remark, it has to be noted that, using the approximation R_p/D in place of R_{eq} results in an even higher error between predicted and simulated noise, due also to the poor estimation of R_{eq}.

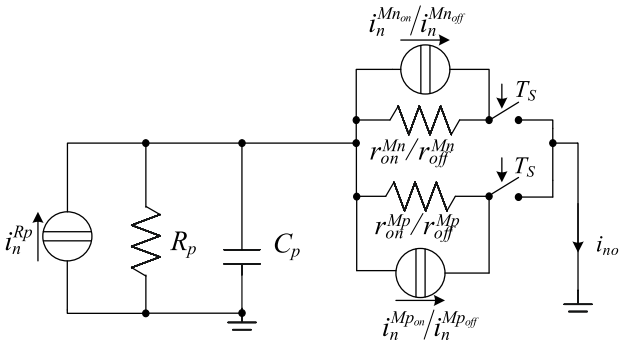

Fig. 7. Equivalent circuit of the switched resistor with all the considered noise sources.

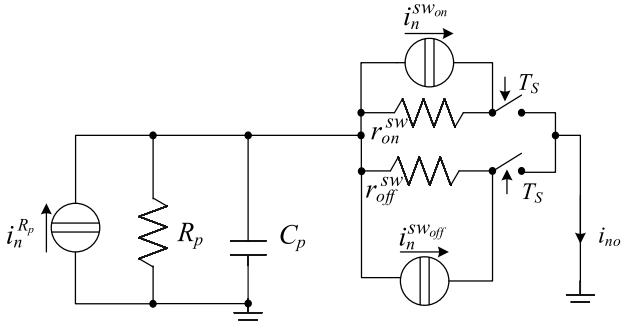

Fig. 8. Simplified equivalent circuit of the switched resistor with counter-phase clock signals driving the switches.

In this paper, in order to develop a model, suitable to accurately describe the cyclostationary noise in S-R circuits, we start from the detailed model of the S-R technique presented in [29] and add to it the most relevant noise sources, thus obtaining the equivalent circuit reported in Fig. 7. The detailed S-R model proposed in [29] is characterized, other than by the parasitic capacitance C_p, also by a finite channel resistance in the *off* state, that significantly affects the average current flowing in the S-R at low duty cycles. Hence the equivalent circuit in Fig. 7 includes five main noise sources:

- the noise source $i_n^{R_p}$ related to the polysilicon resistor R_p;
- the equivalent noise source of each one of the two MOS transistors (the p-channel Mp and the n-channel Mn) implementing the TG switch in the *on* and in the *off* state of the switch itself (denoted as $i_n^{Mn_{on}}$, $i_n^{Mp_{on}}$, $i_n^{Mn_{off}}$ and $i_n^{Mp_{off}}$ respectively).

As shown in Fig. 7, the values of the noise sources due to the MOS transistors of the switch depend on their switching states. In fact, the MOS devices operating in strong inversion (*on* phase) generate a noise which is significantly different from the one obtained when operating MOS transistors in cut-off (*off* phase). In particular, it is found that, for low values of the duty cycle D, the TG switch exhibits a not negligible noise.

It has to be remarked that only white noise sources have been considered in the model; in fact, a preliminary simulation campaign allowed us to verify that flicker noise contributions of MOS transistors are negligible with respect to their white noise counterparts on the integrated noise of the S-R. This point will be better clarified in section IV.

In order to simplify the circuit in Fig. 7, the four noise sources related to the TG switch have been represented with an equivalent noise model that highlights the operating parameters in both the working phases.

In the simplified model reported in Fig. 8, the ideal switches are controlled by clock signals with opposite phases and both the channel resistances and the noise sources of Mp and Mn are substituted with the corresponding equivalent resistances and noise sources as follows:

$$r_{on}^{sw} = r_{on}^{Mn} || r_{on}^{Mp} \tag{13a}$$

$$r_{off}^{sw} = r_{off}^{Mn} || r_{off}^{Mp} \tag{13b}$$

where the symbol || denotes the parallel connection between two resistances.

$$i_n^{sw_{on}} = \sqrt{\left(i_n^{Mn_{on}}\right)^2 + \left(i_n^{Mp_{on}}\right)^2} \tag{14a}$$

$$i_n^{sw_{off}} = \sqrt{\left(i_n^{Mn_{off}}\right)^2 + \left(i_n^{Mp_{off}}\right)^2} \tag{14b}$$

The circuit in Fig. 8 is clearly a LPTV cyclostationary network with sampled output: the clock driving the TG, as shown in Fig. 5, periodically modifies the network changing the value of the switch equivalent resistance from the *on* to the *off* value, and samples the output with a zero-order hold. The approach described in section II can therefore be applied to evaluate the equivalent output noise, sampled by the clock signal, due to the different noise sources. Since different noise sources have to be considered for the TG in the *on* and *off* phases, the approach has to be applied twice, considering the clock signal and its complement.

By applying the adjoint network theory to the equivalent circuit in Fig. 8, the equivalent impulse responses related to the three equivalent noise sources taking into account both the *on* and *off* phases of the TG switch can be computed. These equivalent impulse responses can then be used to evaluate the sampled noise contribution due to each noise source i_n ($i_n^{R_p}$, $i_n^{sw_{on}}$, and $i_n^{sw_{off}}$) according to the block scheme in Fig. 9. The block scheme reported in Fig. 9 highlights that the generic output noise contribution i_{no} related to a specific input noise source i_n has to be calculated by considering two equivalent transfer functions $H_{eq,on}$ and $H_{eq,off}$.

Each one of these equivalent functions is computed by applying an impulse signal $\delta(t)$ to the adjoint circuit in each one of the two working phases as will be better detailed in the following. Fig. 9 also shows that the filtered signals are sampled with period T_S. Since a clock with duty cycle D is used for sampling, a zero-order hold (ZOH) block has to be considered. This can be modelled with a rectangular function *Rect*(t) whose hold time is different for the two clock phases.

In particular, the hold time is DT_S for the *on* phase (block *ZOH(D)* in Fig. 9) and (1-*D*)T_S for the *off* phase (block *ZOH(1-D)* in Fig. 9). Fig. 10 illustrates the sampling instants of the two *ZOH* blocks which are at T_s^- in the *off* phase and at T_s^+ in the *on* phase respectively. In the following subsection *A*, we compute the adjoint network related to the noise sources $i_n^{R_p}$, whereas in subsection *B* we work on $i_n^{sw_{on}}$, and $i_n^{sw_{off}}$.

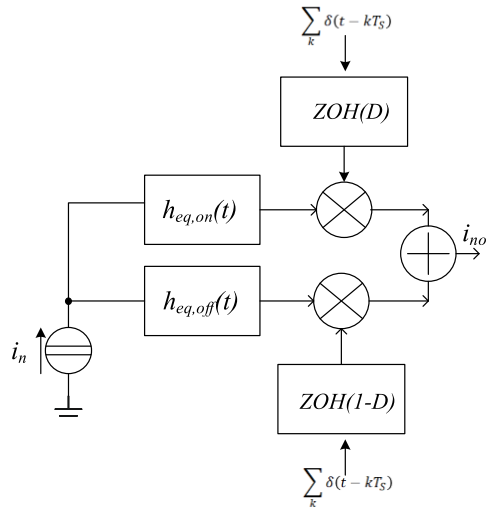

Fig. 9. Block scheme for the computation of the output noise contribution related to the generic input noise source i_n.

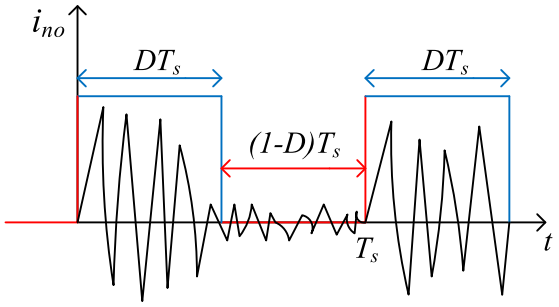

Fig. 10. Sampling instants of the two *ZOH* blocks which are at T_s^- in the *off* phase and at T_s^+ in the *on* phase respectively.

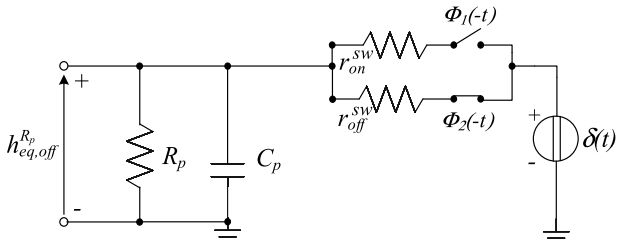

Fig. 11. Adjoint circuit for the computation of the output noise due to the noise source $i_{n,Rp}$ in the off phase.

Finally at the end of this section we will combine the different contributions in order to determine the PSD of the output noise of the S-R circuit.

A. Adjoint Network for Computation of the Noise Contribution Due to the Polysilicon Resistor $i_n^{R_p}$

The adjoint network to calculate the equivalent transfer function related to the noise source of the polysilicon resistor R_p is shown in Fig. 11.

An impulse voltage source $\delta(t)$ is applied at the port where the short-circuit current is measured in Fig. 8, and the output voltage is taken across the resistor R_p, where the current noise source were applied in the original circuit. The switch is modelled by two resistors (r_{on}^{sw} and r_{off}^{sw}) with in series ideal switches controlled by clock signals with opposite

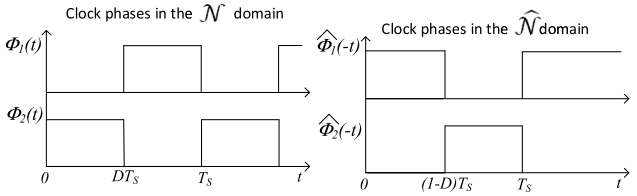

Fig. 12. Clock phases in the $\mathcal{N}$ and in the $\widehat{\mathcal{N}}$ domains.

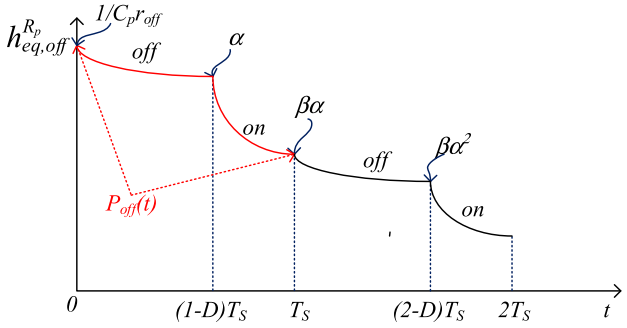

Fig. 13. $h_{eq,off}^{R_p}(t)$ as a function of time highlighting the periodic discharge.

phases, as better detailed in Fig. 12, that also highlights the relationship between the clock phases in the original and adjoint networks.

We evaluate the equivalent impulse response when an ideal impulse signal is applied in any time instant t belonging to the interval $[0, (1-D)\,T_s]$ (*off* phase), given by the open-circuit voltage across R_p:

$$h_{eq,off}^{R_p}(t) = \frac{1}{C_p r_{off}} e^{-\frac{t}{\tau_{off}}} u_{-1}(t) \tag{15}$$

$$\tau_{off} = C_p (R_p || r_{off}) \tag{16}$$

where $u_{-1}(t)$ is the unitary step function. Once the memory element has been charged through the impulse signal, we can analyze the periodic decay of the charge across the parasitic capacitor C_p, illustrated in Fig. 13, determining from it the recursive equation describing the phenomenon [24], [25]. Fig. 13 clearly demonstrates what was modeled in (5), i.e. that the overall impulse response can be seen as a sum of time-shifted nonperiodic impulse responses.

The discharge voltage across the capacitor, and therefore the equivalent impulse response, is characterized by a periodic trend, in which the time constant of the discharge changes its value during each clock cycle according to the clock value as shown by the following equations:

$$h_{eq,off}^{R_p}(t) = \frac{1}{C_p r_{off}} e^{-\frac{t}{\tau_{off}}}$$
$$0 < t < (1-D)\,T_s \tag{17a}$$

$$h_{eq,off}^{R_p}(t-(1-D)\,T_s) = \frac{\alpha}{C_p r_{off}} e^{-\frac{t-(1-D)T_S}{\tau_{on}}}$$
$$(1-D)\,T_s < t < T_s$$

$$h_{eq,off}^{R_p}(t-T_s) = \frac{\alpha\beta}{C_p r_{off}} e^{-\frac{t-T_S}{\tau_{off}}} \tag{17b}$$

where

$$T_s < t < (2-D)T_s \tag{17c}$$

$$\tau_{on} = C_p(R_p||r_{on}) \tag{18}$$

$$\alpha = e^{-\frac{(1-D)T_S}{\tau_{off}}} \tag{19}$$

$$\beta = e^{-\frac{DT_S}{\tau_{on}}} \tag{20}$$

From the equations (17) describing the recursive phenomenon [24] we obtain:

$$\begin{aligned} h_{eq,off}^{R_p}(t) &= p_{off}(t) + \gamma\, h_{eq,off}(t - T_s) \\ &= \sum_{i=0}^{\infty} \gamma^i\, p_{off}(t - iT_s) \end{aligned} \tag{21}$$

where

$$\gamma = \alpha\beta \tag{22}$$

The function $p_{off}(t)$, drawn in Fig. 13, describes the exponential decay of the equivalent impulse response in the first working interval $0 < t < T_s$ after the impulse has been applied and can be expressed as the sum of two terms $p_{off,A}(t)$ and $p_{off,B}(t)$ defined in each half period as follows:

$$p_{off}(t) = p_{off,A}(t) + p_{off,B}(t) \tag{23}$$

$$p_{off,A} = \frac{1}{C_p r_{off}} e^{-\frac{t}{\tau_{off}}} \left[u_{-1}(t) - u_{-1}(t - (1-D)T_s)\right] \tag{24a}$$

$$\begin{aligned} p_{off,B}(t) = \frac{\alpha}{C_p r_{off}} e^{-\frac{t-(1-D)T_S}{\tau_{on}}} &[u_{-1}(t - (1-D)T_s) \\ &- u_{-1}(t - T_s)] \end{aligned} \tag{24b}$$

The two equations (24) describe the discharge of C_p through the switch in the *off* and *on* phases, respectively. Applying the Fourier transform at the recursive impulse function we obtain the equivalent frequency response in the *off* state:

$$H_{eq,off}^{R_p}(f) = P_{off}(f) + \gamma\, H_{eq,off}^{R_p}(f)\, e^{-j2\pi f T_s} \tag{25}$$

$$H_{eq,off}^{R_p}(f) = \frac{P_{off}(f)}{1 - \gamma\, e^{-j2\pi f T_s}} \tag{26}$$

By transforming also the $p_{off}(t)$ function in frequency domain we can explicitly express the equivalent frequency response as a function of circuit parameters.

$$\begin{aligned} P_{off,A}(f) = &\frac{1}{C_p r_{off}} \frac{\tau_{off}}{1 + j2\pi f \tau_{off}} \\ &\times (1 - \alpha e^{-j2\pi f T_s(1-D)}) \end{aligned} \tag{27a}$$

$$\begin{aligned} P_{off,B}(f) = &\frac{\alpha}{C_p r_{off}} \frac{\tau_{on}}{1 + j2\pi f \tau_{on}} e^{-2\pi f T_s(1-D)} \\ &\times (1 - \beta e^{-j2\pi f T_s D}) \end{aligned} \tag{27b}$$

Hence, after algebraic manipulation, $H_{eq,off}^{R_p}$ turns into:

$$\begin{aligned} H_{eq,off}^{R_p}(f) = &\frac{1}{1 - \gamma\, e^{-j2\pi f T_s}} \\ &\cdot \left(\frac{k_{off}}{1 + j2\pi f \tau_{off}} (1 - \alpha e^{-j2\pi f T_s(1-D)}) \right. \\ &+ \frac{r_{on}}{r_{off}} \frac{\alpha k_{on}}{(1 + j2\pi f \tau_{on})} e^{-2\pi f T_s(1-D)} \\ &\left. \times\, (1 - \beta e^{-j2\pi f T_s D}) \right). \end{aligned} \tag{28}$$

$$k_{on} = \frac{R_p}{R_p + r_{on}} \tag{29a}$$

$$k_{off} = \frac{R_p}{R_p + r_{off}} \tag{29b}$$

According to Fig. 9, the output noise component due to the noise source $i_n^{R_p}$ is obtained combining both the equivalent frequency responses in the *off* and *on* phases. In order to compute the equivalent frequency response in the *on* phase, defined when the impulse signal is applied in any instant t belonging to the time interval $[(1-D)T_s,\ T_s]$ we can follow the same steps made for the computation in the *off* state. In this case, the impulse signal is applied at the beginning of the time interval $[(1-D)T_s,\ T_s]$, resulting in a clock configuration shifted with respect to the *off*-state clock configuration by a quantity dependent on D. By analyzing the adjoint circuit in Fig. 14, the equivalent impulse response $h_{eq,on}^{R_p}$ can be computed as:

$$h_{eq,on}^{R_p}(t) = \frac{1}{C_p r_{on}} e^{-\frac{t}{\tau_{on}}} u_{-1}(t) \tag{30}$$

resulting in the transfer function, as in (31), shown at the bottom of the next page.

B. Adjoint Network for the Computation of the Noise Contributions Due to the TG Switch Input Noise Sources

A similar analysis can be repeated for what concerns the noise sources associated with the TG switch: as shown in Fig. 15, the impulse input voltage is still applied at the port 2 of the adjoint network, but now the output voltage is taken across the switch resistance. More in detail, we are interested in calculating the transfer functions related both to the noise produced by the switch in the *on* phase $i_n^{sw_{on}}$ and to the noise produced in the *off* phase $i_n^{sw_{off}}$, thus in the adjoint network the output has to be taken both across the resistance r_{on}^{sw} and r_{off}^{sw}. In both cases, the sampling instant can be both in the *on* phase and in the *off* phase, thus the impulse input voltage has to be applied both in the time interval $[0, (1-D)T_s]$ (*off* phase) and in the time interval $[(1-D)T_s,\ T_s]$, (*on* phase). We consider initially the equivalent impulse response when the impulse voltage $\delta(t)$ is applied in any time instant t belonging to the interval $[0, (1-D)T_s]$ (off phase).

After the application of $\delta(t)$, the voltage drop across the resistance r_{off}^{sw} depends on the charge stored in the parasitic capacitor C_p as follows:

$$h_{eq,off}^{sw_{off}}(t) = \delta(t) - \frac{1}{C_p r_{off}} e^{-\frac{t}{\tau_{off}}} \quad 0 < t < (1-D)T_s \tag{32}$$

The periodic decay of the charge, reported in Fig. 16, allows us to deduce the recursive equation as we did in the previous subsection. In this case, for $(1-D)T_s < t < T_s$, the equivalent impulse response is equal to zero, since the switch connected to r_{off}^{sw} is open ($r_{off}^{sw} I = 0$).

The periodic discharge process, shown in Fig. 16, highlights a discontinuous trend, in which the discharge process of the capacitor goes on through the R_p and r_{on}^{sw} resistances. We can write for the successive phases:

$$\begin{aligned} &h_{eq,off}^{sw_{off}}(t) = \delta(t) - \frac{1}{C_p r_{off}} e^{-\frac{t}{\tau_{off}}} \\ &0 < t < (1-D)T_s \end{aligned} \tag{33a}$$

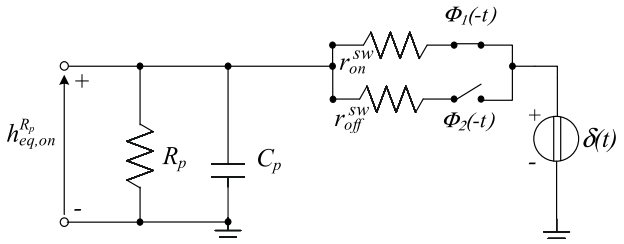

Fig. 14. Adjoint circuit for the computation of the output noise due to the noise source $i_{n,Rp}$ in the on phase.

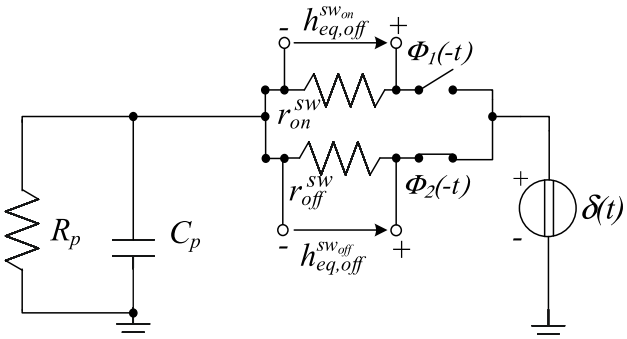

Fig. 15. Adjoint circuit for the computation of the output noise due to the noise source $i_{n,sw}$ in the off phase.

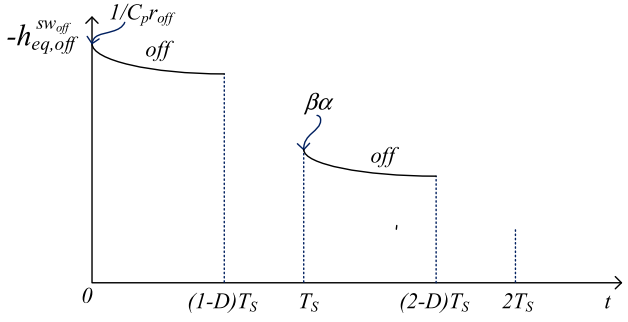

Fig. 16. Graph of $-h_{eq,off}^{sw_{off}}(t)$ vs. time highlighting periodic and discontinuous discharge.

$$h_{eq,off}^{sw_{off}}\left(t-(1+m-D)\,T_s\right)=0$$
$$mT_s+(1-D)\,T_s<t<T_s\,(m+1)\quad m=0,1,2\ldots \tag{33b}$$

$$h_{eq,off}^{sw_{off}}\left(t-T_s\right)=-\frac{\gamma^{\,i}}{C_p r_{off}}e^{-\frac{t-iT_S}{\tau_{off}}}$$
$$iT_s<t<(2-D)\,T_s+iT_s\quad i=1,2\ldots \tag{33c}$$

To obtain the recursive equation of the equivalent impulse response $h_{eq,off}^{sw_{off}}(t)$ we need to consider the impulse $\delta(t)$ separately from the periodic discharge component, getting the following:

$$h_{eq,off}^{sw_{off}}(t)=\delta(t)-\widehat{h_{eq,off}^{sw_{off}}}(t) \tag{34}$$

The recursive component of $h_{eq,off}^{sw_{off}}(t)$ resides inside $\widehat{h_{eq,off}^{sw_{off}}}(t)$, which is possible to rewrite through the $P_{off,A}$ function, already defined in the previous subsection, thus obtaining:

$$\widehat{h_{eq,off}^{sw_{off}}}(f)=\frac{P_{off,A}(f)}{1-\gamma\,e^{-j2\pi fT_S}} \tag{35}$$

Combining the equation (27a) with (35), we obtain the equivalent frequency response related to r_{off}^{sw} in the *off* phase:

$$H_{eq,off}^{sw_{off}}(f)=1-\frac{\frac{k_{off}}{1+j2\pi f\tau_{off}}(1-\alpha e^{-j2\pi fT_s(1-D)})}{1-\gamma\,e^{-j2\pi fT_S}} \tag{36}$$

In the same way, we can compute the impulse response $h_{eq,off}^{sw_{on}}(t)$ taking the output across r_{on}^{sw}, still considering the input applied in the time interval $[0,(1-D)\,T_s]$. In this case, at the application time of the impulse the switch connected to r_{on}^{sw} is open, and consequently the impulse response is equal to zero in the first semi-period.

$$h_{eq,off}^{sw_{on}}(t)=0\quad 0<t<(1-D)\,T_s \tag{37}$$

For the successive phases, equations similar to (33) can be written to describe the discharge of C_p, but considering the alternate phases, as shown in Fig. 17::

$$h_{eq,off}^{sw_{on}}(t-nT_s)=0\quad nT_s<t<(1-D)\,T_s+nT_s$$
$$n=0,1,.. \tag{38a}$$

$$h_{eq,off}^{sw_{on}}\left(t-(1+h-D)\,T_s\right)=-\frac{\alpha\gamma^{\,h}}{C_p r_{off}}e^{-\frac{t-hT_s-(1-D)T_S}{\tau_{on}}}$$
$$\times hT_s+(1-D)\,T_s<t<T_s\,(1+h)\quad h=0,1,.. \tag{38b}$$

Also in this case we can rewrite (38) in a recursive form, exploiting the function $P_{off,B}$ already defined in the previous subsection:

$$h_{eq,off}^{sw_{on}}(t)=-p_{off,B}(t)-\gamma\,h_{eq_{off}}^{SW_{on}}(t-T_s) \tag{39}$$

After computing the Fourier transform of the recursive equation (39) and substituting the expression of $P_{off,B}(f)$ (27b)

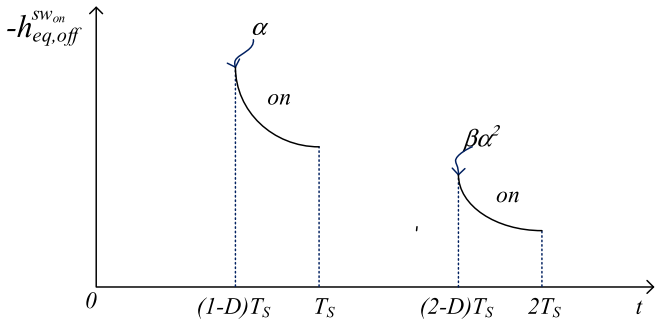

Fig. 17. Graph of $-h_{eq,off}^{sw_{on}}(t)$ vs. time highlighting periodic and discontinuous discharge.

$$H_{eq,on}^{R_p}(f)=\frac{\frac{k_{on}}{1+j2\pi f\tau_{on}}(1-\beta e^{-j2\pi fT_sD})+\frac{r_{off}}{r_{on}}\left(\frac{\beta k_{off}}{1+j2\pi f\tau_{off}}\right)e^{-2\pi fT_sD}(1-\alpha e^{-j2\pi fT_s(1-D)})}{1-\gamma\,e^{-j2\pi fT_s}} \tag{31}$$

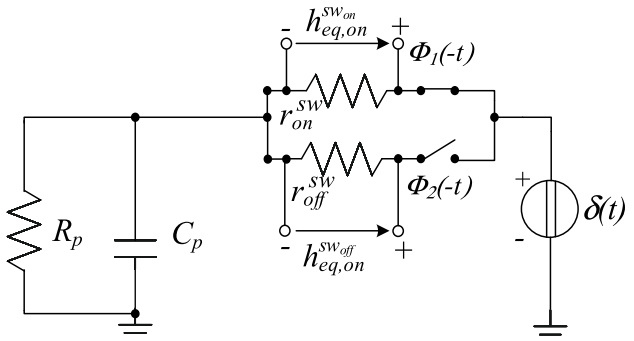

Fig. 18. Adjoint circuit for the computation of the output noise due to the noise source $i_{n,sw}$ in the on phase.

into it, we get the equivalent frequency response related to $i_n^{sw_{on}}$ in the *off* state:

$$H_{eq,off}^{sw_{on}}(f) = -\frac{\frac{\alpha r_{on}}{r_{off}}\left(\frac{K_{on}}{1+j2\pi f\tau_{on}}\right)e^{-2\pi f T_s(1-D)}\left(1-\beta e^{-j2\pi f T_s D}\right)}{1-\gamma e^{-j2\pi f T_S}} \quad (40)$$

The same analysis has to be repeated for an impulse input voltage applied in the time interval $[(1-D)T_s,\ T_s]$, (*on* phase), to calculate the transfer functions related to the noise sources $i_n^{sw_{on}}$ and $i_n^{sw_{off}}$ for a sampling instant in the *on* phase. From the analysis of the adjoint network in Fig. 18, following the procedure already described, we obtain:

$$H_{eq,on}^{sw_{on}}(f) = 1 - \frac{\frac{k_{on}}{1+j2\pi f\tau_{on}}\left(1-\beta e^{-j2\pi f T_s D}\right)}{1-\gamma e^{-j2\pi f T_S}} \quad (41a)$$

$$H_{eq,on}^{sw_{off}}(f) = -\frac{\frac{\beta r_{off}}{r_{on}}\frac{k_{off}}{(1+j2\pi f\tau_{off})}e^{-2\pi f T_s D}\left(1-\alpha e^{-j2\pi f T_s(1-D)}\right)}{1-\gamma e^{-j2\pi f T_S}} \quad (41b)$$

C. Complete Model of Cyclostationary Noise in S-R Circuits

The evaluation of all the equivalent frequency responses in the previous subsections allows us to assemble the complete model of cyclostationary noise in S-R circuits. At this purpose, denoting with $S_n^{R_p}$, $S_n^{sw_{on}}$ and $S_n^{sw_{off}}$ the PSD of the noise sources $i_n^{R_p}$, $i_n^{sw_{on}}$ and $i_n^{sw_{off}}$ respectively, we can exploit the block scheme in Fig. 9 to compute the PSD of the overall output noise. As a first step we compute the overall output noise PSD in the *on* phase $S_{on}(f)$ as follows:

$$S_{on}(f) = S_n^{R_p}(f)\left|H_{eq,on}^{R_p}(f)\right|^2 + S_n^{sw_{on}}(f)\left|H_{eq,on}^{sw_{on}}(f)\right|^2 + S_n^{sw_{off}}\left|H_{eq,on}^{sw_{off}}(f)\right|^2 \quad (42a)$$

and in the *off* phase $S_{off}(f)$ as follows:

$$S_{off}(f) = S_n^{R_p}(f)\left|H_{eq,off}^{R_p}(f)\right|^2 + S_n^{sw_{on}}(f)\left|H_{eq,off}^{sw_{on}}(f)\right|^2 + S_n^{sw_{off}}\left|H_{eq,off}^{sw_{off}}(f)\right|^2 \quad (42b)$$

Then, we apply the sampling operation with a square wave, that provides the contribution of noise folding. Starting from

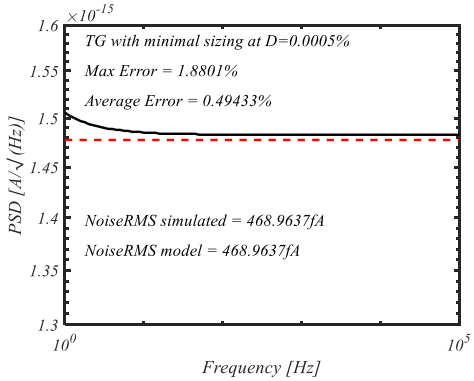

Fig. 19. PSD of the output noise current of the S-R estimated by *Pnoise* simulation (solid line) and the proposed model (dashed line) vs. frequency.

equations (42), their relative sampled PSDs in each working phase are obtained as follows:

$$Sampled_{on}(f) = \sum_{k=-\infty}^{\infty} D^2 Sinc(Dk)^2 S_{on}\left(f-\frac{k}{T_s}\right) \quad (43a)$$

$$Sampled_{off}(f) = \sum_{k=-\infty}^{\infty}(1-D)^2 \times Sinc((1-D)k)^2 S_{off}\left(f-\frac{k}{T_s}\right) \quad (43b)$$

Finally, combining (42) and (43), the complete expression of the cyclostationary noise PSD in a S-R can be computed as shown in the equations (44), as shown at the bottom of the next page.

IV. Validation Results

The proposed noise model has been validated considering a S-R implemented in the 130nm CMOS technology from STMicroelectronics using low-leakage MOS devices. A high resistivity polysilicon resistor with nominal resistance R_p of $100k\Omega$ and an associated parasitic capacitance C_{Rp} of $9.18fF$ has been used to implement the S-R circuit. The TG switch has been implemented with minimum sized MOS devices resulting in r_{on}^{sw} about equal to $13.83k\Omega$ and r_{off}^{sw} in the $T\Omega$ range. The TG switch is driven by a 100kHz clock signal whose duty cycle D is varied from 0.0001% to 100%.

Periodic steady state (*PSS*), and periodic noise (*Pnoise*) simulations are used to estimate the noise PSD as a function of the duty cycle D. The number of harmonic tones in the *PSS* and *Pnoise* simulations has been set to 1,000 and 50 respectively.

The analytical model developed in the previous sections has been approximated using a finite number of spectral replicas k equal to the number of harmonic tones considered in the *Pnoise* simulation. The PSD of the output noise of the S-R is reported in Fig. 19 for $D = 0.0005\%$ showing how the proposed model agrees well with simulation results in spite of the very low value of the duty cycle. In fact, even if we have neglected flicker noise in the model, the average and maximum relative error across the frequency range from $1Hz$ to $100kHz$ are lower than 0.5% and 1.9% respectively. Furthermore, the RMS noise (integrated from $1Hz$ to $100kHz$)

TABLE I
VALUES OF C_p ASSOCIATED TO DIFFERENT VALUES OF R_p

Polysilicon resistance R_p	Parasitic capacitance C_p
$100k\Omega$	9.18fF
$75k\Omega$	6.96fF
$50k\Omega$	4.72fF
$25k\Omega$	2.47fF
$1k\Omega$	0.32fF

from the simulation and from the model are almost identical to each other. Since the Switched-Resistor is often exploited to implement tunable resistances, it is important to provide a validation of its model across a wide range of duty-cycle and circuit parameters values.

The PSD @ $1kHz$ of the output noise current of the S-R estimated by *Pnoise* simulation (solid line) and the proposed model (dashed line) is reported in Fig. 20 as a function of the duty cycle D. Referring to Fig. 20, we can observe different dominant noise contributions for different values of D.

More in detail, for low values of D the dominant noise contribution is the white component of MOS devices in the TG switch and the noise coming from the polysilicon resistor is negligible. On the contrary, the noise coming from the polysilicon resistor becomes dominant for duty cycle values higher than 0.1%. The relative error between *Pnoise* simulation and the proposed noise model vs. D (referring to the traces in Fig. 20) is reported in Fig. 21, showing how the proposed model exhibits a maximum relative error of 9.8% for values of D in which noise contributions of the TG and the polysilicon resistor result quite similar to each other. The average relative error across the duty-cycle range is 2.3% confirming the good accuracy of the proposed model. Similar results have been obtained by evaluating the PSD at 1Hz.

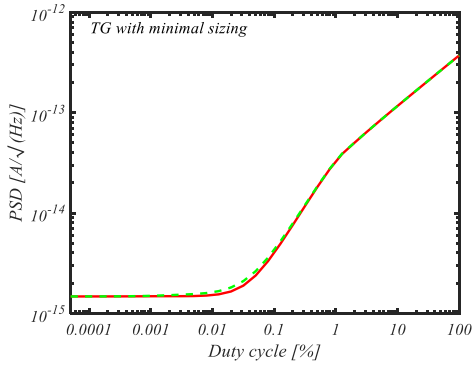

Fig. 20. PSD @ $1kHz$ of the output noise current of the S-R estimated by *Pnoise* simulation (solid line) and the proposed model (dashed line) vs. D.

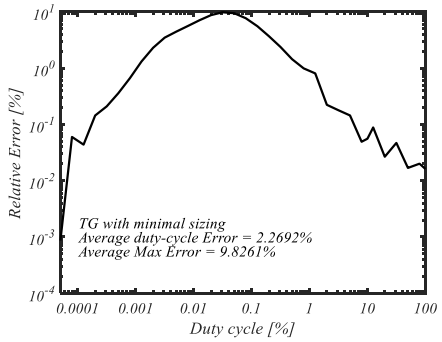

Fig. 21. Relative error between *Pnoise* simulation and the proposed model vs. D in the estimation of the PSD @ $1kHz$ of the output noise current of the S-R.

A. Validation of the Model When Varying Circuit Parameters

A more complete model validation has been carried out by considering the variations of main circuit parameters such as the width and length of MOS transistors implementing the TG switch and the value of the polysilicon resistor R_p with the associated parasitic capacitance C_p.

Fig. 22 shows the maximum (a) and average (b) relative error (@ $1kHz$) of the proposed model with respect to the Pnoise simulation across the whole D range as a function of the width W of MOS transistors implementing the TG switch by keeping the length L equal to the minimum allowed by the technology. The maximum relative error is also in this

$$S_{S-R}(f) = S_{n,s}^{R_p} + S_{n,s}^{sw_{on}} + S_{n,s}^{sw_{off}} \tag{44a}$$

$$S_{n,s}^{R_p} = \sum_{k=-\infty}^{\infty} S_n^{R_p}\left(f-\frac{k}{T_s}\right)\left[D^2 Sinc(Dk)^2\left|H_{eq,on}^{R_p}\left(f-\frac{k}{T_s}\right)\right|^2 + (1-D)^2 Sinc((1-D)k)^2\left|H_{eq,off}^{R_p}\left(f-\frac{k}{T_s}\right)\right|^2\right] \tag{44b}$$

$$S_{n,s}^{sw_{on}} = \sum_{k=-\infty}^{\infty} S_n^{sw_{on}}\left(f-\frac{k}{T_s}\right)\left[D^2 Sinc(Dk)^2\left|H_{eq,on}^{sw_{on}}\left(f-\frac{k}{T_s}\right)\right|^2 + (1-D)^2 Sinc((1-D)k)^2\left|H_{eq,off}^{sw_{on}}\left(f-\frac{k}{T_s}\right)\right|^2\right] \tag{44c}$$

$$S_{n,s}^{sw_{off}} = \sum_{k=-\infty}^{\infty} S_n^{sw_{off}}\left(f-\frac{k}{T_s}\right)\left[D^2 Sinc(Dk)^2\left|H_{eq,on}^{sw_{off}}\left(f-\frac{k}{T_s}\right)\right|^2 + (1-D)^2 Sinc((1-D)k)^2\left|H_{eq,off}^{sw_{off}}\left(f-\frac{k}{T_s}\right)\right|^2\right] \tag{44d}$$

TABLE II
SUMMARY OF RUN-TIME AND AVERAGE ERROR OF THE PROPOSED ANALYTICAL MODEL IMPLEMENTED IN MATLAB VERSUS PSS+PNOISE VIRTUOSO SIMULATIONS

Simulation test-bench	PSS+Pnoise Virtuoso run-time (s)	Analytical Model Matlab run-time (s)	Speed-up	Average Error (%)
Sweep D (Fig. 20)	125.7	4.28	29.4	0.49
Sweep D and W (Fig. 22a-b)	1048	6.7	156.4	1.81
Sweep D and L (Fig. 24a-b)	1045	5.41	193.2	5.3

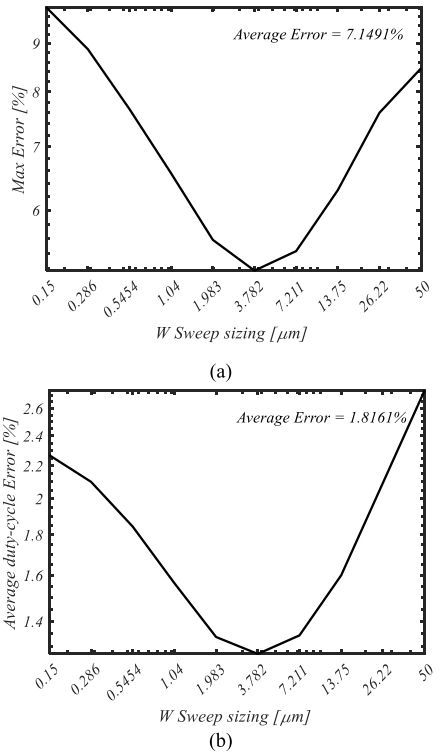

Fig. 22. Maximum (a) and average (b) relative error (@ $1kHz$) of the proposed model with respect to the *Pnoise* simulation across the whole D range as a function of the width W of MOS transistors implementing the TG switch.

case higher for values of D in which noise contributions of the TG and the polysilicon resistor result quite similar to each other. Overall, the average errors over duty cycle ranging from 0.0001% to 100% are below 2.3%, whereas the average error over the considered W values ranging from (0.15 to 50 μm) are below 2.7%. Fig.23 shows the PSD @ $1kHz$ of the output noise current of the S-R estimated by Pnoise simulation and the proposed model versus W for $D = 0.0005\%$, showing a very good agreement between model and simulation results. Similarly, Fig. 24 shows the maximum (a) and average (b) relative error (@ $1kHz$) of the proposed model with respect to Pnoise simulation across the whole D range as a function of the length L of MOS devices implementing the TG switch by keeping the width W equal to the technology minimum. In this case the maximum error approaches 26%, and is much higher than the maximum error over W. Fig. 25 shows the PSD @ $1kHz$ of the output noise current of the S-R estimated by Pnoise simulation and the proposed model versus L for $D = 0.0005\%$.

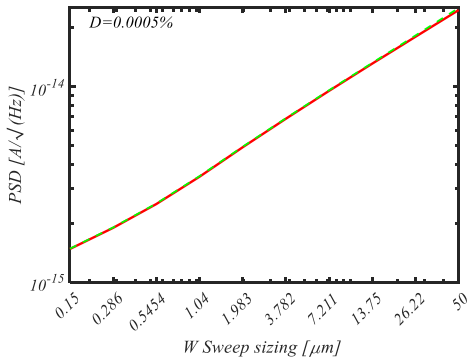

Fig. 23. PSD @ $1kHz$ of the output noise current of the S-R estimated by *Pnoise* simulation (solid line) and the proposed model (dashed line) vs. W for D=0.0005%.

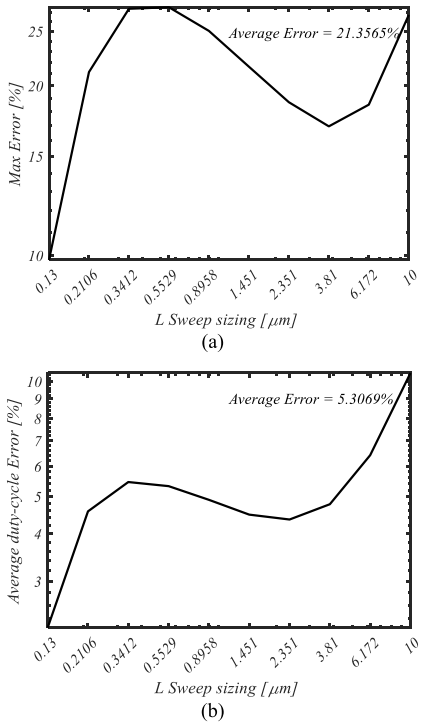

Fig. 24. Maximum (a) and average (b) relative error of the proposed model with respect to the *Pnoise* simulation across the whole D range as a function of the length L of MOS transistors implementing the TG switch.

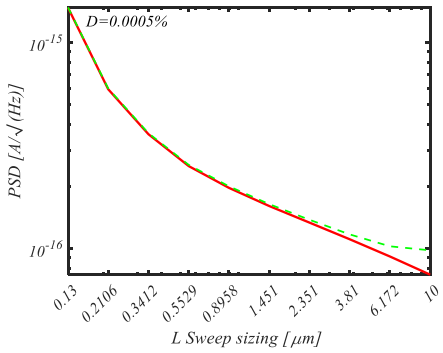

Fig. 25. PSD @ $1kHz$ of the output noise current of the S-R estimated by *Pnoise* simulation (solid line) and the proposed model (dashed line) vs. L for D.

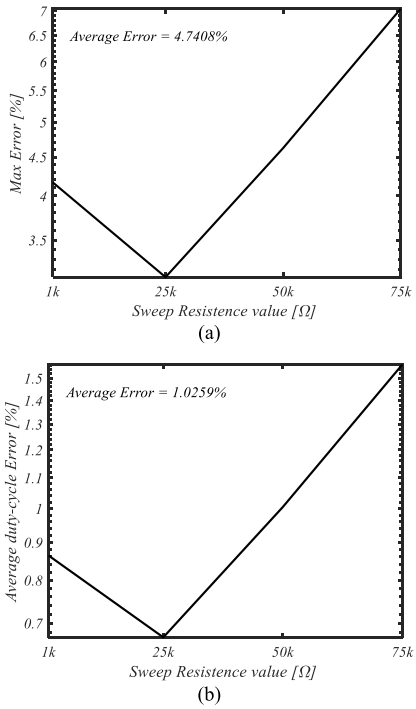

Fig. 26. Maximum (a) and average (b) relative error of the proposed model with respect to *Pnoise* simulation across the whole D range as a function of the value R_p of the polysilicon resistor.

The power spectral density evaluated over the considered values of L highlights a good prediction of the model for the whole L range, except for large value of L (in particular for $L = 10\mu m$), where the Flicker noise contribution is relevant with respect to the white noise contribution. Fig. 26 shows the maximum (a) and average (b) relative error of the proposed model with respect to Pnoise simulation across the whole D range as a function of the value R_p of the polysilicon resistor and the associated value C_p of the relative parasitic capacitance. The resistance values associated to parasitic capacitances for the adopted technology are reported in Table I. The average and maximum error of 4.7% and 1% respectively highlight an accurate prediction of the model for a wide range of R_p values.

Table II summarizes the speed-up and accuracy (in terms of average error) of the proposed analytical model versus the detailed *PSS+Pnoise* circuit simulation for the test-benches used to produce the results reported in Fig. 20, 22 and 24, with the following simulation settings:

- PSS analysis: 1000 harmonics;
- PNOISE analysis: 50 harmonics;
- Number of simulation points in PSS Sweep D: 34 points;
- Number of simulation points in PSS Sweep W and D: 340 points;
- Number of simulation points in PSS Sweep L and D: 340 points;
- PNOISE evaluated a single spot frequency: 1kHz.

We would like to point out that, even if the proposed model is less general than PSS+Pnoise simulations which allow to describe almost all nonlinear circuits with a periodic steady state response, the proposed model is suitable to adequately describe cyclostationary noise in switched resistor applications, and provide a dramatic reduction of simulation run-time as shown in Table II.

V. Conclusion

In this work we have presented a detailed model of the cyclostationary noise in S-R circuits. At this purpose, the theory of the adjoint network applied to LPTV systems has been successfully exploited. The proposed model has been validated by comparing analytical results against *Pnoise* simulations carried out with the design kit of the 130nm CMOS technology from STMicroelectronics. The proposed model exhibits an average relative error across the whole duty cycle range of 2.3%. The average error over the considered W values ranging from (0.15 μm to 50 μm) are below 2.7%. Considering a minimum sized TG switch, the maximum relative error of the model is below 9.8% and this maximum error is found for values of D in which noise contributions of the TG and the polysilicon resistor result quite similar to each other. Due to its accuracy in describing the noise filtering effect of the parasitic capacitances, the proposed model allows a better optimization of the switched resistor (polysilicon value and switch sizing), in terms of the tradeoff between noise performance and linearity, (linearity get worse if the switch resistance is not negligible with respect to the polysilicon resistance).

The proposed analytical model highlights the effect of the different noise sources and the relative transfer functions, allowing to gain insight into the dominant noise contributions and into the effects of the different circuit parameters on the cyclostationary noise. The figures reported in the validation section give a clear picture on the effect of W, L and R_p on the cyclostationary noise of the S-R. As shown in Table II, the proposed analytical model allows a dramatic reduction of simulation run-time especially when design parameters are swept to optimize the circuit.

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Alessandro Fava was born in Rome in 1994. He received the B.Sc. and M.Sc. (cum laude) degrees in electronics engineering from the Sapienza University of Rome, Italy, in December 2017 and October 2020, respectively, where he is currently pursuing the Ph.D. degree in information and communication technology (ICT) with the Department of Information Engineering, Electronics and Telecommunications.

His research interests include integrated circuits design for brain-implanted biomedical devices exploiting analog switching techniques.

Francesco Centurelli (Senior Member, IEEE) was born in Roma, Italy, in 1971. He received the Laurea (cum laude) and Ph.D. degrees in electronic engineering from the University of Roma "La Sapienza," Roma, in 1995 and 2000, respectively.

In 2006, he became an Assistant Professor at the DIET Department, University of Roma La Sapienza. He has published more than 100 papers on international journals and refereed conferences, and has been also involved in research and developed activities held in collaboration between the Università "La Sapienza" and some industrial partners. His research interests include system-level analysis and design of clock recovery circuits and high-speed analog integrated circuits, and now concern the design of analog-to-digital converters and very low-voltage circuits for analog and RF applications.

Giuseppe Scotti (Senior Member, IEEE) was born in Cagliari, Italy, in 1975. He received the M.S. and Ph.D. degrees in electronic engineering from the University of Rome "La Sapienza," Rome, Italy, in 1999 and 2003, respectively. In 2010, he became a Researcher (Assistant Professor) at the DIET Department, University of Rome "La Sapienza," where he was appointed as an Associate Professor in 2015. He teaches undergraduate and graduate courses on basic electronics and microelectronics. In the context of analog design his research activity was concerned with circuit topologies for the realization of low-voltage analog building blocks using ultra-short channel CMOS technology, whereas in the context of cryptographic hardware his focus has been on novel PAAs methodologies and countermeasures. He has been also involved in research and development activities held in collaboration between "La Sapienza" University and some industrial partners, which led, from 2000 to 2015, to the implementation of 13 ASICs. He has coauthored more than 70 publications in international journals, about 70 contributions in conference proceedings, and is the co-inventor of two international patents. His research interests include integrated circuits design and focused on design methodologies able to guarantee robustness with respect to parameter variations in both analog circuits and digital VLSI circuits.

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