The Mismatch Performance of Pseudo Digital Ring Oscillators Used in VCO ADCs: PSRR and CMRR

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***Abstract*— In this work, we focus on the Power Supply Rejection and Common Mode Rejection performance of inverter based ring oscillators intended for use in VCO ADCs. We show that they are closely related to the circuit's mismatch behavior of which we perform a systematic analysis. To this end, we construct a theoretical mismatch model for these ring oscillators, based on Pelgrom's mismatch model. In addition, we generalize this model to include the mismatch in a generic tuning circuit. In this broad analysis, we show that, next to the obvious transistor size dependence, the mismatch is inversely proportional to the number of stages and hence, in theory, can always be suppressed up to the desired level in a VCO ADC, provided that the tune circuit is sized adequately. Furthermore, we demonstrate that the mismatch is dependent on the biasing of the ring, which becomes even more apparent when taking into account the influence of a tuning circuit. More specifically, strong inversion is almost always better than weak inversion, and current control is preferred over voltage control. Finally, we perform extensive Monte Carlo simulations, with a commercially available 65nm CMOS process, which match our analytical predictions nearly perfectly.**

***Index Terms*— VCO-based ADC, ring oscillator, mismatch, PSRR, CMRR.**

I. Introduction

VOLTAGE-Controlled Oscillator (VCO)-based Analog-to-Digital Converters (ADCs) or VCO ADCs have been established as a viable technology for oversampling A/D conversion in a wide range of applications [1], [2], [3], [4], [5], [6], [7], [8], [9]. Advantages of this approach include inherent first-order noise shaping, intrinsic anti-aliasing as well as the fact that the circuits are digital-friendly, enabling enhanced design portability and shorter design cycles [10], [11], [12], [13]. Based on previous work [14], we can distinguish four main performance metrics with respect to VCO ADC systems: linearity, noise, power consumption and sensitivity to interference (e.g. on the power rails) [12], [15], [16]. Linearity issues in VCO ADCs can be tackled by employing proper architectural techniques (e.g. feed-forward, feedback) [12], [17], [18]. Circuit-level improvements also exist in prior art [19], [20] and as a last resort, digital calibration can be used. With all these techniques in mind, linearity is not discussed further. The noise and the associated power consumption were already discussed in [14].

The remaining issue is thus the sensitivity to interference: e.g. inverter based ring oscillators have notoriously bad performance with regard to power supply interference. In VCO ADCs this is commonly tackled by using a pseudo-differential configuration [12]. A study of the effectiveness of this approach, however, has not yet been performed and is exactly the focus of this work. Below, we will show that the *Power Supply Rejection* (PSR) in a pseudo-differential VCO ADC configuration is closely linked to its mismatch performance. Moreover, a similar link with the *Common Mode Rejection* (CMR) will also be established.

There are already numerous publications on the mismatch performance of CMOS devices [21], [22], [23], [24]. In this work, we will build on these results and perform a systematic analysis of the mismatch in three important inverter based ring oscillators.

For this, we will rely on the VCO model proposed in [14]. Based on this VCO model, and Pelgrom's mismatch model proposed in [21], we construct our own theoretical VCO mismatch model in Section II. Afterwards, in Section III, we study the effect of adding a tune circuit to the VCO and its influence on the overall mismatch. This study allows us to analyze the connection between this mismatch behavior and the *Power Supply Rejection* (PSR) and *Common-Mode Rejection* (CMR) of VCO ADCs in a pseudo-differential configuration, which is described in Section IV. To assess the proposed models in the preceding sections, numerous Monte Carlo simulations were performed and are discussed in Section V, with a commercially available 65nm CMOS process. Finally, we present our conclusions in Section VI.

II. Mismatch in VCO Delay Cells

Before starting our actual discussion on mismatch, the following notation is introduced:

$$X = X_n + \Delta X = X_n \cdot (1 + \varepsilon_X) \tag{1}$$

In other words, a parameter can be represented by its actual value X, its nominal value X_n, the deviation ΔX from the nominal value due to mismatch and its relative deviation ε_X.

Fig. 1 shows a simple ring oscillator. The analysis of [14] for such ring oscillators form a very simple dynamic model for every cell: i.e. every kth cell has a falling edge delay, $\tau_{df,k}$ and a rising edge delay $\tau_{dr,k}$. Then the oscillation period can

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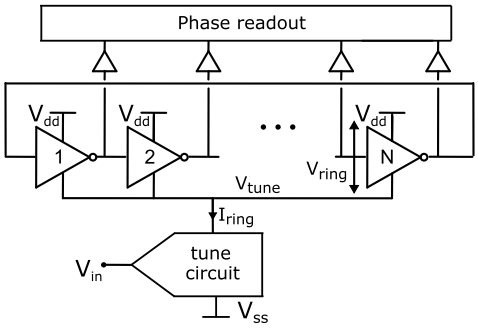

Fig. 1. Schematic of a simple inverter based ring oscillator VCO and its phase readout for use in a VCO ADC.

be written as:

$$T = \sum_{k=1}^{N} (\tau_{df,k} + \tau_{dr,k}) \tag{2}$$

In most VCO ADC designs, all unit cells will be designed (matched) to be nominally equal. Unavoidably, there will be mismatches $\varepsilon_{r,k}$ and $\varepsilon_{f,k}$, both on the rising edge delay as well as on the falling edge delay, making them deviate from their nominal values $\tau_{dr,n}$ and $\tau_{df,n}$. With this in mind, we can rewrite Eq. (2) to include these mismatches:

$$\begin{aligned} T &= \sum_{k=1}^{N} (\tau_{df,n}(1+\varepsilon_{f,k}) + \tau_{dr,n}(1+\varepsilon_{r,k})) \\ &= N(\tau_{df,n} + \tau_{dr,n}) + \sum_{k=1}^{N} (\tau_{df,n}\varepsilon_{f,k} + \tau_{dr,n}\varepsilon_{r,k}) \end{aligned} \tag{3}$$

Now, we introduce the average nominal cell delay $\tau_{d,n}$:

$$\tau_{d,n} = \frac{\tau_{df,n} + \tau_{dr,n}}{2} \tag{4}$$

Such that the weighted average delay mismatch per cell ε_k is:

$$\varepsilon_k = \frac{\tau_{df,n}\varepsilon_{f,k} + \tau_{dr,n}\varepsilon_{r,k}}{2\tau_{d,n}} \tag{5}$$

This approach, from a mismatch standpoint, can also be extended to the effective frequency, which is defined as [14]:

$$\begin{aligned} f_{\text{eff}} &= \frac{2N}{T} = \frac{2N}{2\ N\tau_{d,n} + 2\tau_{d,n}\sum_{k=1}^{N}\varepsilon_k} \\ &\approx \underbrace{\frac{1}{\tau_{d,n}}}_{f_{\text{eff,n}}} \left(1 - \frac{1}{N}\sum_{k=1}^{N}\varepsilon_k\right) \end{aligned} \tag{6}$$

Here $f_{\text{eff,n}}$ stands for the nominal effective VCO frequency, which is equal to $1/\tau_{d,n}$ [14]. Now we obtain the relative VCO frequency error ε_f:

$$\varepsilon_f = -\frac{1}{N}\sum_{k=1}^{N}\varepsilon_k \tag{7}$$

Since mismatch parameters are random parameters that are nominally equal to zero (i.e. their expected value $\mathrm{E}[\varepsilon_k] = 0$), the relative frequency error will also be a random parameter with an expected value $\mathrm{E}[\varepsilon_f] = 0$. We will now investigate the case where these mismatch parameters are independent and are the result of similar random processes and hence their rms value will be the same. This way we can write:

$$\sigma_{\varepsilon_f}^2 = \frac{\sigma_{\varepsilon_k}^2}{N} \tag{8}$$

This equation adds an important element to the system level considerations. While N does not affect the VCO power, input-referred thermal noise (to a 1st-order approximation) or SQNR [11], [14], it does impact the frequency matching, which will be improved by increasing N, the number of VCO unit elements. We will demonstrate below that this also directly translates into improved PSR Ratio (PSRR) and CMR Ratio (CMRR) performance. Note that in [25], [26], [14], [12], and [13] a similar observation was made for the input-referred $1/f$ noise of a ring oscillator. It is important to realize that the number of delay cells, N, also affects the readout performance of the VCO in a VCO-ADC system substantially [27].

We will start our analysis below for the case of ideal voltage control: i.e. the case where the tune circuit drives a fixed voltage V_{ring} on the ring. Later, in section III-B, the analysis will be extended to include current control and an arbitrary tune circuit impedance.

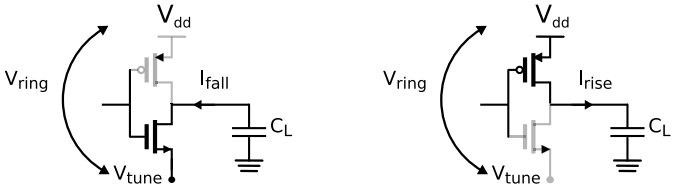

Fig. 2. Switching in a single cell of a simple ring oscillator VCO: (left) falling edge, (right) rising edge.

A. Single-Ended VCO Delay Cell

Before proceeding with the mismatch analysis of the single-ended VCO delay cell, the expression of its cell delay is reprised here from [14], based on Fig. 2.

$$\tau_{df} = \frac{V_{\text{ring}} \cdot C_L}{2 \cdot I_{\text{fall}}} \tag{9}$$

In this expression, τ_{df} is the time needed to toggle the next inverter and I_{fall} is the discharge current, which is assumed constant during the discharge [25]. C_L is the load capacitance seen by the cell and consists of the cell's output capacitance, the input capacitance of the next cell, the input capacitance of the readout buffer and the interconnect capacitance. Finally, V_{ring} is the voltage over the ring, given by:

$$V_{\text{ring}} = V_{\text{dd}} - V_{\text{tune}} \tag{10}$$

Based on the theory presented above and the simple expression obtained for the delay of the single-ended VCO delay cell in Eq. (9), we can proceed with its mismatch analysis. In order to simplify it, we presume that the effect of mismatch is mainly in the cell's discharge current I_{fall} and not in the load capacitance C_L. Additionally, we will adhere to Pelgrom's model [21], rather than resolving to more accurate (but less intuitive) models [23], [24], [28]. According to Pelgrom's model [21], for an NMOS device, both $\beta_N = C_{\text{ox}}\mu W_N/L_N$ and the

threshold voltage $V_{T,N}$ are subject to random mismatch errors with respective variances $\sigma^2_{\beta_N}$ and $\sigma^2_{V_{T,N}}$:

$$\frac{\sigma^2_{\beta_N}}{\beta^2_N} = E\left[\left(\frac{\Delta\beta_N}{\beta_N}\right)^2\right] \approx \frac{A^2_{\beta_N}}{W_N \cdot L_N} \tag{11}$$

$$\sigma^2_{V_{T,N}} = E\left[\left(\Delta V_{T,N}\right)^2\right] \approx \frac{A^2_{V_{T,N}}}{W_N \cdot L_N} \tag{12}$$

where $A^2_{\beta_N}$ and $A^2_{V_{T,N}}$ are technological mismatch parameters (*Pelgrom parameters*) and $W_N \cdot L_N$ corresponds to the transistor gate area. From this, the relative mismatch error on the transistor current can be elaborated into the following expression by simple Taylor expansion:

$$\frac{\Delta I_{\text{fall}}}{I_{\text{fall}}} = \frac{\Delta\beta_N}{\beta_N} + \frac{g_m}{I_{\text{fall}}} \cdot \Delta V_{T,N} \tag{13}$$

Based on Eq. (9), we obtain the inverter falling delay mismatch as meant in Eq. (3), in terms of the current mismatch:

$$\varepsilon_{\text{fall},k} = \frac{\Delta\tau_{df}}{\tau_{df}} = -\frac{\Delta I_{\text{fall}}}{I_{\text{fall}}} \tag{14}$$

Then, by a similar reasoning we obtain the relative error $\varepsilon_{r,k}$ due to mismatch in the rising delay as:

$$\varepsilon_{\text{rise},k} = \frac{\Delta\tau_{dr}}{\tau_{dr}} = -\frac{\Delta I_{\text{rise}}}{I_{\text{rise}}} \tag{15}$$

$$\frac{\Delta I_{\text{rise}}}{I_{\text{rise}}} = \frac{\Delta\beta_P}{\beta_P} + \frac{g_m}{I_{\text{rise}}} \cdot \Delta V_{T,P} \tag{16}$$

In most ring oscillators the NMOS and PMOS transistors will be ratioed in such a way that the rising and falling delays are matched ($I_{\text{fall}} = I_{\text{rise}} = I_{\text{m}}$). Then the weighted average delay mismatch per cell ε_k, as defined in Eq. (5) can be written as:

$$\varepsilon_k = -\frac{1}{2} \cdot \left[\left(\frac{\Delta\beta_N}{\beta_N} + \frac{\Delta\beta_P}{\beta_P}\right) + \frac{g_m}{I_{\text{m}}}\left(\Delta V_{T,N} + \Delta V_{T,P}\right)\right] \tag{17}$$

By substituting Pelgrom's Model we hence obtain:

$$\sigma^2_{\varepsilon_k} = \frac{1}{4}\left[\left(\frac{A^2_{\beta_N}}{W_N \cdot L_N} + \frac{A^2_{\beta_P}}{W_P \cdot L_P}\right) + \left(\frac{g_m}{I_{\text{m}}}\right)^2\left(\frac{A^2_{V_{T,N}}}{W_N \cdot L_N} + \frac{A^2_{V_{T,P}}}{W_P \cdot L_P}\right)\right] \tag{18}$$

And finally, the overall relative frequency error σ_{ε_f} can be obtained by substituting this in Eq. (8). In conclusion, next to the well-known dependence on the transistor size, and the dependence on the number of stages (N) established in Eq. (8), the frequency mismatch is also clearly dependent on the biasing of the ring $\left(\sigma^2_{\varepsilon_k} \sim (g_m/I_{\text{m}})^2 \sim \left(1/V_{\text{ring}} - V_T\right)^2\right)$, with a ring biased in strong inversion substantially outperforming one in weak inversion. This behavior was also observed in [8] and [9], and is backed up here by Eq. (18).

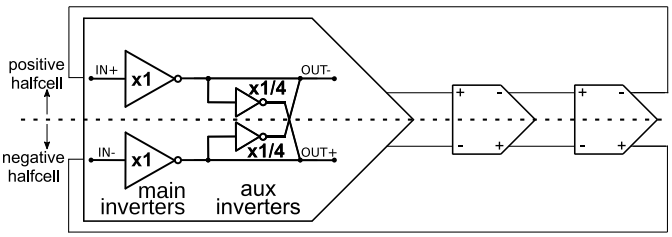

Fig. 3. Schematic of a three-stage voltage-controlled ring oscillator based on the direct cross-coupled delay cell.

B. Differential VCO Delay Cell With Direct Cross-Coupling

Before applying our mismatch model on the differential delay cell with direct cross coupling displayed in Fig. 3, we reprise its expression for the delay here [14]:

$$\tau_{df} = \frac{\tau_{df+} + \tau_{dr-}}{2}, \quad \tau_{dr} = \frac{\tau_{dr+} + \tau_{df-}}{2} \tag{19}$$

where the quantities in the expressions above are given by:

$$\tau_{df+} = \frac{V_{\text{ring}} \cdot C_L}{2 \cdot I_{\text{fall}}}, \quad \tau_{dr+} = \frac{V_{\text{ring}} \cdot C_L}{2 \cdot I_{\text{rise}}} \tag{20}$$

Due to symmetry, the same analysis is valid for the negative half cell, leading to similar expressions for τ_{df-} and τ_{dr-}.

By combining Eqs. (4, 5) and Eq. (19), a similar analysis as for the single-ended cell based on Pelgrom's model, yields the following:

$$\sigma^2_{\varepsilon_k} = \frac{1}{8}\left[\left(\frac{A^2_{\beta_N}}{W_N \cdot L_N} + \frac{A^2_{\beta_P}}{W_P \cdot L_P}\right) + \left(\frac{g_m}{I_{\text{m}}}\right)^2\left(\frac{A^2_{V_{T,N}}}{W_N \cdot L_N} + \frac{A^2_{V_{T,P}}}{W_P \cdot L_P}\right)\right] \tag{21}$$

where W_N, L_N, W_P and L_P stand for the widths and lengths of the NMOS and PMOS transistors respectively of the main inverters. Remark here that this expression for the mismatch is an approximation. The approximation implies that the auxiliary inverters do not affect the mismatch, which is justified by the study in [20]. This study states that the only sensible sizing of these auxiliary inverters is to make them relatively small w.r.t. the main inverters, which implies that in a good design the assumption is always valid.

If we size the main inverter in this differential circuit equal to the inverter in the single-ended circuit, we can compare the resulting mismatch. By comparison with Eq. (18), we see that with such a sizing, the mismatch variance is a factor 2 better. This makes sense, since the delay cell occupies an area that is roughly a factor 2 larger (neglecting the overhead of the auxiliary inverters).

C. Differential VCO Delay Cell With Feed-Forward Cross-Coupling

Finally, the delay for the delay cell showcased in the ring oscillator in Fig. 4, is again defined by Eq. (19), where now the quantities in the expression are given by:

$$\tau_{df+} = \frac{V_{\text{ring}} \cdot C_L}{2 \cdot (I_{M,N} + I_{A,N})} \tag{22}$$

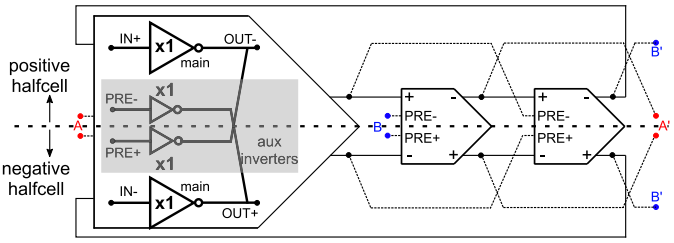

Fig. 4. Schematic of a three-stage voltage-controlled ring oscillator based on feed-forward cross-coupled delay cells. Note: A-A' and B-B' are implicitly connected.

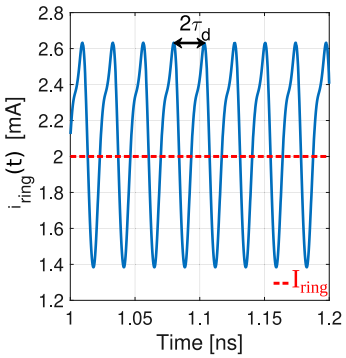

Fig. 5. Current waveform for voltage control of the simple ring oscillator circuit of Fig. 1 based on a case study in [14].

Similar equations can be set up for the rising edge delay τ_{dr+} as well as for the negative half cell delays τ_{df-} and τ_{dr-}.

By subjecting this expression for the delay to the same method as the differential VCO delay cell with direct cross-coupling, we obtain for this cell:

$$\sigma_{\varepsilon_k}^2 = \frac{1}{8(1+\kappa)}\left[\left(\frac{A_{\beta_N}^2}{W_N \cdot L_N} + \frac{A_{\beta_P}^2}{W_P \cdot L_P}\right) + \left(\frac{g_m}{I_m}\right)^2\left(\frac{A_{V_{T,N}}^2}{W_N \cdot L_N} + \frac{A_{V_{T,P}}^2}{W_P \cdot L_P}\right)\right] \quad (23)$$

where κ stands for the ratio of the auxiliary inverter strength over the main inverter strength as in [18], [19], and [20]. For the advocated case in [20] where $\kappa = 1$ (as in Fig. 4), we see that for identically sized main inverters, the matching performance has improved with a factor 2 relative to the other differential delay cell with direct cross coupling (Fig. 3). Again this is very intuitive, since the overall active area is again increased roughly by a factor 2.

III. Adding the Tune Circuit

A. The Link to the VCO's Analog Behavior

Until now, we considered ideal voltage control of the VCO. However, in almost all ring oscillator configurations, it is not driven by an ideal voltage source, but instead by a tune circuit. Hence, the ring current and voltage are set by the electrical interaction of this tune circuit with the ring. To help understand how this works, a diode model was introduced in [14]. Here, the instantaneous ring current $i_{\text{ring}}(t)$ was split in two components: a ripple at very high frequency and a *quasi-static* baseband component I_{ring}, as illustrated in Fig. 5.

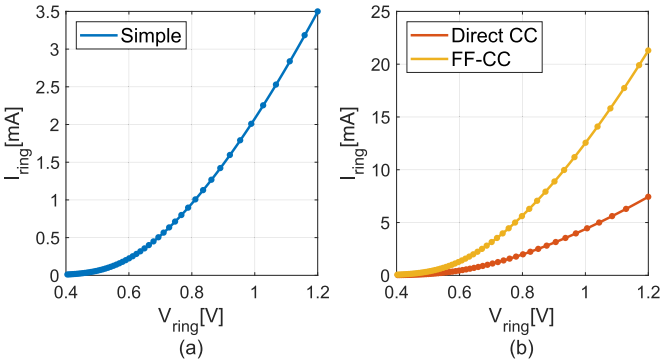

Fig. 6. I_{ring} vs. V_{ring} plots for the sizing of Eq. (74). Left: the simple ring VCO, right: the differential VCOs.

Similarly, the *quasi-static* ring voltage V_{ring} is obtained by removing the voltage ripple. Essentially, it was shown in [14] that the relevant electrical behavior is linked only to the quasi-static components V_{ring} and I_{ring}. Thus, the electrical behavior of the ring is entirely described by its I-V characteristic, illustrated in Fig. 6. This I-V curve is the core characteristic of the ring and can be simulated or approximated analytically. In this work, we have simulated this characteristic and consider it to be known throughout the rest of the manuscript. The effective frequency of Eq. (6) can then be linked to the overall ring current I_{ring} and voltage V_{ring} [14]:

$$f_{\text{eff}} = \frac{2 \cdot I_{\text{ring}}}{V_{\text{ring}} \cdot C_L} \quad (24)$$

In this work, we will convince the reader that also the mismatch behavior is linked only to the quasi-static components V_{ring} and I_{ring}, consolidating the diode-model from [14].

When there is mismatch in circuit, this will lead to a shift in the I-V characteristic. For the case of voltage control, this will lead to a current error ε_I which from Eq. (24) can be understood to be equal to the frequency error of Eq. (7), or:

$$\sigma_{\varepsilon_I} = \frac{\sigma_{\varepsilon_k}}{\sqrt{N}} \quad (25)$$

When we now add the tuning circuit, mismatch in the ring will shift the operating point of the ring and hence there will be both a deviation ΔV_{ring} of the ring voltage as well as a deviation of the ring current ΔI_{ring}. With a Taylor approximation of Eq. (24), we obtain the corresponding frequency error:

$$\varepsilon_{f,\text{tune}} = \frac{\Delta I_{\text{ring}}}{I_{\text{ring,n}}} - \frac{\Delta V_{\text{ring}}}{V_{\text{ring,n}}} \quad (26)$$

B. Tune Circuit Without Mismatch

We will now analyze the shift in the operating point of the ring, when including the tune circuit. To analyze this, the generic tune circuit in Fig. 1 is replaced by its Thévenin equivalent in Fig. 7. The current is now the result of a set of two equations. On the one hand, we have the I-V characteristic of the ring, and on the other hand, we have the load line of

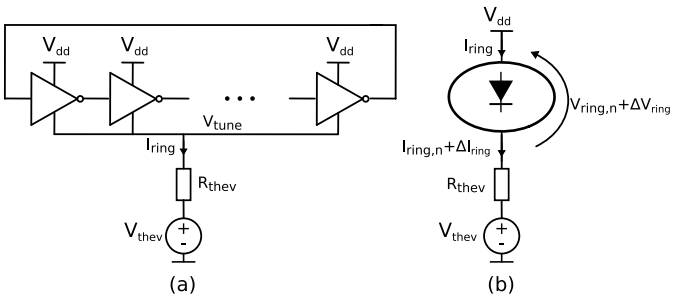

Fig. 7. Simple inverter based ring oscillator VCO (a) with the tune circuit's Thévenin equivalent, and (b) diode model of [14] with the indication that V_{ring} will deviate due to ΔI_{ring}.

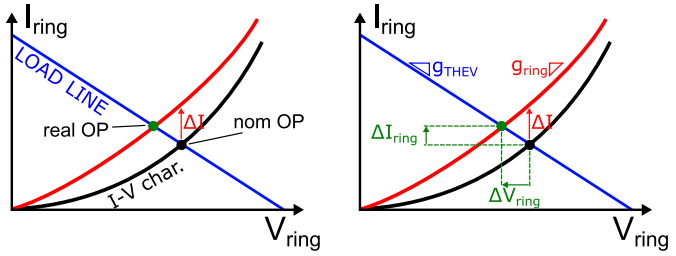

Fig. 8. Influence of the tune circuit on the behavior of the ring current for an arbitrary value of V_{thev}. (Left) Shift of nominal operation point (OP) to real OP, (Right) Associated ring current and voltage mismatch, ΔI_{ring} and ΔV_{ring}.

the tune circuit. When mismatch is introduced in the VCO, we can write this set as equations as displayed below:

$$\begin{cases} I_{\text{ring}}(V_{\text{ring}}) = I_n(V_{\text{ring}}) + \Delta I(V_{\text{ring}}) & \texttt{Ring I-V char.} \\ V_{\text{dd}} = I_{\text{ring}} \cdot R_{\text{thev}} + V_{\text{thev}} + V_{\text{ring}} & \texttt{Load line} \end{cases} \tag{27}$$

In this expression we have written the ring current I_{ring} as the sum of its nominal value I_n, based on the I-V characteristic of the ring and the mismatch with respect to this nominal value ΔI. Remark that both the nominal and the mismatch current are written as function of V_{ring}, see Eqs. (18, 21, 23).

For further investigation, we use a graphical representation of this set of equations in Fig. 8. Now, we can write:

$$\begin{aligned} \Delta I &= \left(g_{\text{ring}} + G_{\text{thev}}\right) \cdot \left(-\Delta V_{\text{ring}}\right) \\ \Delta I_{\text{ring}} &= -G_{\text{thev}} \cdot \Delta V_{\text{ring}} \\ \iff \Delta I_{\text{ring}} &= \Delta I \cdot \frac{G_{\text{thev}}}{g_{\text{ring}} + G_{\text{thev}}} \end{aligned} \tag{28}$$

In this set of equations, $g_{\text{ring}} = r_{\text{ring}}^{-1}$ represents the derivative of the VCO I-V characteristic which, as already established in Section III-A, is a prerequisite for further analysis of the ring. On the other hand, G_{thev} represents the conductance of the Thévenin resistance, R_{thev}. Taking into account that ΔI and ΔI_{ring} both represent an error on the same nominal value $I_{\text{ring,n}}$ (the intersection of the nominal ring I-V characteristic and the load line), the relative error on the ring current, with a tune circuit applied to the ring, can be expressed as:

$$\varepsilon_{I_{\text{ring,tune}}} = \varepsilon_I \cdot \frac{G_{\text{thev}}}{g_{\text{ring}} + G_{\text{thev}}} \tag{29}$$

where we have added subscript *tune*, which denotes that the current mismatch introduced by the VCO (studied in Section II, for which we use the symbol ε_I) is affected by the tune circuit. Its variance can now be written as:

$$\sigma^2_{\varepsilon_{I_{\text{ring,tune}}}} = \sigma^2_{\varepsilon_I} \left(\frac{G_{\text{thev}}}{g_{\text{ring}} + G_{\text{thev}}}\right)^2 = \frac{\sigma^2_{\varepsilon_k}}{N} \left(\frac{r_{\text{ring}}}{r_{\text{ring}} + R_{\text{thev}}}\right)^2 \tag{30}$$

Hence, we can conclude that the tune circuit actually reduces the current mismatch error from the VCO. However, because of the tune circuit, there is now a shift ΔV_{ring} in the ring voltage as well, which can be obtained from Eq. (28):

$$\varepsilon_{V_{\text{ring,tune}}} = -\varepsilon_{I_{\text{ring,tune}}} \cdot R_{\text{thev}} \cdot \frac{I_{\text{ring,n}}}{V_{\text{ring,n}}} \tag{31}$$

From Eqs. (26), (29) and (31), the corresponding overall mismatch in the frequency is obtained:

$$\varepsilon_{f,\text{tune}} = \varepsilon_{I_{\text{ring,tune}}} \cdot \underbrace{\left(1 + R_{\text{thev}} \cdot \frac{I_{\text{ring,n}}}{V_{\text{ring,n}}}\right)}_{\alpha_{\text{tune}}} \tag{32}$$

Here α_{tune} is introduced, which is monotonously rising in function of V_{ring}. Now we can calculate the overall relative frequency error variance $\sigma^2_{\varepsilon_{f,\text{tune}}}$:

$$\begin{aligned} \sigma^2_{\varepsilon_{f,\text{tune}}} &= \sigma^2_{\varepsilon_{I_{\text{ring,tune}}}} \cdot \alpha^2_{\text{tune}} \\ &= \frac{\sigma^2_{\varepsilon_k}}{N} \cdot \left(\frac{r_{\text{ring}}}{r_{\text{ring}} + R_{\text{thev}}}\right)^2 \cdot \alpha^2_{\text{tune}}, \end{aligned} \tag{33}$$

where the cell mismatch variance $\sigma^2_{\varepsilon_k}$ can be obtained for each respective type of delay cell using Eq. (18), (21), or (23).
It is imperative to realize that Eq. (33) is valid for any tune circuit. More specifically, in the case of ideal voltage control ($R_{\text{thev}} = 0$), Eq. (33) reduces to Eq. (8). In the case of ideal current control ($R_{\text{thev}} = \infty$), Eq. (33) can be simplified to:

$$\sigma^2_{\varepsilon_{f,\text{tune}}}\Big|_{R_{\text{thev}}=\infty} = \sigma^2_{\varepsilon_{f,\text{CC}}} = \frac{\sigma^2_{\varepsilon_k}}{N} \cdot \left(r_{\text{ring}} \cdot \frac{I_{\text{ring,n}}}{V_{\text{ring,n}}}\right)^2 \tag{34}$$

By comparing this to the expression for voltage control, Eq. (8), we can conclude that the current control will always lead to better mismatch performance than the voltage control. This can be seen from the fact that the factor $r_{\text{ring}} \cdot \frac{I_{\text{ring,n}}}{V_{\text{ring,n}}}$ is always smaller than 1. This will be confirmed below by the simulation results in Section V-C.

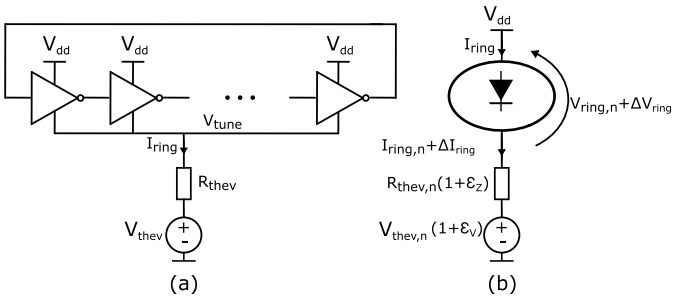

Fig. 9. Simple inverter based ring oscillator VCO (a) with a Thévenin equivalent as input, (b) and with mismatch.

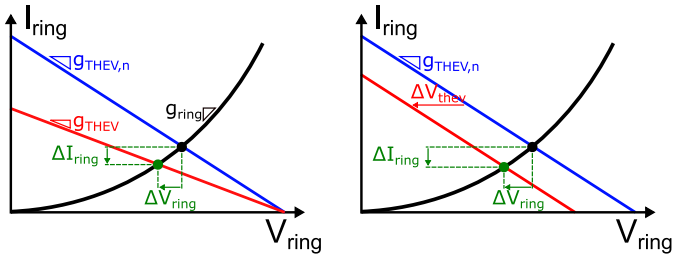

Fig. 10. Influence of mismatch in the tune circuit on the ring current, (left) with mismatch in R_{thev} or (right) mismatch in the open circuit voltage V_{thev}.

C. Tune Circuit With Mismatch - Thévenin as Input

We continue our analysis by introducing mismatch in the tune circuit, which is displayed in Fig. 9. To simplify the analysis, we will consider the case that the VCO is ideal, and hence does not exhibit any mismatch itself. This implies that ΔI_{ring} and ΔV_{ring} in Fig. 9 are the result of variations in the tune circuit. Just as in the previous section, we start with an intuitive graphical representation resulting in Fig. 10. Based on the figure, we can write for both the mismatch in R_{thev} and the mismatch in the open circuit voltage V_{thev} that:

$$\Delta I_{\text{ring}} = g_{\text{ring}} \cdot \Delta V_{\text{ring}} \tag{35}$$

Next, by analysis of the circuit in Fig. 9, we obtain:

$$\Delta V_{\text{ring}} + \varepsilon_V V_{\text{thev,n}} = -R_{\text{thev,n}} \left(\Delta I_{\text{ring}} + \varepsilon_Z I_{\text{ring,n}} \right) \tag{36}$$

Solving Eq. (36) for $\varepsilon_{I_{\text{ring,thev}}} = \frac{\Delta I_{\text{ring}}}{I_{\text{ring,n}}}$ gives:

$$\varepsilon_{I_{\text{ring,thev}}} = -\varepsilon_Z \cdot \frac{R_{\text{thev,n}}}{r_{\text{ring}} + R_{\text{thev,n}}} - \varepsilon_V \cdot \frac{\frac{V_{\text{thev,n}}}{I_{\text{ring,n}}}}{r_{\text{ring}} + R_{\text{thev,n}}} \tag{37}$$

where we have added subscript *thev*, which denotes that it refers to the current mismatch introduced by mismatch in the tune circuit (for which we use the symbols ε_Z and ε_V), not by mismatch in the VCO (which was indicated by the subscript *tune*, and depends on ε_k). Note that the mismatch error in Eq. (37) is independent of the number of VCO delay cells (N). The mismatch in V_{ring} can again be written in function of the mismatch in I_{ring}, based on Eq. (35):

$$\varepsilon_{V_{\text{ring,thev}}} = \varepsilon_{I_{\text{ring,thev}}} \cdot r_{\text{ring}} \cdot \frac{I_{\text{ring,n}}}{V_{\text{ring,n}}} \tag{38}$$

Now, we obtain the overall frequency mismatch due to mismatch in the tune circuit, by substituting the results from Eqs. (37–38) in Eq. (26):

$$\varepsilon_{f,\text{thev}} = \varepsilon_{I_{\text{ring,thev}}} \cdot \underbrace{\left(1 - r_{\text{ring}} \cdot \frac{I_{\text{ring,n}}}{V_{\text{ring,n}}}\right)}_{\alpha_{\text{ring}}} \tag{39}$$

In this expression α_{ring} is introduced, which could be interpreted as a non-linearity parameter of the I-V characteristic (= 0 if perfectly linear). As mentioned before in Section III-A, since the I-V characteristic is known, this α_{ring} is also known, and is displayed in Fig. 11.

Considering the case where the mismatch in R_{thev} and the open circuit voltage V_{thev} are independent from each other,

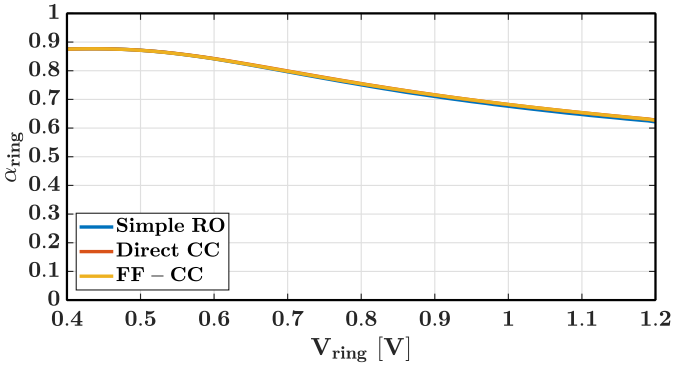

Fig. 11. α_{ring} vs. V_{ring} plot, derived from the simulated I-V characteristics in Fig. 6.

Eq. (39) yields the relative error on the frequency:

$$\begin{aligned}\sigma^2_{\varepsilon_{f,\text{thev}}} &= \sigma^2_{\varepsilon_{I_{\text{ring,thev}}}} \cdot \alpha^2_{\text{ring}} \\ &= \sigma^2_{\varepsilon_Z} \cdot \left(\frac{R_{\text{thev,n}}}{r_{\text{ring}} + R_{\text{thev,n}}} \right)^2 \cdot \alpha^2_{\text{ring}} \\ &\quad + \sigma^2_{\varepsilon_V} \cdot \left(\frac{V_{\text{thev,n}}}{I_{\text{ring}} \cdot \left(r_{\text{ring}} + R_{\text{thev,n}} \right)} \right)^2 \cdot \alpha^2_{\text{ring}}\end{aligned} \tag{40}$$

Clearly this is a quite complex expression. Without going into too much detail, it should be noted that α_{ring} is independent of the ring oscillator type and moderately decreases with increasing values of V_{ring}, see Fig. 11. Note that this is in contrast to the rising behavior of α_{tune}. Later on, the simulations in Section V-D will show that a more pronounced rising characteristic in function of V_{ring} is obtained for the influence of σ_{ε_Z} and a falling characteristic for σ_{ε_V}, which match our predictions of Eq. (40) almost perfectly.

Finally, we can now add the effect of VCO mismatch according to Eq. (33). In the case that the mismatch in the VCO, mismatch in R_{thev} and mismatch in V_{thev} are independent, the total relative frequency error σ_{ε_f} is obtained:

$$\sigma^2_{\varepsilon_f} = \sigma^2_{\varepsilon_{f,\text{tune}}} + \sigma^2_{\varepsilon_{f,\text{thev}}} \tag{41}$$

Remark that it is unlikely that, in a typical Thévenin equivalent, the mismatch in R_{thev} and mismatch in V_{thev} are uncorrelated. In that case, Eq. (37) should be evaluated taking this correlation into account.

D. Tune Circuit With Mismatch - Norton as Input

For instance, consider that a Thévenin equivalent is generated for a current controlled configuration. In this situation, the mismatch in the open circuit voltage will not be independent from the mismatch in the equivalent resistance. As a consequence, Eq. (40) will not be valid. In this section we explore the complementary case of a Norton equivalent as input, displayed in Fig. 12. Again we consider the VCO to be ideal, and hence does not exhibit any mismatch itself. Applying the graphical approach from the previous sections results in a similar figure w.r.t. Fig. 10, displayed in Fig. 13. Based on Fig. 13, we can again write for both the mismatch in R_{thev} and in the short circuit current I_{nort} that:

$$\Delta I_{\text{ring}} = g_{\text{ring}} \cdot \Delta V_{\text{ring}} \tag{42}$$

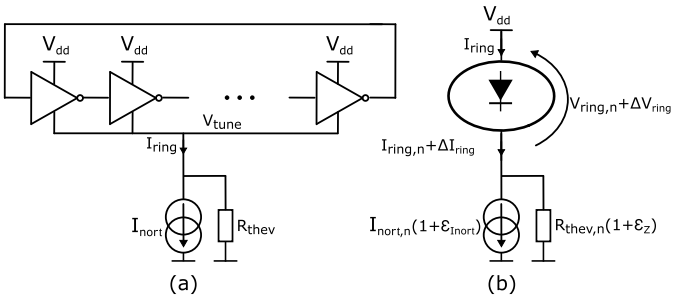

Fig. 12. Simple inverter based ring oscillator VCO (a) with a Norton equivalent as input, (b) and with mismatch.

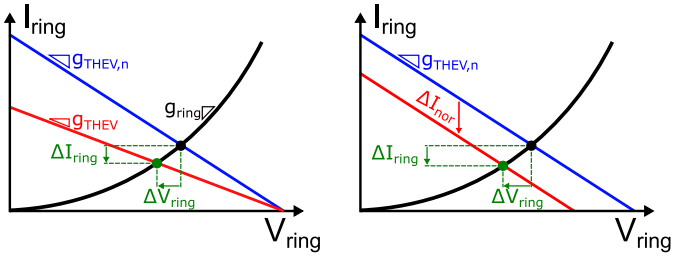

Fig. 13. Influence of mismatch in the tune circuit on the ring current, (left) with mismatch in R_{thev} or (right) mismatch in the short circuit current I_{nort}.

Next, by analysis of the circuit in Fig. 12 we obtain:

$$\Delta V_{\text{ring}} = R_{\text{thev,n}}\left(\varepsilon_{I_{\text{nort}}} I_{\text{nort,n}} - \Delta I_{\text{ring}}\right) + \varepsilon_Z R_{\text{thev,n}}\left(I_{\text{nort,n}} - I_{\text{ring,n}}\right) \quad (43)$$

Solving this equation again for $\varepsilon_{I_{\text{ring,nort}}} = \frac{\Delta I_{\text{ring}}}{I_{\text{ring,n}}}$ gives:

$$\frac{\Delta I_{\text{ring}}}{I_{\text{ring,n}}} = -\varepsilon_Z \cdot \frac{R_{\text{thev,n}}}{r_{\text{ring}} + R_{\text{thev,n}}} \cdot \frac{I_{\text{ring,n}} - I_{\text{nort,n}}}{I_{\text{ring,n}}} + \varepsilon_{I_{\text{nort}}} \cdot \frac{R_{\text{thev,n}}}{r_{\text{ring}} + R_{\text{thev,n}}} \cdot \frac{I_{\text{nort,n}}}{I_{\text{ring,n}}} \quad (44)$$

Now we can link this behavior to an equivalent Thévenin circuit using Eqs. (37,44), and considering that $V_{\text{thev}} = -I_{\text{nort}} \cdot R_{\text{thev}}$ in Fig. 13:

$$\frac{\Delta I_{\text{ring}}}{I_{\text{ring,n}}} = -\varepsilon_Z \cdot \frac{R_{\text{thev,n}}}{r_{\text{ring}} + R_{\text{thev,n}}} - \underbrace{(\varepsilon_Z + \varepsilon_{I_{\text{nort}}})}_{\varepsilon_V} \cdot \frac{\frac{V_{\text{thev,n}}}{I_{\text{ring}}}}{r_{\text{ring}} + R_{\text{thev,n}}} \quad (45)$$

This means that both approaches are equivalent and interchangeable, as long as the correlation between the errors is taken into account, which will be crucial in Section V-C. Now, to obtain the overall cell mismatch, we substitute Eq. (44) into Eq. (39) which yields the following overall relative frequency error in function of σ_{ε_Z} and $\sigma_{\varepsilon_{I_{\text{nort}}}}$:

$$\begin{aligned}\sigma^2_{\varepsilon f,\text{nort}} &= \sigma^2_{\varepsilon_{I_{\text{ring,nort}}}} \cdot \alpha^2_{\text{ring}} \\ &= \sigma^2_{\varepsilon_Z} \cdot \left(\frac{I_{\text{ring,n}} - I_{\text{nort,n}}}{I_{\text{ring,n}}} \cdot \frac{R_{\text{thev,n}}}{r_{\text{ring}} + R_{\text{thev,n}}}\right)^2 \cdot \alpha^2_{\text{ring}} \\ &\quad + \sigma^2_{\varepsilon_{I_{\text{nort}}}} \cdot \left(\frac{I_{\text{nort,n}}}{I_{\text{ring,n}}} \cdot \frac{R_{\text{thev,n}}}{r_{\text{ring}} + R_{\text{thev,n}}}\right)^2 \cdot \alpha^2_{\text{ring}} \end{aligned} \quad (46)$$

Assuming again that the different mismatch contributions are independent from each other, using Eqs. (33,46), the total relative frequency error $\sigma_{\varepsilon f}$ can again be written as:

$$\sigma^2_{\varepsilon f} = \sigma^2_{\varepsilon f,\text{tune}} + \sigma^2_{\varepsilon f,\text{nort}} \quad (47)$$

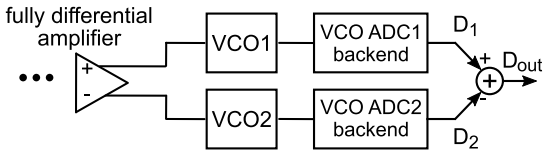

Fig. 14. Pseudo differential VCO ADC configuration.

IV. PSRR and CMRR in Non-Ideal VCO ADCs

We have now finished our mismatch story, where we have shown that the relevant mismatch errors can be written as a function of $\varepsilon_{I_{\text{ring}}}$, which is the sum of a contribution from the VCO (shifted by the tune circuit), $\varepsilon_{I_{\text{ring,tune}}}$, and a contribution from the tune circuit itself, either $\varepsilon_{I_{\text{ring,thev}}}$ (for the Thévenin equivalent) or $\varepsilon_{I_{\text{ring,nort}}}$ (for the Norton equivalent). For the sake of simplicity and clarity, a Thévenin equivalent is chosen as input for the remaining part of this work. Now, we apply this analysis to VCO ADC yielding the PSRR and CMRR in non-ideal VCO ADCs.

We now know that the VCO frequency will deviate from its nominal frequency due to mismatch in the VCO delay cells, according to Eq. (33), and due to mismatch in the tune circuit, according to Eq. (40), or equivalently, Eq. (46). If we now consider the tuning behavior of the VCO, we know that the VCO frequency will depend on the intentional input signal V_{in}. Unfortunately, by simple inspection of Fig. 1, we can immediately see that the power supply terminals (V_{dd} in the figure) also act as a tuning input for the oscillator. In a common linear approximation of a VCO this can be written as:

$$f_{\text{VCO}} = f_0 + K_{\text{V}} V_{\text{in}} + K_{\text{VP}} V_{\text{P}}, \quad (48)$$

where K_{V} is the VCO gain and K_{VP} denotes the ring oscillator sensitivity to disturbances on the power line (represented here by V_{P}). If the VCO is used as a VCO ADC, f_{VCO} will be converted into a digital output value, leading to:

$$D_{\text{single,out}} = D(f_0 + K_{\text{V}} V_{\text{in}} + K_{\text{VP}} V_{\text{P}}) \quad (49)$$

A. Power Supply Rejection Ratio (PSRR)

In most cases, K_{V} and K_{VP} are of the same order of magnitude. E.g. for the case of voltage control they are equal $K_{\text{V}} = K_{\text{VP}}$. Hence, in its basic form, a ring oscillator has poor robustness against interference coupling into the power supply line, as the power terminal also acts as a tuning input for the oscillator. However in a VCO ADC application, the circuit is nearly always operated in a pseudo differential configuration as shown in Fig. 14. The overall ADC output is obtained as the difference $D_1 - D_2$ of both channel outputs D_1 and D_2. Hence the PSRR will now only be due to mismatch effects between both channels.

For this reason, it is always recommended to use a pseudo-differential configuration where two ring VCO ADCs

share the same power line and are driven by a differential input signal:

$$\begin{aligned} D_{\text{out}} &= D_1 - D_2 \\ &= D(f_{0,1} - f_{0,2} + (K_{\text{V1}} + K_{\text{V2}})\, V_{\text{in}} \\ &\quad + (K_{\text{VP1}} - K_{\text{VP2}})\, V_{\text{P}}) \end{aligned} \tag{50}$$

If we now focus on the (undesired) contribution of the power line disturbance signal, and refer this error component to the input (without offset component), we get:

$$V_{\text{P,in,Eq}} = \frac{(K_{\text{VP1}} - K_{\text{VP2}})}{(K_{\text{V1}} + K_{\text{V2}})} V_{\text{P}} \tag{51}$$

Now we can introduce the mismatch parameter ε_P as:

$$\varepsilon_P = \frac{(K_{\text{VP1}} - K_{\text{VP2}})}{(K_{\text{VP1}} + K_{\text{VP2}})} \approx \frac{\varepsilon_{K_{\text{VP1}}} - \varepsilon_{K_{\text{VP1}}}}{2} \tag{52}$$

And the signal vs. power sensitivity ratio γ_P:

$$\gamma_P = \frac{(K_{\text{VP1}} + K_{\text{VP2}})}{(K_{\text{V1}} + K_{\text{V2}})} \approx \frac{K_{\text{VP,n}}}{K_{\text{V,n}}} \tag{53}$$

Then we can rewrite Eq. (51) as:

$$V_{\text{P,in,Eq}} = \varepsilon_P \gamma_P V_{\text{P}} \tag{54}$$

From this equation we see that the PSRR = $\frac{1}{|\varepsilon_P \gamma_P|}$. If both channels are perfectly matched, then $\varepsilon_P = 0$ and the PSRR will be infinity. Now the question remains how the ε_P in Eq. (52) relates to the mismatch errors calculated in the previous section. To find this relation, we start with the definition of the VCO gain w.r.t. the ring voltage [14], where no tune circuit is applied:

$$\begin{aligned} K_{V_{\text{ring}}} &= \frac{\partial f}{\partial V_{\text{ring}}} = f \cdot \left[\frac{1}{V_{\text{ring}}} - \frac{dI_{\text{ring}}}{dV_{\text{ring}}} \cdot \frac{1}{I_{\text{ring}}} \right] \\ &= -f \cdot \frac{1 - r_{\text{ring}} \cdot \frac{I_{\text{ring}}}{V_{\text{ring}}}}{r_{\text{ring}} \cdot I_{\text{ring}}} \end{aligned} \tag{55}$$

When adding the tune circuit, the VCO gain w.r.t. the supply rail, or alternatively w.r.t. the open circuit voltage V_{thev} (see Fig. 7), can be obtained:

$$K_{\text{VP}} = K_{V_{\text{ring}}} \cdot \frac{r_{\text{ring}}}{r_{\text{ring}} + R_{\text{thev}}} = -\frac{f}{I_{\text{ring}}} \cdot \frac{1 - r_{\text{ring}} \cdot \frac{I_{\text{ring}}}{V_{\text{ring}}}}{r_{\text{ring}} + R_{\text{thev}}} \tag{56}$$

With the analysis in Section III in mind, the relative error on the VCO gain with respect to the supply rail, $\varepsilon_{K_{\text{VP}}}$, can be found by a straightforward application of Eq. (56):

$$\begin{aligned} K_{\text{VP}} &= K_{\text{VP,n}} \cdot (1 + \varepsilon_{K_{\text{VP}}}) \\ &= -\frac{f_n \cdot (1 + \varepsilon_f)}{I_{\text{ring,n}} \cdot (1 + \varepsilon_{I_{\text{ring}}})} \\ &\quad \cdot \frac{1 - r_{\text{ring,n}} \cdot (1 - \varepsilon_{g_{\text{ring,n}}}) \cdot \frac{I_{\text{ring,n}} \cdot (1 + \varepsilon_{I_{\text{ring}}})}{V_{\text{ring,n}} \cdot (1 + \varepsilon_{V_{\text{ring}}})}}{r_{\text{ring,n}} \cdot (1 - \varepsilon_{g_{\text{ring,n}}}) + R_{\text{thev,n}} \cdot (1 + \varepsilon_Z)} \end{aligned} \tag{57}$$

Now, by applying a multivariate first-order Taylor approximation, and after a straightforward calculation an estimate of $\varepsilon_{K_{\text{VP}}}$ is obtained:

$$\begin{aligned} \varepsilon_{K_{\text{VP}}} \approx\ & \varepsilon_f \\ & - \varepsilon_{I_{\text{ring}}} \cdot \frac{1}{\alpha_{\text{ring}}} \\ & + \varepsilon_{V_{\text{ring}}} \cdot \frac{1 - \alpha_{\text{ring}}}{\alpha_{\text{ring}}} \\ & + \varepsilon_{g_{\text{ring}}} \cdot \frac{r_{\text{ring}}}{r_{\text{ring}} + R_{\text{thev}}} \cdot \frac{\alpha_{\text{tune}}}{\alpha_{\text{ring}}} \\ & - \varepsilon_Z \cdot \frac{R_{\text{thev}}}{r_{\text{ring}} + R_{\text{thev}}} \end{aligned} \tag{58}$$

In order to further elaborate Eq. (58), we write all mismatch contributions $\left(\varepsilon_f, \varepsilon_{V_{\text{ring}}} \text{ and } \varepsilon_{g_{\text{ring}}}\right)$ in function of the mismatch in the ring current $\varepsilon_{I_{\text{ring}}}$. If we now first focus on the contribution of mismatch in the VCO (which is connected to a tune circuit without mismatch), we have to write everything as a function of $\varepsilon_{I_{\text{ring,tune}}}$, see Eq. (29). Now, by combining Eq. (58) with Eqs. (31–32), we obtain:

$$\begin{aligned} \varepsilon_{K_{\text{VP,tune}}} =\ & \varepsilon_{I_{\text{ring,tune}}} \cdot \alpha_{\text{tune}} \\ & - \varepsilon_{I_{\text{ring,tune}}} \cdot \frac{1}{\alpha_{\text{ring}}} \\ & + \varepsilon_{I_{\text{ring,tune}}} \cdot (1 - \alpha_{\text{tune}}) \cdot \frac{1 - \alpha_{\text{ring}}}{\alpha_{\text{ring}}} \\ & + \varepsilon_{g_{\text{ring,tune}}} \cdot \frac{r_{\text{ring}}}{r_{\text{ring}} + R_{\text{thev}}} \cdot \frac{\alpha_{\text{tune}}}{\alpha_{\text{ring}}} \end{aligned} \tag{59}$$

And if we focus on mismatch in the tune circuit (Thévenin version) with no mismatch in the VCO, we have to combine Eqs. (37–39) and Eq. (58) to obtain:

$$\begin{aligned} \varepsilon_{K_{\text{VP,thev}}} =\ & \varepsilon_{I_{\text{ring,thev}}} \cdot \alpha_{\text{ring}} \\ & - \varepsilon_{I_{\text{ring,thev}}} \cdot \frac{1}{\alpha_{\text{ring}}} \\ & + \varepsilon_{I_{\text{ring,thev}}} \cdot \left(1 - \alpha_{\text{ring}}\right) \cdot \frac{1 - \alpha_{\text{ring}}}{\alpha_{\text{ring}}} \\ & + \varepsilon_{g_{\text{ring,thev}}} \cdot \frac{r_{\text{ring}}}{r_{\text{ring}} + R_{\text{thev}}} \cdot \frac{\alpha_{\text{tune}}}{\alpha_{\text{ring}}} \\ & - \varepsilon_Z \cdot \frac{R_{\text{thev}}}{r_{\text{ring}} + R_{\text{thev}}} \end{aligned} \tag{60}$$

In order to evaluate Eqs. (59–60), $\varepsilon_{g_{\text{ring}}}$ should still be determined. This is done in Appendix A. Finally, by considering the case that the different mismatch contributions are independent from each other, the total relative error on K_{VP} can be calculated by evaluating the following expression:

$$\sigma^2_{\varepsilon_{K_{\text{VP}}}} = \sigma^2_{K_{\text{VP,tune}}} + \sigma^2_{K_{\text{VP,thev}}} \tag{61}$$

With the help of Eq. (61), the PSRR = $\frac{1}{|\varepsilon_P \gamma_P|}$ can now be calculated. Assuming that the error ε_P has a normal distribution, then $|\varepsilon_P|$ will exhibit a half-normal distribution [29] and the expected value of the inverse PSRR can be written as:

$$E\left[\text{PSRR}^{-1}\right] = |\gamma_P| \cdot \sqrt{\frac{2}{\pi}} \cdot \sigma_P = |\gamma_P| \cdot \sqrt{\frac{1}{\pi}} \cdot \sigma_{\varepsilon_{K_{\text{VP}}}} \tag{62}$$

Remark that the PSRR itself will follow a reciprocal half-normal distribution, for which an analytical expression for the

expected value and standard deviation does not exist. For this reason, we will use the expected value of the inverse PSRR in order to characterize the actual PSRR of the circuit.

Unfortunately, as evidenced by Eqs. (59–62), the analytical expression for $\sigma_{\varepsilon_{K_{\mathrm{VP}}}}$ is quite convoluted. Fortunately, when combining these analytical expressions with simulation results in Section V-E below, we will be able to come to simple and clear-cut conclusions. At this point, for instance, it is already clear that decreasing the mismatch in the ring current I_{ring} is always beneficial to reduce the PSRR. This means that, according to Eq. (33), the contribution from the VCO mismatch in the PSRR can be reduced by the usual suspects, the transistor dimensions (W, L) and the number of VCO delay cells (N) and also by biasing the ring in strong inversion (i.e. a relatively high V_{ring}). Similarly, mismatch in the tune circuit directly affects the PSRR and should be carefully considered, and e.g. can be improved by increasing its area [22].

B. Common Mode Rejection Ratio (CMRR)

When the VCO ADC is operated in a pseudo differential configuration, the CMRR will also only be due to mismatch effects between both channels. For its calculation, a similar reasoning can be done as for the PSRR:

$$D_{\mathrm{out}} = D(f_{0,1} - f_{0,2} + (K_{\mathrm{V1}} + K_{\mathrm{V2}})\, V_{\mathrm{in}} + (K_{\mathrm{V1}} - K_{\mathrm{V2}})\, V_{\mathrm{CM}}) \quad (63)$$

Here, V_{CM} depicts the common mode offset between the two oscillators in a pseudo-differential configuration. Again, we can refer this error component to the input (without the offset component due to the mismatch in f_0):

$$V_{\mathrm{CM,in,Eq}} = \frac{K_{\mathrm{V1}} - K_{\mathrm{V2}}}{K_{\mathrm{V1}} + K_{\mathrm{V2}}} \cdot V_{\mathrm{CM}} \quad (64)$$

Now we can introduce the mismatch parameter ε_C again, related to the CMRR in this case.

$$\varepsilon_C = \frac{K_{\mathrm{V1}} - K_{\mathrm{V2}}}{K_{\mathrm{V1}} + K_{\mathrm{V2}}} \approx \frac{\varepsilon_{K_{\mathrm{V1}}} - \varepsilon_{K_{\mathrm{V2}}}}{2} \quad (65)$$

We can now use this to rewrite Eq. (64):

$$V_{\mathrm{CM,in,Eq}} = \varepsilon_C \cdot V_{\mathrm{CM}} \quad (66)$$

In this equation, the CMRR $= \frac{1}{|\varepsilon_C|}$ is easily recognized, and thus, exactly like the PSRR, when the channels are perfectly matched ($\varepsilon_C = 0$) the CMRR will be infinity. Now to calculate the mismatch parameter ε_C, we can exploit the fact that the VCO gain w.r.t. the supply rail is closely related to the VCO gain w.r.t. the input voltage:

$$K_{\mathrm{V}} = \frac{\partial f}{\partial V_{\mathrm{in}}} = \frac{\partial f}{\partial V_{\mathrm{thev}}} \frac{\partial V_{\mathrm{thev}}}{\partial V_{\mathrm{in}}} = -K_{\mathrm{VP}} \cdot \frac{\partial V_{\mathrm{thev}}}{\partial V_{\mathrm{in}}} = -\frac{K_{\mathrm{VP}}}{\gamma} \quad (67)$$

In Eq. (67), γ represents the ratio between the input voltage V_{in} and the open circuit voltage V_{thev} and is dependent on the tune circuit. Note that its nominal value (γ_n) is approximately equal to the power to sensitivity ratio (γ_P), see Eq. (53):

$$\gamma_P \approx \frac{K_{\mathrm{VP,n}}}{K_{\mathrm{V,n}}} = \gamma_n \quad (68)$$

Now to write the mismatch in K_{V}:

$$K_{\mathrm{V}} = -\frac{K_{\mathrm{VP,n}} \cdot (1 + \varepsilon_{K_{\mathrm{VP}}})}{\gamma_n \cdot (1 + \varepsilon_\gamma)} \quad (69)$$

The relative error on K_{V} can thus be written as:

$$\varepsilon_{K_{\mathrm{V}}} \approx \varepsilon_{K_{\mathrm{VP}}} - \varepsilon_\gamma \quad (70)$$

With Eq. (70), the expected (inverse) CMRR can be calculated:

$$E\left[\mathrm{CMRR}^{-1}\right] = \sqrt{\frac{1}{\pi}} \cdot \sigma_{\varepsilon_{K_{\mathrm{V}}}} \quad (71)$$

Based on the theory presented above, it is clear that the PSRR and CMRR are very closely related in the case of a pseudo-differential configuration of ring oscillators. More specifically, in the case of $\varepsilon_{K_{\mathrm{VP}}} \gg \varepsilon_\gamma$ (i.e. the tune circuit exhibits a very good mismatch performance) the PSRR and CMRR are proportional to each other, defined by γ_P:

$$\mathrm{PSRR} = \frac{1}{|\varepsilon_P \gamma_P|}, \quad \mathrm{CMRR} = \frac{1}{|\varepsilon_C|}$$
$$\varepsilon_{K_{\mathrm{VP}}} \gg \varepsilon_\gamma \Rightarrow \mathrm{CMRR} \approx |\gamma_P| \cdot \mathrm{PSRR} \quad (72)$$

In conclusion, this means that, in the case of a well-matched tune circuit, a pseudo-differential ring oscillator configuration with a good PSRR will usually also exhibit a good CMRR.

V. Simulation Results

To assess the theory elaborated above, we performed extensive Monte Carlo simulations with a commercially available 65nm CMOS process, which includes more complex statistical models (such as in [23] and [24]) than the simple Pelgrom Model used in the analysis above. To numerically evaluate our theoretical predictions, we estimated the Pelgrom Parameters based on [22] (p258, p261) as:

$$A_{VT} \approx 2mV \cdot \mu m \quad A_\beta \approx 0.0035\ \mu m \quad (73)$$

In our simulation study, the core inverter used in the delay cell had the following drawn[1] sizing:

$$W_N = 8\ \mu m \quad W_P = 2 \cdot W_N \quad L_N = L_P = 60\ nm \quad (74)$$

A. Frequency Characteristics

In a first batch of simulations, all three ring oscillator configurations (simple, direct cross-coupled, feed-forward cross-coupled) were evaluated with respect to their respective effective oscillation frequency as a function of the ring voltage V_{ring}. The result is shown in Fig. 15, where ideal voltage tuning was used to sweep V_{ring}, using ring oscillators with 9 delay elements ($N = 9$). From the plot it can be seen that the direct cross-coupled differential circuit is slightly slower than the reference single-ended oscillator while the feed-forward cross-coupled differential circuit is remarkably faster. This is in agreement with the results of [14], [20]. The simulations were repeated for varying values of N and it was verified that, for all three circuits, the results were independent of N.

[1]The actual design is scaled to a gate length of 65 nm.

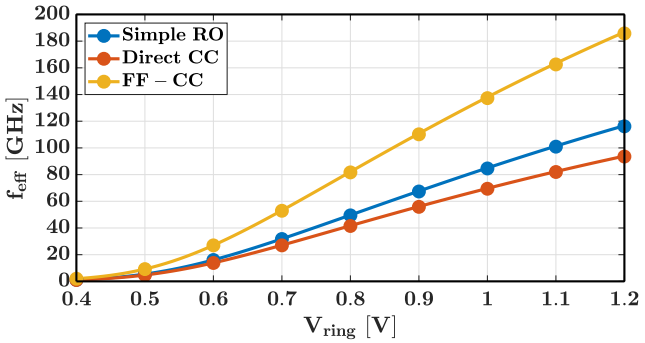

Fig. 15. The nominal effective frequency for the three different VCO types as a function of the ring voltage V_{ring}. The markers highlight where a Monte Carlo run is done.

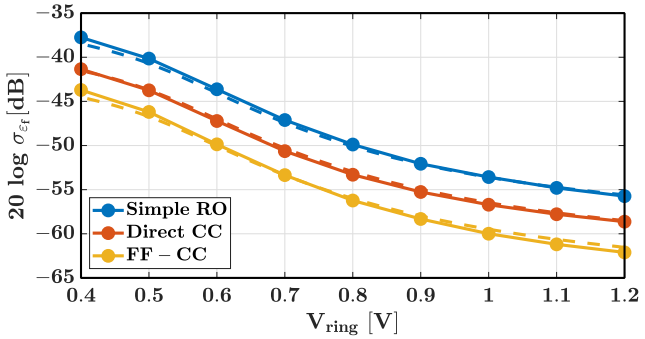

Fig. 16. The relative error on the mean frequency, due to VCO mismatch vs. the ring voltage V_{ring}. The dashed lines represent the calculated values based on our models.

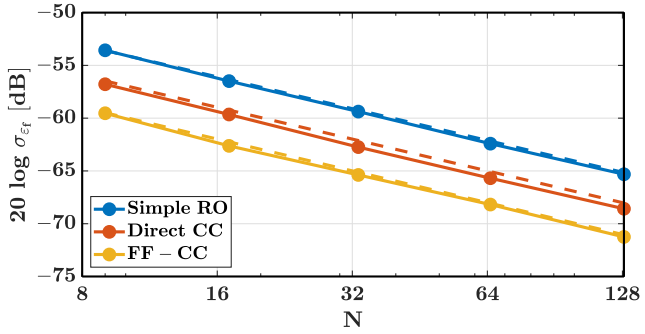

Fig. 17. The relative error on the mean frequency, due to VCO mismatch vs. the number of delay cells N. The dashed lines represent the calculated values based on our models.

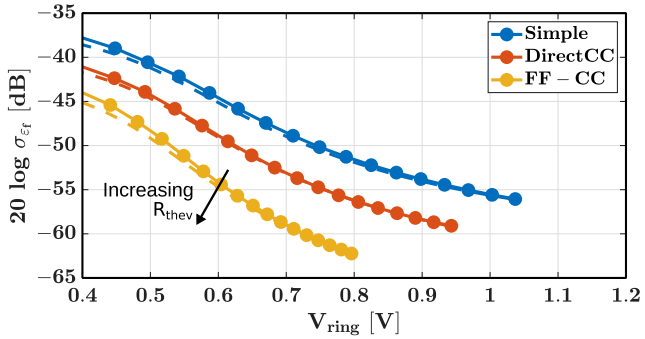

Fig. 18. The relative error on the mean frequency due to VCO mismatch, affected by the tuning circuit, vs. V_{ring}. The dashed lines represent the calculated values based on our models.

B. Standard Deviation of the Relative Frequency Error - VCO Mismatch - No Tune Circuit

In a second batch of simulations, 1000-point Monte Carlo simulations were done for the three considered oscillator circuits as a function of V_{ring} for the case of $N = 9$ cells in the ring. Fig. 16 shows the simulated standard deviation of the relative frequency error, together with our predictions based on Eq. (8) and Eqs. (18), (21) and (23). Despite the simplicity of the models, we can see that there is a very good qualitative matching between the simulation and the theoretical model. Note that the main difference between the three curves is due to the difference in size of the delay cells, and that strong inversion is clearly preferred over weak inversion.

In a third batch of simulations, again 1000-point Monte Carlo simulations were done but now for varying number N of cells at a fixed ring voltage $V_{\text{ring}} = 1\text{V}$. The result, together with the theoretical prediction, is shown in Fig. 17. Again, the plot matches very well with the theoretical prediction. In particular, the predicted $1/\sqrt{N}$ trend is confirmed. Again, the main difference between the curves is determined by the difference in size of the delay cells.

C. Standard Deviation of the Relative Frequency Error - VCO Mismatch - With Tune Circuit

In a fourth batch of simulations, 1000-point Monte Carlo simulations were done, where this time the input voltage was applied through an arbitrarily chosen output resistance $R_{\text{thev}} = 70\ \Omega$ to the same three oscillator circuits, see Fig. 9. In order to properly evaluate the theory presented in Section III-C, first the tune circuit was made ideal, such that only the VCO exhibited mismatch. The result, together with the theoretical prediction in Eq. (33), is shown in Fig. 18. Due to the resistive divider in the circuit (R_{thev} and r_{ring}), when sweeping the input from rail to rail, the mismatch curve is restricted to a smaller range, determined by the value of r_{ring} w.r.t. the value of R_{thev}. In these limited ranges, the theory matches very well with the simulations. Remark that $\sigma^2_{\varepsilon_f}$ in Eq. (33) is a inversely proportional with R_{thev}, which is indicated by the arrow in Fig. 18.

In order to further illustrate the influence of the output resistance of the tune circuit (R_{thev}) and to demonstrate the performance difference between voltage control and current control, the same batch of simulations was repeated, only for the simple ring oscillator, for six different cases. Three cases where a Thévenin drive circuit was used, with $R_{\text{thev}} = 0, 70, 420\,\Omega$ and three cases where a Norton equivalent was used, with $R_{\text{thev}} = 420, 7\text{k}, \infty\,\Omega$. The result of these simulations is plotted in Fig. 19 which clearly confirms the advantage of using current control when considering the mismatch performance of the VCO, see Eq. (34). Finally, remark the difference in available operating regions of the ring.

D. Standard Deviation of the Relative Frequency Error - Tune Circuit Mismatch - With Tune Circuit

In a fifth batch of simulations, the influence of an error on the open circuit voltage V_{thev} and mismatch in the resistor is tested. To this end, a 1000-point Monte Carlo simulation is

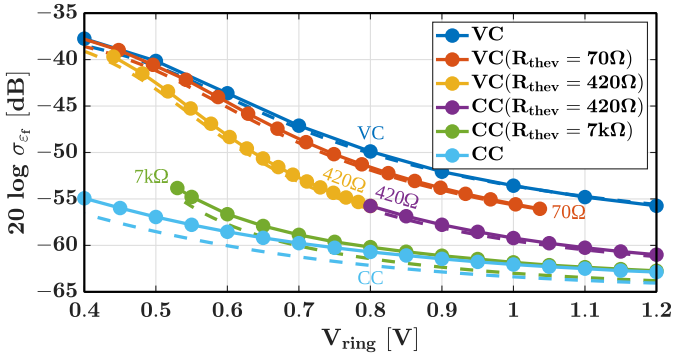

Fig. 19. The relative error on the mean frequency due to VCO mismatch, affected by different tuning circuits, vs. the ring voltage V_{ring} for the simple ring oscillator. The dashed lines represent the calculated values based on our models.

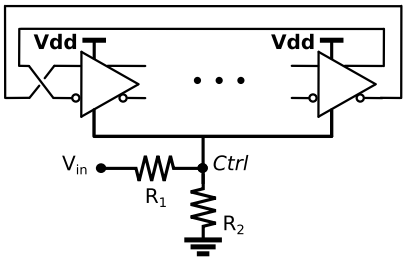

Fig. 20. Resistive tuning circuit achieving a very linear VCO.

executed on the circuit in Fig. 20 with a resistive tuning circuit. In this example, the VCO is exempted from mismatch, and mismatch is only applied to the resistors. As a consequence, mismatch will affect the output resistance of the tune circuit R_{thev} and V_{thev}. The expression for R_{thev} and V_{thev} can be obtained by solving the circuit for its Thévenin equivalent:

$$V_{\text{thev}} = \frac{R_2}{R_1 + R_2} \cdot V_{\text{in}}, \quad R_{\text{thev}} = \frac{R_1 R_2}{R_1 + R_2} \tag{75}$$

In this batch of simulations, we arbitrarily choose $R_1 = R_2 = 70\Omega$, which exhibited a total variance of $\sigma^2_{\varepsilon_Z} = \sigma^2_{\varepsilon_V} = \frac{0.02^2}{2}$ (according to our SPICE models, for this particular resistor sizing, $W_{\text{R}} = 2\,\mu\text{m}$, $L_{\text{R}} = 845\,\text{nm}$) on both the open circuit voltage V_{thev} and the output resistance of the tune circuit R_{thev}, equal to half the variance on the individual resistors. Since both ε_Z and ε_V are determined by the mismatch error on the resistances, they are not independent from each other and should be added to each other linearly, see Eqs. (37,39). Additionally, note that this variance depends on the actual sizing of the resistor. Similar to transistors, the mismatch in the resistance is inversely proportional its area [22].

From the simulation results displayed in Fig. 21, it is clear that the predictions again match very well with the simulation results. Opposing trends in function of V_{ring} are present. Additionally, we can conclude that the mismatch due to an error on the open circuit voltage V_{thev} (dotted lines) will be dominant for low values of V_{ring}, and a good choice for the biasing is critical. For higher values of V_{ring}, the mismatch contribution from the mismatch in the output resistance of the tune circuit (dashed lines) becomes dominant.

It is interesting to remark that by scaling the inverters in the simple and the direct cross-coupled ring oscillator cells to

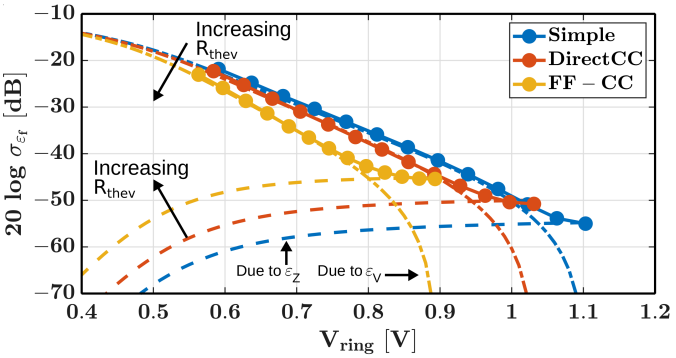

Fig. 21. The relative error on the mean frequency, due to mismatch in the resistive driver circuit of the VCO vs. the ring voltage V_{ring}. The dashed lines represent the calculated values for the impedance mismatch (ε_Z), the dotted lines represent the calculated values for the mismatch in V_{thev} (ε_V).

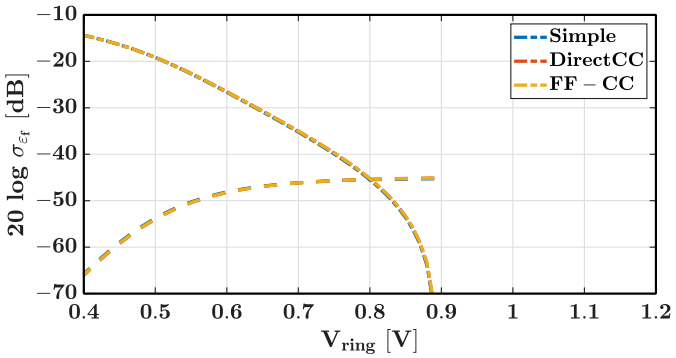

Fig. 22. A similar simulation experiment as displayed in Fig. 21, where the inverters of the simple and direct cross-coupled ring oscillator were scaled to exhibit identical I-V characteristics (not identical active area). The FF-CC characteristic was used as a reference.

match the I-V curve of the feed-forward cross-coupled based ring oscillator, the mismatch curves in Fig. 21 all collapse onto the yellow curves, and are visually indiscernible. This is shown in Fig. (22) which shows the calculated mismatch performance for all three ring oscillators. This can also be verified analytically using Eqs. (37,39). Remark that this scaling does not result in identical VCO area, and thus there will be a difference in mismatch performance w.r.t. the contribution of mismatch in the VCO (cfr. Eq. (18)).

E. Expected Value of PSRR^{-1} - all Mismatch Contributions

In our sixth batch of simulations, the expected value of PSRR^{-1} is evaluated in order to characterize the power supply rejection of the three ring oscillator types. Again, a 1000-point Monte Carlo simulation is executed on the circuit in Fig. 20 with a resistive tuning circuit. This resistive tuning circuit is identical to the one in Section V-C. The only difference here is that the supply voltage is varied, instead of the input voltage. Remark that, when using the tune circuit displayed in Fig. 20, $K_{\text{VP,n}}$ is a factor two higher than the nominal signal gain ($K_{\text{V,n}}$) due to the voltage division over the two matched resistors R_1 and R_2 in the nominal signal path. This leads to a PSRR of -6 dB for a single-ended configuration with a signal vs. power sensitivity ratio $\gamma_n = \frac{\partial V_{\text{thev,n}}}{\partial V_{\text{in,n}}} = 2$. As mentioned before, however, we will use a pseudo-differential setup, where

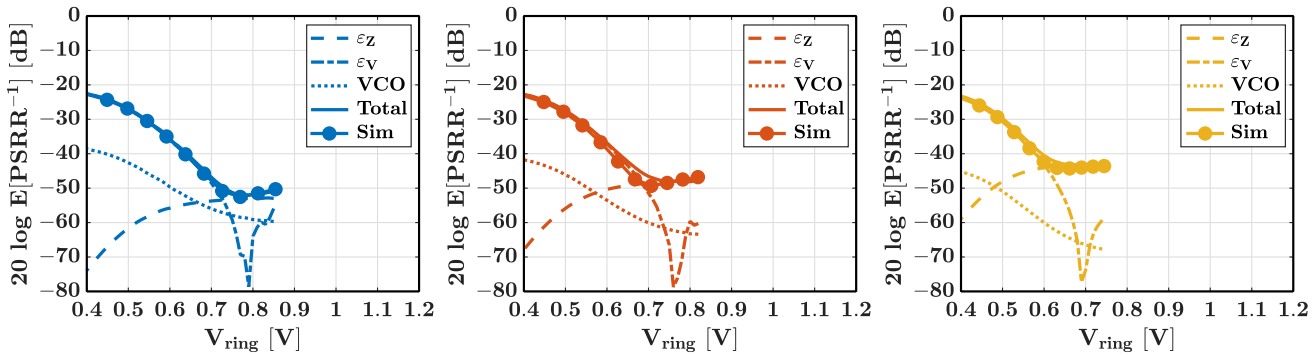

Fig. 23. The expected value of the inverse PSRR w.r.t. the ring voltage V_{ring}. The calculated values for the mismatch due to mismatch in the resistive driver circuit of the VCO (dashed line), due to an error on the open circuit voltage (dash-dotted line), due to mismatch in the VCO (dotted line) and the combination of the three (solid line) are also displayed.

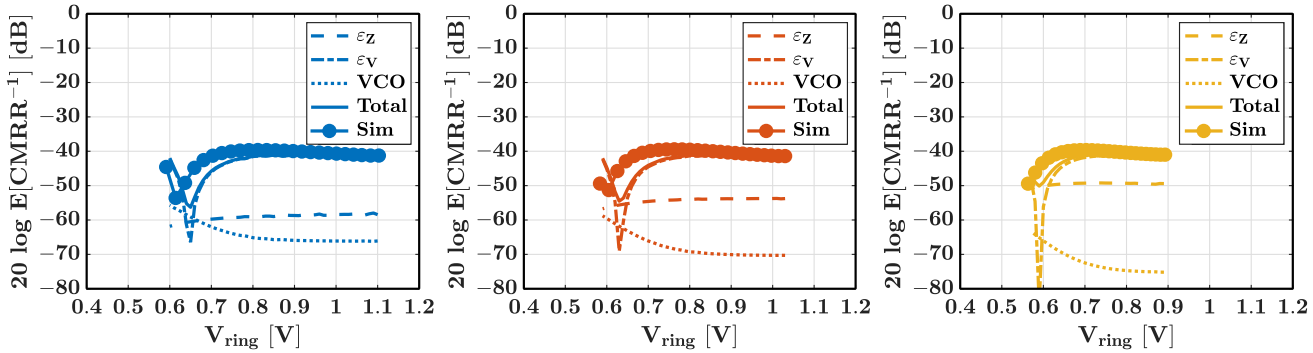

Fig. 24. The expected value of the inverse CMRR w.r.t. the ring voltage V_{ring}. The calculated values for the mismatch due to mismatch in the resistive driver circuit of the VCO (dashed line), due to an error on the open circuit voltage (dash-dotted line), due to mismatch in the VCO (dotted line) and the combination of the three (solid line) are also displayed.

the PSRR is due to mismatch effects between both channels as analyzed and simulated above, see Eq. (62).

In order to include the mismatch due an error on the open circuit voltage, a common mode voltage of $V_{\text{CM}} = \frac{V_{\text{dd}}}{2} = 0.6\,\text{V}$ is applied at the input ($V_{\text{thev}} \neq 0\,\text{V}$), and the supply voltage V_{dd} was swept to vary the bias point V_{ring}. Finally, instead of isolating the different mismatch contributions, mismatch is introduced in every component. The result of these simulations is displayed in Fig. 23. Remark that applying the common voltage at the input, limits the range of V_{ring} in Fig. 23.

From the results displayed in Fig. 23, we can conclude that similar trends are observed in function of the ring voltage V_{ring} w.r.t the previous simulations. Upon closer investigation it was observed that the influence of the VCO mismatch and the influence of an error on V_{thev} was alleviated, whereas the influence of mismatch in the output resistance of the Thévenin was exacerbated slightly. With the sizing used for these simulations it is clear that the influence of an error on V_{thev} continues to be dominant for lower values of V_{ring}, and that the influence of ε_Z takes over for larger values of V_{ring}. It is remarkable that in all three cases, for the chosen sizing, the influence of mismatch in the VCO is negligible. This implies that increasing the dimensions of the tune circuit resistors (decreasing ε_Z and ε_V) would be beneficial to improve the overall mismatch performance. Thus, when the PSRR is a critical specification in the design, or when the supply voltage can not be controlled reliably, the tune circuit should be carefully designed and cover a large area. When this is the case, the biasing V_{ring} can be increased to improve the mismatch contribution from the VCO. Alternatively, the overall dimensions of the VCO (W,L), or the number of VCO delay cells (N) can be increased to improve the PSRR.

F. Expected Value of CMRR^{-1} - all Mismatch Contributions

In the seventh batch of simulations, the expected value of CMRR^{-1} is evaluated in order to characterize the common-mode rejection of the three ring oscillator types. Once more, a 1000-point Monte Carlo simulation is executed on the circuit in Fig. 20 with a resistive tuning circuit. The result of these simulations is displayed in Fig. 24.

The only difference between the mismatch in K_{V} and in K_{VP}, when the tune circuit displayed in Fig. 20 is used, is an additional contribution to the total mismatch due to ε_V:

$$\varepsilon_\gamma = -\varepsilon_V \tag{76}$$

Remark that by sweeping the common mode of the input, instead of V_{dd}, another range of V_{ring} will be valid. Additionally, due to the additional contribution of ε_γ the influence of the error on V_{thev} on the overall mismatch becomes dominant over the entire range of V_{ring}, with a very flat characteristic as a result, apart from a very narrow notch. Note that in this case $\varepsilon_{K_{\text{VP}}} \gg \varepsilon_\gamma$ is not valid. In conclusion, for a good design, the tune circuit should be carefully designed to limit its mismatch contribution (e.g. by using large devices),

TABLE I
REFERENCE CASE FOR COMPARISON OF THE MISMATCH

Case 1: Reference case ($N = 9$, $V_{\text{ring}} = 1\text{V}$)					
VCO Type	$W_{n,main}$ [μm]	f_{eff} [Hz]	P_{DC} [W]	$V_{n,in}$ [V/$\sqrt{Hz}$]	$E\left[\text{PSRR}^{-1}\right]$ [dB]
Simple	8	84.98G	2.08m	2.35n	-64.7
Direct CC	8	69.67G	4.38m	1.87n	-67.7
FF-CC	8	138.00G	12.53m	1.03n	-70.7

TABLE II
SCALED CASE FOR THE COMPARISON OF THE MISMATCH

Case 2: Scaled for equal active area ($N = 9$, $V_{\text{ring}} = 1\text{V}$)					
VCO Type	$W_{n,main}$ [μm]	f_{eff} [Hz]	P_{DC} [W]	$V_{n,in}$ [V/$\sqrt{Hz}$]	$E\left[\text{PSRR}^{-1}\right]$ [dB]
Simple	32	84.98G	8.31m	1.17n	-70.68
Direct CC	12.8	69.67G	7.01m	1.48n	-69.66
FF-CC	8	138.00G	12.53m	1.03n	-70.64

TABLE III
SCALED CASE FOR THE COMPARISON OF THE MISMATCH

Case 3: Scaled for equal active area ($N = 9$, $V_{\text{ring}} = 0.4\text{V}$)					
VCO Type	$W_{n,main}$ [μm]	f_{eff} [Hz]	P_{DC} [W]	$V_{n,in}$ [V/$\sqrt{Hz}$]	$E\left[\text{PSRR}^{-1}\right]$ [dB]
Simple	32	1.18G	16.32μ	3.97n	-50.53
Direct CC	12.8	1.02G	13.25μ	4.39n	-49.59
FF-CC	8	2.00G	24.02μ	3.20n	-50.55

such that the VCO ADC performance is not limited by $\sigma_{\varepsilon V}$. As a demonstration, in the following section we will explore a case study where the VCO ADC performance is not limited by the tune circuit.

G. Overall Performance Comparison

In a final batch of simulations, all cells were evaluated in terms of typical performance measures for VCO ADCs. For simplicity, and to emulate a case where the tune circuit does not limit the VCO-ADC performance, ideal voltage-control was chosen as a case study. Note that this means that the PSRR and CMRR are equal, with a signal vs. power sensitivity ratio $\gamma = 1$ and that mismatch in the tune circuit is not present. Table I shows the power consumption and input referred noise performance, next to the area, effective oscillation frequency and mismatch performance at a ring biasing level of $V_{\text{ring}} = 1\,\text{V}$. For the interpretation of these simulation results, it is important to realize that they are obtained for the same sizing of the core inverter. However, each of the circuits has a very different area, power consumption as well as very different input referred white noise, which was obtained according to the methodology described in [26] and [14].

In order to get a more realistic comparison, the unit cells of every VCO circuit were scaled, to obtain the same active area. The resulting performance is wrapped up in Table II.

Finally, the same circuits as in Table II are evaluated at $V_{\text{ring}} = 0.4\,\text{V}$ in order to properly evaluate the influence of biasing the ring in weak inversion. This is shown in Table III.

At first glance, from the mismatch data in Tables I–III, we can conclude that for the same active area the direct cross-coupled is the worst option, due to the overhead of the auxiliary inverters. The mismatch performance of the simple and the feed-forward based ring oscillator are virtually identical with the same active area, with the feed-forward solution consuming more power, but providing a better noise performance and faster oscillation frequency. Additionally, the data in Table III also confirms the fact that strong inversion significantly outperforms (by $\sim$ 20 dB) weak inversion in terms of mismatch, a fact which was also observed in [8] and [9]. Remark that this is in stark contrast with the advocated biasing for noise efficiency for a ring oscillator with ideal voltage control [14], which was optimal in weak inversion.

VI. CONCLUSION

We have performed a systematic analysis of the mismatch in three types of important inverter based ring oscillators. We have started this analysis by constructing a mismatch model for these ring oscillators, based on the intuitive Pelgrom mismatch model for CMOS devices. This model was generalized, by including the effect of adding a generic tuning circuit on the mismatch. Using this novel mismatch model, we concluded that, next to the obvious transistor size dependence, the mismatch is inversely proportional to the number of stages and hence in theory can always be suppressed up to the desired level in a VCO ADC. Furthermore, we demonstrated that the mismatch is dependent on the biasing of the ring, which is even more apparent when taking into account the influence of a tuning circuit. More specifically, it was shown that ring oscillators in strong inversion outperform those in weak inversion, and ring oscillators with current control perform substantially better than those with voltage control. The tune circuit should also be designed with large enough devices, in order for the VCO-ADC performance not to be limited by mismatch in this tune circuit. Finally, we established a link between this mismatch model and the PSRR, and the closely related CMRR when using a pseudo differential VCO ADC configuration. From these results, we concluded that, in order to get adequate values for the PSRR and CMRR, it is crucial to design a large enough tune circuit and to bias the ring in strong inversion. Our systematic analysis was consolidated through extensive Monte Carlo simulations using a design kit of a commercially available 65nm CMOS process, which match the predictions of our novel mismatch model nearly perfectly.

APPENDIX

A. Determining $\varepsilon_{g_{\text{ring}}}$, the Relative Error on g_{ring}

Remember that we advocate that, in any VCO design, the I-V characteristic of the ring should be determined upfront [14]. Since for the entire I-V characteristic, the transistors' region of operation goes from weak inversion, into strong inversion into velocity saturation, an analytical approach is not viable and hence the I-V characteristic should be available in a numerical form. Hence all its partial derivatives should also be available (in a numerical form). Since g_{ring} is the derivative of the I-V characteristic of the ring, we can write:

$$g_{\text{ring}} = g_{\text{ring,n}} \cdot \left(1 + \varepsilon_{g_{\text{ring}}}\right) = \frac{\partial I_{\text{ring}}}{\partial V_{\text{ring}}} = \frac{\partial \left(I_{\text{ring,n}} \cdot \left(1 + \varepsilon_{I_{\text{ring}}}\right)\right)}{\partial V_{\text{ring,n}}} \left(\frac{\partial \left(V_{\text{ring,n}} \cdot \left(1 + \varepsilon_{V_{\text{ring}}}\right)\right)}{\partial V_{\text{ring,n}}}\right)^{-1}$$

This leads to:

$$\varepsilon_{g_{\text{ring}}} \approx \varepsilon_{I_{\text{ring}}} + I_{\text{ring}} r_{\text{ring}} \cdot \frac{\partial \varepsilon_{I_{\text{ring}}}}{\partial V_{\text{ring,n}}} - \varepsilon_{V_{\text{ring}}} - V_{\text{ring}} \cdot \frac{\partial \varepsilon_{V_{\text{ring}}}}{\partial V_{\text{ring,n}}}$$

This equation is correct both for the case of mismatch in the VCO as well as for the case of mismatch in the (Thévenin equivalent of the) tune circuit. If we focus on the mismatch in the VCO (connected to a tune circuit without mismatch), we have to add the subscript *tune* to the error contributions in the above equation and collect the corresponding values of $\varepsilon_{I_{\text{ring,tune}}}$ and $\varepsilon_{V_{\text{ring,tune}}}$ from Eqs. (29) and (31). However, we also need the corresponding partial derivatives $\frac{\partial}{\partial V_{\text{ring,n}}}$. In this work we decided to evaluate this also numerically (e.g. in MATLAB by using the 'gradient' function). The contribution of mismatch in the (Thévenin equivalent of the) tune circuit is determined similarly, where now the values of $\varepsilon_{I_{\text{ring,thev}}}$ and $\varepsilon_{V_{\text{ring,thev}}}$ should be collected from Eqs. (37) and (38).

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