MWSCAS Guest Editorial Special Issue Based on the 64th International Midwest Symposium on Circuits and Systems

THE International Midwest Symposium on Circuits and Systems is the oldest Circuits and Systems Symposium sponsored by the IEEE CAS Society. This conference contributes to its strong history by reporting the latest research results and innovations in the field of circuits and systems through distinguished speakers featuring the newest innovations relevant to this field and shedding light on its evolution toward breaching the gaps among technologies. The 64th International Midwest Symposium on Circuits and Systems (MWSCAS-2021) was held virtually due to the COVID-19 pandemic on August 9–11, 2021. Among all the accepted contributions, a subset of these articles were selected and invited for this Special Issue. The invited articles went through a peer-review process consisting of world-recognized reviewers in related fields. The process has been conducted by a Guest Editorial team formed by Kenneth Jenkins, Khurram Waheed, and Zaid Albataineh. A brief description of the selected articles is as follows.

In [A1], Zhao et al. describe an adaptive noise generator circuit suitable for ON-chip simulations of stochastic chemical kinetics. The circuit uses amplified BJT white noise and adaptive low-pass filtering to emulate the power spectrum and autocorrelation of random telegraph signals (RTSs) with Poisson-distributed level transitions. A current-mode implementation in the AMS 0.35 μm BiCMOS process shows excellent agreement with theoretical results from the Gillespie stochastic simulation algorithm over a 60 dB range in mean current levels. The circuit has an estimated layout area of 0.032 mm^2 and typically consumes 400 μA, which are 73% and 50% less, respectively, than prior implementations. Moreover, it does not require any OFF-chip capacitors. Experimental results from a discrete board-level implementation of the circuit are in good agreement with theoretical predictions.

In [A2], Bautista et al. developed a superconducting, magnetically-coupled, shuttle-flux shift register (SF-SR) that stores single flux quantum (SFQ) pulses. This shift register has a dc bias operating margin of $\pm$34% at 10 GHz, with a power dissipation of 3.6μW and 38% fewer Josephson junctions (JJs) when scaled up to multiple stages compared to a data flip-flop (DFF) based shift register. The clock input is inductively coupled and is independent of the data input. The experiments with three applications demonstrate that the SF-SR can implement with fewer JJs and lower power consumption compared to DFF-based shift registers.

In [A3], Pelzers et al. propose a passive switched-capacitor single-ended-to-differential-converter (SDC) as a front-end of a differential SAR ADC. As the SDC is passive, the overall solution is power efficient compared to active SDC solutions, and is especially suitable for lower/medium resolutions. As opposed to active SDC solutions with a static bias current, the switched capacitor network only consumes dynamic power, so its consumption scales linearly with the sampling frequency. A prototype implementation in 65 nm CMOS achieves a figure-of-merit of 6.1 fJ/conversion-step at 20 MS/s, while reaching an SNDR of 54.7 dB up to Nyquist and occupying a chip area of only 60 $\times$ 36 μm.

In [A4], Wohrle et al. describe a methodology for co-optimizing application-specific neural network (NN) accelerators for accuracy and energy expenditure per inference. The architecture of the NN is co-optimized with the concrete ASIC implementation of the accelerator to provide reliable estimates of energy efficiency. The method is demonstrated on an application-specific NN accelerator for the detection of atrial fibrillation in human electrocardiograms that is implemented in 22 FDX/FDSOI technology. The NN accelerator is highly parameterizable, i.e., it can map NNs with different architectural properties to a synthesizable register transfer level representation. The parameter space is further expanded by the parameters of the physical implementation (e.g., memories, clocking, and voltage domains).

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APPENDIX: RELATED ARTICLES

[A1] H. Zhao, R. Sarpeshkar, and S. Mandal, "A compact and power-efficient noise generator for stochastic simulations," *IEEE Trans. Circuits Syst. I, Regular Papers*, early access, Aug. 24, 2022, doi: 10.1109/TCSI.2022.3199561.

[A2] M. G. Bautista, P. Gonzalez-Guerrero, D. Lyles, and G. Michelogiannakis, "Superconducting shuttle-flux shift register for race logic and its applications," *IEEE Trans. Circuits Syst. I, Regular Papers*, early access, Oct. 10, 2022, doi: 10.1109/TCSI.2022.3210023.

[A3] K. Pelzers, M. van der Struijk, and P. Harpe, "A 0.0022 mm^2 10 bit 20MS/s SAR ADC with passive single-ended-to-differential-converter," *IEEE Trans. Circuits Syst. I, Regular Papers*, early access, Sep. 9, 2022, doi: 10.1109/TCSI.2022.3203792.

[A4] H. Wöhrle et al., "Multi-objective surrogate-model-based neural architecture and physical design co-optimization of energy efficient neural network hardware accelerators," *IEEE Trans. Circuits Syst. I, Regular Papers*, early access, Dec. 26, 2022, doi: 10.1109/TCSI.2022.3209574.