Scalable Multi-Stage CMOS OTAs With a Wide C_L-Drivability Range Using Low-Frequency Zeros

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***Abstract*— This work introduces a multi-stage CMOS OTA design technique that allows cascading identical gain stages (for arbitrarily scalable high DC gain) while driving an ultra-wide range of capacitive loads (C_Ls). At the heart of the proposed design is a new frequency compensation technique (FCT) that relies on low-frequency left-half-plane zeros to allow the proposed OTA to operate for a desired closed-loop behavior. In this work, classical gain-stages (i.e., differential pair and common source transistors) are used to design fully-differential 2-, 3-, 4- and 5-stage CMOS OTAs. The proposed 2-to-4-stage designs have been fabricated in TSMC 65 nm CMOS process and the measurement results show that the 2-stage OTA is achieving a DC gain of 50 dB with a C_L-drivability ratio (i.e., $C_{L,max}/C_{L,min}$) of 10,000×, the 3-stage OTA is achieving a DC gain of 70 dB with a C_L-drivability of 1,000,000×, and the 4-stage OTA is achieving a DC gain of 90 dB with a C_L-drivability of 1,000,000×. This is a 10-to-1000-time improvement in the state-of-the-art, as the highest C_L-drivability reported to date is 1000×. Accordingly, the proposed OTAs can cover a wider range of applications than any other reported works.**

***Index Terms*— Capacitive load, compensation circuit, low-frequency zeros, Miller R-C circuit, multi-stage, operational transconductance amplifiers, pole-zero pair, unity-gain frequency.**

I. Introduction

OPERATIONAL Transconductance Amplifiers (OTAs) have enormous applications in analog and mixed-signal circuit design. Driving a wide range of Capacitive Loads (C_L) (i.e., in the range of pF-to-μF) is one of these well-known applications where robust high Gain-Bandwidth Product (GBW) OTAs are required. Fig. 1(a) shows some applications where such wide range of C_L is required [1], [2], [3], [4], [5], [6], [7], [8], [9], [10], [11]. These applications have a set of different requirements that the CMOS OTAs must satisfy. For example, the approximated settling time requirements vs. C_L of these applications [1], [2], [3], [4], [5], [6], [7], [8], [9], [10], [11] can be seen in the shaded areas of Fig. 1(a). Other important parameters are also required, such as OTA's DC gain, power consumption, silicon area, etc.

On the other hand, since these applications are being fabricated using advanced nanometer CMOS technology nodes, OTAs are facing challenges to achieve high DC gain values. Consequently, many CMOS OTA architectures have been proposed in the literature to meet the various design requirements to drive a wide range of C_L while achieving adequate DC gain.

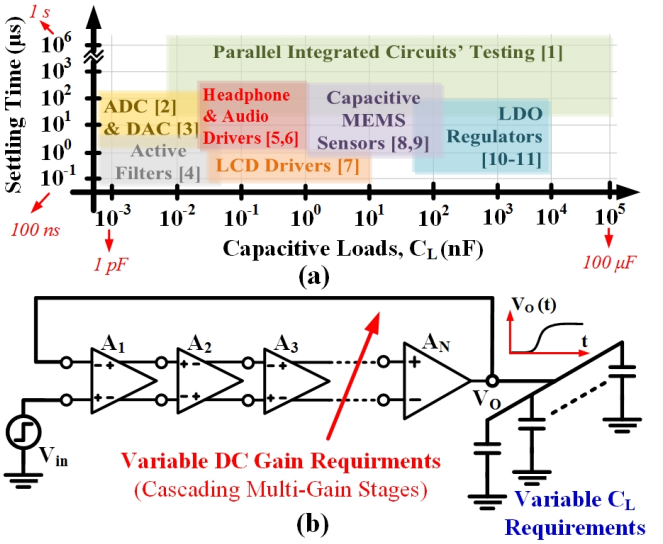

Fig. 1. (a) Applications' examples where a wide-range of C_Ls are being driven by CMOS amplifiers and the approximated range of settling time requirements for these applications as a function of C_L, and (b) the proposed topology of cascading multi-stage CMOS amplifiers while driving a wide range of C_Ls in closed-loop configuration.

Despite having stability challenges once configured in closed loop, cascading gain stages is believed by the authors to be the preferred method to achieve sufficient DC gain in modern CMOS technology processes operating with low voltage supply levels [12], [13]. Fig. 1(b) shows the cascading scheme of N gain-stages to achieve high DC gain. Ultimately, such OTAs are configured in a closed loop as also seen in Fig. 1(b), where the output voltage ($V_O(t)$) must remain bounded. To easily discuss the previously reported works, one can categorize them based on the number of gain stages placed in cascade and evaluate their C_L-drivability ratio (i.e., $C_{L,max}/C_{L,min}$).

Single-stage and 2-stage CMOS amplifiers are relatively easy to stabilize, but their DC gain is limited in advanced node CMOS technologies. Many works have managed to demonstrate single- and 2-stage CMOS amplifiers with wide C_Ls [14], [15], [16], [17], [18], [19], [20], [21]. However, they all make use of additional circuit techniques to achieve adequate DC gain while handling such C_L. In the case of single-stage amplifiers, the maximum-reported C_L-drivability ratio is 150× [17]. In the case of 2-stage OTAs, the maximum C_L-drivability ratio is 1000× [18].

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Consequently, to achieve both the load driving capability and the DC gain requirement, most works found in the literature deploy 3-stage amplifiers [22], [23], [24], [25], [26], [27], [28], [29], [30], [31]. With these extensive works on 3-stage amplifiers, stability is ensured through different Frequency Compensation Techniques (FCTs), such as nested-Miller compensation (NMC) [22], single-Miller capacitor (SMC) [23], [24], [25], and capacitor-free compensation techniques [26], [27], to name just a few. However, the maximum C_L-drivability ratio that has been reported in literature with 3-stage amplifiers is 555.5× [27].

As for 4-stage CMOS amplifiers, they can provide higher DC gains, but once they are configured in closed-loop, they are a challenge to stabilize. Therefore, only a few works have proposed 4-stage designs to drive a wide range of C_Ls, such as [32] and [33]. However, the maximum C_L-drivability ratio was limited to 30× [33]. To the best of the author's knowledge, there is no reported 5-stage OTA with a wide C_L-drivability.

Looking at the previously reported works on OTAs/ amplifiers driving a wide range of C_Ls [14], [15], [16], [17], [18], [19], [20], [21], [22], [23], [24], [25], [26], [27], [28], [29], [30], [31], [32], [33], and regardless of the number of stages, one can conclude the following: (1) previously reported works are proposing FCTs which are suitable for OTAs with specific number of stages and/or circuit topologies, and (2) the proposed OTAs' maximum C_L is limited to the nF-range. Thus, the proposed FCTs have the following limitations: (1) they are specific to the chosen topology, and/or the number of stages placed in cascade, consequently, they cannot offer different choices for DC gain and power consumption and (2) they cannot be used in applications with capacitive loads C_L in the μF-range.

Therefore, in this work a new FCT is proposed to enable cascading multiple gain-stages while driving an ultra-wide range of capacitive loads. The proposed FCT is ideally applicable to N-stage CMOS OTAs, which offers wider design choices for DC gain and power consumption. However, for simplicity and as a proof of concept, 2-, 3-, 4- and 5-stage CMOS OTAs are demonstrated in this work. Furthermore, the proposed FCT uses a multi-Miller R-C compensation circuit across the gain stage to position the Pole-Zero Pair (*P-ZP*) created by the R-C compensation networks below the unity-gain frequency (ω_t) of the compensated OTAs. On doing so, the *P-ZP* will increase ω_t of the compensated OTA once the zeros are positioned at low frequencies. The additional increase in ω_t can be traded off for higher C_L by placing the dominant pole at higher frequencies.

This paper is structured as follows: the overall proposed idea is presented in Section II. In Section III, the design choice for the gain-stages is introduced. In Section IV and V, the detailed implementation of the proposed FCT is discussed. In Section VI, verification of the proposed technique is discussed based on schematic and post-layout simulations. Section VII shows the experimental results and robustness of the proposed FCT, while Section VIII compares the proposed 2-, 3-, and 4-stage OTAs with the state-of-the-art works. Finally, Section V concludes the work presented in this paper.

II. Cascading Multi-Stage CMOS OTAs and Increasing Their C_L-Drivability: The Overall Proposed Idea

The proposed design of the scalable multi-stage CMOS OTA, shown in Fig. 1(b), consists of cascaded-gain stages

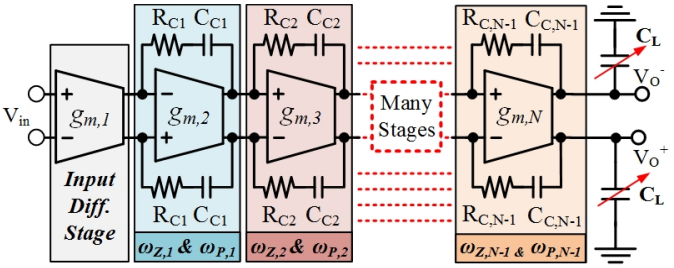


Fig. 2. Circuit level realization of the proposed differential-ended N-stage CMOS OTA driving a wide range of capacitive loads.

which can achieve an overall DC gain ($A_{DC,N}$) of

$$A_{DC,N} = \prod_{i=1}^{N} (A_i), \tag{1}$$

where Ai is the gain provided by the i^{th} gain stage and N is the number of gain-stages. On the other hand, and since this is a CMOS-based OTA, poles and zeros will be part of the OTA's realization. Usually, in such OTAs, in addition to the 3-dB frequency, each gain stage will produce a *P-Z* Pair. Therefore, the open-loop input-output Transfer Function (*TF*) takes on a cascade of bilinear forms as follows

$$A(s) = \frac{A_{DC,N}}{\left(1+\frac{s}{\omega_{P0}}\right)} \times \prod_{i=1}^{N-1} \frac{\left(1+\frac{s}{\omega_{Zi}}\right)}{\left(1+\frac{s}{\omega_{Pi}}\right)}, \tag{2}$$

where ω_{P0} is the 3-dB frequency, ω_{Pi} and ω_{Zi} are the open-loop *P-Z* pairs which are produced by the compensation circuit of each stage.

The diagram of Fig. 1(b) and its bilinear *TF* of Eqn. (2) can be realized by using the differential-ended circuit level implementation of Fig. 2. The *gm*-blocks will be responsible for achieving the required DC gain, while the R-C compensation networks (which are connected across each stage) will properly place the open-loop *P-Z* pairs at the required frequencies.

The purpose of the proposed architecture is to provide a uniform scalable DC gain while driving a wide-range of capacitive loads. Therefore, all gain-stage will be designed to achieve the same *Ai*. However, for such cascading of multi gain-stages to be stable and to allow the OTA to drive a wide range of C_Ls (regardless of the number of gain stages) a new FCT is proposed in this work using low-frequency zeros. *It is the application of these low frequency zeros that make this work unique in the field of OTA design.*

A. The Use of Low-Frequency Compensation Zeros

The objective of the proposed FCT is to identify the placement of the proposed scalable multi-stage OTA's poles and zeros, so that the load-drive capability and unity-gain bandwidth are maximized (while the OTA is exhibiting a stable closed-loop response). This is further constrained by requiring the settling time of a unity-gain closed-loop configuration be bounded by some desired value denoted by T_S^D. This can be mathematically expressed as follows:

$$\begin{array}{lll} \textit{maximize:} & & \textit{subject to:} \\ \{\omega_t \text{ and } C_L\} & \rightarrow & \{T_S < T_S^D\}. \end{array} \tag{3}$$

Solving this problem will lead to an OTA with a higher GBW and greater C_L driving capability. It is important to

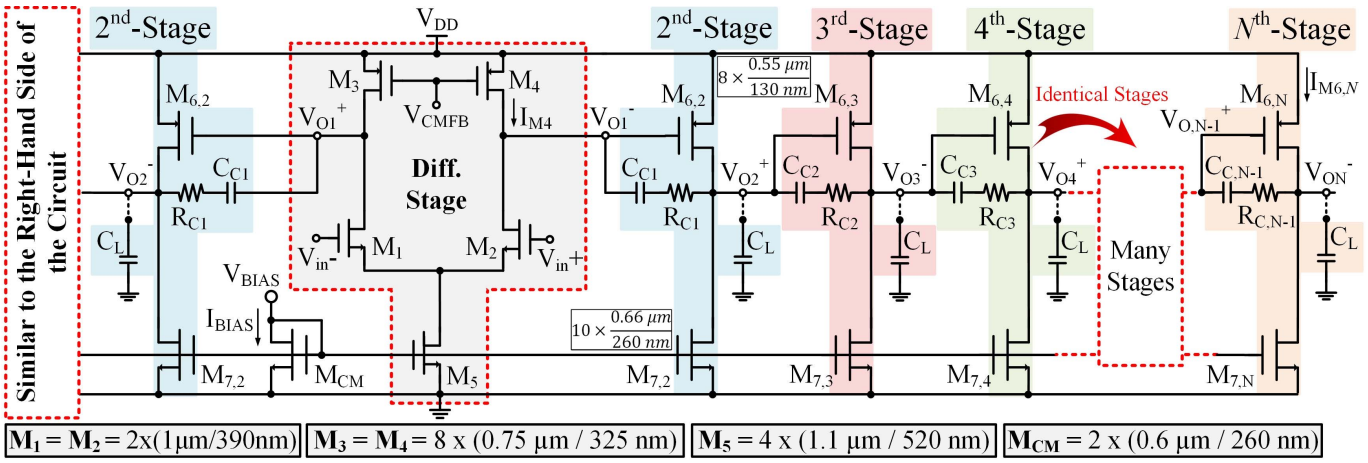


Fig. 3. Transistor level implementation of the scalable N-stage CMOS OTAs. The circuit uses a differential-ended configuration, the right-hand side is shown here only, and an identical left-hand side has been omitted for simplicity.

note that this problem includes both small and large-signal effects. Eqn. (3) contains a two-dimensional objective function involving ω_t and C_L, which are inversely inter-dependent. That is, if C_L increases, ω_t decreases. This makes it difficult to identify the maximum. Instead, this optimization problem is performed in two steps using the following sequential, non-iterative procedure. The first step is to solve the problem expressed as

$$\textit{maximize:} \quad \{\omega_t\} \quad \rightarrow \quad \textit{subject to:} \quad \{C_{L,min} = 0.5 \text{ pF}\}. \tag{4}$$

This can be performed using a small-signal AC analysis, so it takes very little time to perform with a transistor-level simulation. This step places the poles and zeros at desired frequency locations for maximum unity-gain frequency while having the minimum required capacitive load, $C_{L,min}$, (say 0.5 pF). Next, a transient analysis is performed on the OTA in a closed-loop configuration subject to an input step V_{in} with different load conditions, i.e.

$$\textit{maximize:} \quad \{C_L\} \quad \rightarrow \quad \textit{subject to:} \quad \{T_S < T_S^D \text{ for input step} = V_{in}\} \tag{5}$$

While this approach can be executed in a sequential, non-iterative manner, the result may not be optimal but orders of magnitude simpler to implement with excellent results.

Consequently, to satisfy Eqn. (4) and (5), the proposed FCT positions the open-loop P-Z pairs of Eqn. (2) at frequencies below ω_t and above ω_{P0}, without being excluded or canceled (i.e., unlike conventional FCTs [34]), such that

$$\omega_{P0} < \omega_{z1} < \omega_{P1} < \ldots < \omega_{zi} < \omega_{Pi} < \omega_t. \tag{6}$$

Based on the P-Z pair arrangement in Eqn. (6), ω_t can now be maximized (to satisfy Eqn. (4)) where it is no longer equal to the GBW (as it is usually the case in conventional FCTs) but it is now given by

$$\omega_t = A_{DC,N} \times \omega_{P0} \times \prod_{i=1}^{N-1} \left(\frac{\omega_{Pi}}{\omega_{Zi}} \right). \tag{7}$$

According to Eqn. (7), the lower the zeros' frequencies the higher ω_t is; hence the higher C_L is for a desired settling time.

Interestingly, having open-loop P-Z pairs below ω_t creates P-Z doublets in closed-loop. It was shown [35] that the closed-loop P-Z doublet deteriorates the OTA's settling time. Therefore, such P-Z pairs' arrangement has not been introduced in the literature before. However, a fundamental theory has been introduced in [12] revealing that the impact of the P-Z doublets on the settling time of CMOS OTAs can be minimized by positioning the open-loop zeros (i.e., ω_{Zi}) at low frequencies provided there is sufficient DC gain. Consequently, this theory revealed untapped opportunities to cascade many gain stages, which will be exploited in this work.

Since the objective of the proposed FCT is to identify the positions of the OTA's poles and zeros according to Eqn. (6), it is required to identify what governs these poles and zeros from the circuit level realization's perspective. Once these relationships are identified, the detailed steps of implementing the proposed FCT can be easily revealed.

III. The Circuit Level Implementation of the Proposed Scalable Multi-Stage CMOS OTAs

The proposed design of the scalable multi-stage CMOS OTA, shown in Fig. 2, consists of a differential input-stage, cascaded by many identical gain-stages. Fig. 3 shows the transistor level implementation of the differential stage, which serves as the first stage (i.e. M_1 – M_5), followed by identical common-source (CS) gain-stages (the second stage consists of $M_{6,2}$ and $M_{7,2}$ while subsequent stages consist of transistors identical to them, i.e., $M_{6,3}$ and $M_{7,3}$, …, $M_{6,N}$ and $M_{7,N}$).

Having a differential pair followed by CS gain stages is a conventional way to configure OTAs. However, when $N = 2$, this particular OTA has long been assumed to be limited to applications with pF-range loads [36]. Here, through employing the proposed FCT on this circuit, it will be shown that it can increase its C_L-drivability up to the nF-range. Also, when $N = 3$, similar architectures have been described in the literature having a Nested-Miller Capacitor (NMC), as in [22], to help stabilize the OTA. Interestingly, this NMC is of no use in the proposed design technique, and this will contribute to having an area-efficient OTA design. Moreover, using this conventional architecture will show that the proposed FCT is unconstrained by a specific OTA circuit topology.

As mentioned earlier, the purpose of the proposed architecture is to provide a uniform scalable DC gain, where each gain-stage will produce the same DC gain. Hence, all gain

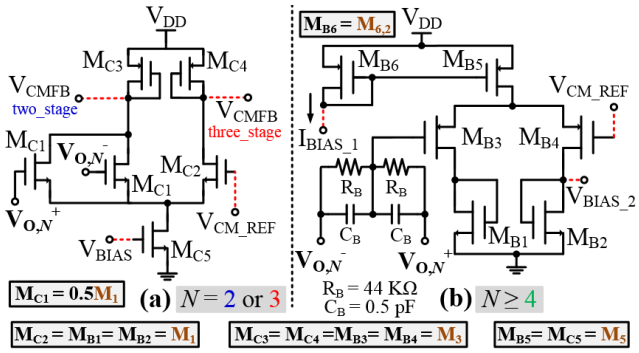


Fig. 4. Common Mode Feedback circuits: (a) The CMFB circuit used for $N = 2$ or 3, and (b) an extra CMFB circuit used for $N \geq 4$.

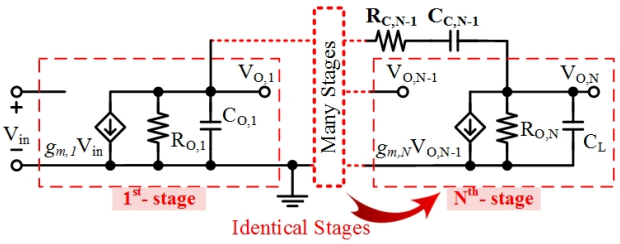


Fig. 5. Single-ended small-signal model of the proposed CMOS OTA.

stages will be biased at the same voltage, and all transistors' sizes of the CS gain stages will be identical. However, one can design the gain stages to have different DC gains and get a non-uniform increase in A_{DC} without increasing the compensation effort.

These gain stages are biased with the current mirror transistors M_{CM}, M_5 and $M_{7,i}$. However, to ensure proper biasing of the output voltages, the Common-Mode Feedback (CMFB) circuits of Fig. 4 have been included in the design. These CMFB circuits are based on standard techniques as described in [36] and [37]. If the 2-stage OTA is to be designed, then the CMFB circuit of Fig. 4(a) is to be used, and the CMFB voltage (V_{CMFB}) is to be created at the drain of M_{C1}. But if N = 3 (i.e., the 3-stage OTA is to be designed), V_{CMFB} is created at the drain of M_{C2} (in Fig. 4(a)). When more than three gain-stages are required, the DC gain will significantly increase, thus, the CMFB circuit of Fig. 4(a) will not be able to hold the biasing voltages at the output of all gain-stages. Therefore, an extra CMFB circuit will be used to keep the biasing voltages of these additional gain-stages within the required values. Fig. 4(b) shows the extra CMFB circuit that will be included when N ≥ 4. In this case, the CMFB circuit of Fig. 4(a) will be connected at the differential output of the 3rd gain-stage, while the CMFB circuit of Fig. 4(b) will be connected at the differential output of each new gain-stage (i.e., N ≥ 4).

Now, to identify the exact DC gain equation of the proposed OTA, the small signal model is to be discussed.

A. The Small-Signal Model of the Proposed OTA

Fig. 5 shows the ideal single-ended small-signal model of the circuit level realization seen in Fig. 2. From circuit theory, one can identify that the small-signal low-frequency gain of each stage is $(g_m \cdot R_O)$. Therefore, the overall DC gain, $A_{DC,N}$, can be expressed as

$$A_{DC,N} = \prod_{i=1}^{N} (g_{m,i} R_{O,i}) \tag{8}$$

where $g_{m,i}$ is the transconductance of each stage, $R_{O,i}$ is the output resistance of each stage.

The first step in the proposed design technique involves setting the voltage gain of the OTA to some desired value. This will pin-down the required sizes of all transistors to meet power consumptions and overdrive voltage requirements. Also, this step will define the values of the small-signal parameters (i.e., $g_{m,i}$ and $R_{O,i}$) of all stages.

Once $g_{m,i}$ and $R_{O,i}$ are defined, the multi-Miller R-C compensation circuits will control the positions of the open-loop *P-Z* pairs. Interestingly, positioning the poles and zeros is not limited to the use of Miller R-C compensation circuits, as other compensation schemes can also be used for this purpose.

According to the *TF* of Eqn. (2), the OTA will have a different number of poles and zeros based on the designer's choice for N. For example, if $N = 2$, one can identify that the 2-stage OTA has three poles and one zero. Typically, only two-poles of this circuit are of concern, as the third is assumed to be at a frequency much higher than ω_t. As a result, the frequency locations of the two-poles and the zero are approximated based on some assumptions as follows [36], [37]:

$$\omega_{P0} \approx \frac{g_{m,2} C_{C1}}{C_{O,1} C_L + C_C \left(C_{O,1} + C_L\right)} \approx \frac{g_{m,2}}{C_L} \tag{9}$$

$$\omega_{P1} \approx \frac{1}{g_{m,2} R_{O,1} R_{O,2} C_{C1}} \tag{10}$$

$$\omega_{Z1} \approx -\left(\frac{g_{m,2}}{C_{C1}}\right) \frac{1}{\left(1 - g_{m,2} R_{C,1}\right)} \tag{11}$$

The third pole at ω_{P_par} - typically ignored in the analysis - has an important design value in the proposed theory and needs to be considered here. It can be approximated by [37]:

$$\omega_{Ppar} \approx \frac{1}{R_{C1} C_{O,1}} \tag{12}$$

where $C_{O,1}$ represents the total shunt capacitance to ground on the output node of the first stage of the OTA and it consists of numerous parasitic elements.

Since the R-C compensation circuits are creating paths between the inputs and outputs of all gain-stages, coupling between stages and correlation between the poles and zeros' positions will occur. Therefore, apart from the two-stage OTA, identifying the exact positions of poles and zeros and/or deriving their exact expressions (using the R-C compensation circuit of Fig. 3) is limited. Also, due to the existence of the parasitic capacitances (i.e., $C_{O,1}$, $C_{O,2}$, …, and $C_{O,N-1}$), parasitics poles will also exist and they will also correlate with the open-loop *P-Z* pairs. In addition, relying on the exact equations of poles and zeros will require re-defining them whenever a new stage is added, hence re-designing the R-C compensation circuit with the addition of each new gain-stage. This will highly complicate the design process. Moreover, adding the CMFB circuits of Fig. 4 to the small-signal model to derive the exact poles and zeros' equations will add a new complexity dimension.

Consequently, to avoid the complexity of using the exact poles and zeros' equations, a scalable FCT is proposed in this work. The proposed FCT starts by designing the compensation circuit of the 2-stage OTA first to satisfy Eqn. (4). This is achieved by adjusting $R_{C1,(2-stage.)}$ and $C_{C1,(2-stage.)}$ such that ω_{Z1} is positioned at low frequency (LF) so that ω_t is increased, provided it meets certain conditions (to be described later).

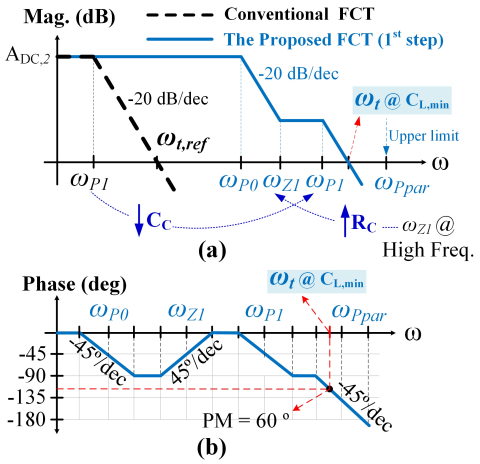


Fig. 6. Ideal AC open-loop response of conventional FCT and the proposed FCT for $N = 2$: (a) the ideal magnitude response showing the impact of the proposed FCT on the value of ω_t according to Step (1), (b) the ideal phase response showing the possible location of ω_t to achieve a PM of 60°.

Then, the proposed FCT will scale the R-C compensation circuit for higher stages while maintaining sufficient values for ω_t. Finally, the proposed FCT follows Eqn. (5) to increase C_L-drivability of the proposed OTAs for a desired settling time. These steps will be clarified in the following sections.

IV. Implementation of the Proposed FCT - Step (1): Increase ω_t Under Small C_L Using LF-Zeros

Conventional FCTs are usually applicable for specific number of stages and/or specific OTAs' circuit topologies. However, the proposed FCT has the advantage of being ideally applicable to N-stage CMOS OTAs, as well it is not constrained by any specific circuit topology, and it is technology independent. Therefore, the key idea of this work is to accurately perform the proposed FCT which is described by Eqn. (4) and Eqn. (5). In this section we shall start by following the technique described by Eqn. (4) to design the 2-stage OTA of Fig. 3, then scale it for higher stages.

A. Implementation of the Proposed FCT Having $N = 2$

The starting point in implementing the proposed FCT is to begin with a two-stage OTA, thus, Eqs. (9) - (12) will govern the positions of ω_{P0}, ω_{P1}, ω_{Z1}, and ω_{P_par}, respectively.

Usually, in conventional 2-stage OTAs, where Miller R-C compensation networks are used, stability is ensured by positioning ω_{P1} at low frequencies (by increasing the value of C_{C1}) and placing ω_{P0} and ω_{Z1} at frequencies above ω_t or by positioning them at the exact same frequency to achieve a pole-zero cancellation [34]. Thus, ω_t in such conventional designs is the GBW, and will be referred to (here) as: $\omega_{t,ref}$. Fig. 6(a) shows the magnitude response (i.e., black-dashed line) of such conventional designs, where $\omega_{t,ref}$ is given by

$$\omega_{t,ref} = A_{DC,2}\omega_{P1}. \tag{13}$$

However, relying on large values of C_{C1} to compensate for the 2-stage OTA will slow down the OTA's response, increase the silicon area, and most importantly, prevent the R-C compensation circuit from being scaled for higher stages as will be discussed in the next subsection.

Consequently, the proposed FCT adapts a different arrangement of poles and zeros to enhance ω_t while having a small C_L ($C_{L,min}$) (i.e., say 0.5 pF); hence, Eqn. (13) will be extended to accurately express the new proposed arrangement of the poles and zeros. Then, the additional increase in ω_t can be traded off for higher C_L.

According to Eqn. (13), it should be obvious that the value of $\omega_{t,ref}$ can be increased by increasing $A_{DC,2}$ and/or ω_{P1}. However, $A_{DC,2}$ has already been pre-defined, consequently, increasing $\omega_{t,ref}$ is simply achieved by increasing ω_{P1}, or in other words; by reducing the value of C_{C1} according to Eqn. (9). The new position of ω_{P1} after reducing C_{C1} is shown (in blue) in Fig. 6(a). Interestingly, pushing ω_{P1} to higher frequencies, by reducing C_{C1} will allow ω_{P0} to become the 3-dB pole of the OTA instead of ω_{P1} (i.e., ω_{P0} mainly depends on $g_{m,2}$ and C_L). This will become useful when increasing the C_L-drivability in the next section. However, reducing the value of C_{C1} alone is a bad design practice because it will alter the stability of the OTA as ω_{P1} will move towards ω_{P0}, and at the same time, ω_{Z1} will be shifted to higher frequencies (i.e., as depicted by Eqn. (11)). Therefore, the gain roll-off will drop to values around −40 dB/dec, and thus, the Phase Margin (PM) will also drop. But, if one can properly re-position ω_{Z1} (after reducing C_{C1}) according to Eqn. (6), ω_{Z1} will counteract the effect of the two poles on the gain-roll off and the PM. As a result, the stability issue can be controlled and the new expression of ω_t can be seen in Eqn. (7).

To re-position ω_{Z1} according to Eqn. (6) and shift it from higher to lower frequencies as seen in Fig. 6(a), one can use a large R_C (i.e., $\sim$ kΩ). As a result, the impact of the proposed FCT in this 1st step, compared to the conventional design, is shown in the AC response of Fig. 6(a).

Since $A_{DC,2}$ is pre-defined, and ω_{P0} is almost independent of the R-C network, Eqn. (7) indicates that the maximum value of ω_t (i.e., near-optimum) can be achieved, ideally, by increasing ω_{P1} while decreasing ω_{Z1}. However, the limitation of the upper value of ω_t is ω_{Ppar}, seen in Eqn. (12) and Fig. 6(a); as there is no full-design control over this parasitic pole. Also, increasing ω_{P1} while decreasing ω_{Z1} should be done so that the PM is greater than some desired value. For example, to obtain a PM of 60°, one can arrange the poles and zeros as shown in the AC phase response of Fig. 6(b). Here, the PM is

$$PM = 180 - \sum_{i=1}^{N-1} \theta_{P,i} + \sum_{i=1}^{N-1} \theta_{Z,i}, \tag{14}$$

where $\theta_{P,i}$ is the phase of the i^{th}-pole and $\theta_{Z,i}$ is the phase of the i^{th}-zero.

To achieve this at the circuit level, one can start with the minimum possible value of C_{C1} given by a certain CMOS technology (i.e., slightly higher than $C_{O,1}$). Then, R_C ($\sim$ kΩ) is increased in value to achieve the required PM so that $\omega_t \leq \omega_{Ppar}$, or until the value of R_C becomes impractical in the given CMOS technology. This will allow the R-C circuit to occupy a small-silicon area. Accordingly, with this, the 1st step of the design process, described by Eqn. (4), would have now been completed for $N = 2$.

B. Scaling the Two-Stage R-C Compensation Circuit for $N \geq 3$ Under $C_{L,min}$

To design the 3-stage OTA, a new gain-stage is added to the 2-stage OTA as depicted in Fig. 2 and Fig. 3. Also, to design a 4-stage OTA, two gain-stages are added to the 2-stage OTA, and so on. Each new gain-stage comes with its own compensation circuit. Consequently, a new P-Z pair

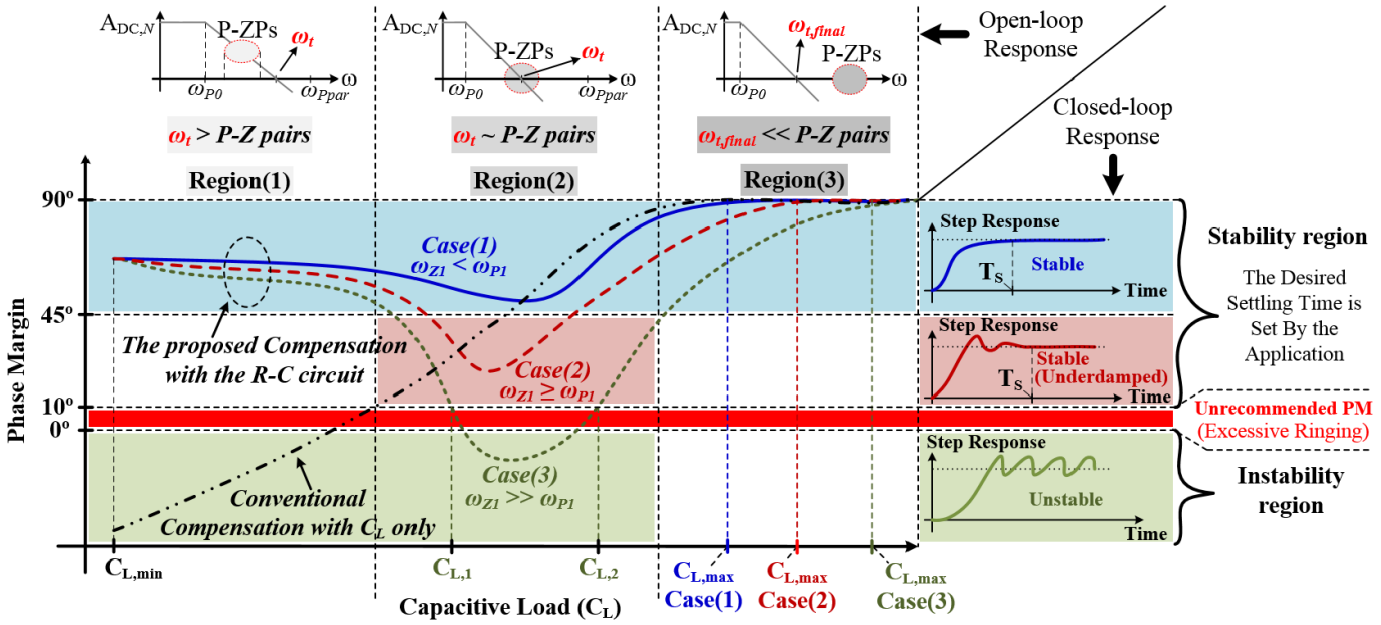


Fig. 7. Phase margin vs. C_L showing the impact of positioning the open-loop *P-Z* pair on the closed-loop step response of the proposed OTAs.

will be added to the *TF* with each new stage as described in Eqn. (2). Also, according to Eqn. (7), ω_t will significantly increase, as $A_{DC,N}$ will also increase. However, this new value of ω_t will most likely exceed the previously defined upper limit of ω_t, and parasitic pole at ω_{Ppar} will impact the OTA's PM. Therefore, it would be necessary to re-adjust the value of ω_t by re-positioning the poles and the zeros, according to Eqn. (6), whenever a new stage is added to keep $\omega_t \leq \omega_{Ppar}$. This can be done by re-sizing the R-C circuit with the addition of each new stage.

Instead of deriving new equations for the poles and zeros for each stage separately, and by knowing that the *P-Z* pairs have an inverse relationship with R_C and C_C, the values for C_C which was found for the 2-stage OTA can be adjusted according to the constraint equations listed below [12]:

$$C_{C(i-1),(N-stage)} = C_{C(i-2),[(N-1)-stage]}, \quad 3 \leq i \leq N \tag{15}$$

and

$$C_{Ci,(N-stage)} > C_{Ci,[(N-1)-stage]}, \quad 1 \leq i \leq N-1. \tag{16}$$

While the R_Cs can be sized in the opposite manner described by the following two constraint equations [12]:

$$R_{Ci,(N-stage)} \leq R_{Ci,[(N-1)-stage]}, \quad 1 \leq i \leq N-1 \tag{17}$$

and

$$R_{C(N-1),(N-stage)} \leq R_{C(N-2),(N-stage)}. \tag{18}$$

Thus, the new compensation capacitor ($C_{C(N-1),(N-stage)}$) is sized to the minimum capacitance value, which was found for the 2-stage OTA (i.e., $C_{C(N-1),(N-stage)} = C_{C1,(2-stage)}$). This highlights the difference between the proposed technique and the conventional methods that rely on large C_{C1} values to realize 2-stage CMOS OTAs.

Since the constraint equations in (15)-to-(18) show an intuitive technique of sizing the R-C compensation circuits for $N \geq 3$, and since there is no need for exact positioning of the poles and zeros, one can slightly tweak these patterns to enhance the open-loop and closed-loop responses if necessary. For example, such tweaking can be done if an exact PM of 60° is required under $C_{L,min}$ of 0.5 pF. Although such re-sizing of the R-C circuits is not considered systematic, an algorithm can be applied to meet the pole-zero constraints of Eqn. (6).

At this point the proposed scalable *N*-stage CMOS OTA is compensated to drive $C_{L,min}$ under the required PM.

V. Implementation of the Proposed FCT - Step (2): Maximize C_L for a Desired Settling Time

Since the design achieved through Step (1) is transferring the dependency of the dominant pole to ω_{P0} (i.e., $C_{L,min}$), one should distinguish between compensating the OTAs with C_L only and the proposed FCT. Interestingly, one can remove the R-C compensation circuit and rely only on C_L to position ω_{P0} below ω_t while leaving the P-Z pairs (i.e., ω_{P1}, ω_{Z1}, ω_{P2}, ω_{Z2} …ω_{Pi} and ω_{Zi}) uncontrolled. On doing so, the stability can be achieved once $C_{L,min}$ is increased such that ω_t is shifted to frequencies much lower than the P-Z pairs. However, this technique is associated with some important drawbacks. First, this technique is technology dependent, in other words; leaving the P-Z pairs uncontrolled, will allow the parasitic capacitances (which are technology dependent) to decide their frequency positions. Second, this technique will work, if and only if, a large $C_{L,min}$ is required (i.e., in the range of tens of nano-Farads). Also, this large $C_{L,min}$ is increasing with the addition of extra gain stages, due to the increase in $A_{DC,N}$ (i.e., ω_t). For these reasons and others, this dependency of the dominant pole on C_L has been claimed to be a bad design practice in [38]. Nevertheless, this will not be an issue in the proposed FCT, since the P-Z pairs have already been positioned at the required frequencies. Consequently, one can define the range of C_L that prevents the P-Z pairs from alternating the OTA's stability. To easily capture the shortage of relying on C_L only to compensate the OTA, and to clearly discuss the advantages of the proposed FCT in increasing C_L-drivability of the proposed OTA, Fig. 7 introduces the relationship between the PM and C_L.

The PM is an open-loop parameter that can indicate the closed-loop step response behavior. Fig. 7 shows how the PM is changing with the increase in C_L based on different scenarios of positioning the OTA's poles and zeros in the proposed FCT. Accordingly, it indicates the behavior of the closed-loop step response. Also, one can use Gain Margin (GM) to indicate the closed-loop behavior as will be done while verifying the proposed OTA designs.

Since the design achieved through Step (1) was still loaded with a very small C_L (i.e., $C_{L,min} = 0.5$ pF) and achieved a sufficient PM (say 60°), one can carry on from this point and investigate the impact of increasing C_L on the PM. According to Eqn. (9), increasing $C_{L,min}$ will result in shifting ω_{P0} to lower frequencies, thus, shifting ω_t to lower frequencies as well. As can be seen in Fig. 7, this will create three different regions based on the new positions of ω_t with respect to the P-Z pairs. In each region the impact of increasing C_L on the PM will depend on the position of ω_{Zi} with-respect-to ω_{Pi}, thus, three cases will be created in each region. To clarify this, let's consider the cases when $N = 2$, and discuss the PM behavior in these three regions based on the position of ω_{Z1} and ω_{P1}.

A. Region (1): $\omega_t >$ P-Z Pairs

This region starts at $C_{L,min}$, where the OTA exhibits a stable response (as discussed in Step (1) of the proposed FCT) and the P-Z pairs are positioned below ω_t. As C_L increases, ω_t moves towards the P-Z pair and a slight drop in the PM will occur. However, this will not affect the closed-loop response as the PM $\geq$ 45°. Therefore, the impact of positioning ω_{Z1} with-respect-to ω_{P1} will not impact the OTA's stability in this region. Nonetheless, it is recommended to achieve sufficient values for PM in Step (1) (i.e., PM $\geq$ 60°) to expand this region as much as possible. This can be done by positioning ω_{Z1} at low frequencies.

In this region, one can clearly distinguish between the proposed FCT and the conventional techniques that depend on C_L only (i.e., the dashed-dotted black line in Fig. 7), where stability cannot be ensured at small values of C_L.

B. Region (2): $\omega_t \sim$ P-Z Pairs

Once increasing C_L to higher values, such that ω_t will be located slightly above, in between, or slightly below the *P-Z* pair, the impact of positioning ω_{Z1} with-respect-to ω_{P1} will become significant. In other words, according to Eqn. (14), if ω_{Z1} is positioned at low frequency (i.e., Case (1): $\omega_{Z1} < \omega_{P1}$), it will compensate the PM drop that will be caused by ω_{P1}, and the PM will be kept above 45° (i.e., the solid-blue line in Fig. 7 is always within the blue shaded area). However, ω_{Z1} will have less impact on the PM if it is positioned slightly above ω_{P1} (i.e., Case (2): $\omega_{Z1} \geq \omega_{P1}$). Consequently, the PM might drop to values below 45° and above 10° (i.e., the dashed-red line is entering the light-red-shaded area in Fig. 7). Nonetheless, the step response will exhibit a stable underdamped behavior, which will be seen as an increase in settling time. However, if $\omega_{Z1} \gg \omega_{P1}$ (i.e., Case (3)), the PM drop (with the increase in C_L) might reach values below 10°, hence, the step response will become unstable within a specific range of C_L (i.e., the dotted-green line will enter the green-shaded area between $C_{L,1}$ and $C_{L,2}$ in Fig. 7). Consequently, Case (3) shows the worst case of stability with the proposed technique. Although the step response might exhibit a stable response for 0° $\leq$ PM $\leq$ 10°, it is assumed unusable in Fig. 7 (i.e., the dark-red shaded area) as it will be associated with excessive ringing [39].

Interestingly, further increase in C_L, within Region (2), will allow ω_t to be at frequencies lower than the *P-Z* pair, thus, the PM will start increasing toward 90°.

Despite having a stable response for 10° $\leq$ PM $\leq$ 45°, the amount of ringing might introduce untolerated noise for some applications. Therefore, the *P-Z* pairs must be optimized for such applications by setting the local minimum PM ($PM_{,min}$) to a given value (say 45°) for a range of C_Ls. If the $PM_{,min}$ cannot be achieved, then the proposed OTA might not be suitable for the given application.

C. Region (3): $\omega_t \ll$ P-Z Pairs

Once the PM reaches 90°, the proposed FCT reaches its definition for the maximum capacitive load ($C_{L,max}$), because at PM = 90°, the R-C compensation circuits will have no more impact on the PM, and C_L will compensate the OTA. Accordingly, one can define C_L-drivability ratios as

$$C_{L-drivability} = \begin{cases} \dfrac{C_{L,max}}{C_{L,min}}, & Case\ (1)\ and\ (2) \\ \dfrac{C_{L,max}}{C_{L,min}} \times \dfrac{C_{L,1}}{C_{L,2}}, & Case\ (3). \end{cases} \tag{19}$$

Since the *P-Z* pairs will have no impact on ω_t in this region, the unity-gain frequency will be referred to as $\omega_{t,final}$ (seen in Fig. 7) and it can be written as: $(A_{DC,N}\omega_{P0})$. Also, the step response will follow a single-time-constant behavior.

Apparently, the proposed OTA will exhibit a stable response once increasing C_L beyond $C_{L,max}$, where the PM will always be $\sim$ 90°, but it will not be included in the discussion to avoid confusing the proposed FCT with conventional ones.

D. Settling Time Requirements

According to Eqn. (5), the objective of this section is to define the range of C_L that corresponds to a desired settling time. Since the design achieved through Step (1) was still loaded with a very small capacitance (i.e., $C_{L,min} = 0.5$ pF), the settling time ($T_{S,initial}$) of the closed-loop amplifier would be very short. Indeed, it is assumed to be much shorter than the desired settling time T_S^D, and hence an increase in settling time can be traded-off for a higher C_L. Knowing that T_S^D is widely varying based on the required application, as seen in Fig. 1(a), one can define a range of C_L's that corresponds to a range of different settling time values by searching on the step response of the closed-loop amplifier beginning with $C_{L,min}$. This can be simply done by increasing C_L, starting from $C_{L,min}$, until the desired settling time is reached, as long as $C_L \leq C_{L,max}$. At this point, the desired C_L ($C_{L,desired}$) can be identified. Here, V_{in} can be driven with a step input whose magnitude can be in the small or large-signal range. There are no constraints on the input condition.

Increasing C_L, starting from $C_{L,min}$, will result in different closed-loop responses based on the P-Z pair's positions, as can be seen on the right-hand side of Fig. 7. Therefore, Fig. 8 builds on these different cases for positioning the P-Z pairs and indicates the relationship between settling time and C_L. Here one sees three curves of settling time T_S vs. C_L

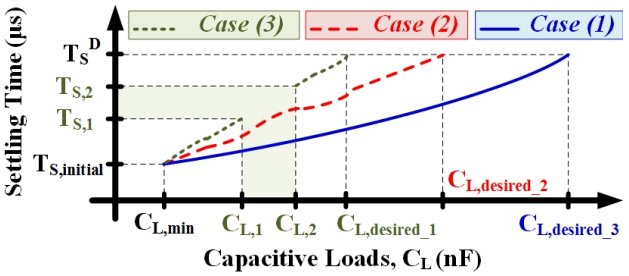


Fig. 8. Relationship between settling time and C_L, showing the different cases that will be created based on the proposed FCT. Note: the nonlinear shape of curves is only for illustrative purposes.

TABLE I

COMPONENT VALUES USED IN THE COMPENSATION CIRCUITS FOR THE REALIZATION OF DIFFERENT OTA STAGES

# of Stage	Compensation Capacitors (pF)				Compensation Resistors (kΩ)			
	C_{C1}	C_{C2}	C_{C3}	C_{C4}	R_{C1}	R_{C2}	R_{C3}	R_{C4}
2	0.05	-	-	-	21	-	-	-
3	0.25	0.05	-	-	44*	21	-	-
4	0.5	0.25	0.25*	-	12.6	44	21	-
5	2	1	0.5	0.5*	10	9	8	8

* These values are not exactly following the scalable pattern of Eqs. (15) and (18) as they have been tweaked to achieve PM values of around 60°.

for different P-Z pairs' positions and maximum C_L conditions. It should be noted here that curves of T_S vs. C_L are nonlinear.

For all scenarios of positioning the P-Z pairs, settling time is increasing with the increase in C_L, however, when $\omega_{Z1} < \omega_{P1}$ the OTA will exhibit faster closed-loop response as the region of underdamped behavior will not be entered (this is shown in the solid-blue line in Fig. 7 and also seen as the solid-blue line of Fig. 8). As for $\omega_{Z1} \geq \omega_{P1}$ and $\omega_{Z1} \gg \omega_{P1}$, the closed-loop response will be partially experiencing stable-underdamped response (as seen in Fig. 7); which will result in slower settling times. Consequently, for the same T_S^D the case of positioning ω_{Z1} at low frequencies will achieve higher C_L-drivability, as $C_{L,desired}$ will be larger (i.e., $C_{L,desired,3} > C_{L,desired,2} > C_{L,desired,1}$ in Fig. 8). But, for the case when $\omega_{Z1} \gg \omega_{P1}$ (i.e., green-dotted line of Fig. 8) the OTA will not be stable between $C_{L,2}$ and $C_{L,1}$ as the PM might drop to values below 10° (the green-shaded area of Fig. 7). Clearly, the benefit of adding zeros at LFs is to boost ω_t and PM. This will also allow increasing C_L while still achieving sufficient GBW. However, it is the GBW that will define the speed of the proposed OTAs and not necessarily the boosted ω_t.

If the C_L range between $C_{L,min}$ and $C_{L,max}$ does not meet the requirements on T_S^D, one can re-adjust the reference design of the OTA by optimizing the biasing voltages and the transistors' aspect ratios. Consequently, the R-C compensation circuits are to be re-designed according to the proposed FCT. If this still does not allow the proposed technique to meet the requirements on T_S^D, then the proposed OTA is not suited for the given application.

VI. VERIFICATION OF THE PROPOSED DESIGN TECHNIQUE

Following the steps in Eqs. (4) and (5), and the detailed procedure of section IV and V, the OTA of Fig. 3 has been designed to achieve a scalable DC gain while driving a wide range of C_Ls. The standard TSMC 65 nm CMOS process has been used to design this OTA with a supply voltage (V_{DD}) of 1 V. Lower V_{DD} values can still be used to drive the proposed OTAs while still achieving sufficent open-loop and closed-loop performances. However, since the goal here is to verifiy the proposed design technique, a nominal V_{DD} value of 1 V will be used. Also, Cadence CAD tools have been used for all simulation investigations. Despite being applicable to N-stage OTAs, the proposed FCT will be verified using 2-, 3-, 4- and 5-stage OTAs.

First, each gain stage has been designed to achieve a DC gain of about 25 dB, thus, the 2-, 3-, 4- and 5-stage OTAs of Fig. 3 are providing a post-layout A_{DC} of 51.18 dB, 77.2 dB, 92 dB, and 110 dB, respectively. To achieve this, the gain stages have been biased with gate voltages at about 0.5 V (i.e, $V_{DD}/2$) and the CS gain stages are designed to be identical (but different than the Diff. Stage) with the sizes shown in Fig. 3. Also, the current source transistors (i.e., M_5 and $M_{7,i}$) are biased at $I_{BIAS} \approx 6\ \mu$A. Consequently, simulation results show that $g_{m,M2} = 112.2\ \mu$A/V, $g_{m,M4} = 113.6\ \mu$A/V, $g_{m,M6} = 540.9\ \mu$A/V, $g_{m,M7} = 695.7\ \mu$A/V, $r_{O,M2} = 70.23$ kΩ, $r_{O,M4} = 68.4$ kΩ, $r_{O,M6} = 11.96$ kΩ, and $r_{O,M7} = 12$ kΩ.

For the 2- and 3-stage OTA, the CMFB circuit of Fig. 4(a) has been used, while the CMFB circuit of Fig. 4(b) has also been added for the 4-stage OTAs with $I_{BIAS_1} \approx 3\ \mu$A, while V_{BIAS_2} has been connected to V_{BIAS} to reduce the number of pins once fabricating the chip. As for the 5-stage OTA, an extra CMFB circuit has been added with $I_{BIAS_1} \approx 3\ \mu$A, and $V_{BIAS\_2} \approx 0.37$ V. Due to the loading effect of the CMFB circuit of Fig. 4(b), the 4-stage OTA has achieved an $A_{DC,4}$ of 92 dB instead of values around 100 dB. The same can be said for the 5-stage OTA. The A_{DC} values for all stages are shown in Fig. 9(a).

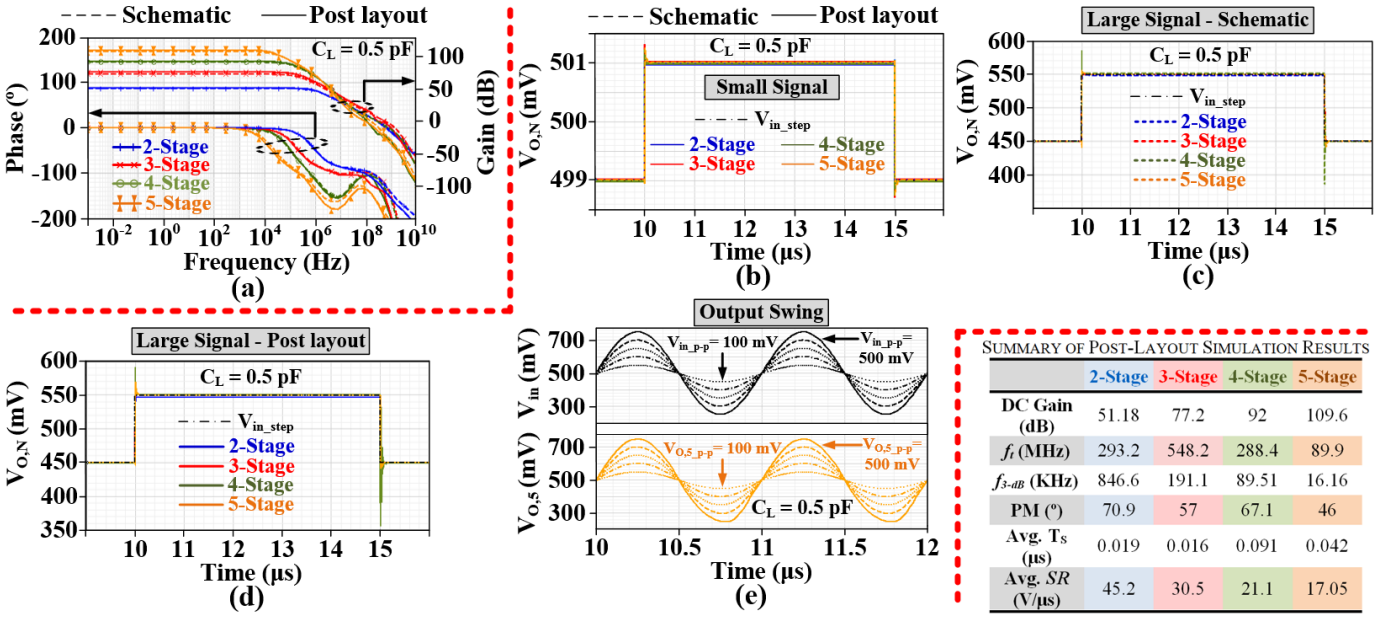
After designing the OTA for the required DC gain, the focus will now be on verifying the proposed FCT by designing the compensation circuits according to Step (1) and (2) (i.e., Eqn. (4) and (5)), so that ω_t is enhanced to a near-optimum value to allow the OTA to drive a wide C_L range.

A. Verification of Step (1): Increase ω_t Under $C_L = 0.5$ pF

The proposed FCT starts by designing the 2-stage OTA's R-C compensation circuit (according to Step (1)) having $C_{L,min} = 0.5$ pF. Therefore, the value of $C_{C1,(2-stage)}$ has been selected to be almost 5 times the value of the parasitic capacitance given by the technology (i.e. $C_{C1} = 50$ fF). For $R_{C1,(2-stage)}$, the value has been swept starting from 1 kΩ, and increased till $R_{C1,(2-stage)}$ reached a value of 21 kΩ. Thus, f_t becomes 293.2 MHz. This value of f_t is near optimum as PM = 70.9 °, which is a reasonable value to indicate stability.

The frequency positions of the P-Z pair after designing the 2-stage OTA's R-C circuit according to Step (1) are: $f_{Z1} =$ 166 MHz and $f_{P1} = 180.5$ MHz. Clearly, these values satisfy Eqn. (6) and the parasitic pole constraint at 787 MHz, which is twice the value of f_t.

Following the scalable technique given by Eqs. (15)-to-(18), the R-C compensation circuits of the 3-, 4-, and 5-stage OTAs are designed as shown in Table I. Based on these values, Eqn. (6) is not satisfied as some P-Z pairs have poles frequencies ω_{Pi} that are less than the zero frequencies ω_{Zi}. However, this is not a concern. For example, in the 3-stage OTA, $f_{Z1} = 15.03$ MHz and $f_{P1} = 10.06$ MHz (i.e., $\omega_{Z1} > \omega_{P1}$), while for the 4-stage OTA, $f_{Z1} =$ 14.58 MHz, $f_{P1} = 1.8$ MHz, $f_{Z2} = 29.1$ MHz, and $f_{P2} =$ 12.4 MHz (i.e., $\omega_{Z1} \gg \omega_{P1}$ and $\omega_{Z2} > \omega_{P2}$). Nevertheless,



SUMMARY OF POST-LAYOUT SIMULATION RESULTS

	2-Stage	3-Stage	4-Stage	5-Stage
DC Gain (dB)	51.18	77.2	92	109.6
f_t (MHz)	293.2	548.2	288.4	89.9
$f_{3\text{-}dB}$ (KHz)	846.6	191.1	89.51	16.16
PM (°)	70.9	57	67.1	46
Avg. T_S (µs)	0.019	0.016	0.091	0.042
Avg. *SR* (V/µs)	45.2	30.5	21.1	17.05

Fig. 9. Schematic and post-layout simulations of the open-loop and unity-gain closed-loop configurations of the differential-ended 2-, 3-, 4-, and 5-stage CMOS OTAs of Fig. 3 after implementing the proposed FCT under $C_L = 0.5$ pF, (a) the AC magnitude and phase responses, (b) the small-single step response (schematic and post-layout) of all stages subject to a step-input of 2 mV, (c) the large-single step response (schematic) of all stages subject to a step-input of 100 mV, (d) the large-single step response (post-layout) of all stages subject to a step-input of 100 mV, and (e) the output swing of the proposed 5-stage OTA subject to different input peak-to-peak voltages (i.e., 100 mV, 200 mV, 300 mV, 400 mV and 500 mV).

the PM has reached values around 60°. Also, ω_t is at high frequencies and ω_{Ppar} are still higher than ω_t.

Fig. 9 summarizes all schematic and post-layout results for open-loop and closed-loop configurations after implementing Step (1) of the proposed FCT under $C_L = 0.5$ pF. A summary of the most important metrics that can be drawn from these simulations are shown on the right-bottom corner of Fig. 9.

Clearly, all stages are achieving the required DC gain while exhibiting a stable response. However, the 4-stage post-layout magnitude response is affected by the parasitics after extraction, and its gain roll-off at ω_t is less than - 20 dB/dec. As a result, the 4-stage OTA step response (under $V_{in} = 100$ mV) is showing some ringing, which is translated as an increase in its settling time compared to other stages.

Also, one can notice a dip in the 4- and 5-stage phase responses. Therefore, for further tests of stability, the output swing of the proposed 5-stage OTA has been simulated for different peak-to-peak input voltages as can be seen in Fig. 9(e). The results indicate no unforeseen stability issues. Also, the proposed OTAs have been tested having a closed-loop gain of 10 dB and the results exhibit a stable response as well.

Also, as can be seen in Fig. 9's summary of results, the Average Slew Rate (Avg. *SR*) is decreasing as the number of gain stages is increasing, where the Avg. *SR* of the proposed OTAs can be approximated by

$$\text{Avg. } SR \approx \min\left(\frac{I_{M4\_AVG}}{C_{C,1\_eq}}, \frac{I_{M6,2\_AVG}}{C_{C,2\_eq}}, \ldots, \frac{I_{M6,N\_AVG}}{C_{C,N\_eq}}\right) \tag{20}$$

where $I_{M,4\_AVG}$, $I_{M6,2\_AVG}$, …, I_{M6,N_AVG} are the average currents (i.e., average of the rising and falling edges) flowing at the output node of each gain stage, while $C_{C,1\_eq}$, $C_{C,2\_eq}$, …, C_{C,N_eq} are the equivalent compensation capacitances which are seen at these output nodes. For instance, ($C_{C,1\_eq} \approx C_{C1}$), ($C_{C,2\_eq} \approx C_{C1} + C_{C2}$), …, and ($C_{C,N\_eq} \approx C_{C,(N\text{-}1)} + C_L$). The simulations are showing that $I_{M,4\_AVG}$ is 7.1 µA, while I_{M6,N_AVG} (for $N = 2$ to 5) is 358.5 µA. Since $I_{M,4\_AVG} \ll I_{M6,N\_AVG}$, the output node of the 1st stage is dominating the *SR* behavior of the proposed OTAs given that the OTAs are driving pF-range C_L. Thus, since C_{C1} is the capacitance seen at the output node of 1st-stage, and according to the proposed FCT, C_{C1} is increasing as the number of stages is increasing; hence, the Avg. *SR* is decreasing as the number of stages is increasing.

If a very large C_L is required (i.e., in the nF-range), the dependency of the SR will be transferred to the output node of the last gain-stage. Consequently, one can increase the value of $I_{M6,N}$ to keep the SR within sufficient values. However, by designing the OTA to have a high $I_{M6,N}$, the power consumption will increase. This will become a trade-off between C_L, *SR*, and power consumption. Interestingly, some designs in the literature have adapted alternative class AB implementations that preserve *SR* with lower power consumption as in [31]. However, adding such class AB output stage might affect the proposed poles/zeros arrangement, which might require further optimization. The post-layout power consumption in the proposed designs is 106 µW, 180.1 µW, 276.7 µW, and 387 µW, for the 2-, 3-, 4-, and 5-stage OTAs, respectively. Also, one should consider that this value is for a fully differential-ended topology.

Even though many resistors are being used in the proposed OTAs, the noise has not been affected that much, because the resistors mainly affect the noise of the output stage, while the 1st stage noise is the dominant noise. Therefore, the post-layout input referred noise at 10 kHz is 82.2 nV/$\sqrt{\text{Hz}}$ for the 2- and 3-stage OTAs and 78.1 nV/$\sqrt{\text{Hz}}$, for the 4-stage OTA.

B. Verification of Step (2): Maximize C_L for a Desired T_S

After designing the proposed OTAs to properly drive $C_{L,min}$ of 0.5 pF, the goal now is to define the range of C_L under which the 2-, 3-, 4- and 5-stage OTAs' closed-loop responses are stable, and to find the corresponding settling time for this

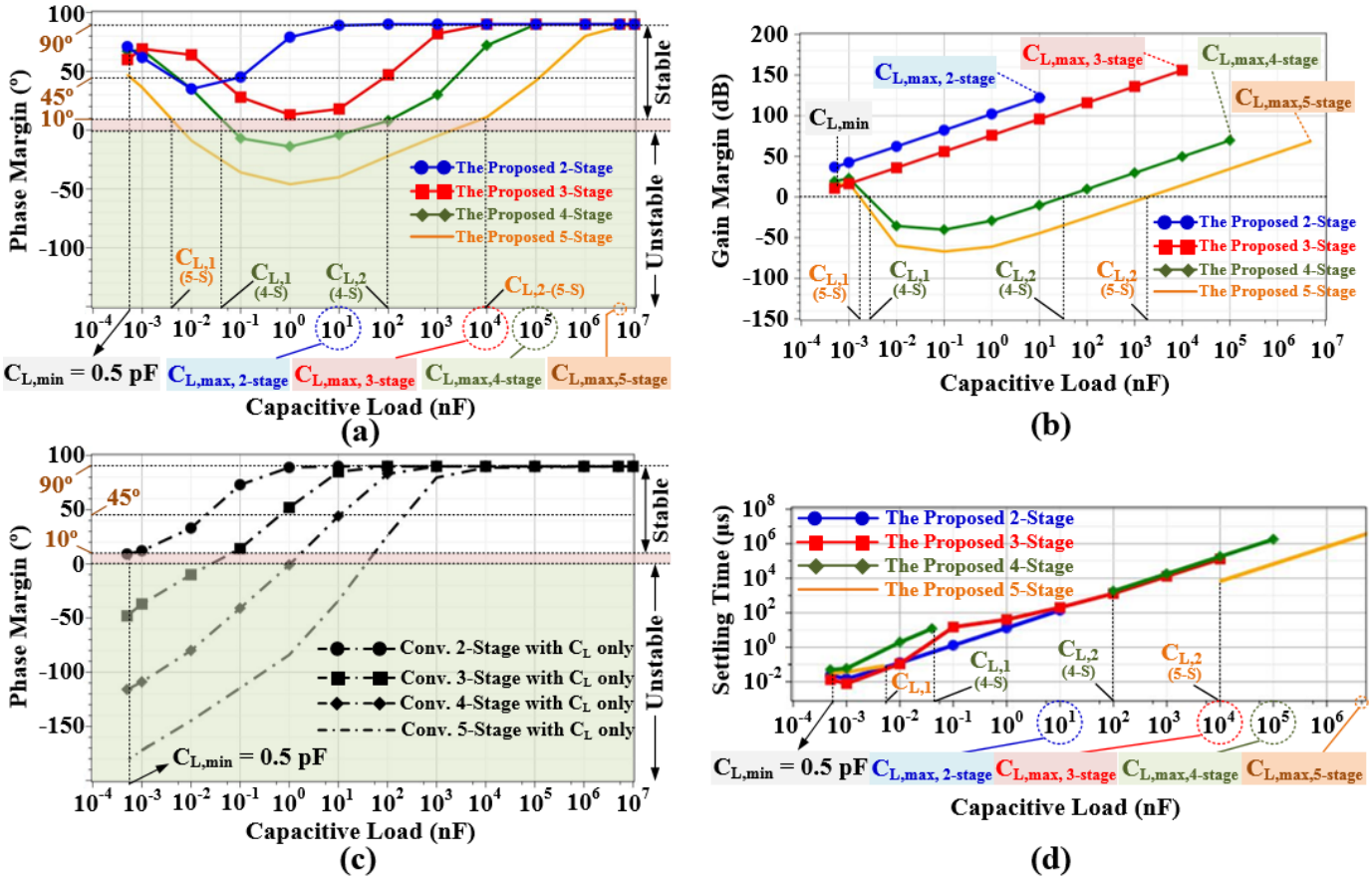


Fig. 10. Impact of maximizing C_L according to Step (2) of the proposed FCT on PM, GM, and settling time: (a) the relationship between PM and C_L as described in Fig. 7 for the proposed OTA, (b) the relationship between GM and C_L for the proposed OTAs, (c) the relationship between PM and C_L when designing the proposed OTAs with a conventional FCT that depends on C_L only, and (d) the relationship between settling time and C_L as described in Fig. 8.

range of C_L. Therefore, similar steps of creating Fig. 7 and Fig. 8 (i.e., investigating the PM and the settling time variations vs. the increase in C_L) are being followed here.

Consequently, Fig. 10(a) shows the simulation results of PM vs. C_L. Apparently, the proposed 2-stage OTA (solid-blue line with circles) is stable with PM $\geq 45°$, for all values of C_L, except between 10 pF to 100 pF where it goes slightly below 45°. Therefore, it mainly follows *Case (1)* of Fig. 7, which is the expected response since $\omega_{Z1} < \omega_{P1}$. To define $C_{L,max}$, one can observe the C_L value of Fig. 10(a) at which the PM becomes 90°. Clearly, $C_{L,max}$ is 10 nF; thus, C_L-drivability ratio according to Eqn. (19) is 20,000×.

As for the proposed 3-stage OTA, the closed-loop response is always stable as the PM doesn't reach the instability region (i.e., green-shaded area of Fig. 10(a)) with the increase in C_L. Clearly, the PM follows *Case (2)* of Fig. 7, which is an expected response since $\omega_{Z1} > \omega_{P1}$ of the 1st *P-Z* pair as mentioned earlier. Interestingly, with $C_{L,max}$ of 10 μF, C_L-drivability ratio of the proposed 3-stage OTA is 20,000,000x.

As for the proposed 4-stage OTA, the PM behavior follows *Case (3)* of Fig. 7, where it goes below 10° in between $C_{L,1} = 40$ pF and $C_{L,2} = 100$ nF. Again, this is an expected behavior due to the 1st and 2nd *P-Z* pairs' arrangement, where $\omega_{Z1} \gg \omega_{P1}$. Nonetheless, the proposed 4-stage OTA is operating properly under all other values and exhibiting a C_L-drivability ratio of 80,000x. The same can be said for the proposed 5-stage OTA,, where the PM goes below 10° in between $C_{L,1} = 5$ pF and $C_{L,2} = 10$ μF, exhibiting a C_L-drivability ratio of 5000x, with $C_{L,max} = 5$ mF.

Since the PM might not always reflect the actual closed-loop step response, and since the open-loop AC response of Fig. 9(a) shows a dip in the phase response below ω_t for the 4- and 5-stage OTAs, one can use the GM test to ensure its full agreement with the PM and there will be no multiple phase crossover points with −180°. Fig. 10(b) shows the simulation results of GM vs. C_L. Clearly, the GM is ≥ 0 dB in the stability regions which have been defined by the PM in Fig. 10(a).

To clearly measure the improvement that has been done by the proposed FCT on C_L-drivability of CMOS OTAs, one can compensate the proposed OTAs with the conventional FCT (i.e., which relies on C_L only to compensate the OTA) and compare the results. Fig. 10(c) shows the PM behavior once conventional techniques are used to compensate for the proposed 2-, 3-, 4- and 5-stage OTAs. Clearly, the conventional technique might only work for 2-stage OTA, but it cannot be scaled for higher number of stages (i.e., it is not suitable for scaled-down CMOS technologies) unless large C_Ls are only required, which is not the case in most applications as depicted in Fig. 1(a).

The results in Fig. 10(a)-(c) pave the way to verify the unity-gain closed-loop step-response of the proposed OTAs to find the relationship between settling time and C_L. Since the settling time is expected to vary based on the different cases of positioning the open-loop *P-Z* pairs as stated in Fig. 8, the 2-stage OTA is expected to have the fastest response as it mostly follows *Case (1)*. Fig. 10(d) verifies this for all C_L values above 100 pF. However, although the 3-stage OTA is following *Case (2)*, it exhibits faster response for C_L values

TABLE II
MEASUREMENTS' BIASING VOLTAGES AND CURRENTS

Biasing Parameters	Two-Stage	Three-Stage	Four-Stage
V_{CM_REF} (V)	0.43	0.47	0.5
V_{IN_BIAS} (V)	0.43	0.49	0.43
I_{BIAS} (µA) & I_{BIAS_1} (µA)	27.2 & N/A	27.2 & N/A	27.2 & 13.6

TABLE III
MEASUREMENTS' RESULTS OF THE OPEN-LOOP PERFORMANCE METRICS

Metric	Two-Stage		Three-Stage		Four-Stage	
DC gain (dB)	~ 50		~ 70		~ 90	
Power (µW)	126.8 @ 1V		227.9 @ 1V		353.1 @ 1V	
C_L	1 pF	10 nF	1 pF	10 µF	1 pF	100 µF
$f_{t,final}$ (MHz)	6.17	0.06	7.75	0.0011	0.47	0.000002

below 100 pF. The reason for this can be indicated from Fig. 10(a), where the 3-stage OTA is having higher PM values than the 2-stage OTA in between 1 pF to 100 pF.

All other open-loop and closed-loop parameters are being considered as the value of C_L is increasing; but for simplicity and to avoid repetition, these parameters will be shown as the proposed OTAs are being validated with measurement results in the following section.

VII. EXPERIMENTAL RESULTS AND ROBUSTNESS TESTS

The standard TSMC 65 nm CMOS process is used to fabricate the differential-ended 2-, 3- and 4-stage CMOS OTAs of Fig. 3 with the devices' sizes shown in Fig. 3, Fig. 4, and Table I. However, the proposed 5-stage OTA has not been fabricated. Fig. 11 shows the fabricated chip's microphotograph. Since a wide range of C_L is required, each proposed OTA has been fabricated twice (i.e., with C_L on-chip for a small $C_L = 1$ pF and C_L off-chips for higher values). To illustrate the area and the elements in fabricating the proposed differential-ended 2-, 3-, and 4-stage CMOS OTAs, the layout drawing of the 2-stage OTA is embedded and enlarged in Fig. 11, where the overall dimensions is 53.9 μm × 39.7 μm, resulting in an area of 0.0021 mm^2. As seen in the layout drawing, R_{C1} dominates the chip's size and occupies almost half the chip's silicon area. But, as C_{C1} is set just above the parasitic level, the overall silicon area remains quite small (total area = 0.0021 mm^2). The R_C used here is the standard N-well resistor with sheet resistance 316 Ω/square. As for the C_{C1}, a mimcap with the same length and width of 4.8 μm is used for a C_{C1} value of 50 fF. The same can be said for the 3- and 4-stage OTAs, except more silicon area is required as seen in Fig. 11.

A. Measurements' Results

This chip has been tested in a unity-gain closed-loop configuration to obtain the closed-loop and open-loop performance metrics of each OTA. Table II lists the critical OTA biasing parameters from a step response test involving a 100 mV step input. Subsequently, Fig. 12 show the output step response of the 2-, 3-, and 4-stage OTAs under different values of C_L (i.e., starting from $C_{L,min}$ up to $C_{L,max}$) as captured by an Agilent DSA80000B oscilloscope. The closed-loop performance metrics (i.e. settling time and SR), for different values of C_L, are included on each time plot shown in Fig. 12. Also, Table III shows the DC gain of the proposed OTAs, along with a summary of the open-loop measurements' results for the proposed 2-, 3-, and 4-stage CMOS OTAs under $C_{L,min}$ and $C_{L,max}$ for each OTA.

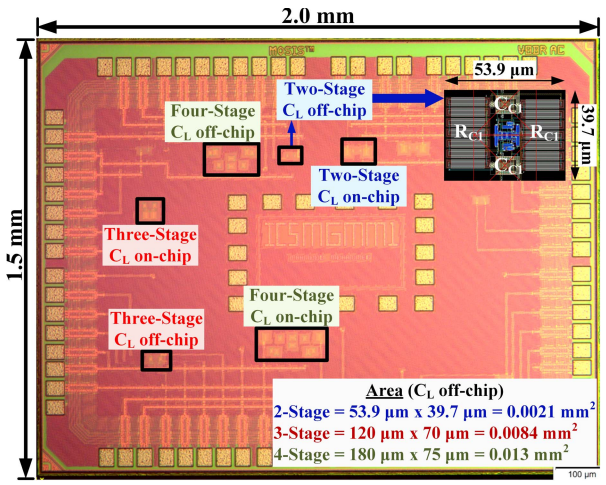


Fig. 11. Chip's microphotograph showing the proposed differential-ended 2-, 3- and 4-stage CMOS OTAs with C_L on- and off-chip for each OTA.

TABLE IV
SCHEMATIC-BASED MONTE-CARLO SIMULATIONS OF THE PROPOSED OTAS FOR DIFFERENT PERFORMANCE PARAMETERS UNDER $C_{L,min} = 0.5$ PF, FOR 400 RUNS

# of Stages	*PM* (°)		*BW* (kHz)		*DC gain* (dB)		*GM* (dB)	
	μ	σ_D	μ	σ_D	μ	σ_D	μ	σ_D
2	71.3	0.16	903.9	29	50.49	0.14	36.8	0.38
3	59.1	1.17	199	8.2	72.4	0.26	11.3	0.28
4	70.5	0.77	95.2	4.4	90.6	0.43	17.5	0.53
5	40	5.3	21.6	3.1	104.5	4.5	15.4	2

By comparing these measurement results with the schematic and post-layout simulation results we found during the verification, one can conclude that these results are in general agreement with one another. Thus, the proposed FCT is being applied properly. It should be noted, however, that the 4-stage OTA has a $C_{L,1}$ and $C_{L,2}$ values that is slightly different than what was predicted by simulation, i.e., 40 pF versus 100 pF for $C_{L,1}$, and 100 nF versus 10 nF for $C_{L,2}$.

B. Robustness Tests

To ensure the robustness of the proposed design, process corners and Monte-Carlo (MC) simulations have been conducted for different OTAs' parameters, under different C_L's, in open-loop and closed-loop configurations. This was conducted for both schematic-based and post-layout-based designs. Table IV shows a test for the design robustness using the schematic-based MC simulations for the 2-, 3-, 4- and 5-stage CMOS OTAs. Here, the Process Variation Coefficient (PVC) $[(\sigma_D/\mu) \times 100\%]$ for all 2-, 3-, and 4-stage OTAs' parameters is less than 5 %. However, PVC increases to values slightly above 10 % for the proposed 5-stage OTA's parameters, except for the DC gain, where the PVC is 4.3 %.

Moreover, to test the proposed OTAs robustness under PVT variations, the post layout-based process corners of the proposed 2-, 3-, 4- and 5-stage OTAs under C_L of 1 pF are conducted. Fig. 13 reports the results of different performance metrics' behavior under these process corners. As can be seen in Fig. 13, all process corners, for all metrics, indicates no unforeseen sensitivity issues. Consequently, using the results shown in Table IV and Fig. 13, one can conclude that the proposed OTA designs are robust under PVT variations.

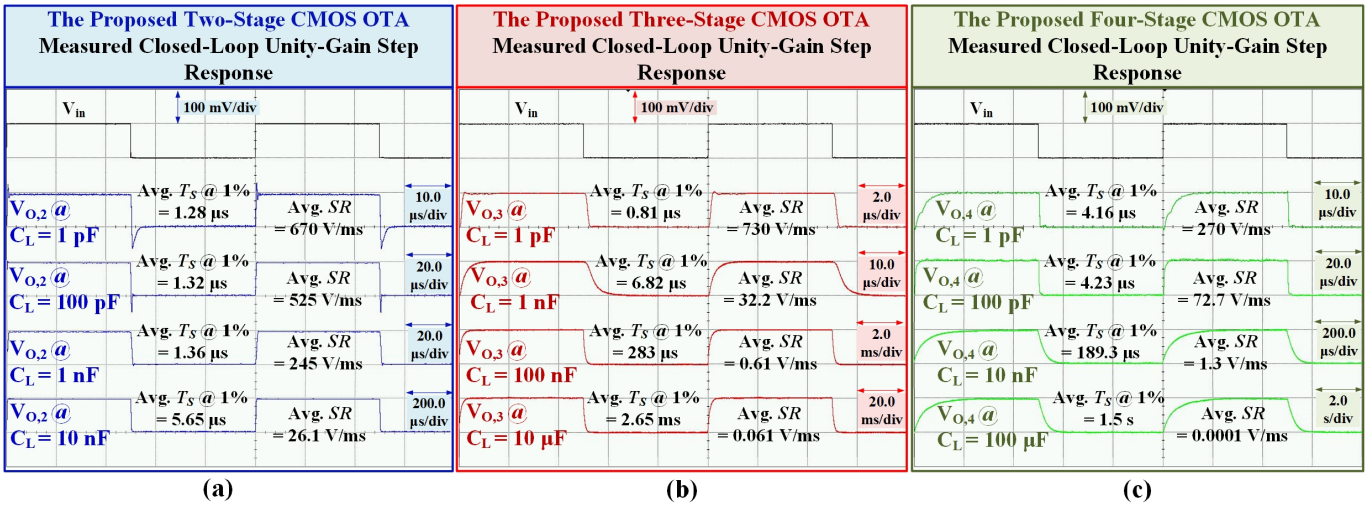


Fig. 12. Measurement's results of the unity-gain closed-loop step response under different capacitive load values (a) the proposed two–stage CMOS OTA of Fig. 3, (b) the proposed three–stage CMOS OTA of Fig. 3, and (c) the proposed four–stage CMOS OTA of Fig. 3.

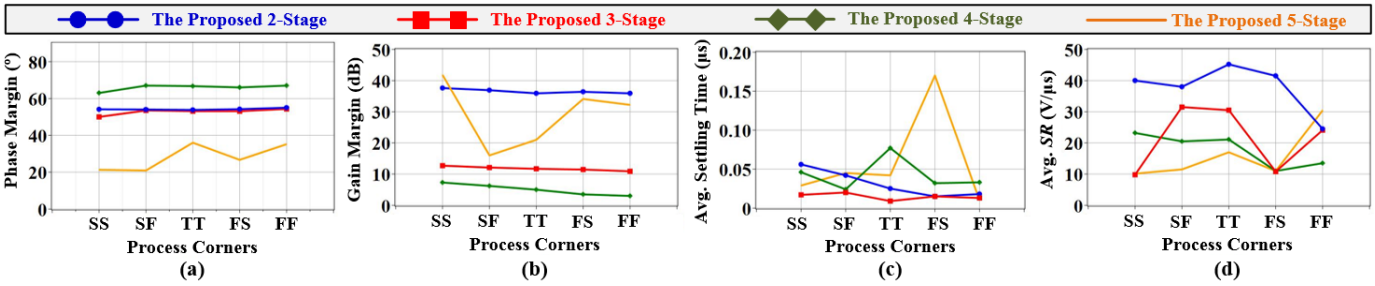


Fig. 13. Robustness tests using process corners at T = 25 °C for the proposed OTAs under C_L = 1 pF: (a) PM, (b) GM, (c) avg. settling time, and (d) avg. SR.

Clearly, the 5-stage OTA shows less robustness compared to other stages. With ft = 89.9 MHz, positioning the 5-stage OTA *P-Z* pairs becomes tight, which increases the sensitivity to the PVT variations. This indicates that the proposed technique will reach a limit in the number of cascaded gain-stages, which was found to be 8 stages in [12], given that each stage is achieving 25 dB per stage.

VIII. Comparison

To clearly highlight the achieved advancements of this work, the proposed 2-, 3-, 4- and 5-stage OTA designs have been compared with previously reported OTA designs. For fair comparison, measurement-based works, where CMOS OTAs can drive a wide range of C_Ls have been reported in Table V. Therefore, op-amps, simulation-based works (including the proposed 5-stage OTA), and OTAs with a single C_L driving capability have been excluded from Table V.

Referring back to Fig. 1(a) where the settling time requirements vs. C_L for different applications are shown, one can appreciate the need for an OTA with a wide-ranging drivability features, even if the OTA settles in seconds. Fig. 14 superimposes a load-drivability summary of the OTA results of this work with the best results found in the literature [27] and [33], as it compares with the applications reported in Fig. 1(a). As is clearly evident, *the proposed OTAs cover more applications than any other reported work.*

In addition to the simplicity of the proposed design which uses conventional gain stages with multi-Miller R-C compensation circuits across gain stages, the proposed FCT is applicable to 2-, 3-, 4- and 5-stage OTAs. This is a feature

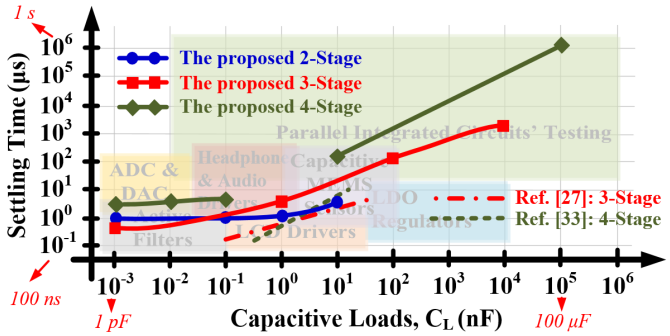


Fig. 14. Comparing the proposed measured-based OTA designs with the previously reported works in terms of C_L drivability from the applications' perspective.

that is not available in any of the previously published works. This offers wider design choices for DC gain and power consumption for different applications.

To set the comparison in a conventional way, the following well-established figures of merit (FOMs) have been used [27]:

$$FOM_S = \frac{\text{GBW}.C_L}{\text{Power}.\text{Area}} \times C_{L-drivability} \tag{21}$$

$$SIFOM_L = \frac{\text{GBW}.C_L}{\text{Power}.\text{Area}} \times \frac{C_{L-drivability}}{T_S} \tag{22}$$

Table V shows that the proposed OTAs outperform all other reported works in FOM_S, where the highest values is reported for the proposed 3-stage OTA, followed by the proposed 4-stage OTA and then comes the proposed 2-stage

TABLE V

PERFORMANCE COMPARISON WITH THE STATE-OF-THE-ART MEASUREMENT-BASED OTAS THAT DRIVE A WIDE RANGE OF C_LS

Ref.	# of Stages	Circuit/ Compensa. Topology	CMOS process (nm)	DC gain (dB)	Power (µW) @V_{DD}(v)	Chip Area (mm^2)	C_L (nF)	C_L-drivability	GBW (MHz)	T_S @1% (µs)	FOM_S	SI-FOM_L
[16] '15 JSSC	1	Signal-Cur. Enhancer	130	100	16.8 @ 0.7	0.0027	10	3x	1.99	0.974	1316	1351
							30		0.77	2.61	1527	585
[24] '16 TCAS-I	3	Single Miller Capacitor	350	136*	49.8 @ 2	0.003	5	3x	2.85	0.63	286	454
							15		2.8	0.93	843	906
[25] '18 TCAS-II	3	Single Miller Capacitor	350	113	8.9 @ 1.4	0.0025	10	10x	1.7	2	7640	3820
							100		0.43	7.7	19320	2500
[26] '15 JSSC	3	Current Enhancer	130	~100	16.8 @ 0.7	0.0027	10	3x	1.99	0.97	1316	1356
							30		0.77	2.61	1527	585
[27] '20 TCAS-I	3	Cap. Free	130	~72	185 @ 1 95 @ 1	0.006	0.09	555.5x	4.23	0.2	194.5	972.8
							50		0.46	4.62	22410	4850
[33] '20 TVLSI	4	Active Parallel Amp.	130	107	175.2 @ 1.2	0.007	0.4	30x	2.75	0.33	67.2	203.8
							12		1.18	9.75	28.8	2.96
This Work	**2**	Multi-Miller R-C	65	~50	126.8 @ 1	**0.0021**	0.001	10,000x	6.17	1.28	231.7	181
							10		0.06	5.65	22,532	3,988
	3	Multi-Miller R-C	65	~70	227.9 @ 1	0.0084	0.001	**1,000,000x**	7.75	0.81	4048.3	4997.9
							10000		0.0011	2650	**5,746,045**	2100
	4	Multi-Miller R-C	65	~ 90	353.1 @ 1	0.013	0.001	**1,000,000x**	0.47	4.16	102.3	24.5
							0.1		1	4.23	21,785	**5150.1**
							10		0.018	189.3	39,213	207.1
							100,000		0.000002	1.5x10^6	43570	0.025

* Simulation-based.

OTA. Also, the proposed OTAs outperform all other reported works in $SIFOM_L$, where the highest values is reported for the proposed 4-stage OTA (at $C_L = 100$ pF), followed by the proposed 3-stage OTA and then comes the proposed 2-stage OTA. However, the proposed 4-stage OTA has a low $SIFOM_L$ at $C_{L,max} = 100$ μF due to the long settling time of such large C_L. Also, looking at the OTAs' metrics individually, one can see that the proposed 4-stage OTA has the highest $C_{L,max}$ of 100 μF. Moreover, the proposed 4- and 3-stage OTAs have the maximum C_L drivability of 1,000,000x, followed by the proposed 2-stage OTA with a C_L-drivability of 10,000x. Moreover, the proposed differential-ended 2-stage OTA occupies the smallest silicon area of 0.0021 mm^2. Finally, despite using the smallest CMOS technology node of 65 nm and achieving a slightly lower DC gain than other reported works in Table V, the proposed technique can be scaled for higher number of stages and achieve higher DC gain as shown in the post-layout results of the proposed 5-stage OTA with a DC gain of $\sim$ 110 dB.

IX. CONCLUSION

A new frequency compensation technique that allows cascading multi-stage CMOS OTAs and driving a very wide range of C_L (i.e., pF- to μF-range) was introduced. The proposed technique involves positioning the OTA's zeros at low frequencies to increase ω_t of the OTA. The additional increase in ω_t can be traded off for higher C_L by transferring the dependency of the dominant pole to C_L. To achieve this, the OTA was designed using multi-Miller R-C compensation circuits across the OTA's gain-stages. Also, the proposed technique was shown to be unconstrained by the OTA's circuit topology. Hence, conventional gain-stages (i.e., differential pair and common source transistors) were used to design fully-differential 2-, 3-, 4-, and 5-stage CMOS OTAs with a C_L-drivability of 10,000×, 1,000,000x, 1,000,000x, and 5,000x, respectively. This is 10-to-1000-time improvement in the state-of-the-art. Accordingly, the proposed OTAs can cover a wider range of applications than any other reported works. The proposed 2-, 3-, and 4-stage OTA designs have been fabricated in the standard TSMC 65 nm CMOS process and the measurement results validate the claims made in this work.

REFERENCES

[1] N. Aghaee, Z. Peng, and P. Eles, "Temperature-gradient-based burn-in and test scheduling for 3-D stacked ICs," *IEEE Trans. VLSI*, vol. 23, no. 12, pp. 2992–3005, Dec. 2015.

[2] M. Mohammed, S. Kawar, and K. Abugharbieh, "Methodology for designing and verifying switched-capacitor sample and hold circuits used in data converters," *IET Circuits, Devices Syst.*, vol. 8, no. 4, pp. 252–262, Jul. 2014.

[3] A. S. Emara et al., "An area-efficient high-resolution segmented $\Sigma\Delta$-DAC for built-in self-test applications," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 29, no. 11, pp. 1861–1874, Nov. 2021.

[4] *Active Filters for Video, Reference Design 3172*, Maxim Integrated, San Jose, CA, USA, Jul. 2004.

[5] V. Dhanasekaran, J. Silva-Martinez, and E. Sanchez-Sinencio, "Design of three-stage class-AB 16 Ω headphone driver capable of handling wide range of load capacitance," *IEEE J. Solid-State Circuits*, vol. 44, no. 6, pp. 1734–1744, Jun. 2009.

[6] F. Xiao and P. K. Chan, "A performance-aware low-quiescent headphone amplifier in 65-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 52, no. 2, pp. 505–516, Feb. 2017.

[7] W.-J. Huang, S. Nagayasu, and S.-I. Liu, "A rail-to-rail class-B buffer with DC level-shifting current mirror and distributed Miller compensation for LCD column drivers," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 58, no. 8, pp. 1761–1772, Aug. 2011.

[8] B. Li, W. Wang, J. Liu, W.-J. Liu, Q. Yang, and W.-B. Ye, "A 1 pF-to-10 nF generic capacitance-to-digital converter using zero-crossing $\Delta\Sigma$ modulation," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 65, no. 7, pp. 2169–2182, Jul. 2018.

[9] C. Stagni et al., "CMOS DNA sensor array with integrated A/D conversion based on label-free capacitance measurement," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2956–2964, Dec. 2006.

[10] K. N. Leung and P. K. T. Mok, "A capacitor-free CMOS low-dropout regulator with damping-factor-control frequency compensation," *IEEE J. Solid-State Circuits*, vol. 38, no. 10, pp. 1691–1702, Oct. 2003.

[11] W. Oh and B. Bakkaloglu, "A CMOS low-dropout regulator with current-mode feedback buffer amplifier," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 54, no. 10, pp. 922–926, Oct. 2007.
[12] M. A. Mohammed and G. W. Roberts, "Generalized relationship between frequency response and settling time of CMOS OTAs: Toward many-stage design," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 68, no. 12, pp. 4993–5006, Dec. 2021.
[13] M. A. Mohammed and G. W. Roberts, "A scalable many-stage CMOS OTA for closed-loop applications," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, May 2021, pp. 1–5.
[14] K. H. Mak and K. N. Leung, "A signal- and transient-current boosting amplifier for large capacitive load applications," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 61, no. 10, pp. 2777–2785, Oct. 2014.
[15] Z. Yan, P.-I. Mak, M.-K. Law, R. P. Martins, and F. Maloberti, "Nested-current-mirror rail-to-rail-output single-stage amplifier with enhancements of DC gain, GBW and slew rate," *IEEE J. Solid-State Circuits*, vol. 50, no. 10, pp. 2353–2366, Oct. 2015.
[16] K. H. Mak et al., "A 0.7 V 24 μA hybrid OTA driving 15 nF capacitive load with 1.46 MHz GBW," *IEEE J. Solid-State Circuits*, vol. 50, no. 11, pp. 2750–2757, Nov. 2015.
[17] S.-W. Hong and G.-H. Cho, "A pseudo single-stage amplifier with an adaptively varied medium impedance node for ultra-high slew rate and wide-range capacitive-load drivability," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 63, no. 10, pp. 1567–1578, Oct. 2016.
[18] Z. Yan, P.-I. Mak, and R. Martins, "Two stage operational amplifiers: Power and area efficient frequency compensation for driving a wide range of capacitive load," *IEEE Circuits Syst. Mag.*, vol. 11, no. 1, pp. 26–42, Jan./Mar. 2011.
[19] Z. Yan, P. Mak, and R. P. Martins, "A 0.0045-mm^2 32.4-μW two-stage amplifier for pF-to-nF load using CM frequency compensation," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 62, no. 3, pp. 246–250, Mar. 2015.
[20] M. Ho et al., "A two-stage large-capacitive-load amplifier with multiple cross-coupled small-gain stages," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 24, no. 7, pp. 2580–2592, Jul. 2016.
[21] M. A. Mohammed and G. W. Roberts, "Conventional CMOS OTAs driving nF-range capacitive loads," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, May 2021, pp. 1–5.
[22] S. Guo and H. Lee, "Dual active-capacitive-feedback compensation for low-power large-capacitive-load three-stage amplifiers," *IEEE J. Solid-State Circuits*, vol. 46, no. 2, pp. 452–464, Feb. 2011.
[23] Z. Yan, P. I. Mak, M. K. Law, and R. P. Martins, "A 0.016-mm^2 144-μW three-stage amplifier capable of driving 1-to-15 nF capacitive load with >0.95-MHz GBW," *IEEE J. Solid-State Circuits*, vol. 48, no. 2, pp. 527–540, Feb. 2013.
[24] D. Marano, A. D. Grasso, G. Palumbo, and S. Pennisi, "Optimized active single-Miller capacitor compensation with inner half-feedforward stage for very high-load three-stage OTAs," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 63, no. 9, pp. 1349–1359, Sep. 2016.
[25] A. D. Grasso, D. Marano, G. Palumbo, and S. Pennisi, "High-performance three-stage single-miller CMOS OTA with no upper limit of CL," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 65, no. 11, pp. 1529–1533, Nov. 2018.
[26] K. H. Mak et al., "A 0.7 V 24 μA hybrid OTA driving 15 nF capacitive load with 1.46 MHz GBW," *IEEE J. Solid-State Circuits*, vol. 50, no. 11, pp. 2750–2757, Nov. 2015.
[27] J. Riad, J. J. Estrada-Lopez, I. Padilla-Cantoya, and E. Sanchez-Sinencio, "Power-scaling output-compensated three-stage OTAs for wide load range applications," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 67, no. 7, pp. 2180–2192, Jul. 2020.
[28] M. Tan and W.-H. Ki, "A cascode Miller-compensated three-stage amplifier with local impedance attenuation for optimized complex-pole control," *IEEE J. Solid-State Circuits*, vol. 50, no. 2, pp. 440–449, Feb. 2015.
[29] W. Qu, S. Singh, Y. Lee, Y. S. Son, and G. H. Cho, "Design-oriented analysis for Miller compensation and its application to multistage amplifier design," *IEEE J. Solid-State Circuits*, vol. 52, no. 2, pp. 517–527, Feb. 2017.
[30] X. Peng, W. Sansen, L. Hou, J. Wang, and W. Wu, "Impedance adapting compensation for low-power multistage amplifiers," *IEEE J. Solid-State Circuits*, vol. 46, no. 2, pp. 445–451, Feb. 2011.
[31] S. Pourashraf, J. Ramirez-Angulo, A. J. Lopez-Martin, and R. González-Carvajal, "A highly efficient composite class-AB-AB Miller op-amp with high gain and stable from 15 pF up to very large capacitive loads," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 26, no. 10, pp. 2061–2072, Oct. 2018.
[32] M. Mojarad and M. Yavari, "A low-power four-stage amplifier for driving large capacitive loads," *Int. J. Circuit Theory Appl.*, vol. 42, no. 9, pp. 978–988, Sep. 2014.
[33] S. A. Fordjour, J. Riad, and E. Sanchez-Sinencio, "A 175.2-mW 4-stage OTA with wide load range (400 pF–12 nF) using active parallel compensation," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 28, no. 7, pp. 1621–1629, Jul. 2020.
[34] M. A. Mohammed and G. W. Roberts, "Investigating the developments on the frequency compensation techniques of the two-stage OTAs—A brief guide and updated review," in *Proc. 31st Int. Conf. Microelectron. (ICM)*, Dec. 2019, pp. 219–222.
[35] B. Y. Kamath, R. G. Meyer, and P. R. Gray, "Relationship between frequency response and settling time of operational amplifiers," *IEEE J. Solid-State Circuits*, vol. SC-9, no. 6, pp. 347–352, Dec. 1974.
[36] A. Sedra and K. Smith, *Microelectronic Circuits*, 7th ed. New York, NY, USA: Oxford Univ. Press, 2015, pp. 996–1006.
[37] D. A. Johns and K. Martin, *Analog Integrated Circuit Design*. Hoboken, NJ, USA: Wiley, 1997, p. 290.
[38] R. J. Reay and G. T. A. Kovacs, "An unconditionally stable two-stage CMOS amplifier," *IEEE J. Solid-State Circuits*, vol. 30, no. 5, pp. 591–594, May 1995.
[39] J. Stevens, "Simplifying stability checks," Texas Instrum., Dallas, TX, USA, Tech. Rep. SLVA381B, Nov. 2013, p. 3.

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