A High Step-Up Cost Effective DC-to-DC Topology Based on Three-Winding Coupled-Inductor

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***Abstract*—Owing to the low voltage level that renewable energy sources like solar panels frequently provide, and limited capability of simple boost converter, need for high gain step-up dc-to-dc converters are increased. In this article a single switch high step-up dc-to-dc topology with high efficiency is developed. To obtain high voltage gain, the described step-up dc-to-dc topology employs three windings coupled inductor and voltage multiplier cell method. To get the high voltage gain, this innovative converter does not require to work at a high duty cycle state by increasing the turns ratio of the coupled inductor. The suggested converter's working modes and theoretical model are investigated, and finally, a prototype setup is used to verify the theoretical and simulation analyses' correctness.**

***Index Terms*—Coupled-inductor, dc-to-dc converter, high gain converter.**

I. Introduction

PHOTOVOLTAIC (PV) based renewable energy generation share is quickly growing, with an annual growth rate of approximately 55 GW predicted in 2018 [1]. In the creation of microgrids, and optimal utilization of electricity supplied by series linked PV modules, need for a voltage boost of up to 320–400 V for the dc microgrid level interfaces is crucial [2]. As stated in [3] and [4], this degree of voltage boost is accomplished by connecting boost converters in a cascading configuration. For low duty ratio operating of main switches, two cascade-connected topologies produce quadratic boost with such a gain restriction. Numerous switching devices can also add to the complexity of the converter's design and control. Chen et al. [5] proposed a single-MOSFET quadratic boost converter with two-stage amplifying capabilities to decrease the number of transistors. Likewise, Habibi et al. [6] proposed a quadratic boost topology with a single resonant network and soft-switching capabilities. Divya Navamani et al. [7] described a thorough examination of a large converting range converter, including gain factor changes due to duty ratios operating and switching network combinations. Hu et al. [8] described a thorough design of a cascaded dc–dc topology for PV applications, including efficiency optimization. Abbasian et al. [9] presented a single-switch high-gain dc–dc converter based on a voltage multiplier cell (VMC) with the additional benefit of low voltage stresses on components. A series of high-gain boost converters that employ a clamped mode coupled inductor (CI) for high gain and efficiencies is introduced in [10].

Switched capacitor-based boost topologies are another versatile class of high gain dc-to-dc converters [11], [12]. This method can increase voltage gain at a moderate duty cycle without employing magnetic elements. The downsides of this approach include inrush current at startup and capacitor susceptibility to equivalent series resistance (ESR). A new topology with switched capacitor circuits is presented in [11] to raise the voltage level up to 10 times based on the conventional configuration.

Compared to the typical boost converter, switched inductor-based boost converters are also another effective approach for achieving high voltage gain [13]. The minimal input current rippling is one of the benefits of this class of converters. Furthermore, Zhang et al. [26], Hasanpour et al. [27], and Farsijani et al. [28] introduced different kinds of single-MOSFET step-up topologies with regeneration passive clamp circuit. The primary power MOSFET in such converters is operated under ZCS conditions and low voltage stress. Furthermore, the CI's leakage inductor aids in the resolution of the diode's reverse recovery issue. But, the topologies stated cannot provide a broad range of voltage gain are expensive due to the huge number of components used.

Under ZCS conditions, the power switches in [24] and [25] turn ON. In addition, the reverse recovery issue with power diodes has been solved. To produce high voltage-gain, these designs use a mix of CI and VMCs. But such converters have an excessive number of components, as well as a significant cost and complexity. Furthermore, the leakage inductances of the CIs and high-frequency transformers create spike turn-OFF losses in such configurations. The power MOSFETs in [29] are soft-switched ON and the diodes are operated with zero currents, that avoids the reverse recovery concerns. The amount of power MOSFETs and voltage stresses across the voltage multiplier capacitors were noted to be excessive in [28].

A new development for a cost effective nonisolated high step-up dc-to-dc topology based on the voltage multiplier cell

Manuscript received 29 March 2022; revised 4 July 2022, 27 September 2022, and 14 October 2022; accepted 14 October 2022. Date of publication 25 October 2022; date of current version 28 December 2022. *(Corresponding author: Hossein Hafezi.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/JESTIE.2022.3217017.

Digital Object Identifier 10.1109/JESTIE.2022.3217017

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method and CI is given in this article. The main advantages of this converter are as follows.

1) The power MOSFET and diodes operate in ZCS condition. So, the reverse recovery of the diodes is resolved.
2) Using the three degrees of freedom, the voltage gain can be adjusted. (N_2, N_3, and D).
3) Low voltage stress on main switch and output diode.
4) Despite the small number of converter parts, the voltage gain of the prototype converter is equal to 10.5 when duty cycle value is around 0.5.
5) Due to the low voltage stress of the power switch, we can use a low price low R_{DS} switch.
6) Considering the number of converter parts and voltage stress on the semiconductors, this converter can be found to be optimal in terms of total price.

This kind of high gain dc–dc converter is essential in several emerging applications such as: Dc microgrid application, LED lightning, automobile headlight, robotics and PV systems.

The high gain dc–dc converters are of interest specially in renewable energy systems (RES) integration since these emerging technologies are crucial to address recent energy crises in EU and worldwide. In this regard, PV systems are one the most extensively utilized RES type. The dc input of a PV cell, modules, strings, or array, varies from sub-1 V to 1500 V, must be converted to an intermediate dc voltage by a dc–dc converter(s) for providing stable dc power for grid integration in a PV system. As a result, the dc–dc conversion plays important role in the overall operation of the PV system, including efficiency and reliability, among other elements.

The rest of this article is organized as follows. Section II evaluates the proposed structure operation concept as well as steady-state analyses in continuous conduction mode (CCM). The suggested converter's design principles and voltage stress of components are provided in Section III. In Section IV, the presented converter is compared to different similar designs. The experimental measurement outcomes of a laboratory prototype of the suggested topology are shown in Section V. Finally, Section VI concludes this article.

II. Converter: Operation Principles

The equivalent power circuit of the described high step-up voltage gain single MOSFET dc-to-dc topology based on CI and VMC with low input current ripple is shown in Fig. 1.

As seen in Fig. 1, an active power switch S, one three-windings CI, three capacitors C_1–C_3, three diodes D_1–D_3, an output filter capacitor C_O, and an output diode D_O are included in the proposed construction. One power switch is a benefit for the converter in the suggested topology's construction. The CI's turns ratio n_2 is equivalent to N_2 /N_1, and n_3 is equivalent to N_3 /N_1, wherein N_1, N_2, and N_3 are the inductor's winding turns. Fig. 2 depicts the various modes of operation. Fig. 3 shows the steady-state waveform of the proposed converter operated in CCM.

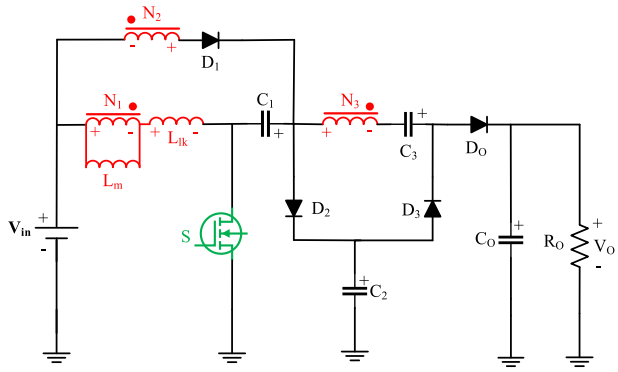

Fig. 1. Configuration of the suggested dc-to-dc boost converter.

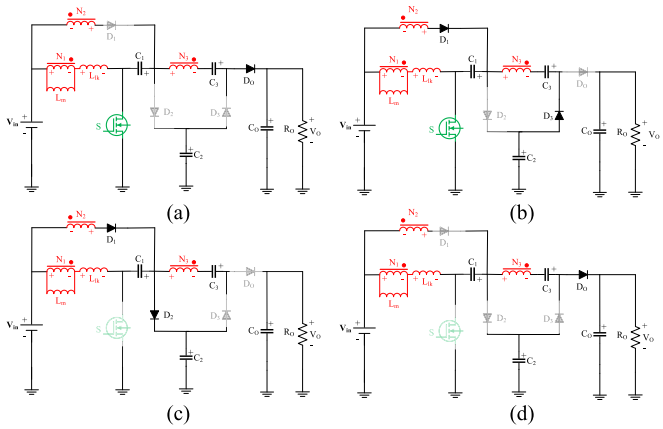

Fig. 2. (a) Current flow path in Mode I. (b) Current flow path in Mode II. (c) Current flow path in Mode III. (d) Current flow path in Mode IV.

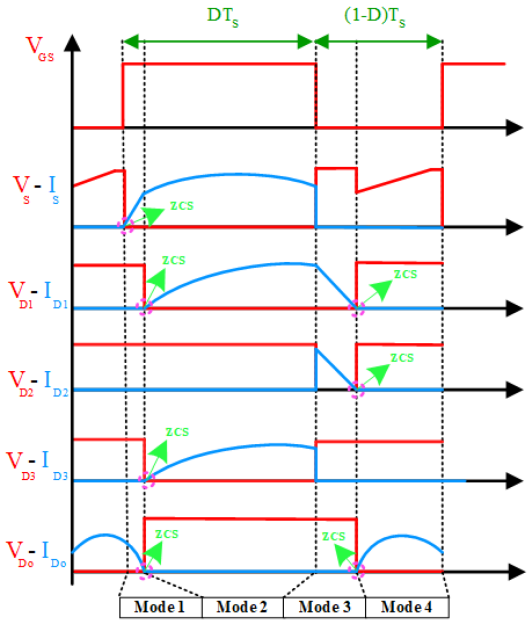

Fig. 3. Characteristic waveform of the suggested topology.

A. Mode 1

At t_0, the active power MOSFETS is turned ON throughout this period. All of diodes stayed on their pervious mode due to the leakage inductance (L_{lk}). In this mode, the active power MOSFET turns ON very softly and has a soft switching operation due to the presence of leakage inductance. Fig. 2(a) depicts the current flow direction. By using Kirchhoff's voltage law in this mode, the following equations can be obtained:

$$V_{Lm}^{D} = \left[\frac{L_m}{L_m + L_k}\right] V_{\text{in}} = kV_{\text{in}} \tag{1}$$

$$V_{Lk}^{D} = \left[\frac{L_k}{L_m + L_k}\right] V_{\text{in}} = (1-k)\, V_{\text{in}}. \tag{2}$$

B. Mode 2

The active power switch S is still turned ON during this time period. The energy of leakage inductance (L_{lk}) is getting empty and D_1 and D_3 are forward biased diodes, whereas D_2 and D_o are reverse biased diodes. Fig. 2(b) depicts the current flow direction of this mode. The magnetizing inductor L_m and the leakage inductor L_{lk} continue to charge from the power supply V_{in}, and the currents through all these inductors increase linearly. In this mode, the capacitor C_3 is charging and reaching its final voltage. In this mode, because the D_1 and the second winding are placed in series, the diode turns ON softly. By using Kirchhoff's voltage law in this mode, the voltage of capacitors C_1, C_3 and voltage of secondary and tertiary windings can be obtained

$$V_{C1} = V_{\text{in}} + V_{N2}^{D} \tag{3}$$

$$V_{C3} = V_{C2} - V_{C1} + V_{N3}^{D} \tag{4}$$

$$V_{N2}^{D} = n_2 V_{Lm}^{D} \tag{5}$$

$$V_{N3}^{D} = n_3 V_{Lm}^{D}. \tag{6}$$

C. Mode 3

This time interval starts at t_2 when the MOSFET is turned OFF. The stored energy in CI's charges capacitor C_2 via diode D_2. This mode ends when diode D_2 is reverse biased. By using Kirchhoff's voltage law in this interval, the voltage of magnetizing inductance and voltage of secondary and tertiary windings can be obtained

$$V_{Lm}^{D'} = k(V_{\text{in}} + V_{C1} - V_{C2}) \tag{7}$$

$$V_{N2}^{D'} = n_2 V_{Lm}^{D'} \tag{8}$$

$$V_{N3}^{D'} = n_3 V_{Lm}^{D'}. \tag{9}$$

D. Mode 4

The active power switch S is still turned off during this time interval. All diodes are reverse biased, whereas D_o is forward biased diode. when the MOSFET is OFF, all parts of capacitors C_1, C_3 and first, tertiary windings are placed in series together, increasing the output voltage gain. The voltage of output capacitor C_O can be calculated as follows:

$$V_O = V_{in} - kV_{Lm}^{D'} + V_{C1} - V_{N3}^{D'} + V_{C3} \approx V_{C2} - V_{N3}^{D'} + V_{C3}. \tag{10}$$

III. Steady-State Analysis of the Present Topology

A. Voltage Gain Calculation

By substituting (1) in (5) and (6) these equations are obtained

$$V_{N2}^{D} = n_2 k V_{\text{in}} \tag{11}$$

$$V_{N3}^{D} = n_3 k V_{\text{in}}. \tag{12}$$

By substituting (11) into (3) V_{C1} can be obtained

$$V_{C1} = (1 + kn_2)\, V_{\text{in}}. \tag{13}$$

By utilizing the volt-second equilibrium axiom for magnetic inductor (L_m) ((1) and (7)) and by according to (13) V_{C2} is found as

$$V_{C2} = \left(1 + \frac{1}{D'} + kn_2\right) V_{\text{in}}. \tag{14}$$

By substituting (12), (13), and (14) into (4) V_{C3} is obtained

$$V_{C3} = \left(\frac{1}{D'} + kn_3\right) V_{\text{in}}. \tag{15}$$

According to (13) and (14) in (7) $V_{Lm}^{D'}$ can be calculated

$$V_{Lm}^{D'} = -k\frac{D}{D'} V_{\text{in}}. \tag{16}$$

By substituting (1) in (8) and (9) these equations are obtained

$$V_{N2}^{D'} = -kn_2 \frac{D}{D'} V_{\text{in}} \tag{17}$$

$$V_{N3}^{D'} = -kn_3 \frac{D}{D'} V_{\text{in}}. \tag{18}$$

By substituting (14), (15), and (18) into (10) the nominal gain of suggested topology can be found

$$\frac{V_O}{V_{\text{in}}} = \left(\frac{2 + D'}{D'}\right) + k\left(n_2 + \frac{n_3}{D'}\right). \tag{19}$$

As just a result, if the CI leakage inductance is ignored, the coupling parameter k is close to unity and the recommended converter ideal voltage gain is as follows:

$$M = \frac{V_O}{V_{\text{in}}} = \frac{(1 + n_2)\, D' + 2 + n_3}{D'}. \tag{20}$$

Fig. 4 depicts a curve of voltage gain M vs turns ratio and duty ratio D. This demonstrates that the turns ratio has a considerable effect on step-up voltage gain. Furthermore, the high voltage gain would be obtained in the suggested topology without the use of an excessive duty ratio or a large turns ratio. It should be noted that in this image, some parameters have been omitted due to their small size and effects, such as winding resistance. The voltage drop due to the coupled-inductor in this topology is extremely low due to the resistance and current flowing through it. By considering these parameters in practice, the voltage gain will be slightly reduced, an example of which will be shown in Section V (see Fig. 13).

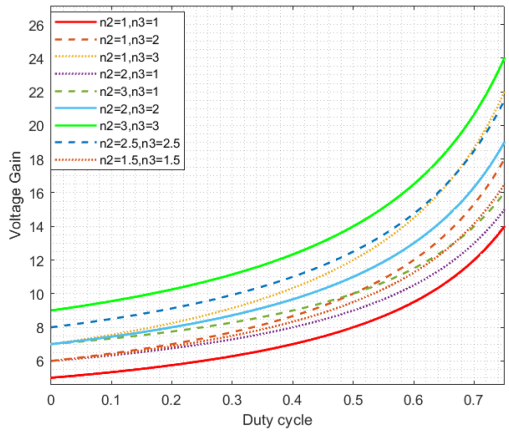

Fig. 4. Ideal voltage gain versus duty ratio for different turn ratio.

B. Voltage Stress of Semiconductors

The voltage stress of the power MOSFET and diodes for the recommended 3Windings CI design must be evaluated in order to make the appropriate selection. The voltage stress on diode D_2 is equal to the power MOSFETs, and the voltage stress on diode D_O is equal to diode D_1. A 3Windings CI converter's voltage stresses are computed, as shown in (21)–(23). By using (13), (14) the voltage stress on the MOSFET and diode D_2 can be obtained

$$V_S = V_{D2} = \frac{V_{\text{in}}}{D'} = \frac{V_o}{(1+n_2)\,D' + 2 + n_3}. \tag{21}$$

By using (20), (14) the voltage stress on the diodes D_3, D_O and by using (14), (16), (17) the voltage stress on the diode D_1 can be obtained

$$V_{D1} = \left(\frac{D}{D'} + 1\right)(1+n_2)\,V_{\text{in}} \tag{22}$$

$$V_{D3} = V_{DO} = (1+n_3)\,\frac{V_{\text{in}}}{D'} = \frac{(1+n_3)\,V_o}{(1+n_2)\,D' + 2 + n_3}. \tag{23}$$

It is observed that (21)–(23) are dependent on the turn ratios of CI. Therefore, we can choose the parts cheaper with lower voltage stress based on the turn ratios of the CI.

C. Current Stress of the Components

The incredibly small-time intervals are disregarded to ease the process. As the magnetizing inductor L_M is sufficiently large, the magnetizing current is considered as a fixed. So, by using the Kirchhoff's current law, the following equations can be obtained:

$$I_{in} \approx I_{in(avg)} = G_m I_O \tag{24}$$

$$I_S = \left(G_m + \frac{3}{D}\right) I_O \tag{26}$$

$$I_{D1} = I_{D3} = \frac{2I_O}{D} \tag{27}$$

$$I_{D2} = \left(G_m + \frac{1}{D}\right) I_O \tag{28}$$

$$I_{DO} = \frac{I_O}{D'}. \tag{29}$$

D. Efficiency Estimation

To correctly judge the converter's effectiveness, it is preferable to study the converter losses by computing the converter efficiency around its nominal power (at 200 W). In general, the converter losses can be divided into four groups.

1) Switch Losses: Switch losses are classified as switching losses and ohmic losses. Because the converter switches softly when the switch is turned ON, its switching losses only comprise losses when the MOSFET is switched OFF. The following equation is required to compute ohmic losses and switching losses:

$$P_{\text{loss(turn OFF)}s} = \left(\frac{1}{2} * V_{DS} * I_{DS} * t_{\text{turn-OFF fall time}}\right) * f_s \tag{30}$$

$$P_{\text{loss(conduction)}} = R_{DS(\text{ON})} \times I^2_{DS(\text{rms})} \tag{31}$$

$$P_{\text{loss(MOSFET)}} = P_{\text{loss(turn OFF)}} + P_{\text{loss(conduction switch)}}. \tag{32}$$

2) Diode Losses: For the scenario of diodes, the ohmic losses and reverse recovery losses of the diodes are ignored in this topology due to use Schottky diodes, and the major losses of the diodes are due to the voltage drops of the diodes in their average currents. As a result, the relevant equation can also be assumed

$$\begin{aligned} P_{\text{loss(diodes)}} &= V_{\text{forward diode}} \times I_{D(\text{average})} + r_D \times I^2_{D(\text{rms})} \\ &= V_{fD1} \times I_{D1} + V_{fD2} \times I_{D2} + V_{fD3} \\ &\quad \times I_{D3} + V_{fDO} \times I_{DO}. \end{aligned} \tag{33}$$

Due to small amount of r_D, it is not considered.

3) Capacitor Ohmic Loss: In order to obtain the internal resistance loss of capacitors, the following equation can be considered:

$$P_{\text{loss(capacitor)}} = \text{ESR} \times I^2_{Co(\text{rms})}. \tag{34}$$

The rest of capacitors have a small ESR due to their material (MKT).

4) Coupled Inductor Losses: The core loss of the CI ($P_{\text{loss(core)}}$) can be calculated using the datasheet parameters. Moreover, the CI's other loss can be obtained as follows:

$$P_{\text{loss(ohmic)}} = \left(I_{L_k(\text{rms})}\right)^2 R_L \tag{35}$$

$$P_{\text{total}_{\text{core}}} = P_{\text{loss}_{(\text{core})}} + P_{\text{loss(ohmic)}}. \tag{36}$$

The efficiency of topology can be derived using the equation of losses from past parts as follows:

$$\eta = \frac{P_O}{P_O + P_{\text{loss}}} \tag{37}$$

Under full load, the converter's efficiency can theoretically reach 97.44%.

E. Design Considerations

1) Capacitors Design: The following equations are used to calculate the size of capacitors by assuming 4% voltage ripple for C_1, C_2 , C_3, and 0.1% voltage ripple for C_O assumed capacitors average current equal to I_O

$$C_1 = \frac{P_O}{V_O \Delta V_{C1} f_s} \tag{38}$$

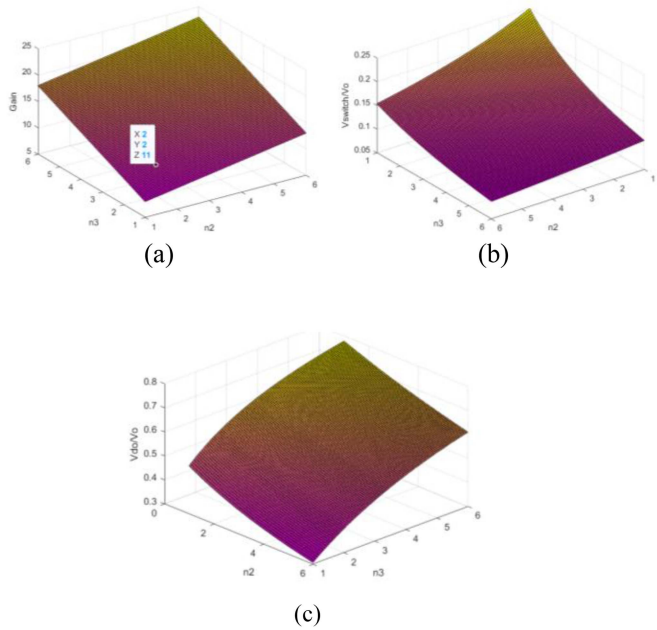

Fig. 5. (a) V_O/V_{in}. (b) V_{SW}/V_O. (c) V_{dout}/V_O when duty cycle is 0.5.

$$C_2 = \frac{P_O}{V_O \Delta V_{C2} f_s} \tag{39}$$

$$C_3 = \frac{P_O}{V_O \Delta V_{C3} f_s} \tag{40}$$

$$C_O = \frac{P_O}{V_O \Delta V_{CO} f_s}. \tag{41}$$

The peak-to-peak ripple of the output capacitor (and other capacitors in the converter circuit) is suggested to be kept under 5% [27]. In this article, we have tried to design the converter by compromising the performance and cost factors.

2) Coupled Inductor Magnetizing Inductance Design (L_m): By assuming 50% current ripple, the amount of the magnetic inductance is obtained from the following equation:

$$L_m = \frac{V_{in} D}{\Delta I_{Lm} f_s} \rightarrow L_{m1} > \frac{V_{in} D}{0.5(n_2 + n_3) I_O f_s}. \tag{42}$$

Voltage gain, normalized voltage stress of the main MOSFET and output diode are showed in Fig. 5(a)–(c), respectively.

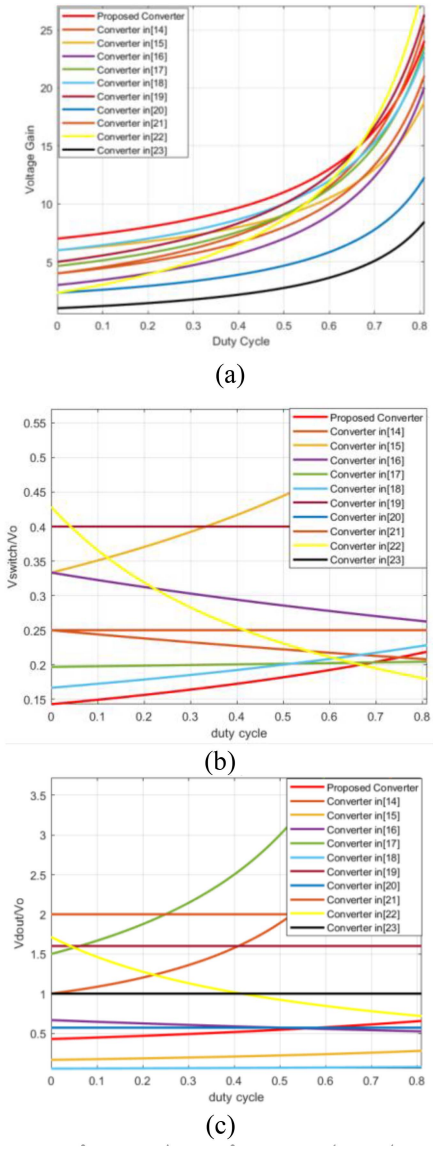

Fig. 6. Outcomes of comparison of suggested topology with certain related boost topologies. (a) Voltage gain of various topologies for various duty cycles. (b) Normalized voltage stress of master switch against duty cycle in some topologies [14], [15], [16], [17], [18], [19], [20], [21], [22], [23]. (c) Normalized voltage stress of output diode against duty cycle in some topologies [14], [15], [16], [17], [18], [19], [20], [21], [22], [23].

IV. Comparison

A. General Comparison

Several comparisons are explored in this part to clarify the advantages of the provided topology. In the first comparison, our goal is the voltage gain of similar topologies and it is much more important than the output voltage. Table I summarizes characteristics of the recommended topology and comparable designs reported in [14], [15], [16], [17], [18], [19], [20], [21], [22], and [23]. For different duty cycles (with $n_2 = 2$ and $n_3 = 2$ for 3-windings and n = 4 for 2 windings CI based converters), Fig. 6(a) displays voltage gain comparison outcomes of recommended topology and topologies described in [14], [15], [16], [17], [18], [19], [20], [21], [22], and [23]. According to this graph, the voltage gain of the suggested design is better than the others except [19], [22] throughout all duty cycle ranges. Also, the voltage gain of proposed topology is better than [19], [22] for all duty cycle amounts less than 0.67. This benefit is owing to the proposed configuration's incorporation of a CI with voltage multiplier cell. As shown in Fig. 6(b), the normalized voltage stress across the MOSFET in the given topology is smaller than in the other configurations for most values of duty amount. As shown in Fig. 6(c), the normalized voltage stress over the output diode in the suggested topology is smaller than configurations [14], [16], [17], [19], [20], [21], [22], [23]. Thus, in the proposed topology, a power MOSFET with low $R_{DS(ON)}$ resistance may be employed to save costs while improving the total efficiency.

TABLE I
DETAILED COMPARISON OF THE SUGGESTED CONVERTER WITH VARIOUS CIS TOPOLOGIES

Converters	S/D/C/CI+L	Component Count	Common Ground	Nominal power Input & Output Voltage	Voltage Gain	Voltage Stress of main switch	Voltage Stress of output diode
[23]	4/1/4/1[2w]+1	11	✓	100 W 48 to 120 V	$\frac{3D+n}{n(1-D)}$	Vo	Vo
[22]	2/2/4/2[2w]+0	10	✓	200 W 28 V to 440 V	$\frac{(2n-1)+nD(n-1)}{(1-D)(n-1)}$	$\frac{(n-1)V_o}{(2n-1)+nD(n-1)}$	$\frac{n(n-1)V_o}{(2n-1)+nD(n-1)}$
[21]	2/2/4/1[2w]+1	10	✓	300 W 48 V to 400 V	$\frac{n}{1-D}$	$\frac{1}{n}Vo$	$2Vo$
[20]	4/0/3/1[2w]0	8	✓	200 W 25 V to 200 V	$\frac{2n-1}{(n-1)(1-D)}$	2Vo	$\frac{nV_o}{2n-1}$
[19]	2/2/5/1[2w]+0	10	✓	250 W 42 V to 400 V	$\frac{n+1}{1-D}$	$\frac{2V_o}{n+1}$	$\frac{(2n)V_o}{n+1}$
[18]	1/3/3/1[3w]+0	8	✓	225 W 29 V to 300 V	$1+\frac{\frac{n_1+n_2}{n_1}}{1-D}+\frac{n_3}{n_1}$	$Vo/((((n_1+n_2)/n_1+1)/(D-1)-n_3/n_1)*(D-1))$	$Vo*(\frac{n_1}{(n_1+n_2)*\left(\frac{\frac{n_1+n_2}{n_1}+1}{D-1}-\frac{n_3}{n_1}\right)*(D-1)})$
[17]	1/3/3/1[3w]+1	9	✓	500 W 50 V to 400 V	$\frac{2+n_2-n_3(1+D)}{(1-D)(1-n_3)}$	- Vo *((n3 + (n2 - n3*(d + 1) + 2)/(d - 1))*(d - 1)*(n3 - 1))/((n2 + 2)*(n2 - n3*(d + 1) + 2))	$\frac{1+n_2}{2+n_2-n_3(1+D)}Vo$
[16]	2/4/4/1[3w]+0	11	×	500 W 50 V to 400 V	$\frac{1+n_3+D}{1-D}$	$\frac{1}{1+n_3+D}Vo$	$\frac{n_3}{n_3+1+D}Vo$
[15]	1/4/4/1[3w]+0	10	✓	2000 W (60–90) V to 400 V	$n_3+\frac{2-D+n_2}{1-D}$	$\frac{n_3}{2-D+n_2(1-D)+n_3}Vo$	$\frac{1}{2-D+n_2(1-D)+n_3}Vo$
[14]	1/3/3/1[3w]+0	8	✓	200 W 20 V to 300 V	$\frac{n_2+n_3+D(n_3-1)}{(1-D)(n_3-1)}$	$\frac{n_3-1}{n_2+n_3+D(n_3-1)}Vo$	$\frac{(n_3-1)(1-D)-1}{n_2+n_3+D(n_3-1)}Vo+\frac{n_2+n_3+D(n_3-1)}{(1-D)}{n_2+n_3+D(n_3-1)}Vo$
Proposed Converter	1/4/4/1[3w]+0	10	✓	200 W 20 V to 210 V	$\frac{(1+n_2)D'+2+n_3}{D'}$	$\frac{V_o}{(1+n_2)D'+2+n_3}$	$\frac{(1+n_3)V_o}{(1+n_2)D'+2+n_3}$

S: Switches, D: Diodes, C: Capacitors, CI: Coupled-inductor, L: Inductor

The suggested converter, according to this part, have a high voltage ratio with reduced voltage stress on the MOSFET, making it suitable for renewable energy purposes.

B. Comparison With Two-Windings Converters

In this section, in order to compare the proposed converter with two-windings converters, three comparisons have been made. In these comparisons, it is assumed that the proposed converter has a ratio of (1:0:2, $n_2 \approx 0$ (The windings of secondary is very, very low, and negligible), $n_3 = 2$), and the turns ratio of the two windings converters is 1:2. Fig. 7(a) displays voltage gain comparison outcomes of recommended topology and topologies described in [19], [20], [21], [22], and [23]. The voltage gain of suggested converter is high and appropriate especially in lower duty cycle values. As shown in Fig. 7(b), the normalized voltage stress across the MOSFET in the given topology is smaller than in the other two windings topologies for most values of duty amount. As shown in Fig. 7(c), the normalized voltage stress over the output diode in the suggested topology is smaller than configurations [23], [19], [20], [21].

V. EXPERIMENTAL RESULTS

The laboratory prototype has been designed and implemented in order to verify the performance and practicality of the dc–dc converter combination that have been discussed in this article. Fig. 8(a) shows a picture of the experimental setup and the power circuit that was constructed and Table II shows the details of its components. In all experimental results, the output power of the converter is 200 W, and the LA200-P current sensor is used to measure the current.

TABLE II
SYSTEM PARAMETERS OF THE SUGGESTED TOPOLOGY

Parameters	Description/ Value
Switch S	HY3912 MOSFET 6.3 mΩ on-resistance
Diodes D_1, D_2, D_3, D_O	1zMBR20200C schottky diode, V_F=0.6 V
Magnetic coupled Inductor CI	Turns ratio: 2 (N_1:N_2=20:40) 2 (N_1:N_3=20:40) Core: PC47ETD44-Z ferrite core Magnetizing inductance: 130μH With PSTPST winding Leakage inductance: 1μH
Capacitors **C_1, C_2** **C_3** **C_O**	 10 μF, 100 V (MKT) 10 μF, 250 V (MKT) 68 μF, 400 V
Switching Frequency	50 kHz
Output Power	200 W
Input Voltage	20 V
Nominal output Voltage	210 V
Nominal Gain	10.5

Experimental waveforms of the elements illustrated in Fig. 9. The gate pulse with 50% duty cycle is depicted in Fig. 9(a). Fig. 9(b) shows the voltage and current waveforms of the main

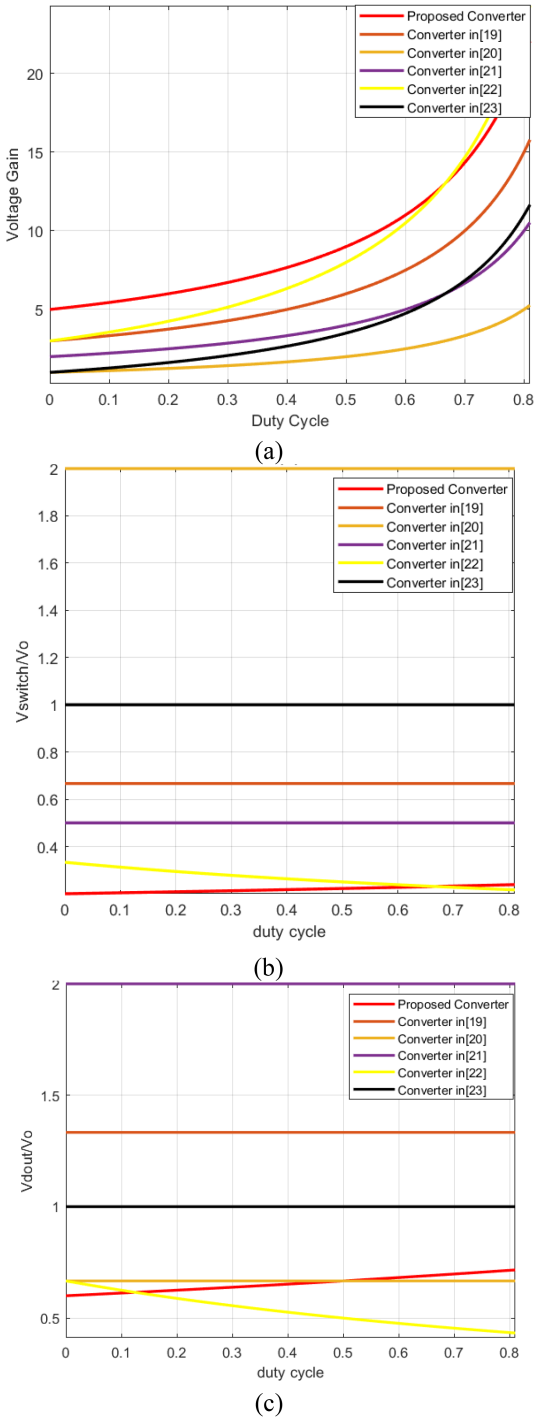

Fig. 7. Comparison of suggested converter when the windings of secondary is very low and negligible with other two winding converters. (a) Voltage gain comparison. (b) Normalized voltage stress of master switch comparison. (c) Normalized voltage stress of output diode comparison. (Turns ratio: 1:2).

power MOSFETs. It is important to note that the turning-ON loss of the MOSFET is very low due to its ZCS operation.

The voltage across the power MOSFETs is measured to be 40 V, which confirms (21). The voltage and current waveform of diode D_1 is shown in Fig. 9(c). The voltage across the diode is measured to be 80 V, confirming (22). The voltage and current

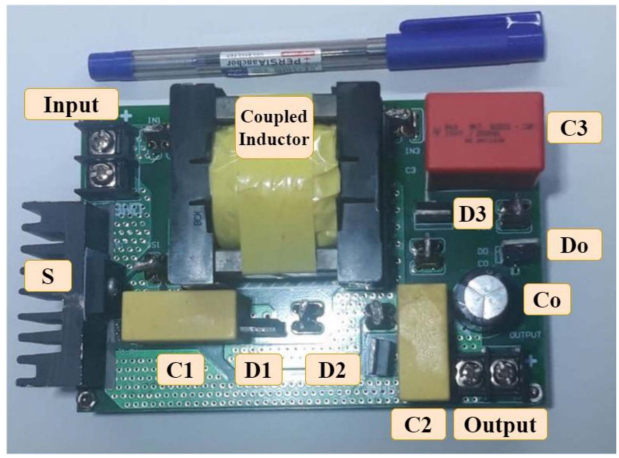

Fig. 8. Experimental setup of suggested converter.

waveforms of diodes D_2, D_3 and output diode D_O are shown in Fig. 9(d)–(f). The voltages throughout the diodes are reported to be 40 V, 100 V, 100 V verifying (21) and (23).

The diodes have a ZCS operation. Fig. 9(g) and (h) indicates the current and voltage from the tertiary side and primary inductance of the CI, accordingly. Fig. 9(i) depicts the experimental waveforms of output load acquired from the prototype suggested topology working at full load.

The distribution of different losses resulting in the proposed high-gain topology under nominal-load conditions is depicted in Fig. 10(a). The efficiency values achieved while calculating and testing with the prototype at different output power range are shown in Fig. 10(b). The calculated results are quite near to the practical ones. It is important to note that the output voltage of these converters is not equal to each other and is equal to its values in Table I.

Furthermore, the purpose of Fig. 10(b) is to show that the proposed converter with the used components (power switches, coupled-inductors, and diodes) has an appropriate efficiency compared to the topologies available in the state of art with their special components. Moreover, by using newest components such as using SiC switches with lower R_{DS}, we may expect better efficiency from the proposed converter which needs to be investigated.

In order to have a more detailed look at the soft switching operation in this converter, the conducting current and breaking voltage on switch S is presented in Fig. 11. It can be seen that the active power MOSFET turns ON very softly due to the presence of leakage inductance (see the Mode 1 of converter operation)

It is important to note that, by using the snubber correctly in the proposed converter, the maximum amplitude voltage on components (switch or diodes) can be reduced. Fig. 12(a) and (b) shows the voltage and current of the switch and the voltage and current of the diode, respectively, after applying the snubber.

To evaluate the correctness of the generated ideal voltage-gain and compare it to actual voltage gain, nominal, and experimental prototype output voltages are shown in Fig. 13.

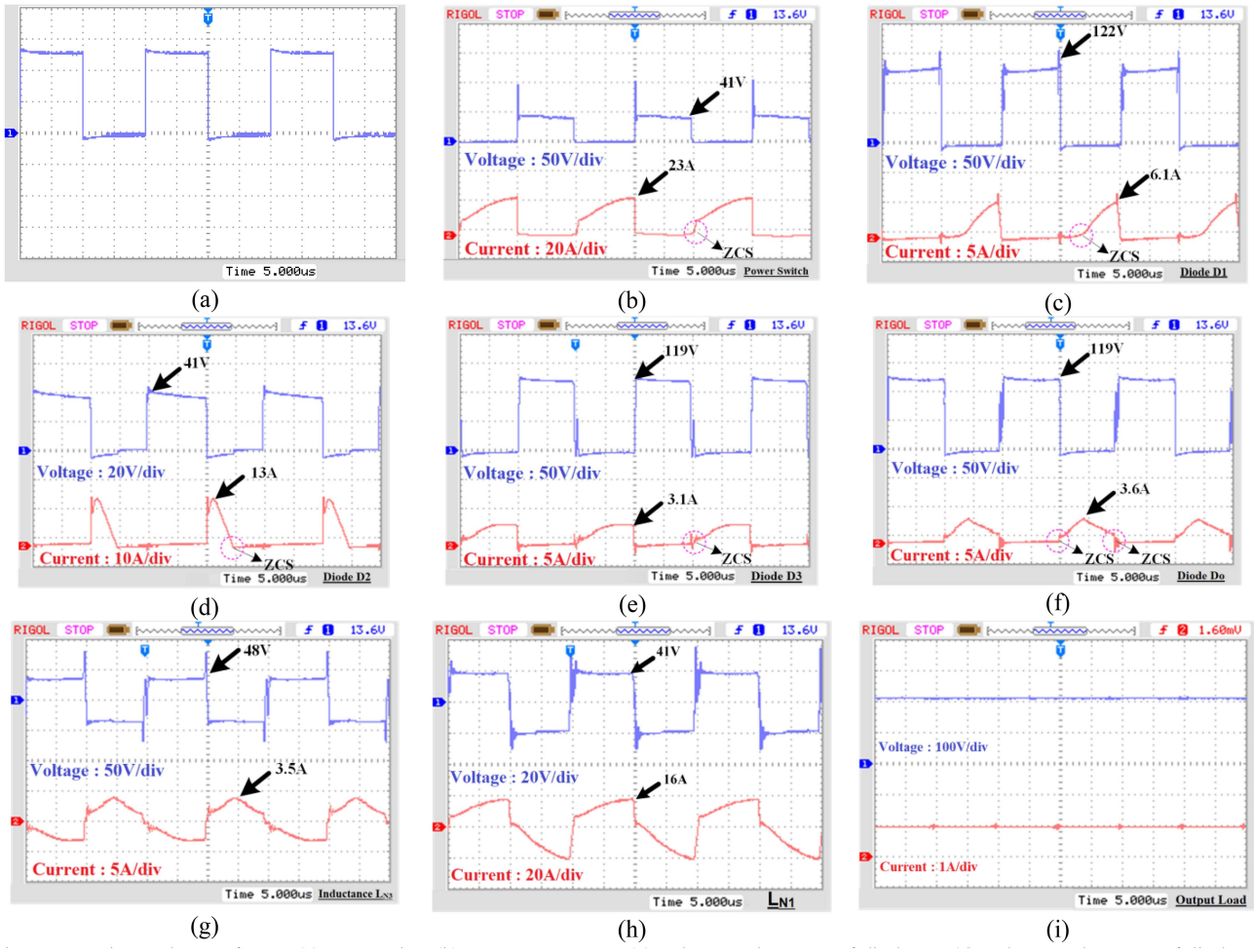

Fig. 9. Experimental waveforms. (a) Gate Pulse. (b) Power MOSFET. (c) Voltage and current of diode D_1. (d) Voltage and current of diode D_2. (e) Voltage and current of diode D_3. (f) Voltage and current of output diode D_o. (g) Voltage and current of L_{N3}. (h) Voltage and current of L_{N1}. (i) Voltage and current of output load.

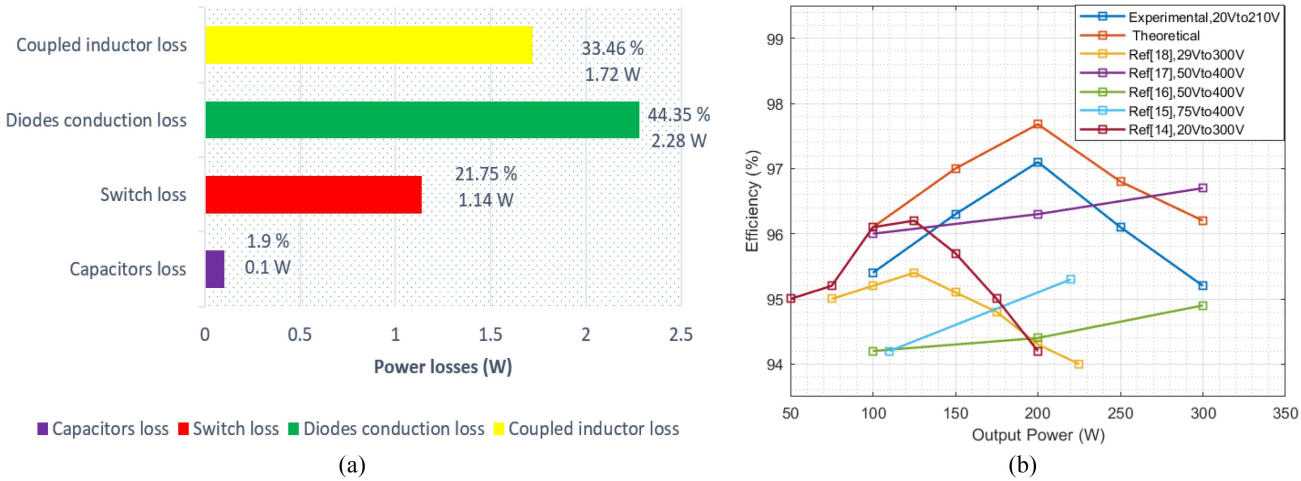

Fig. 10. Distribution of losses in different components under full-load conditions and the efficiency curve. (a) Power loss dissipated in several components of the Suggested topology (at 200W output). (b) Calculated and experimented efficiency curves of suggested converter and topologies in [14], [15], [16], [17], [18]. (Note: This figure is case sensitive and based on the results presented in the referred research papers knowing that the components used in those converters are not the same. Therefore, considering the same components in the practical structure, some curves may be slightly different).

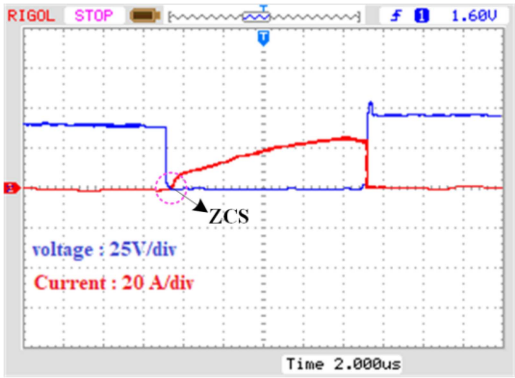

Fig. 11. Conducting current and drain to source voltage on MOSFETs.

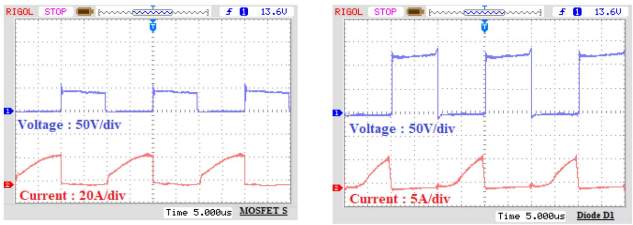

Fig. 12. Experimental results after applying the appropriate snubber. (a) Drain to source voltage and current of MOSFET. (b) Diode D_1.

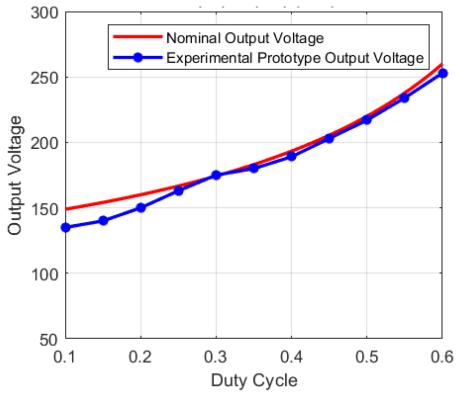

Fig. 13. Nominal and experimental output voltages.

VI. Conclusion

A design based on a CI with three windings for a nonisolated, high gain, single switch dc-to-dc converter was presented in this article. High voltage gain is accomplished in the proposed design by utilizing a 3Windings CI and voltage multiplier cell. By increasing the CI turn ratio, the voltage conversion ratio of the given topology is enhanced. Because the voltage stress on the main MOSFET is minimal, a power MOSFET with a lower ON-state resistance could be chosen. The behavior of the converter and steady-state evaluation in CCM were explicitly explained. As a final demonstration of the converters' abilities to operate, experimental measurement results were provided. It should be noted that the performance of this converter is preferred in CCM and if it needs to be used in discontinuous mode, the voltage gain and some other equations will be different.

The main advantages of the proposed structure over the conventional boost converter are as follows.

1) Soft switching operation for main switch and diodes.
2) Higher voltage gains especially in lower duty cycle values.
3) Greater degree of freedom to design and increase voltage gain (turn ratios n_2, n_3 and duty cycle).
4) Lower normalized voltage stress on the main switch.

This topology can find its application in several emerging technologies such as in Solar Home Systems for rural/urban environments or to supply high intensity discharge lamp used in automobile head lamps or dc microgrid application or traffic lights or other low-cost systems. If the output power has a significant drop (lower than %15 of nominal output power), the soft switching performance of the converter will be compromised and the efficiency will decrease from our desired level.

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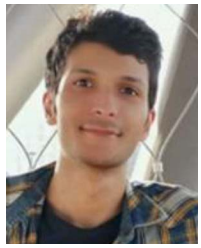

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