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Thévenin Equivalent Circuits for Modeling Common-Mode Behavior in Power Electronic Systems

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ABSTRACT Modeling the common-mode behavior of power electronic systems can be a challenge. This research aims to simplify the process by developing a modeling approach based on Thévenin common-mode equivalent circuits. The Thévenin common-mode equivalent circuits prove to be both straightforward to construct and reliable in predicting worst-case common-mode behavior. In this paper, a theoretical understanding of the Thévenin-based modeling approach is first provided. Subsequently, methods to characterize the Thévenin parameters are established. The modeling approach is then validated experimentally on a dc micro-grid.

INDEX TERMS Electromagnetic interference (EMI), leakage current, common-mode (CM), Thevenin equivalent circuit, micro-grid.

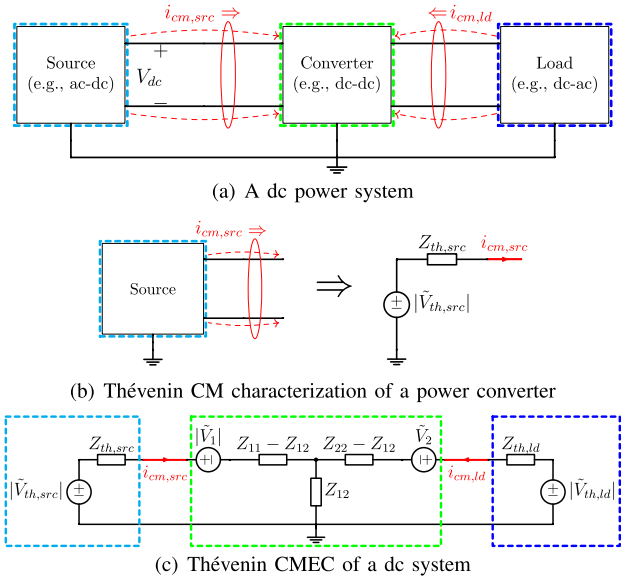
I. INTRODUCTION

WHEN designing power systems that are composed of multiple power electronic (PE) converters, predicting the expected common-mode (CM) current within the interconnected system can be a challenge. A potential approach is to identify dominant parasitic coupling paths and develop detailed common-mode equivalent circuits (DCMECs) to represent the CM behavior of the system. Within these DCMECs, ideal voltage sources are used to model the switching of the transistors (diodes), and linear passive elements are used to model the conductive CM paths. Early references using such an approach to model CM behavior in electric drives include [1]–[4]. Researchers have since applied DCMECs to other types of PE converters (for a recent example, see [5]). A formal method to construct DCMECs and assemble them for system analysis is described in [6]. A challenge in applying the DCMEC approach is that it requires significant knowledge of each converter design to correctly identify parasitic paths. In addition, knowledge of the switching strategy being utilized or measurement of the switch voltage(s) is needed to establish the CM voltage sources.

As an alternative to DCMECs, some researchers have modeled the CM behavior of a converter using a Thévenin equivalent circuit [7]–[11]. A benefit of this approach is that it is possible to characterize the Thévenin CMEC (TCMEC) experimentally, without the need to characterize parasitic paths or switch voltages. To date, TCMECs have been applied to single converter systems. For example, in [9] the approach is applied to a boost converter, in [10] a buck converter, and in [10], [11] a three-phase inverter. The focus of this paper is to outline and demonstrate a procedure for applying the TCMEC modeling approach to PE-based *systems*.

An illustration of the system-level TCMEC modeling approach is shown in Fig. 1. Therein, each component of the dc system shown in Fig. 1(a) is first independently characterized as a TCMEC as shown in Fig. 1(b). From the individual TCMEC models, a system-level TCMEC is constructed as shown in Fig. 1(c). This system-level TCMEC is used to obtain an upper-bound on the expected CM current conducted in each branch of the system.

The remainder of this work is outlined as follows: First, theoretical justification is provided for using Thévenin models to represent the CM behavior of power converters (Section II). Subsequently, a least-squares experimental characterization procedure used to obtain the TCMEC parameters is highlighted (Section III). A means to couple two-or-more

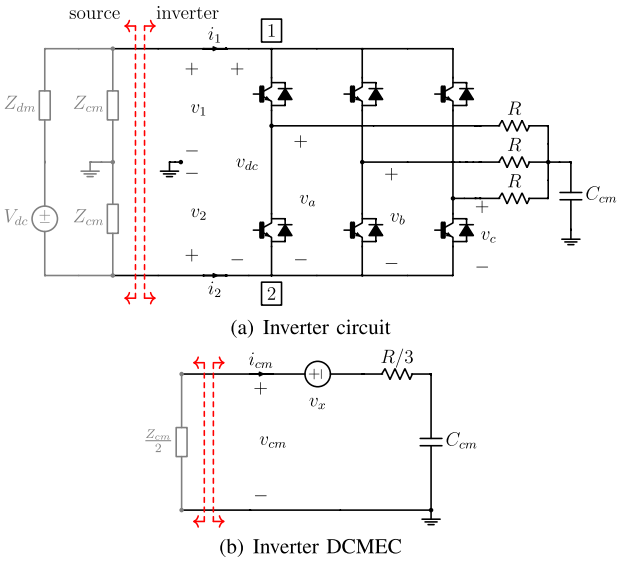


(a) A dc power system

(b) Thévenin CM characterization of a power converter

(c) Thévenin CMEC of a dc system

FIGURE 1. **Common-mode model of a dc system.**



(a) Inverter circuit

(b) Inverter DCMEC

FIGURE 2. **Demonstrative inverter circuit.**

individual TCMEC models together is then established which enables one to predict the worst-case CM current expected in a PE system (Section IV). Finally, the approach is validated experimentally in a dc micro-grid consisting of a generator, dc cable, and an isolated dc-dc converter supplying a 3-phase inverter/load (Section V). The work extends an early version of the research presented in [12]. Important extensions herein include the theoretical justification, details related to the characterization procedure and experimental validation of the proposed approach.

II. Thévenin CMECs

A. BACKGROUND

Before considering how a Thévenin equivalent circuit can model the CM behavior of a power converter, we first provide a brief description of CMECs using the inverter circuit shown in Fig. 2(a) as an example. This circuit shows for simplicity a single parasitic coupling path to ground at the neutral of the load, although more detailed parasitic couplings paths could have been included. Further, it is noted that the inverter shown in Fig. 2(a) is a symmetric converter; i.e., one where the path to ground from node $\boxed{1}$ is symmetric to the path to ground from node $\boxed{2}$. Both the DCMEC and TCMEC approaches are complicated by CM/differential-mode (DM) coupling in asymmetric converters [13]. Thus, in the remainder of this work the authors limit the discussion to the class of symmetric PE converters.

Referring to Fig. 2(a), the CM voltage and current looking into the inverter are defined as:

$$\begin{aligned} v_{cm} &= \frac{v_1 + v_2}{2} \\ i_{cm} &= i_1 + i_2 \end{aligned} \tag{1}$$

The corresponding DM definitions are given in (2).

$$\begin{aligned} v_{dm} &= v_1 - v_2 \\ i_{dm} &= \frac{i_1 - i_2}{2} \end{aligned} \tag{2}$$

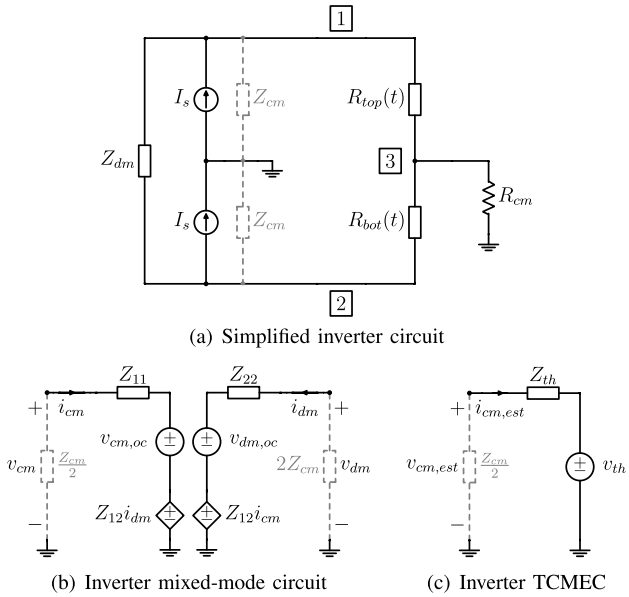
From (1), it is apparent that if no current flows through C_{cm}, then $i_2 = -i_1$ and thus $i_{cm} = 0$. On the other hand, if current flows through C_{cm} (and returns through the Z_{cm}'s), then $i_{cm} \neq 0$. Following the techniques given in [6], a DCMEC of the inverter and its CM load can be constructed as shown in Fig. 2(b). In Fig. 2(b),

$$\begin{aligned} v_x &= \frac{v_{dc}}{2} - \frac{v_a + v_b + v_c}{3} \\ z_x &= \frac{R}{3} + \frac{1}{pC_{cm}} \end{aligned} \tag{3}$$

where $p = d/dt$ is the Heaviside operator.

It is noted that in furnishing an equivalent voltage source, namely v_x, to the DCMEC model of Fig. 2(b), one is modeling the linear time-varying (LTV) circuit of Fig. 2(a) with an equivalent linear time-invariant (LTI) circuit [9], [10], [14], [15], [16]. A PE converter is LTV since the corresponding impedance of the transistors change in time (ideally, from a infinite value when gated off – to a infinitesimal value when gated on). Therefore, a limitation of the DCMEC modeling approach is that the resulting LTI model of the original LTV circuit can only be constructed with *a priori* knowledge of v_{dc}, v_a, v_b and v_c. In other words, the DCMEC of Fig. 2(b) can only be formed after the effect of V_{dc}, Z_{dm} and even Z_{cm} are implicitly incorporated into v_x.

Thus, although the right hand side of Fig. 2(b) is LTI and resembles a Thévenin equivalent circuit, it is indeed not one since v_x can depend on Z_{cm} and a Thévenin equivalent circuit by definition has a voltage source that is independent of its "load." This then motivates the fundamental



(a) Simplified inverter circuit

(b) Inverter mixed-mode circuit

(c) Inverter TCMEC

FIGURE 3. Inverter circuit and Thévenin equivalent.

question addressed in this section: What is the theoretical basis for using LTI Thévenin equivalent circuits to model the CM behavior of LTV power electronic converters? We first address this question analytically in Section II-B to show that: formally, a TCMEC is only applicable if the inverter is sourced by an ideal supply (i.e., one with zero DM impedance). Subsequently, in Section II-C, we demonstrate by numerical example that in some instances the predominate CM behavior of the LTV circuit can be accurately modeled by an LTI TCMEC, even if $Z_{dm} \neq 0$. Section II-C also demonstrates an example in which the CM behavior of a converter cannot be accurately modeled with an LTI TCMEC. Concluding remarks regarding the applicability of LTI TCMECs are made in Section II-D.

B. TCMEC ANALYTICAL DEMONSTRATION

In this section we develop a TCMEC for the inverter from Section II-A. From this case study, we can establish the basic assumptions/limitations that are involved in the TCMEC modeling approach. Fig. 3(a) shows a simplified schematic of Fig. 2(a) in which all time-varying components are lumped into the generic impedances labeled $R_{top}(t)$ and $R_{bot}(t)$. Therein, $I_s = V_{dc}/Z_{dm}$ (Thévenin to Norton conversion) and the parasitic CM capacitor, C_{cm}, has been replaced with a resistor, R_{cm}, so that we can assume all the components of Fig. 3(a) are resistive. We make this assumption for the time being since it simplifies the analysis of the time-varying circuit. In Fig. 3(a), $R_{top}(t)$ takes on values from the set $\{\infty, R, R/2, R/3\}$, depending on if zero, one, two, or three top switches, respectively, are closed at a given instant in time. A similar statement can be made regarding $R_{bot}(t)$ and we assume for simplicity that the top and bottom switches are always gated in a complimentary fashion.

We now develop a Thévenin equivalent circuit for the inverter. The aim of this equivalent circuit is to model the CM behavior of the inverter independent of the CM behavior of the source. Thus, in Fig. 3(a), we first set $Z_{cm} = \infty$. Then, applying nodal analysis, one can form a system of equations

$$\begin{bmatrix} I_s \\ -I_s \\ 0 \end{bmatrix} = \begin{bmatrix} Y_{11} & -1/Z_{dm} & -1/R_{top}(t) \\ * & Y_{22} & -1/R_{bot}(t) \\ * & * & Y_{33} \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ v_3 \end{bmatrix}$$
$$Y_{11} = 1/Z_{dm} + 1/R_{top}(t)$$
$$Y_{22} = 1/Z_{dm} + 1/R_{bot}(t)$$
$$Y_{33} = 1/R_{cm} + 1/R_{top}(t) + 1/R_{bot}(t) \tag{4}$$

or, compactly,

$$\hat{\mathbf{i}}_{src} = \hat{\mathbf{Y}}\hat{\mathbf{v}} \tag{5}$$

where $\hat{\mathbf{Y}}$ is the (symmetric) nodal admittance matrix and v_1, v_2, v_3 correspond to the voltages at the nodes labeled in Fig. 3(a). (The circumflex notation is used to indicate that these are temporary quantities.)

In order to proceed, Kron reduction is used to eliminate node 3, yielding:

$$\hat{\mathbf{i}}_{src,k} = \hat{\mathbf{Y}}_k\hat{\mathbf{v}}_k \tag{6}$$

where subscript k indicates Kron reduced quantities. Solving (6),

$$\hat{\mathbf{v}}_k = \hat{\mathbf{Z}}_k\hat{\mathbf{i}}_{src,k} \tag{7}$$

expresses the vector of node 1 and node 2 open circuit voltages, $\hat{\mathbf{v}}_k$, in terms of the Kron reduced impedance matrix, $\hat{\mathbf{Z}}_k = \hat{\mathbf{Y}}_k^{-1}$. A change of variables is then performed that separates the CM and DM behavior of the circuit [13]. That is,

$$\mathbf{v} = \mathbf{T}_\mathbf{v}\hat{\mathbf{v}}_k$$
$$\begin{bmatrix} v_{cm} \\ v_{dm} \end{bmatrix} = \begin{bmatrix} \frac{1}{2} & \frac{1}{2} \\ 1 & -1 \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \end{bmatrix} \tag{8}$$

and

$$\mathbf{i} = \mathbf{T}_\mathbf{i}\hat{\mathbf{i}}_{src,k}$$
$$\begin{bmatrix} i_{cm} \\ i_{dm} \end{bmatrix} = \begin{bmatrix} 1 & 1 \\ \frac{1}{2} & -\frac{1}{2} \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \end{bmatrix} \tag{9}$$

which implies

$$\mathbf{v} = \mathbf{T}_\mathbf{v}\hat{\mathbf{Z}}_k\mathbf{T}_\mathbf{i}^{-1}\mathbf{i}$$
$$= \mathbf{Z}\mathbf{i} \tag{10}$$

The CM and DM behavior of Fig. 3(a) can now be represented by a two-port equivalent circuit, as shown in Fig. 3(b). Expressions for the corresponding elements of the impedance matrix, $\mathbf{Z}$, are given in (11); expressions for the corresponding

voltage sources are given in (12):

$$Z_{11} = Z_{22} + \frac{R_{top}(t)R_{bot}(t)}{Z_{den}} + R_{cm}$$
$$Z_{22} = \frac{Z_{dm}\left(R_{top}(t) + R_{bot}(t)\right)}{Z_{den}}$$
$$Z_{12} = \frac{Z_{dm}\left(R_{top}(t) - R_{bot}(t)\right)}{Z_{den}} \quad (11)$$

$$\begin{bmatrix} v_{cm,oc} \\ v_{dm,oc} \end{bmatrix} = \begin{bmatrix} \frac{V_{dc}\left(R_{top}(t) - R_{bot}(t)\right)}{Z_{den}} \\ \frac{V_{dc}\left(R_{top}(t) + R_{bot}(t)\right)}{Z_{den}} \end{bmatrix} \quad (12)$$

where $Z_{den} = R_{top}(t) + R_{bot}(t) + Z_{dm}$.

It is noted that while Fig. 3(b) models the CM and DM behavior of the inverter independent of the CM behavior of the source, this two-port network is clearly not independent of the DM behavior of the source since the parameters given in (11) and (12) are functions of V_{dc} and Z_{dm}. Further, it is noted that (11) is a function of time, which implies Fig. 3(b) is not an LTI circuit.

We now show the following: first, as $Z_{dm} \to 0$, the CM and DM behavior of Fig. 3(b) become uncoupled; second, as $Z_{dm} \to 0$, the CM behavior of Fig. 3(b) becomes time invariant. This implies that as $Z_{dm} \to 0$, Fig. 3(b) reduces to Fig. 3(c), which is a TCMEC, with $Z_{th} = Z_{11}$ and $v_{th} = v_{cm,oc}$. To show this, we note that:

$$\lim_{Z_{dm}\to 0} Z_{12} = \lim_{Z_{dm}\to 0} Z_{22} = 0 \quad (13)$$

Thus, the CM and DM behavior become uncoupled as $Z_{dm} \to 0$. Furthermore,

$$\lim_{Z_{dm}\to 0} Z_{11} = R_{top}(t) \| R_{bot}(t) + R_{cm} \quad (14)$$

If one substitutes any possible valid values for $R_{top}(t)$ and $R_{bot}(t)$ into (14), one obtains a unit set with element

$$Z_{th} \in \left\{ \frac{R}{3} + R_{cm} \right\} \quad (15)$$

Thus, when $Z_{dm} \to 0$, Z_{th} in Fig. 3(c) becomes time invariant.

Interestingly, Z_{th} in (15) corresponds with z_x in (3), provided we undo the substitution of ($C_{cm} \to R_{cm}$). Moreover, in the case $Z_{dm} \to 0$, if one substitutes valid values for $R_{top}(t)$ and $R_{bot}(t)$ into (12) one obtains values for v_{th} in the set:

$$v_{th} \in \left\{ \pm\frac{V_{dc}}{2}, \pm\frac{V_{dc}}{6} \right\} \quad (16)$$

which can readily be verified corresponds with the v_x in (3).

Thus, to review, it has been shown that if $Z_{dm} = 0$, a TCMEC of the simplified inverter can be constructed which is equivalent to the right-hand side of the DCMEC shown in Fig. 2(b). In the following section we use a periodic linear time-varying (PLTV) analysis technique described in [14], [15] to analyze the CM behavior of a more realistic inverter (i.e., one with inductors/capacitors) and show that, even if the source $Z_{dm} \neq 0$, it is possible a TCMEC will still give a reasonable approximation of the terminal CM behavior of a converter.

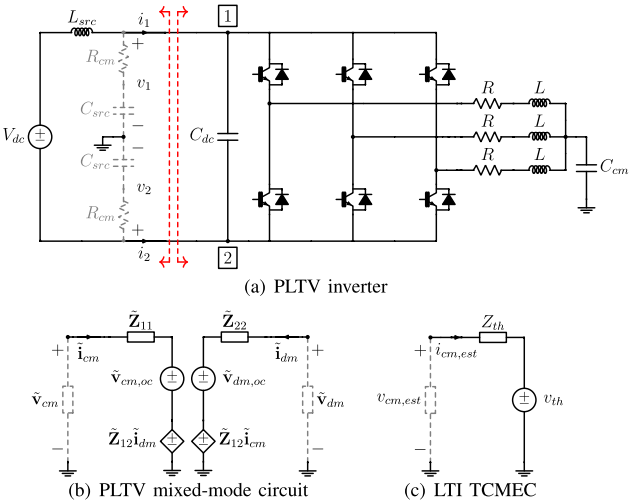


FIGURE 4. PLTV inverter circuit and corresponding TCMEC.

C. PLTV TCMEC NUMERICAL DEMONSTRATION

As discussed in [14], [15] and the references therein, since the steady-state voltages/currents of a periodically switched linear circuit are themselves periodic, the steady-state solution of the circuit can be obtained by solving a weakly formulated, Fourier expansion-based system of nodal equations. This system of equations is formed in an analogous manner to traditional nodal analysis – e.g., (5) – except instead of scalar admittances (e.g., Y_{11}), the current through an element is related to the voltage across that element by a matrix relationship (called harmonic ohm's law). In theory, these Fourier-based matrix relationships are infinite dimensional; in practice, the Fourier series is truncated to only include the first N user specified harmonics.

In order to simplify subsequent discussion, it is noted that the harmonic ohm's for a passive element (which relates the N voltage harmonics across the element to the N current harmonics that flow through it) is a diagonal matrix whose entries corresponding to the scalar admittance (which in general can depend on the harmonic number). The harmonic ohm's law for a switch element, in contrast, is a full matrix. This is because in the time-domain the voltage across a switch is equal to the product of the current through the switch times a square wave window function corresponding to the on/off cycling of the switch admittance. Therefore, in the frequency domain the voltage across the switch is defined by a convolution of the current spectrum and the window spectrum. Since the window is periodic, this convolution can be formulated as a Toeplitz matrix-multiplication.

We use the PLTV approach to analyze the inverter shown in Fig. 4(a), noting that since we are no longer restricted to resistive elements as in Section II-B, we have incorporated more realistic CM and DM impedances (e.g., a dc-link capacitor). The parameters for the inverter are given in Table 1. These values are representative of the parameters found in the dc micro-grid considered in Section V. The differential mode

TABLE 1. Fig. 4 parameters.

Parameter	Value	Parameter	Value
V_{dc}	360 V	C_{dc}*	100 μF or 1 μF
L_{src}*	40 μH	R	2 Ω
R_{cm}	20 Ω	L	1 mH
C_{src}	1 μF	C_{cm}	10 nF

* includes effective series resistance (ESR) = 0.1 Ω

series impedance L_{src} is representative of the cable impedance between components. The PLTV nodal matrix equation for Fig. 4(a) is shown in (17):

$$\hat{\tilde{\mathbf{i}}} = \hat{\tilde{\mathbf{Y}}}\hat{\tilde{\mathbf{v}}} \tag{17}$$

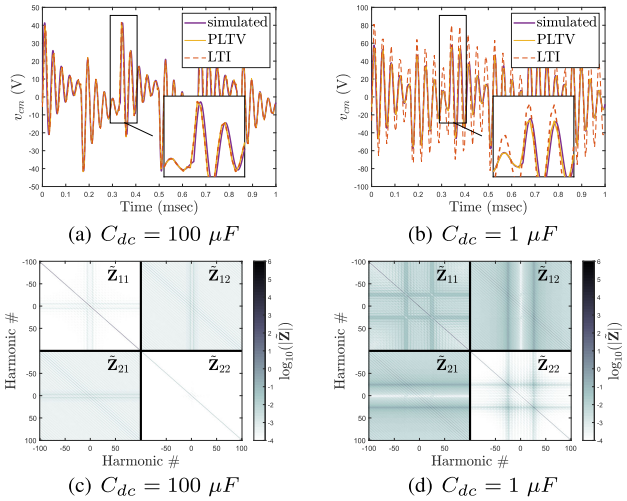
where $\hat{\tilde{\mathbf{i}}}$ is the vector of injected currents which consists of one sub-vector for each circuit node and each sub-vector contains the N current harmonics; $\hat{\tilde{\mathbf{v}}}$ is similar and contains the node voltage harmonics; and $\hat{\tilde{\mathbf{Y}}}$ is the corresponding admittance matrix defined by the harmonic ohm's law relations and the circuit topology. The tilde is used here to distinguish the PLTV quantities from the notation used in Section II-B.

We now proceed as in Section II-B by first eliminating via Kron reduction all nodes except $\boxed{1}$ and $\boxed{2}$. Then, solving (17) for $\hat{\tilde{\mathbf{v}}}$ and performing a change of variables analogous to (10) we arrive at:

$$\begin{aligned} \tilde{\mathbf{v}} &= \tilde{\mathbf{Z}}\tilde{\mathbf{i}} \\ \begin{bmatrix} \tilde{\mathbf{v}}_{cm} \\ \tilde{\mathbf{v}}_{dm} \end{bmatrix} &= \begin{bmatrix} \tilde{\mathbf{Z}}_{11} & \tilde{\mathbf{Z}}_{12} \\ \tilde{\mathbf{Z}}_{21} & \tilde{\mathbf{Z}}_{22} \end{bmatrix} \begin{bmatrix} \tilde{\mathbf{i}}_{cm} \\ \tilde{\mathbf{i}}_{dm} \end{bmatrix} \end{aligned} \tag{18}$$

where $\tilde{\mathbf{v}}_{cm}$ contains the N CM voltage harmonics and $\tilde{\mathbf{v}}_{dm}$ contains the N DM voltage harmonics. Equation (18) is depicted as a schematic in Fig. 4(b). In general for a PLTV circuit, $\tilde{\mathbf{Z}}$ is a full matrix. That is, due to the modulation action of the switches, each harmonic component of $\tilde{\mathbf{v}}$ is coupled to all of the harmonic components of $\tilde{\mathbf{i}}$. This is in contrast with an LTI circuit, which if represented in a similar fashion, would be diagonal.

We now show that for the particular inverter circuit shown in Fig. 4(a), both the time-varying nature of the circuit and the CM-DM coupling of (18) are minimal if C_{dc} is sufficiently large, even though the source DM impedance is nonzero. We show this in Fig. 5, wherein we consider two different values for $C_{dc} \in \{100\ \mu F,\ 1\ \mu F\}$. Figs. 5(a) and 5(b) compare the time domain simulation results of the voltage across the CM load (computed with ANSYS Simplorer and labeled *simulated*) to the time domain results computed using the PLTV method. Time domain results for the PLTV method were obtained by taking the inverse Fourier transform of $\tilde{\mathbf{v}}_{cm}$. In Figs. 5(a) and 5(b), the signal labeled *PLTV* corresponds to the PLTV solution using the full matrix $\tilde{\mathbf{Z}}$, with $N = 100$. The signal labeled *LTI* corresponds to the PLTV solution when only the diagonal of $\tilde{\mathbf{Z}}_{11}$ is considered. From Figs. 5(a) and 5(b), it is clear that if $C_{dc} = 100\ \mu F$, the PLTV and LTI solutions are almost identical; in contrast, if $C_{dc} = 1\ \mu F$, the PLTV and LTI solutions diverge considerably.



(a) $C_{dc} = 100\ \mu F$ (b) $C_{dc} = 1\ \mu F$

(c) $C_{dc} = 100\ \mu F$ (d) $C_{dc} = 1\ \mu F$

FIGURE 5. PLTV analysis of inverter.

TABLE 2. Fig. 5 matrix norms†.

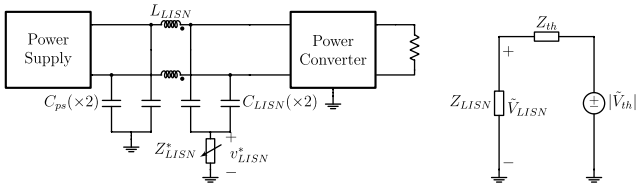
	$C_{dc} = 100\ \mu F$	$C_{dc} = 1\ \mu F$
$\|\tilde{\mathbf{Z}}_{12}\|_2$	0.194	16.944
$\|\tilde{\mathbf{Z}}_{11} - \mathcal{D}(\tilde{\mathbf{Z}}_{11})\|_2$	0.047	3.943

† $\mathcal{D}(\cdot)$ is a matrix function which returns the argument with off-diagonal terms set to zero

This behavior can be explained by considering Figs. 5(c) and 5(d), which show the magnitude of each element of $\tilde{\mathbf{Z}}$ using a darker color for larger impedances and a lighter color for smaller impedances (a log-scale is used for the color distribution). From Figs. 5(c) and 5(d), it is clear that when $C_{dc} = 100\ \mu F$, the sub-matrix $\tilde{\mathbf{Z}}_{11}$ is nearly diagonal – hence nearly LTI, and $\tilde{\mathbf{Z}}_{12}$ is generally small at all frequencies – hence there is little coupling between CM and DM. This implies that the PLTV mixed-mode two-port network shown in Fig. 4(b) can accurately be reduced to the LTI TCMEC shown in Fig. 4(c). In contrast, if $C_{dc} = 1\ \mu F$, both $\tilde{\mathbf{Z}}_{11}$ and $\tilde{\mathbf{Z}}_{12}$ contain significant impedances both on and off the diagonal, which implies that the CM behavior of the inverter circuit cannot be accurately modeled by an LTI TCMEC. The conclusions drawn about Figs. 5(c) and 5(d) by visual inspection can be verified by considering the matrix norms given in Table. 2.

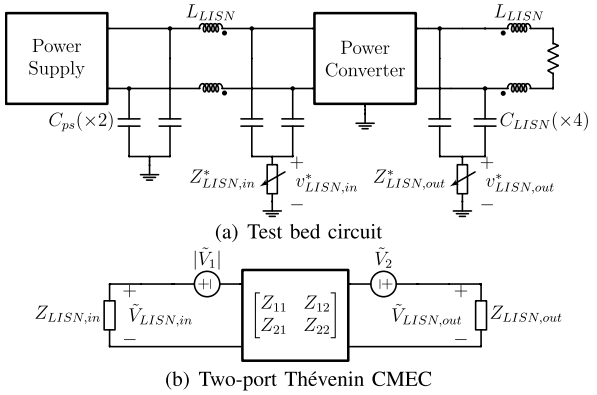
D. REMARKS

In the remainder of the this work, we assume all power converters of interest can be accurately modeled in terms of CM behavior by a Thévenin equivalent circuit. We make this assumption with two provisions in mind: First, all converters to be studied have large capacitors supporting the dc-link of the transistor module, which based on the analysis given in Section II-C, minimizes CM-DM coupling and masks the



(a) Test bed circuit (b) Thévenin CMEC

FIGURE 6. CM characterization of a power converter.



(a) Test bed circuit

(b) Two-port Thévenin CMEC

FIGURE 7. CM characterization of a two-port power converter.

time-varying nature of the circuit. Second, as mentioned in Section II-A, only balanced (i.e., symmetric) converters will be considered, thus limiting other potential CM-DM coupling effects.

III. Thévenin CHARACTERIZATION PROCEDURE

A least-squares experimental CM characterization procedure outlined in [12] is briefly reviewed and then expanded in this section. Power electronic converters that are ''terminated'' (i.e., converters that only connect to the power system as either a source or a load) are considered in Section III-A; in Section III-B we consider the two-port Thévenin characterization of ''unterminated'' (i.e., input/output) converters, which were studied in [11]. In Section III-C we provide experimental details related to the characterization procedure which are common to both terminated and unterminated converters.

A. ONE-PORT Thévenin

A schematic of the experimental setup used to characterize the Thévenin parameters of a terminated power converter is shown in Fig. 6. Fig. 6(a) illustrates how the power converter to be characterized is connected to a power supply through a LISN. The purpose of the LISN is to isolate the CM behavior of the power converter from the CM behavior of the power supply, while at the same time presenting an adjustable CM impedance load to the power converter under study. With the CM behavior of the power converter represented by a Thévenin equivalent circuit, the mixed-mode schematic in Fig. 6(a) reduces to the CM-only schematic in Fig. 6(b). It is noted that in Fig. 6, Z^*_{LISN} represents the user-selected impedance(s) to be used in the characterization procedure whereas Z_{LISN} is the actual impedance seen by the converter which may differ from Z^*_{LISN} due to the practical limitations of the LISN (see Section III-C).

In view of Fig. 6(b), the CM Thévenin characterization procedure proceeds by loading the converter with various known CM loads ($Z_{LISN,1}, Z_{LISN,2}, \ldots Z_{LISN,m}$) and recording oscilloscope measurements of v_{LISN} ($v_{LISN,1}, v_{LISN,2}, \ldots v_{LISN,m}$). From these LISN/voltage measurements, curve-fitting is then used to determine the Thévenin parameters. Specifically, a number of measurements, $m \geq 3$, are considered so as to over-determine the unknown Thévenin parameters, yielding a corresponding least-squares solution. This is summarized by (19)-(21)

$$\arg\min_{\mathbf{x}\in\mathbb{R}^3} \sum_m \Big(|\tilde{V}_{LISN}| - v_{calc}(x) \Big)^2 \tag{19}$$

where

$$\mathbf{x} = \left[\mathrm{Re}(Z_{th})\ \ \mathrm{Im}(Z_{th})\ |\tilde{V}_{th}|\right]^T \tag{20}$$

and

$$v_{calc} = \frac{|Z_{LISN}|\,|\tilde{V}_{th}|}{|Z_{LISN} + Z_{th}|} \tag{21}$$

and $\tilde{V}_{LISN}$ is the frequency-domain spectrum of v_{LISN}.

It is noted that (19) is evaluated independently for each frequency, so $\tilde{V}_{LISN}$ can be considered to be a scalar corresponding to a particular frequency. Further, v_{calc} corresponds to the calculation of $\tilde{V}_{LISN}$ via voltage division, as in (21). Inspection of (21) reveals that v_{calc} is nonlinear with respect to the Thévenin impedance parameters, thus making (19) a nonlinear-least-squares (NLLSQ) problem.

Additionally, it is noted that only the Thévenin voltage magnitude $|\tilde{V}_{th}|$ is determined by the curve-fitting, instead of a complex-valued spectrum which would contain the phase information. This allows for the various m measurements of v_{LISN} to be made in an unsynchronized fashion with respect to the instantaneous phase of v_{th} (which is unavailable without access to the converter's switch voltage(s)). However, this magnitude-only characterization also leads to some uncertainty in the expected CM current in a power system with two-or-more converters operating simultaneously, as will be considered in Section IV.

B. TWO-PORT Thévenin

In this section a characterization procedure for a two-port TCMEC is given, which is used to model the CM behavior of an unterminated power converter [11]. The experimental setup for this characterization is shown in Fig. 7. Therein, the test-bed circuit containing two LISNs, Fig. 7(a), is used to fit the two-port Thévenin equivalent circuit shown in Fig. 7(b).

TABLE 3. Z^*_{LISN} **values.**

Type	Value	Unit
R	$10,\ 100,\ 500,\ 1k$	Ω
C	$1n,\ 10n,\ 100n$	F
L	$10\mu,\ 200\mu,\ 1m$	H

In a similar way to Section III-A, the two-port Thévenin CM characterization procedure involves loading the converter with various CM loads – at both the input and output – and using curve-fitting to determine the Thévenin parameters based on measurements of $v_{LISN,in}$ and $v_{LISN,out}$. Accordingly, a NLLSQ problem can be formulated

$$\arg\min_{\mathbf{x}\in\mathbb{R}^9} \sum_m \left\| \begin{bmatrix} \tilde{V}_{LISN,in} \\ \tilde{V}_{LISN,out} \end{bmatrix} - \begin{bmatrix} v_{calc,in} \\ v_{calc,out} \end{bmatrix} \right\|_2^2 \tag{22}$$

where $\mathbf{x}$ is given by (23) and $v_{calc,in}$ and $v_{calc,out}$ are given by (24).

$$\begin{aligned} \mathbf{x} = \big[&\mathrm{Re}(Z_{11})\ \mathrm{Im}(Z_{11})\ \mathrm{Re}(Z_{12})\ \mathrm{Im}(Z_{12})\ldots \\ &\ldots\ \mathrm{Re}(Z_{22})\ \mathrm{Im}(Z_{22})\ |\tilde{V}_1|\ \mathrm{Re}(\tilde{V}_2)\ \mathrm{Im}(\tilde{V}_2)\big]^T \end{aligned} \tag{23}$$

$$v_{calc,in} = \frac{Z_{LISN,in}(|\tilde{V}_1|(Z_{22}+Z_{LISN,out}) - \tilde{V}_2 Z_{12})}{Z_d}$$

$$v_{calc,out} = \frac{Z_{LISN,out}(\tilde{V}_2(Z_{11}+Z_{LISN,in}) - |\tilde{V}_1|Z_{12})}{Z_d}$$

$$Z_d = -Z_{12}^2 + (Z_{11}+Z_{LISN,in})(Z_{22}+Z_{LISN,out}) \tag{24}$$

It is noted that in (23), the two Thévenin voltage sources $\tilde{V}_1$ and $\tilde{V}_2$ are treated differently from one-another; specifically, only the magnitude of $\tilde{V}_1$ is considered to be an unknown, whereas both the real and imaginary parts of $\tilde{V}_2$ are unknowns. Thus, the relative phase between $\tilde{V}_1$ and $\tilde{V}_2$ is determined by the fitting-procedure, which is accomplished by taking synchronized measurements of $v_{LISN,in}$ and $v_{LISN,out}$ (for a given load condition).

C. Thévenin CHARACTERIZATION DETAILS

1) Z_{LISN}

It is noted that the Thévenin parameter curve-fitting problems (21) and (24) are influenced by both the real and imaginary parts of Z_{LISN}. Thus, to obtain reliable Thévenin parameters, the Z_{LISN} impedances should be selected to span as much of the complex impedance plane as possible. In this research the authors chose $m = 10$ different Z^*_{LISN} impedances whose component values are shown in Table 3. Z_{LISN} may be expressed in terms of Z^*_{LISN} by,

$$Z_{LISN} = \left(Z^*_{LISN} + Z_{Clisn}\right) \parallel \left(Z_{Llisn} + Z_{Cps}\right) \tag{25}$$

where Z_{Clisn} is the frequency dependent impedance of the parallel C_{LISN} capacitors, Z_{Llisn} is the impedance of L_{LISN}, and Z_{Cps} is the impedance of the parallel C_{ps} capacitors.

Fig. 8 shows a plot of Z_{LISN} for the various Z^*_{LISN} loads. Overall it is clear that the LISN is able to load the converter

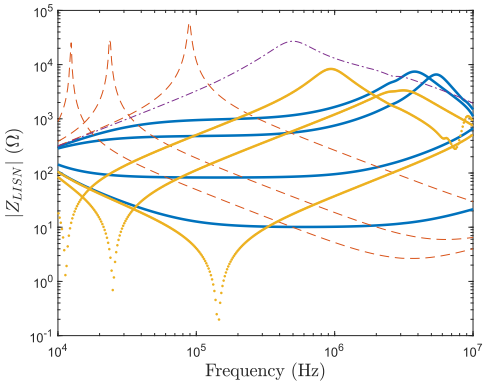


FIGURE 8. Z_{LISN} **impedances (blue/solid: resistors, orange/dashed: capacitors, yellow/dotted: inductors).** Z_{Llisn} **is shown in purple/dash-dot.**

with a broad range of CM impedances over the frequency range of interest (here considered to be 10 kHz to 10 MHz). It is noted from (25), however, that the maximum impedance of Z_{LISN} (assuming Z_{Clisn} and Z_{Cps} are small) is limited by the magnitude of Z_{Llisn}, which is also plotted in Fig. 8. Therein, it is observed that the reduced impedance of L_{LISN} at low frequencies limits to some extent the ability of the LISN to load the converter with a diverse set of Z_{LISN}'s which can reduce the accuracy of the characterization at these frequencies. Physically, L_{LISN} is a 5 mH Schaffner RT Series common-mode inductor (CMI), C_{LISN} is a 0.22 μF low ESR/ESL polypropylene capacitor, and C_{ps} is a 2 mF electrolytic capacitor. The design decision of using a CMI for L_{LISN} was in part based on the analysis presented in Sections II-B and II-C, which shows that a low DM impedance minimizes the risk of the LISN introducing mode-coupling.

2) FREQUENCY SPECTRUM ESTIMATION

The time-domain measurements of v_{LISN} are converted to a useful frequency-domain representation by first transforming the data to the frequency domain via an FFT, then finding the envelope of $\tilde{V}_{LISN}$ using a peak-finding algorithm (`findpeaks` in MATLAB). Using the envelope of the LISN voltage spectrum in the curve-fitting process results in smooth/interpolatable Thévenin parameters.

3) NLLSQ

The nonlinear-least-squares problems of (19) and (22) were solved using the MATLAB `lsqnonlin` function with the default `'trust-region-reflective'` algorithm – which can handle bound constraints. Bound constraints are used to ensure the real part of the characterized impedances remain positive (i.e., $\mathrm{Re}(Z_{th}) \geq 0$, $\mathrm{Re}(Z_{11}) \geq 0$, etc.).

IV. WORST-CASE ANALYSIS

As mentioned in Section III, only the magnitude of the Thévenin voltage sources are determined by the least-squares characterization procedure. Although this means no time synchronization between the sequential m measurements of

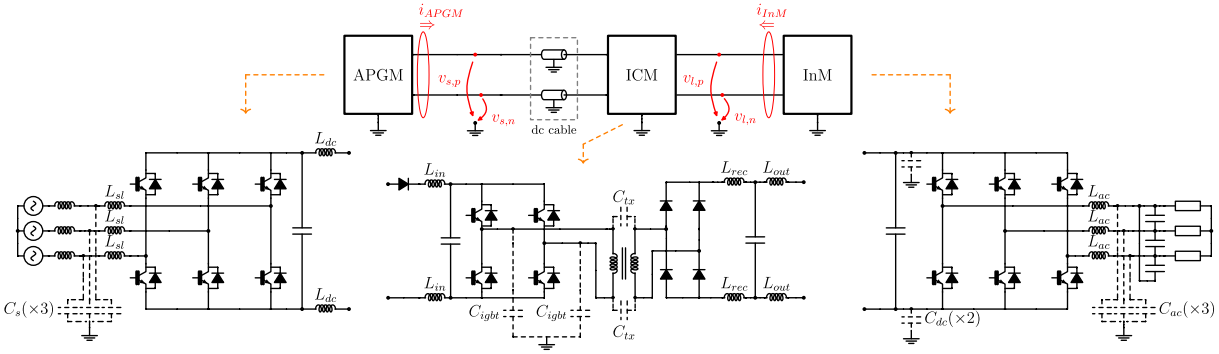


FIGURE 9. System-level CM study of dc micro-grid [17].

v_{LISN} (or $v_{LISN,in}$ / $v_{LISN,out}$) is needed, a consequence of the magnitude-only characterization is that when two or more converters in a system are operating simultaneously, only a worst-case estimate of the CM behavior is available.

This can be understood by considering that when $n \geq 2$ linear Thévenin equivalent circuits are connected together {Thévenin A, Thévenin B, ... etc.} the "solution" to the resulting circuit is found by considering each Thévenin voltage source's impact separately and summing the corresponding results. Such a sum, however, cannot be computed if the relative phase of the n Thévenin voltage sources are unknown. Nevertheless, using the triangle inequality, one can compute an upper bound for the sum. For example, the theoretical maximum of the voltage at an arbitrary node k can be computed as in:

$$|\tilde{V}_{k,A} + \tilde{V}_{k,B} + \ldots| \leq |\tilde{V}_{k,A}| + |\tilde{V}_{k,B}| + \ldots \qquad (26)$$

where each $\tilde{V}_{k,i}$ corresponds to the voltage at node k due solely to the ith Thévenin voltage source. Indeed, each $|\tilde{V}_{k,i}|$ is proportional the corresponding ith Thévenin voltage source. That is,

$$|\tilde{V}_{k,i}| = |\tilde{V}_{th,i}| f(Z_{th,A},\ Z_{th,B},\ \ldots,\ Z_{th,i},\ \ldots) \qquad (27)$$

where each $|\tilde{V}_{th,i}|$ is determined by the least-squares Thévenin characterization procedure. Moreover, since the envelope of each $\tilde{V}_{LISN}$ measurement is used in the fitting process, we are guaranteed that the resulting $|\tilde{V}_{th,i}|$ for each converter is an upper bound for the actual $\tilde{V}_{th,i}$. Thus, in using (26) and (27) we are guaranteed to be computing an upper bound for the expected CM behavior of a given system.

V. SYSTEM-LEVEL DEMONSTRATION

A system-level CM study of a dc micro-grid was conducted to demonstrate the proposed TCMEC modeling approach. A schematic of the micro-grid is shown in Fig. 9. Therein, the auxiliary power generation module (APGM, [17]) is a permanent magnet synchronous machine coupled to a active (PWM) rectifier; the machine was operated at 1500 rpm and the output voltage is regulated to 600 V_{dc}. The ICM is an isolated dc-dc converter (600 V_{dc} input, 420 V_{dc} output) which is considered an unterminated converter since it is used in a series connection with other

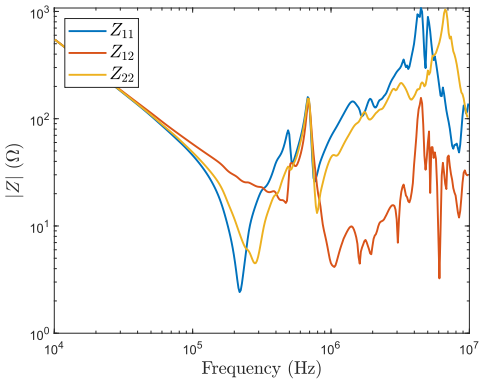


FIGURE 10. DC cable impedance parameters.

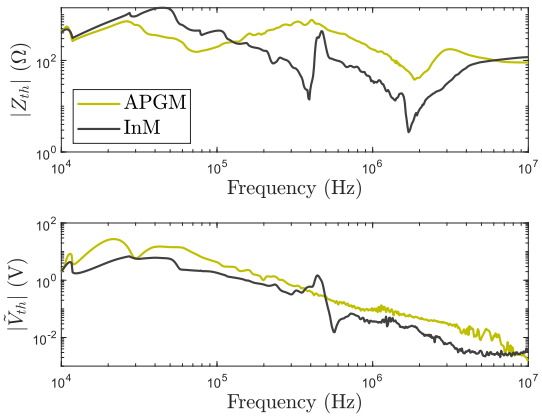


FIGURE 11. APGM and InM TCMEC parameters.

PE converters. Last, the InM is a three-phase inverter module which is operated with a 420 V_{dc} input and feeds a balanced three-phase resistive load at approximately 2 kW. As part of this system-level demonstration, an electrically long dc cable was used to connect the APGM to the ICM. This cable is incorporated into the TCMEC with a two-port network whose corresponding impedance parameters are shown in Fig. 10.

The APGM and InM shown in Fig. 9 where characterized as one-port TCMECs using the procedure of Section III-A. The corresponding TCMEC parameters for these converters are shown in Fig. 11. Likewise, the two-port TCMEC parameters for the ICM which were characterized according the

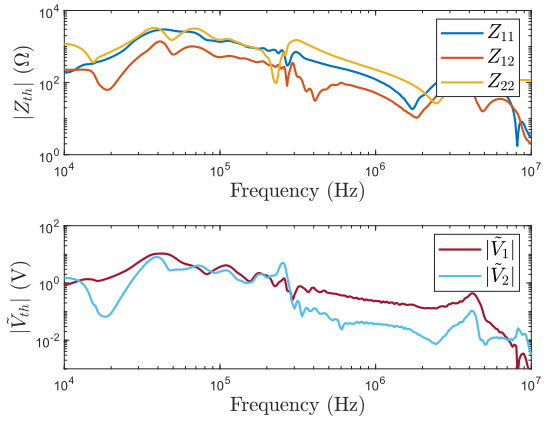


FIGURE 12. ICM two-port TCMEC parameters.

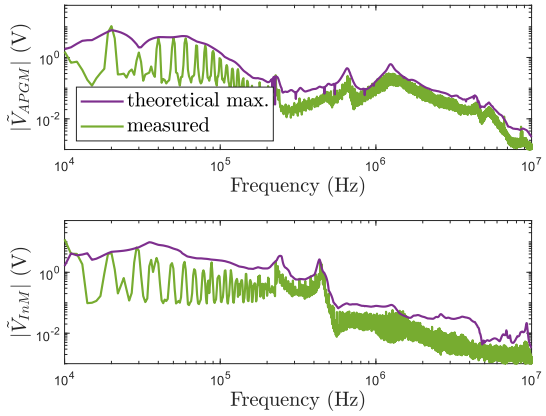


FIGURE 13. Worst-case CM voltage in dc micro-grid.

procedure described in Section III-B are shown in Fig. 12. Overall, the TCMEC parameters obtained are in agreement with the authors' expectations based on familiarity with the converters design/construction [12].

After combining the APGM, ICM and InM TCMECs together with the two-port network for the dc cable, a system-level worst-case CM study was performed. The predicted worst case CM voltage spectrums are compared to the measured values in Fig. 13. The locations of the measurements are highlighted in Fig. 9. The measured CM voltage at the APGM was obtained by taking the FFT of $v_{APGM} = \frac{1}{2}(v_{s,p} + v_{s,n})$. Similarly, the measured CM voltage at the InM was obtained by taking the FFT of $v_{InM} = \frac{1}{2}(v_{l,p} + v_{l,n})$. CM currents flowing through the APGM and InM were also measured and are compared to the theoretical worst-case predictions in Fig. 14. These CM currents were measured by passing both +/− dc cables through a Yokogawa 701930 current probe.

From Fig. 13 it is clear that the *theoretical max* worst-case CM voltage prediction appropriately bounds the corresponding measured voltage over the frequency range of interest. The anomalous underestimation of CM voltage at 10 *kHz* in the lower plot of Fig. 13 is likely due to an error in the characterization. As noted in Section III-C, the LISN

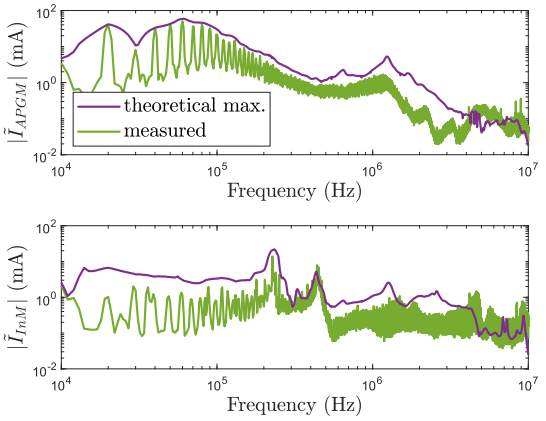


FIGURE 14. Worst-case CM current in dc micro-grid.

characterization impedances have relatively similar values at low frequencies (Fig. 8), which may reduce characterization accuracy at these frequencies.

In Fig. 14, the worst-case CM current prediction also appropriately bounds the corresponding measured CM current over much of the frequency range of interest, although above ∼5 *MHz* the TCMEC model tends to underestimate the measured CM current at both the APGM and InM. This underestimation at higher frequencies was not observed in the CM voltage predictions. Subsequent to the hardware testing, it has been found that the current probes used measure appreciable ambient background noise at these higher frequencies, which is likely caused by equipment, including dynamometers, that are not modeled in the TCMEC.

It is noted that in both Figs. 13 and 14 there are frequencies at which the measured values are much less than the worst case predictions. This is not unexpected, given that deconstructive interference can occur at frequencies where two or three converters simultaneously generate harmonic noise. In theory, if switching is synchronized between some of the converters, deconstructive effects could be accounted for by characterizing them together. For example, having both the ICM and InM characterized as a single Thévenin circuit as viewed from the DC bus would yield a less conservative upper bound than that obtained with each converter characterized separately. However, in practice, it is unlikely that the converters will be synchronized. If the converters were to be characterized together, one must accept a Thévenin model which has a degree of uncertainty due to the randomness of the relative phase between switching waveforms, which may not present an advantage over characterizing components separately.

VI. CONCLUSION

A Thévenin-based common-mode modeling approach for power electronic systems has been developed in this work. First, theoretical justification for modeling the CM behavior of power converters with Thévenin equivalent circuits was provided. Next, an experimental characterization technique

used to obtain the Thévenin parameters was proposed. Last, an analysis method used to predict the theoretical worst-case CM behavior in a PE system was given. Experimental results illustrating the proposed CM modeling approach have been provided. Further work on this topic aims to investigate the applicability of the Thévein equivalent circuit modeling approach for asymmetric converter topologies.

REFERENCES

[1] S. Chen, T. A. Lipo, and D. Fitzgerald, "Modeling of motor bearing currents in PWM inverter drives," *IEEE Trans. Ind. Appl.*, vol. 32, no. 6, pp. 1365–1370, Nov. 1996.

[2] S. Ogasawara and H. Akagi, "Modeling and damping of high-frequency leakage currents in PWM inverter-fed AC motor drive systems," *IEEE Trans. Ind. Appl.*, vol. 32, no. 5, pp. 1105–1114, Sep. 1996.

[3] L. Ran, S. Gokani, J. Clare, K. J. Bradley, and C. Christopoulos, "Conducted electromagnetic emissions in induction motor drive systems. I. Time domain analysis and identification of dominant modes," *IEEE Trans. Power Electron.*, vol. 13, no. 4, pp. 757–767, Jul. 1998.

[4] J. M. Erdman, R. J. Kerkman, D. W. Schlegel, and G. L. Skibinski, "Effect of PWM inverters on AC motor bearing currents and shaft voltages," *IEEE Trans. Ind. Appl.*, vol. 32, no. 2, pp. 250–259, Mar. 1996.

[5] S. Ohn *et al.*, "Three-terminal common-mode EMI model for EMI generation, propagation, and mitigation in a full-SiC three-phase UPS module," *IEEE Trans. Power Electron.*, vol. 34, no. 9, pp. 8599–8612, Sep. 2019.

[6] A. D. Brovont and S. D. Pekarek, "Derivation and application of equivalent circuits to model common-mode current in microgrids," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 5, no. 1, pp. 297–308, Mar. 2017.

[7] M. Jin and M. Weiming, "A new technique for modeling and analysis of mixed-mode conducted EMI noise," *IEEE Trans. Power Electron.*, vol. 19, no. 6, pp. 1679–1687, Nov. 2004.

[8] Q. Liu, F. Wang, and D. Boroyevich, "Modular-terminal-behavioral (MTB) model for characterizing switching module conducted EMI generation in converter systems," *IEEE Trans. Power Electron.*, vol. 21, no. 6, pp. 1804–1814, Nov. 2006.

[9] A. C. Baisden, D. Boroyevich, and F. Wang, "Generalized terminal modeling of electromagnetic interference," *IEEE Trans. Ind. Appl.*, vol. 46, no. 5, pp. 2068–2079, Sep. 2010.

[10] H. Bishnoi, A. C. Baisden, P. Mattavelli, and D. Boroyevich, "Analysis of EMI terminal modeling of switched power converters," *IEEE Trans. Power Electron.*, vol. 27, no. 9, pp. 3924–3933, Mar. 2012.

[11] H. Bishnoi, P. Mattavelli, R. Burgos, and D. Boroyevich, "EMI behavioral models of DC-fed three-phase motor drive systems," *IEEE Trans. Power Electron.*, vol. 29, no. 9, pp. 4633–4645, Sep. 2014.

[12] T. J. Donnelly, S. D. Pekarek, D. Fudge, N. Vaks, and N. Zarate, "Predicting worst case common-mode behavior in power electronic based systems," in *Proc. IEEE Electric Ship Technol. Symp. (ESTS)*, Aug. 2019, pp. 396–402.

[13] A. D. Brovont, "Generalized differential-common-mode decomposition for modeling conducted emissions in asymmetric power electronic systems," *IEEE Trans. Power Electron.*, vol. 33, no. 8, pp. 6461–6466, Aug. 2018.

[14] R. Trinchero, I. S. Stievano, and F. G. Canavero, "Steady-state analysis of switching power converters via augmented time-invariant equivalents," *IEEE Trans. Power Electron.*, vol. 29, no. 11, pp. 5657–5661, Nov. 2014.

[15] R. Trinchero, I. S. Stievano, and F. G. Canavero, "EMI modeling of switching circuits via augmented equivalents and measured data," in *Proc. IEEE Int. Symp. Electromagn. Compat. (EMC)*, Aug. 2015, pp. 130–133.

[16] A. Ales, J.-L. Schanen, D. Moussaoui, and J. Roudet, "Impedances identification of DC/DC converters for network EMC analysis," *IEEE Trans. Power Electron.*, vol. 29, no. 12, pp. 6445–6457, Dec. 2014.

[17] S. D. Sudhoff *et al.*, "A reduced scale naval DC microgrid to support electric ship research and development," in *Proc. IEEE Electric Ship Technol. Symp. (ESTS)*, Jun. 2015, pp. 464–471.

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