Loop Dynamics Analysis of PAM-4 Mueller–Muller Clock and Data Recovery System

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ABSTRACT This paper provides a framework for analyzing the loop dynamics of the clock and data recovery (CDR) system of ADC-based PAM-4 receivers, which will assist in extending the timing recovery loop bandwidth. This paper formulates an accurate linear model of linear and signed Mueller–Muller phase detector for baud-rate clock recovery. Different equalization configurations of continuous-time linear equalizer (CTLE) and feed-forward equalizer (FFE) are evaluated from a phase detector performance perspective to enable high CDR loop bandwidth. The impact of loop latency on the timing recovery of ADC-based PAM-4 receivers is also analyzed and demonstrated using accurate behavioral simulations. The analysis and behavioral results show that, to achieve high CDR loop bandwidth with a good jitter tolerance, the phase detector gain to noise ratio should be maximized, and CDR loop latency should be minimized.

INDEX TERMS Analog-to-digital converter (ADC)-based receiver, clock and data recovery, digital equalization, feed-forward equalizer (FFE), time interleaving.

I. INTRODUCTION

THE DRAMATIC increase in the demand for higher data communication speed in recent decade has made multi-level signaling and analog-to-digital (ADC)-based receivers popular in wireline communications [1], [2], [3], [4]. For these high-speed ADC-based receivers, clock and data recovery is one of the main challenging functions [5]. One concern is the power consumption. Designers tend to opt for baud-rate clock recovery instead of conventional oversampling architectures to save the number of comparators and the corresponding power consumption. For example, bang-bang phase detectors (BBPD) require both data and edge samples [5], [6], while baud-rate phase detectors such as Mueller–Muller phase detectors (MMPD) require only data samples [1], [2], [3], [4].

Mueller and Muller first proposed a decision-directed baud- or symbol-rate timing recovery algorithm in 1976 [7]. In literature, different architectural implementations of MMPD are presented and are categorized into two general categories: linear [8] and signed MMPD [9], [10], [11]. For ADC-based receivers, the linear MMPD retains the quantization accuracy of the ADC, whereas the signed MMPD has a binary output (early/late) that can reduce the hardware complexity and the resulting power consumption significantly.

Another concern is the CDR loop bandwidth (f_{BW}), which is limited to few MHz ($f_{BW} \simeq f_{baud}/1000$) [1], [2], [12] mainly due to complex loop dynamics. The limited CDR loop bandwidth leads to a major drawback of stringent transmitter (Tx) jitter requirements, as the CDR cannot track the jitter components beyond its bandwidth. This further results in increased Tx clocking power [13]. Also, in the Peripheral Component Interconnect Express (PCI-e) standard, the CDR bandwidth scales up along with the data rate with each new generation. For example, in PCI-e 5.0, CDR bandwidth increased by two folds compared to PCI-e 4.0 [14]. Designers would like to continue the legacy of doubling the CDR bandwidth in the next generation of PCI-e standards.
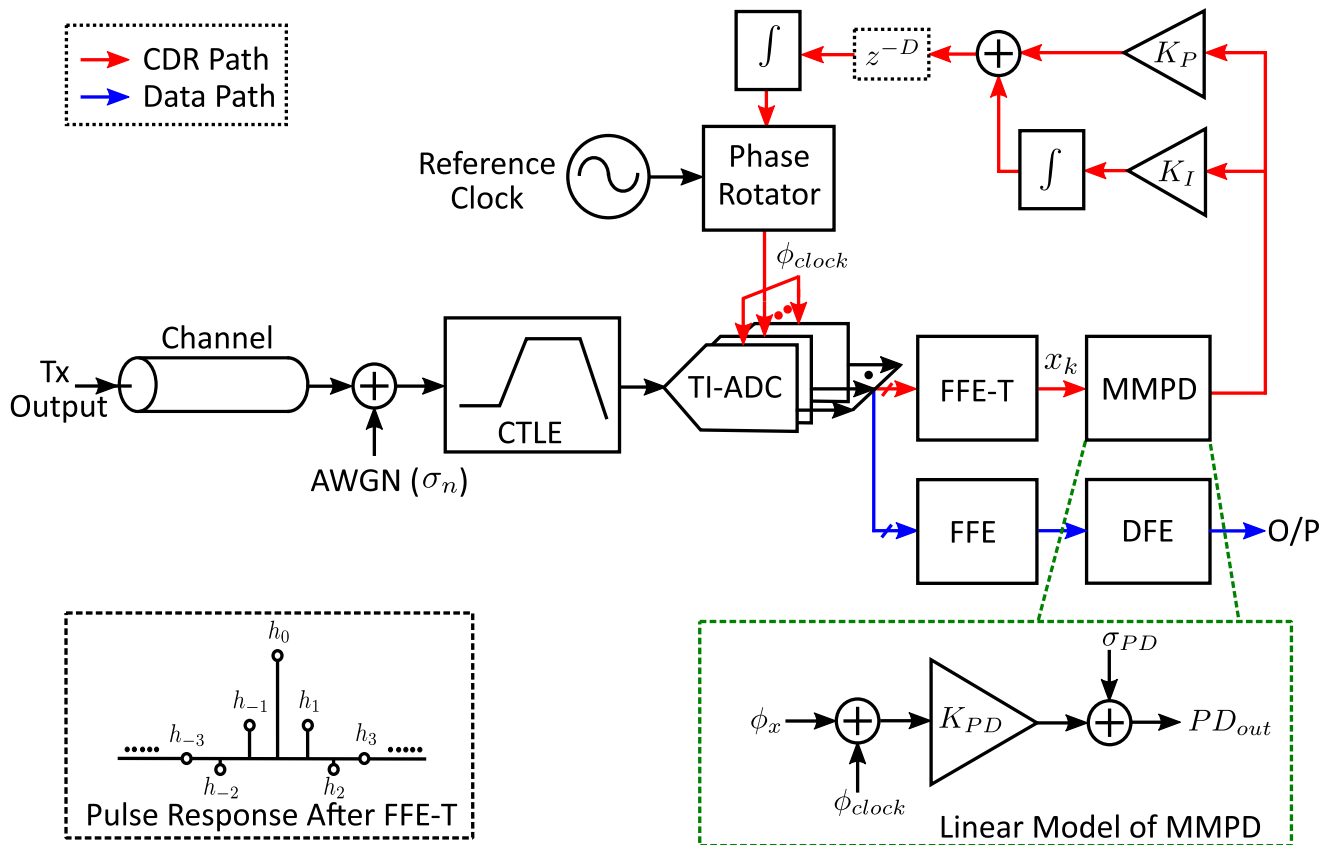
FIGURE 1. System model of ADC-based PAM-4 receiver with MMPD-based timing recovery.

The factors that impact the CDR loop bandwidth can be clubbed into three major components:

- Inter-symbol interference (ISI): The residual ISI at the CDR input impacts the phase detector's gain. It also appears as noise at the phase detector output. This consequently impacts the jitter tolerance (JTOL) performance.
- Noise at the CDR input: The noise translates to jitter of the recovered clock decreasing JTOL.
- Latency in the CDR loop: The latency is introduced due to time-interleaved sampling in the front end, which is necessary to allow practical operating frequencies in the ADC and the following digital signal processing (DSP) equalizer. For example, in [15], the DSP operates at a clock frequency of $f_{baud}/32$. These factors introduce a latency of many UI's in the CDR loop, causing peaking in the jitter transfer function and reducing high-frequency jitter tolerance.

To address the issue of limited CDR bandwidth, a rigorous understanding of CDR loop dynamics is required. However, compared to the Mueller–Muller baud-rate sampling technique, much work has been done on the oversampling Bang-Bang phase detector analysis. In [16], [17], the authors proposed a linear model for BBPD by considering the effect of metastability and input jitter, enabling analysis of the jitter transfer and jitter tolerance performance. On the other hand,

for CDR with MMPD, most of the previous work emphasized the different architectural implementations of the phase detector rather than a comprehensive analysis that provides design insights. For example, Spagna et al. [9] introduced a sign-sign MMPD, while Dokania et al. [10] modified it and presented an unequalized Mueller–Muller-CDR that allows the adjustment of the phase lock position.

In this paper, we first quantify the performance of linear and signed MMPD with a small-signal linear model in Section II. Section III demonstrates how equalization by different blocks of analog front-end (AFE) impacts the MMPD performance using a behavioral system model. Section IV describes how the loop latency introduced by time-interleaved sampling affects the baud rate CDR bandwidth. Finally, in Section V, concluding remarks are made.

II. LINEARIZED MODEL AND ANALYSIS OF MUELLER–MULLER PHASE DETECTOR

Fig. 1 illustrates the block diagram of an ADC-based PAM-4 receiver with MMPD-based CDR. The behavioral model is implemented in MATLAB to verify the analytical findings presented in Sections II–IV. Here, we consider a baud rate of 56 Gbaud/s in our analysis, and we use the channel model from IEEE802.3ck [18], with the channel's frequency response shown in Fig. 2. The channel attenuates the Tx
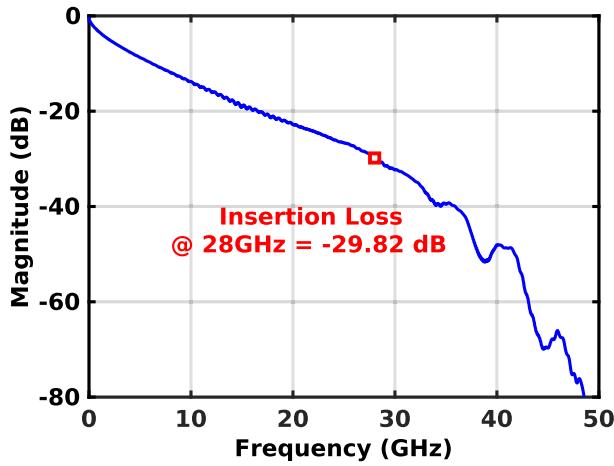
FIGURE 2. Frequency response of channel [18].

driver output with an insertion loss of 29.8 dB at the Nyquist frequency of 28 GHz.

The CTLE conditions the attenuated channel output before forwarding it to the time-interleaved (TI) ADC. The digitized output of ADC is sent to two separate paths: the data path and the timing recovery path. The ADC output is equalized in the data path by a long digital FFE and decision feedback equalizer (DFE) to increase the signal-to-noise ratio (SNR), while, in the timing recovery path, another short FFE equalizes the ADC output before forwarding it to the phase detector. The phase detector output is further processed by a digital loop filter (DLF) consisting of a proportional and an integral path, with the gain of K_P and K_I, respectively. The loop filter output adjusts the reference clock phase using a phase rotator, whose gain is K_{DPC} (DPC: Digital to Phase Converter). Furthermore, to emulate the loop delay introduced by the ADC time-interleaving and the FFE-T, a delay element z^{-D} is inserted in the CDR loop.

As this paper focuses on timing recovery, we will consider only the CDR path. We do not model ADC's quantization noise and the error introduced by sampling jitter. These noise sources from the ADC can be included in the input-referred noise, σ_n, as shown in Fig. 1. Typically, these are negligible compared to other random noise sources. Nevertheless, they still count towards defining the specifications of the ADC.

To characterize the phase detector (PD), we use the global figure of merit *KNR* (Gain-to-Noise Ratio) as mentioned in [8]. *KNR* is defined as the ratio of phase detector gain (K_{PD}) to phase detector output standard deviation (σ_{PD}).

$$KNR = \frac{K_{PD}}{\sigma_{PD}} \qquad (1)$$

KNR is similar to the phase detector efficiency criteria γ in [19]. However, unlike γ, *KNR* is independent of the CDR loop bandwidth. *KNR* can be depicted as the inverse of the phase detector's input-referred noise; a higher *KNR* leads to lower phase detector input-referred noise, which improves the jitter tolerance of CDR at higher frequencies.

In the following two sub-sections, we will analyze the behavior of linear and signed MMPD and provide a linear model of MMPD, as shown in Fig. 1, to enable the analysis on CDR loop dynamics.

A. LINEAR MMPD

The linear MMPD operation involves the concept of a "timing function (F)," which provides the information on phase error between the clock and data input. A typical timing function for linear MMPD is $F_L = h_1 - h_{-1}$ (i.e., the difference between the first post-cursor, h_1, and the first pre-cursor, h_{-1}). This timing function can be derived by taking the expectation of the linear combination of phase detector output, as shown in Eq. (2).

$$F_L(\phi) = \mathbb{E}[x(k, \phi)\widehat{x}(k - 1) - x(k - 1, \phi)\widehat{x}(k)] \qquad (2)$$

where $x(k, \phi)$ is the equalized sample with time index k and sampling phase error ϕ, and $\widehat{x}(k)$ is the corresponding estimate of $x(k)$.

Fig. 3 (a) and (b) show the pulse response example and the corresponding timing function $F_L(\phi)$. When the sampling phase shifts to the left, F_L becomes positive; conversely, F_L becomes negative if the sampling phase shifts to the right. A stable CDR feedback loop will lock at the point where $F_L = 0$, and that is when the first pre-cursor and the first post-cursor become equal.

To evaluate the linear MMPD performance, the KNR_L can be calculated analytically from the pulse response. The gain of linear MMPD is calculated by measuring the slope of timing function F_L at zero crossing, as shown in Fig. 3 (b). The gain can further be expressed as Eq. (3), i.e., the difference in pulse response slopes at h_1 and h_{-1} of the locking sampling phase, as shown in Fig. 3(a).

$$K_L = \frac{d(h_1)}{d\phi} - \frac{d(h_{-1})}{d\phi} \quad when \quad h_1 = h_{-1} \qquad (3)$$

Due to ISI and noise, the linear MMPD output has a standard deviation σ_L which was evaluated analytically in [7] and can be expressed as:

$$\sigma_L = \sqrt{2\sum_{k \neq 0} h_k^2 - \left[2 - \frac{\mathbb{E}\{a_k^4\}}{\mathbb{E}\{a_k^2\}^2}\right]\left(h_1^2 + h_{-1}^2\right) + \frac{2\sigma_n^2}{\mathbb{E}\{a_k^2\}}} \qquad (4)$$

For the independent, equiprobable PAM-4 data with symbols as $a_k = \{\frac{-3}{\sqrt{5}}, \frac{-1}{\sqrt{5}}, \frac{1}{\sqrt{5}}, \frac{3}{\sqrt{5}}\}$ and zero input noise ($\sigma_n = 0$), σ_L can be expressed as:

$$= \sqrt{\cdots + 2h_{-3}^2 + 2h_{-2}^2 + 1.64h_{-1}^2 + 1.64h_1^2 + 2h_2^2 + 2h_3^2, \cdots} \qquad (5)$$

The gain, output standard deviation, and the resulting KNR_L are verified with the system model in Fig. 1. With a 29.82-*dB*-loss channel shown in Fig. 2, the CTLE is set to provide a boost of 14 *dB* at the Nyquist frequency, and, as will be explained in Section III, a 5-tap FFE is adopted in the timing recovery path to maximize the resulting *KNR*. For the
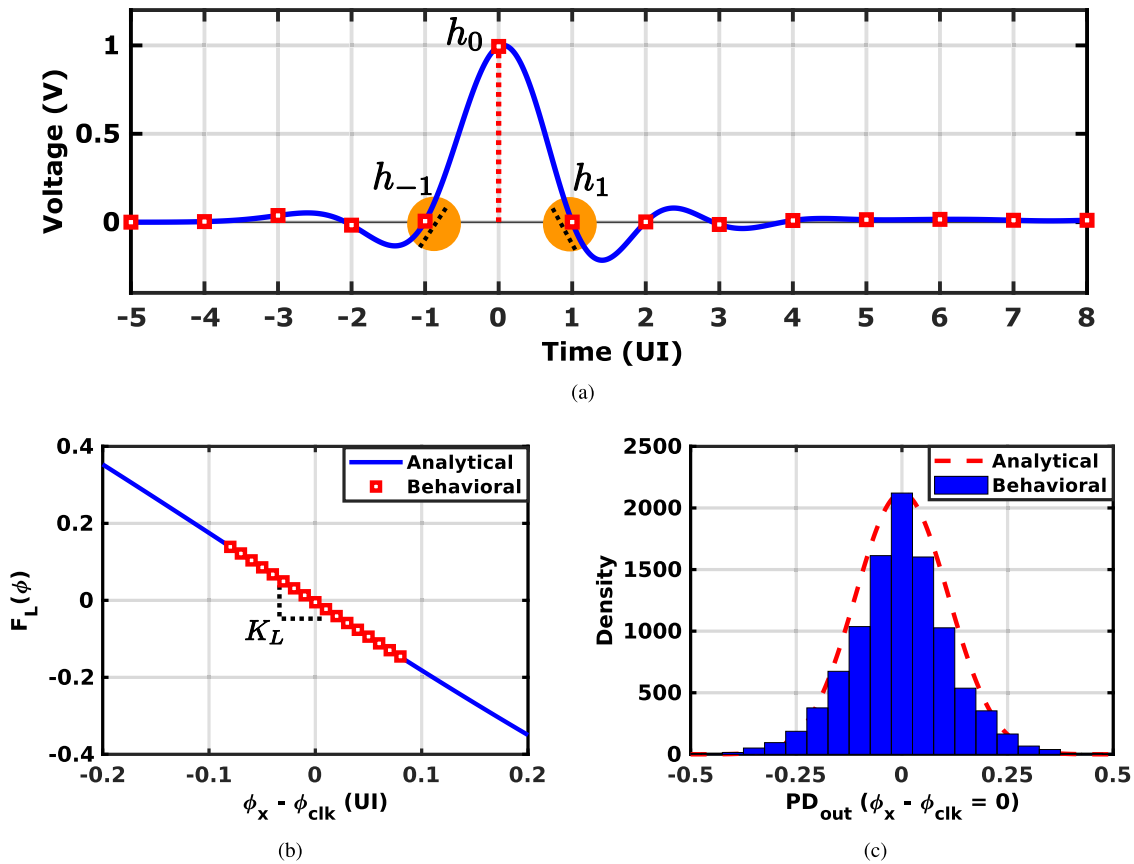
(a)

(b)

(c)

FIGURE 3. (a) Pulse response example. The highlighted area illustrates the slope measurement at the first pre and post-cursor to evaluate phase detector gain. (b) Analytical and behavioral results of the linear MMPD timing function (F_L) for the pulse response presented in (a). (c) MMPD output distribution at phase $\phi_x - \phi_{clk} = 0$ (lock position).

TABLE 1. Linear MMPD analytical and behavioural results.

Parameters	Analytical results	Behavioural results
K_L	0.285	0.286
σ_L	0.110	0.115
KNR_L	2.57	2.48

described equalization settings, the resultant pulse response at the input of MMPD is shown in Fig. 3(a). Table 1 and Fig. 3 (b) and (c) demonstrate that the behavioral results accurately match the analytical findings.

B. SIGNED MMPD

The signed MMPD is a nonlinear phase detector that takes the sign of MMPD output and provides only early or late information, as shown in Fig. 4. The key advantage of signed MMPD over the linear version is that the limited number of phase detector outcomes ($s = \{1, -1\}$) simplifies the digital implementation of the subsequent CDR loop. In comparison to linear MMPD, the signed MMPD has a higher gain; however, the variance of phase detector output is also high.

To evaluate the signed MMPD's performance, we need to consider the distribution of the intermediate node l, the linear version's output, as shown in Fig. 5(a). Due to ISI and noise, l may not always be positive with $\phi < 0$, and vice versa. In fact, the distribution of l at sampling phase
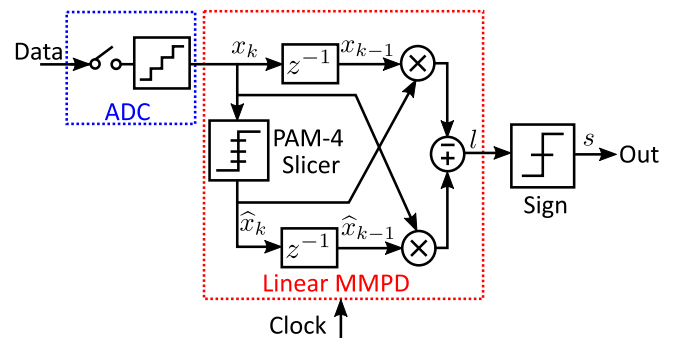

FIGURE 4. Signed Mueller–Muller phase detector architecture.

ϕ exhibits a mean value $\mu_l(\phi)$ and a standard deviation of $\sigma_l(\phi)$. This results in a smoothening effect on the signed MMPD's timing function, F_S [17], [20], and the average output of the signed MMPD can be written as:

$$s = (1) \cdot P_r(l > 0|\phi) + (-1) \cdot P_r(l < 0|\phi) \qquad (6)$$

as illustrated by the shaded area for three different sampling phases in Fig. 5 (b)-(d). If we further assume that the distribution of l to be Gaussian with the standard deviation given by Eq. (4), the signed MMPD's timing function F_S can be
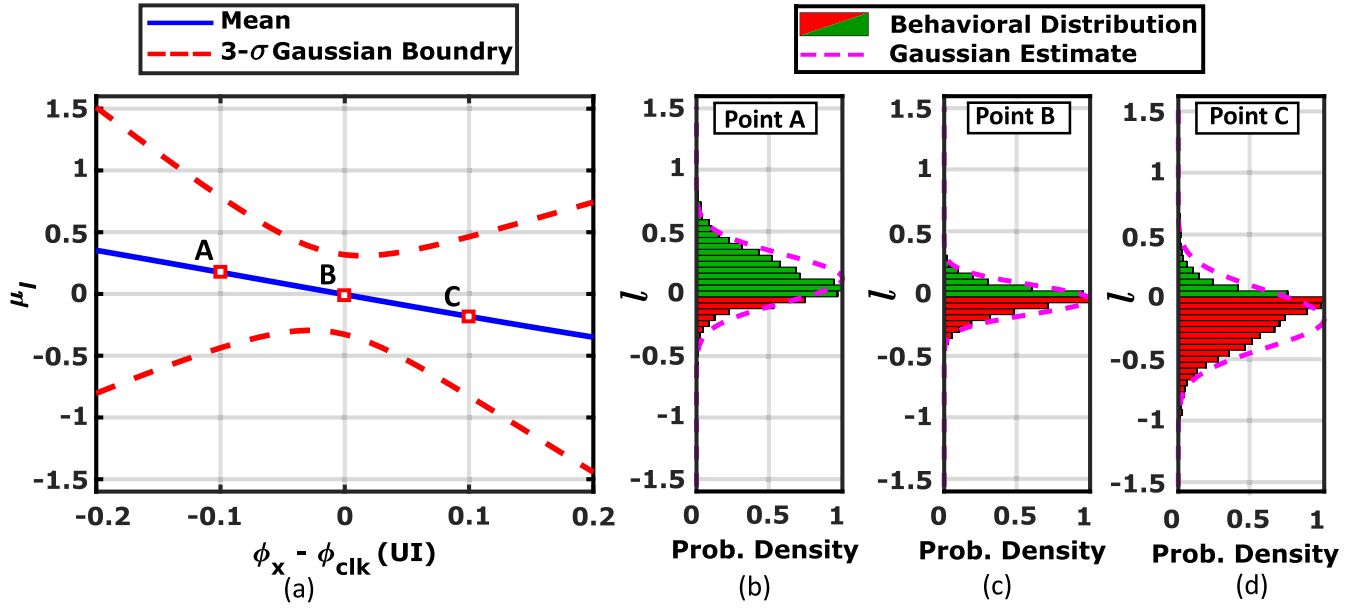
FIGURE 5. (a) Output at SMMPD intermediate node l versus phase error. (b) Behavioral distribution and Gaussian estimate at node l for phase error ($\phi_x - \phi_{clk}$) -0.1 UI (Point A in (a)). (c) Distribution and Gaussian estimate at phase error 0 (Point B in (a)). (d) Distribution and Gaussian estimate at phase error 0.1 UI (Point C in (a)).

TABLE 2. Signed MMPD analytical and behavioural results.

Parameters	Analytical results	Behavioural results
K_S	2	1.95
σ_S	1	1
KNR_S	2	1.95

calculated as:

$$F_S(\phi) = 2Q\left(\frac{0 - \mu_l(\phi)}{\sigma_l(\phi)}\right) \qquad (7)$$

While most distribution is non-Gaussian, as shown with the sampling phases of ± 0.1 UI in Fig. 5 (b) and (d), Eq. (7) provides a decent estimate without much error when the distribution is unknown. The gain of the signed MMPD at the locking phase can, therefore, be expressed as

$$K_S = \sqrt{\frac{2}{\pi}} \cdot \frac{K_L(0)}{\sigma_l(0)} = \sqrt{\frac{2}{\pi}} \cdot KNR_L(0), \qquad (8)$$

with the derivation provided in Appendix. Because of the binary output, the phase detector output standard deviation at the locking phase is 1, making KNR_S equal to the phase detector gain K_S. Therefore, the KNR_S is 0.79 times smaller than KNR_L. Although the signed output greatly reduces the hardware cost of the following digital CDR implementation, designers need to be aware of the lower KNR_S and resulting poorer jitter tolerance when choosing between linear and signed MMPD.

This analytical model is verified using the same behavioral model and equalization setting as the linear version in Fig. 3. As shown in Table 2 and Fig. 6, our analysis provides an accurate model for the operation of signed MMPD.
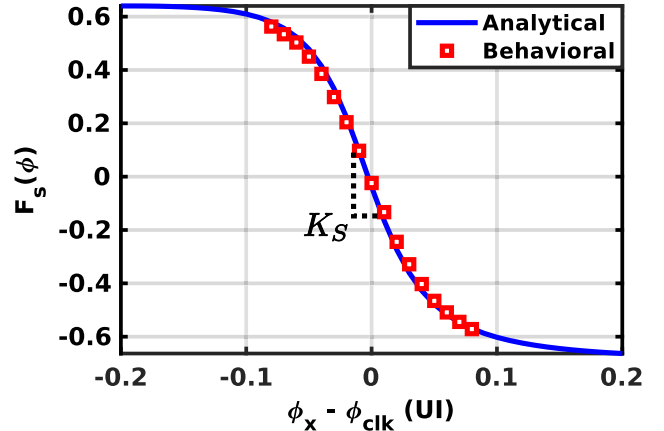

FIGURE 6. Analytical and behavioral results of the signed MMPD timing function $F_S(\phi)$.

III. DESIGN CONSIDERATIONS OF AFE FOR HIGHER PHASE DETECTOR *KNR*

As mentioned in the previous section, it is desirable to have a phase detector with high gain and low output noise (i.e., high *KNR*), enabling low input-referred noise, which increases the CDR jitter tolerance at high frequencies. Fig. 7 shows the analytical JTOL curves for two link equalization configuration cases which provide the phase detector *KNR* of 2.57 and 0.6, while all the other timing recovery settings are the same. The results demonstrate the advantage of a higher phase detector *KNR*. The MMPD CDR with the phase detector *KNR* of 2.57 has twice the jitter tolerance compared to the phase detector with a *KNR* of 0.6.

As the AFE equalization shapes the pulse response and noise at the input of the phase detector, it has a direct impact
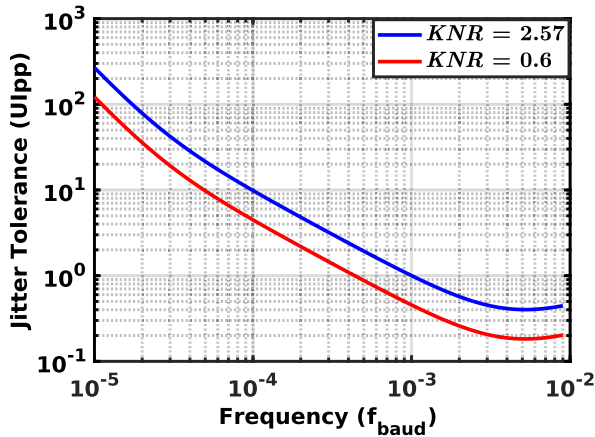
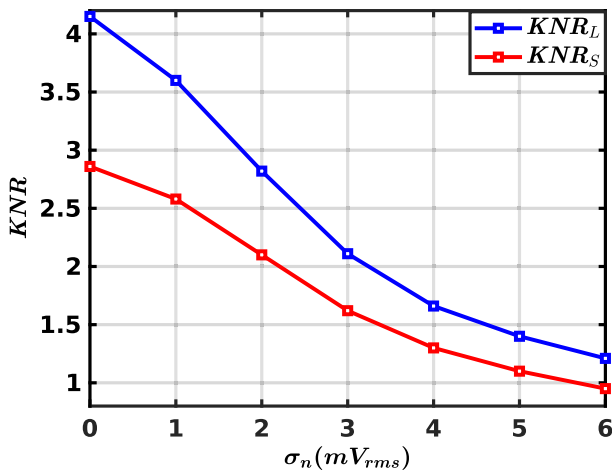FIGURE 7. Jitter tolerance curve of MMPD CDR for *KNR* = 2.57 and 0.6.

FIGURE 9. *KNR* of linear and signed MMPD for different number of taps in timing path FFE.

FIGURE 8. *KNR* of linear and signed MMPD for different AFE input-referred noise (σ_n).

proportional to σ_{PD}, and from (4), σ_{PD} of a linear MMPD (σ_L) is a function of σ_n. As KNR_S is directly proportional to KNR_L from (8), KNR_S also drops with an increase in AFE input-referred noise.

B. PHASE DETECTOR KNR VS. FFE EQUALIZATION

In our system model in Fig. 1, a short FFE is adopted in the timing recovery path to supplement the CTLE in shaping the pulse response and noise before forwarding it to the phase detector. In our analysis to determine the FFE equalization impact, a 2-mV$_{rms}$ input-referred AFE noise (σ_n) is added to channel output, and the CTLE is set to provide a boost of 16 dB. Here, we analyze the impact of FFE equalization by increasing the number of FFE taps from 3 to 8, and the tap coefficients are evaluated using the MMSE algorithm.

As shown in Fig. 9, we observe that both KNR_L and KNR_S increase with the inclusion of FFE in the timing path and the increase in the number of FFE taps. This increase in *KNR* can be attributed to the decrease in ISI with an increase in FFE taps. We also notice that the *KNR* curves flatten out after six FFE taps, which can be explained by the fact that the ISI becomes insignificant for this equalized pulse response after six taps.

One thing to notice is that, as each additional tap decreases the ISI, it also adds the latency in the CDR loop, which is not desirable and will be discussed in details in Section IV. Designers need to strike a balance between ISI and latency while selecting the number of taps. For the mentioned channel loss and CTLE configuration, a 5-Tap FFE seems to be the suitable choice.

C. PHASE DETECTOR KNR VS. FFE TAP COEFFICIENT VALUE

So far, we have set the FFE tap coefficients using the MMSE algorithm in the previous subsections. The MMSE algorithm works on the principle of maximizing the *SNR* when evaluating the tap coefficients [19], [21]. However, the maximum *SNR* does not necessarily guarantee the maximum *KNR*.

on *KNR*. In the following subsections, we will discuss different equalization options and evaluate their impact on phase detector performance by the resulting *KNR*. For the analysis, we have employed the wireline receiver model presented in Fig. 1 and the channel in Fig. 2. Furthermore, the swing at Tx driver output is held constant at 800 mV_{pp}.

A. PHASE DETECTOR KNR VS. AFE INPUT-REFERRED NOISE (σ_n)

This subsection analyzes the impact of AFE input-referred noise on MMPD *KNR*. To quantify the impact, the noise injected at channel output of Fig. 1 is increased from 0 to 6 mV$_{rms}$ in steps of 1 mV$_{rms}$. The noisy channel output is equalized initially by the CTLE and then by the 5-tap FFE in the timing recovery path. The CTLE is set to provide a boost of 16 dB that maximizes *KNR* and will be discussed later in Section III-D. The FFE tap coefficients are evaluated using the minimum mean square error (MMSE) algorithm.

As shown in Fig. 8, we observe that linear and signed MMPD *KNR* drops with an increase in σ_n. This observation aligns with analytical results. From (1), KNR_L is inversely
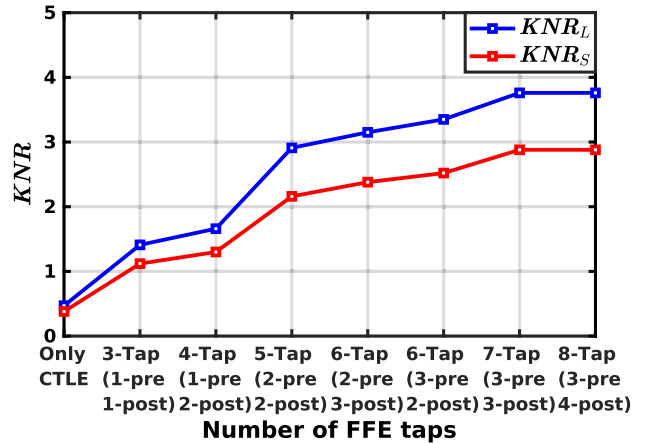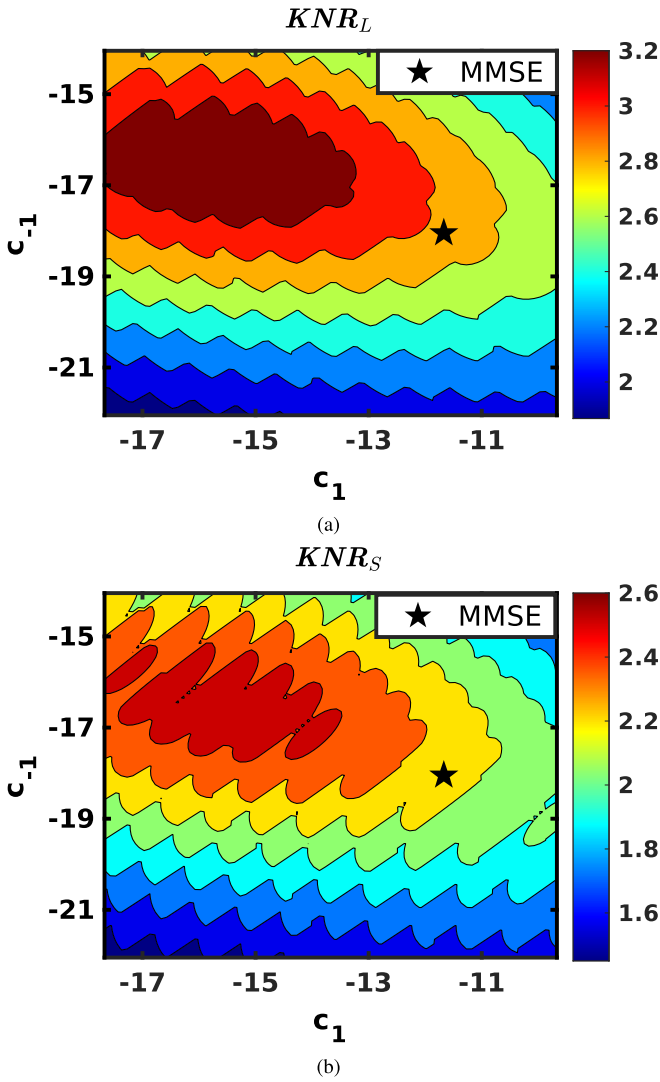
(a)

(b)

FIGURE 10. (a) Contour plot of *KNR* for the linear MMPD for the different sets of first pre-cursor (c_{-1}) and first post-cursor (c_1) tap coefficient value of a 5-tap timing path FFE. (b) Signed MMPD *KNR* contour plot.

To determine the tap coefficients that maximize *KNR*, we sweep the tap values of the 5-tap FFE in the timing path of our system model with a 2-mV$_{rms}$ input-referred AFE noise and a 16-*dB* boost from CTLE.

As shown with the contour plots in Fig. 10, where the coefficients for the first pre-cursor (c_{-1}) and the first post-cursor (c_1) are swept, we observe that a higher *KNR* can be achieved using FFE tap coefficients different from what was obtained with MMSE algorithm.

This is because, when it comes to maximizing *KNR* for the timing recovery, while the *SNR* at the sampling phase is an important factor, K_{PD} and σ_{PD} further depend upon the pulse shape. The specific slope at the lock point, as shown in Fig. 3, translates the voltage error into a timing error. With the optimal FFE coefficient setting, although the *SNR* is slightly lower, the K_{PD} and the resulting *KNR* are higher.

Also, we observe that the *KNR* contour plot of the signed MMPD has ripples. This is expected as the signed MMPD
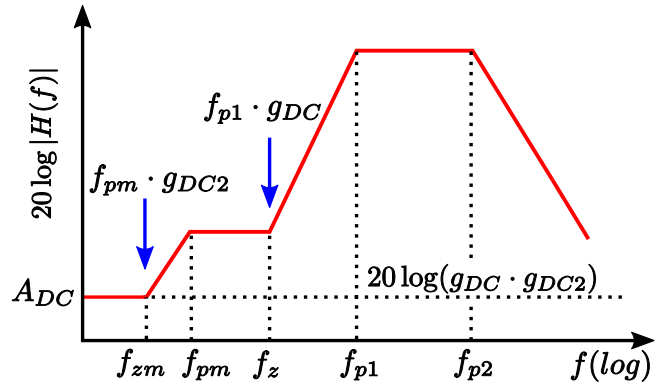

FIGURE 11. Conceptual Bode plot of CTLE with mid-band shaping.

gain depends upon the distribution at the intermediate node *l*, which is a function of phase, as demonstrated in Fig. 5. The complex phase and output distribution dependency changes with each FFE tap coefficient value, leading to ripples in the signed *KNR* contour plot.

D. PHASE DETECTOR KNR VS. CTLE EQUALIZATION

CTLE is a critical block in wireline receivers. It reshapes the pulse response and impacts both the data path and timing recovery path performance. In this subsection, we focus on the timing recovery path by evaluating the effect of CTLE equalization on the phase detector's *KNR*.

In this analysis, a 2 mV$_{rms}$ noise is added to the channel output, and a 5-tap FFE in the timing recovery path supplements the CTLE in shaping the pulse response. Further, for each CTLE boost setting, the FFE tap coefficients are adjusted accordingly to maximize *KNR*.

Equation (9) depicts the transfer function of a 2-stage CTLE with mid-band shaping used in this analysis, and Fig. 11 presents the conceptual Bode plot [22].

$$H_{CTLE}(f) = \frac{g_{DC} \cdot g_{DC2}\left(1 + j\frac{f}{f_z}\right)\left(1 + j\frac{f}{f_{zm}}\right)}{\left(1 + j\frac{f}{f_{p1}}\right)\left(1 + j\frac{f}{f_{p2}}\right)\left(1 + j\frac{f}{f_{pm}}\right)} \quad (9)$$

The high-frequency zero f_z is set to $f_{p1} \cdot g_{DC}$, and the low-frequency zero f_{zm} is set to $f_{pm} \cdot g_{DC2}$ in (9). As we scale g_{DC} and g_{DC2}, both the DC gain and the zero frequencies are adjusted, changing the resulting gain boosting, as shown in Fig. 11. The CTLE parameter values and sweep range are provided in Table 3. In our analysis, the CTLE gain boosting is changed from 1 dB to 23 dB, as shown in Fig. 12, and the resulting KNR_L and KNR_S are shown in Fig. 13.

From analysis, we observe that neither high nor low CTLE boosting is suitable for high MMPD *KNR*. With low boost settings, we have a long residual ISI tail, whereas, with high boost settings, we have undershoots, which increase the first few pre- and post-cursors. For the 28.9-dB-loss channel from Fig. 2, the optimal CTLE setting provides a 3-dB mid-band shaping and another 16-dB peaking at the Nyquist frequency, as shown in Fig. 13.

TABLE 3. CTLE parameters and range.

CTLE Parameter	Symbol	Min.	Typ.	Max.
Signaling Rate (Gbaud/s)	f_{baud}		56	
DC Gain2 (dB)	g_{DC2}	-6		0
Low-Frequency Zero	f_{zm}		$(f_{baud}/80) \cdot g_{DC2}$	
Low-Frequency Pole	f_{pm}		$f_{baud}/80$	
DC Gain (dB)	g_{DC}	-20		-2
Zero Frequency	f_z		$(f_{baud}/2.5) \cdot g_{DC}$	
Pole Frequencies	f_{p1}		$f_{baud}/2.5$	
	f_{p2}		f_{baud}	
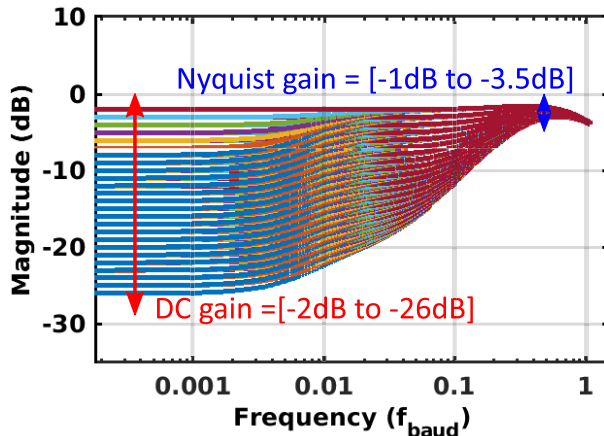
FIGURE 12. CTLE frequency response for different boost settings. The boost is changed from 1 dB to 23 dB.

FIGURE 13. (a) Linear MMPD *KNR* contour plot for different CTLE boost settings. (b) Signed MMPD *KNR* contour plot. A 5-tap timing recovery path FFE is used in conjunction with CTLE to maximize *KNR*.

Fig. 14 shows the pulse response at the outputs of CTLE and the 5-tap FFE in the timing recovery path with the equalization setting that maximizes *KNR* ($KNR_L = 3.4$ and $KNR_S = 2.6$). We notice that CTLE and FFE work in different ways to maximize *KNR*. While CTLE reduces ISI and improves *SNR*, the output pulse response is smooth with low K_{PD}. It is the following FFE that provides a stronger shaping effect, leading to higher K_{PD} and the resulting *KNR*.

IV. EFFECT OF LATENCY ON MMPD CDR LOOP DYNAMICS

Although the ADC-DSP-based receiver enables sophisticated equalization, it also makes the broadband timing recovery challenging.

With digital CDR, the input data is processed in parallel with time interleaving due to the low operating speed of digital circuits compared to the baud rate. This time interleaving introduces a latency of many UI's [23], [24] between sampling the CTLE output and recovering the clock, limiting the CDR jitter tracking bandwidth.

Impact of CDR loop latency has been studied for the PAM-2 transceivers with bang-bang phase detectors [24], [25], [26], [27]. This section explores the effect of loop latency on MMPD CDR for ADC-DSP-based receivers, in which the latency is much more severe than the AMS receivers. This is due to the equalization in the DSP domain, leading to hundreds of UI's latency and adversely affecting the CDR performance. In this section, the behavioral simulations are carried out with linear MMPD CDR. Nevertheless,
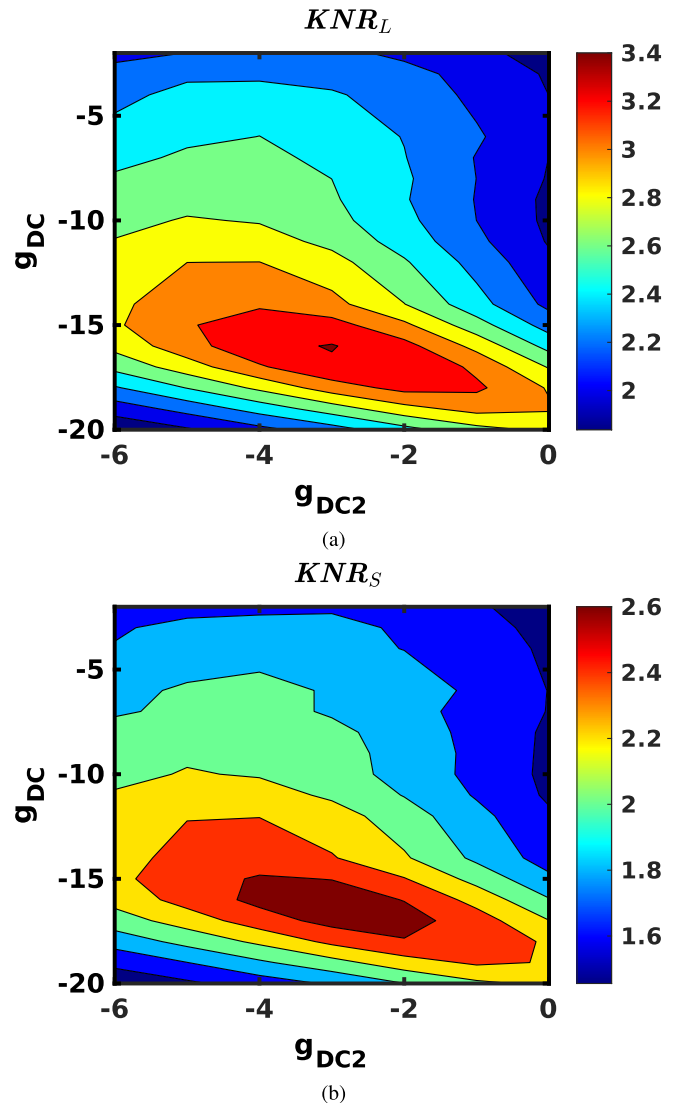
the analysis is also valid for signed MMPD CDR. Fig. 15 presents the linearized MMPD CDR model used to analyze loop latency impact on jitter tracking performance. The z-domain open-loop transfer function of the model can be expressed as:

$$G(z) = K_{PD}\left(K_P + \frac{K_I}{1 - z^{-1}}\right)\left(\frac{K_{DPC}}{1 - z^{-1}}\right)\left(z^{-D}\right) \quad (10)$$

Four main parameters influence the open-loop transfer function: 1) two integrations, one from the phase rotator and the other from the integral path, which shapes the amplitude response to $1/s^2$ and adds a $-180°$ phase shift; 2) the loop gain $K_{PD} \cdot K_P \cdot K_{DPC}$, which moves the amplitude vertically; 3) left-half plane zero K_I/K_P, which improves the phase margin at high frequency; 4) loop delay (D), which results in phase delay proportional to the frequency and leads to the bending of the phase response downwards.
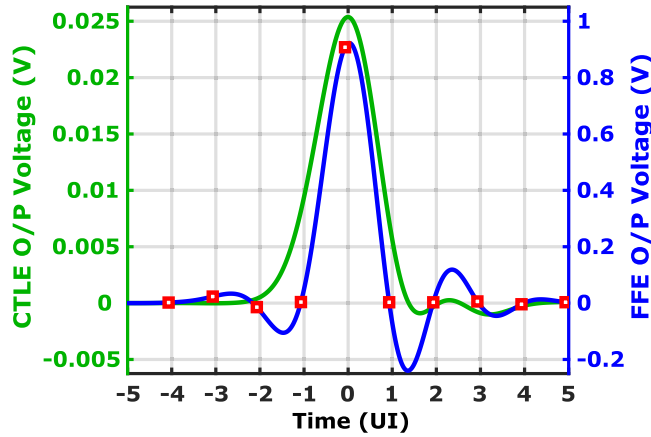
FIGURE 14. Pulse response at the CTLE and FFE output for maximum *KNR* setting. The square box is the locking position of the recovered clock.
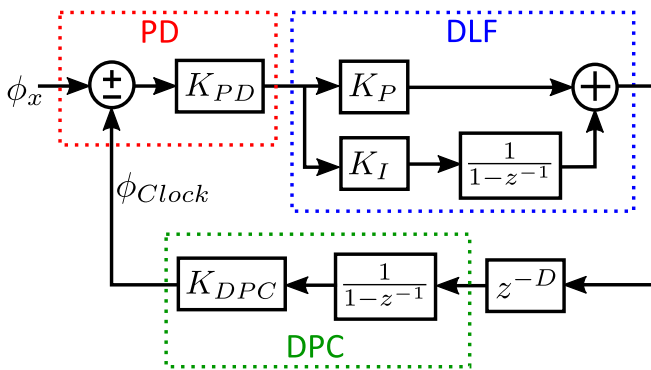

FIGURE 15. The z-domain linearized model of CDR.

TABLE 4. CDR parameters and values.

Parameters	Case (a)	Case (b)	Case (c)	Case (d)
f_{baud} (GBd/s)	56	56	56	56
3-dB Bandwidth	$f_{baud}/560$	$f_{baud}/560$	$f_{baud}/560$	$f_{baud}/5600$
K_{PD} $(radian^{-1})$	0.151	0.151	0.151	0.151
K_P	11.7e-3	11.7e-3	11.7e-3	1.17e-3
K_I	1.91e-6	1.91e-6	1.91e-6	1.91e-8
K_{DPC}	2π	2π	2π	2π
D (UI)	32	64	128	512
Simulated Bandwidth	$f_{baud}/330$	$f_{baud}/239$	$f_{baud}/239$	$f_{baud}/2400$

The latency impact analysis is carried out for four different cases. For cases (a) to (c), CDR loop bandwidth is set to $f_{baud}/560$ using the parameter values listed in Table 4, and three different loop latency of 32, 64, and 128 UI are considered. The parameter K_P and K_I values are selected so there is no in-band peaking for the chosen bandwidth with zero loop latency. In case (d), we lower the CDR bandwidth to $f_{baud}/5600$ by scaling the proportional (K_P) and integral path (K_I) gain while keeping a constant damping ratio.

As shown with the open-loop transfer functions in Fig. 16, for the cases with loop bandwidth of $f_{baud}/560$, the larger the loop latency D is, the earlier the phase bent occurs. As a
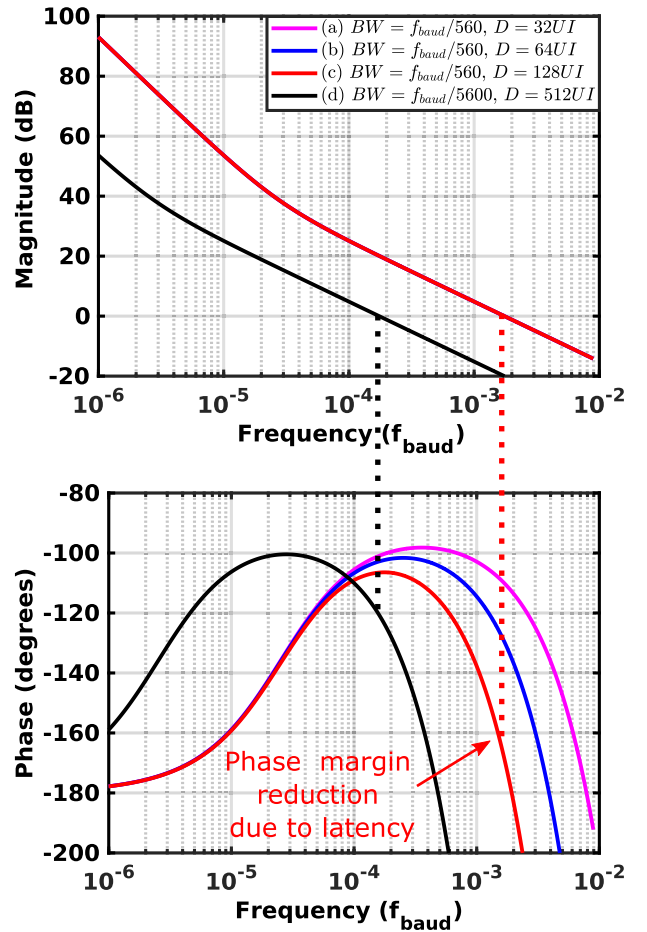

FIGURE 16. Magnitude and phase plot of CDR open-loop transfer function. For cases (a) to (c), the loop bandwidth is set to $f_{baud}/560$, and the latency of 32, 64, and 128 UI is considered. For case (d), the bandwidth is lowered to $f_{baud}/5600$, and loop latency of 512 UI is considered.

result, as D increases, the phase margin reduces. On the other hand, CDR with the lower loop bandwidth of $f_{baud}/5600$ in case (d) has a considerable phase margin for the increased loop delay of 512 UI.

The phase margin degradation due to latency introduces peaking in the jitter transfer function, as shown in Fig. 17. This peaking marginally increases the CDR loop bandwidth, as observed from the simulated bandwidth in Table 4. However, this peaking also degrades the high-frequency jitter tolerance performance, as shown in Fig. 18.

The loop latency also makes the CDR more sensitive to gain variations, as shown with the dashed lines in Fig. 17. For a ±10% variation in K_{PD}, the in-band peaking varies by 9% for case (a) with 32-UI loop latency and 47% for case (b) with 64-UI loop latency. The CDR becomes unstable for the 128-UI loop latency case with a ±10% variation in K_{PD}.

The analytical results with the linear model are verified with behavioral simulations with the system model in Fig. 1. At Tx, an input sinusoidal jitter of 0.1-UI$_{pp}$ amplitude is injected at different frequencies. The resulting jitter transfer performance is shown in Fig. 17, confirming the peaking for loop latency of 64 UI and above for the loop bandwidth
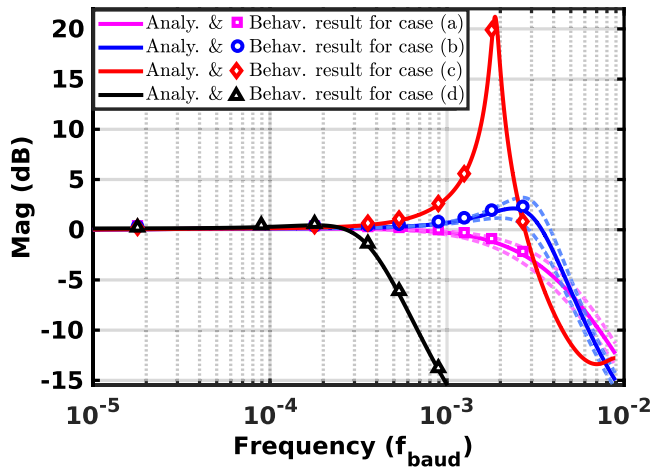
FIGURE 17. Analytical and behavioral jitter transfer curves for the different bandwidth and loop latency cases. The dashed traces highlight the variation in the transfer curves with ±10% variation in K_{PD}.
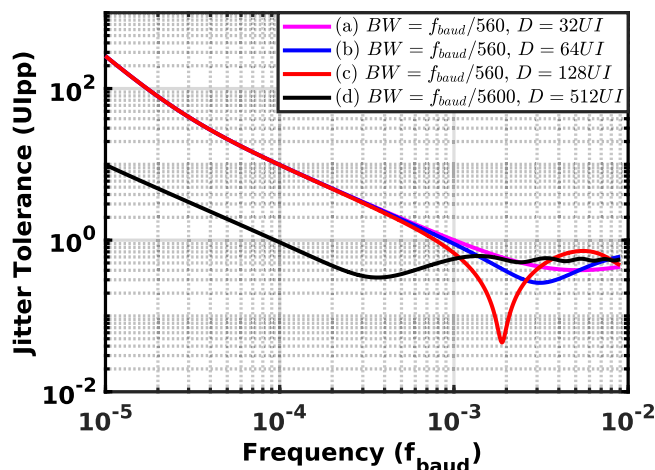

FIGURE 18. Jitter tolerance curve of MMPD CDR for the different bandwidth and loop latency cases. Case (c) highlights the impact of loop latency on jitter tolerance at high CDR loop bandwidth.

of $f_{baud}/560$. In case (d), there is no peaking in the jitter transfer function due to ample phase margin, enabling higher jitter tolerance at high frequencies.

The analysis is extended to reveal how CDR bandwidth choice and the loop latency impact the jitter transfer peaking, as shown in Fig. 19. While lower bandwidth and latency at the lower-left corner of the figure show little to no peaking, the results clearly demonstrate that, with lower bandwidth settings, higher latency can be tolerated as less peaking is incurred. As the bandwidth increases from $f_{baud}/1000$ to $f_{baud}/300$, the maximum latency for $\sim$ 1-dB peaking reduces from 256 down to 96 UI. For high CDR loop bandwidth, the rapid increase in peaking eventually renders the CDR loop unstable even with low latency.

V. CONCLUSION
We have analyzed the loop dynamics of the MMPD-based timing recovery and factors impacting its performance for
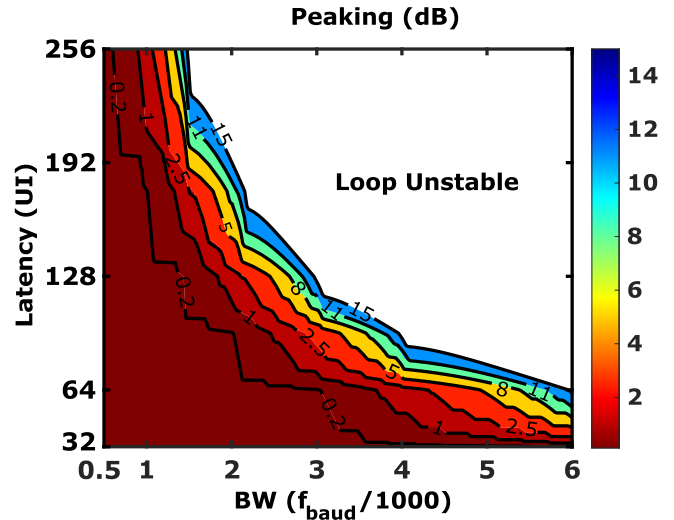

FIGURE 19. CDR jitter transfer peaking vs. latency and 3-dB simulated bandwidth.

ADC-based PAM-4 receivers. We first formulated the accurate linear model of linear and signed MMPDs, providing a framework for performance analysis, which are further confirmed with behavioral simulation results.

Using the figure of merit *KNR*, we evaluated different AFE equalization options by considering the impact of AFE input-referred noise, timing recovery path FFE equalization, and CTLE equalization. The results confirm that the low input noise and custom equalization of CTLE and timing-path FFE are required. Furthermore, the great shaping ability from the timing-path FFE helps to maximize *KNR* while the designers need to consider the loop latency when choosing the number of taps. Our analysis further demonstrated that evaluating the FFE tap coefficient values using the MMSE algorithm does not provide the best results from the phase detector performance perspective.

We then analyzed how the CDR loop latency impacts the jitter transfer peaking and eventually limits the achievable CDR loop bandwidth in ADC-DSP-based receivers.

Finally, we conclude that, to achieve high loop bandwidth in MMPD-based CDR with good jitter tolerance, the *KNR* should be maximized, and the loop latency should be minimized.

APPENDIX
As we noted, the output l and s of Fig. 5 are random processes whose statistics depend upon the phase difference (ϕ) between the input data (ϕ_x) and the recovery clock (ϕ_{clock}).

Let $C(\phi, x)$ be the cumulative distribution function (CDF) of random variable l.

$$C(\phi, x) = P_r(l(\phi) < x) \qquad (11)$$

As mentioned in (6), the average output of signed MMPD at phase ϕ can be evaluated by:

$$s(\phi) = 1 \cdot P_r(early|\phi) + -1 \cdot P_r(late|\phi)$$
$$= 1 \cdot P_r(sign(l) > 0) + -1 \cdot P_r(sign(l) < 0) \quad (12)$$

If we assume the distribution at l to be Gaussian, then (12) can be evaluated as:

$$s(\phi) = 2 \cdot Q(\phi, 0) - 1 \quad (13)$$

Since $Q(x) = 1 - C(x)$, therefore (13) can be expressed as:

$$s(\phi) = 1 - 2 \cdot C(\phi, 0) \quad (14)$$

The phase detector gain can be derived by differentiating (14) with respect to ϕ

$$K_S = \left.\frac{ds}{d\phi}\right|_{\phi=0}$$
$$= \left.\frac{d(1 - 2C(\phi, 0))}{d\phi}\right|_{\phi=0}$$
$$= -2 \cdot C'(0, 0) \cdot K_L(0) \quad (15)$$

As we have assumed the distribution at l to be Gaussian, therefore:

$$C'(0, 0) = \frac{1}{\sigma_l(0) \cdot \sqrt{2\pi}} \quad (16)$$

putting the value of C'(0,0) from (16) to (15) we have

$$K_S = \frac{\sqrt{2}}{\sigma_l(0) \cdot \sqrt{\pi}} \cdot K_L(0) \quad (17)$$

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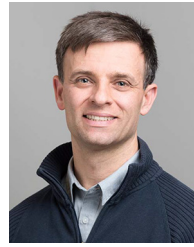
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