IEEE Open Journal of
Circuits and Systems

Received 11 March 2022; revised 8 May 2022; accepted 23 May 2022. Date of current version 20 September 2022.

Digital Object Identifier 10.1109/OJCAS.2022.3179046

SEKV-E: Parameter Extractor of Simplified EKV *I-V* Model for Low-Power Analog Circuits

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This article was recommended by Associate Editor M. Ballini.

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This work was supported by the European Union's Horizon 2020 Research and Innovation Program (SEQUENCE) under Grant 871764.

ABSTRACT This paper presents the open-source Python-based parameter extractor (SEKV-E) for the simplified EKV (sEKV) model, which enables the modern low-power circuit designs with the inversion coefficient design methodology. The tool extracts the essential sEKV parameters automatically from the given *I-V* curves using the direct extraction and the multi-stage optimization process. It also handles the overfitting issue because of non-linear least squares. Moreover, this work demonstrates the SEKV-E as a universal tool by widely applying it to different silicon technologies, temperatures, dimensions, and back-gate voltages.

INDEX TERMS Bulk MOSFET, charge-based model, cryogenic, FDSOI, FinFET, inversion coefficient, IC design, low power, simplified EKV.

I. INTRODUCTION

As THE metal-oxide-semiconductor field-effect transistors (MOSFETs) are down-sized to the nanometer scale, the quadratic function is not sufficient anymore. On the contrary, the compact models such as BSIM family [1] and Leti-UTSOI [2], [3] become much more complicated to meet the need of the extremely down-scaled CMOS technologies, where hundreds of physical and empirical parameters are needed. This model complexity challenges the analog IC designers to find the right tradeoff for sizing the transistors and setting the bias currents for achieving a given specification. The simplified charge-based EKV model (sEKV) has very few parameters that can truly help designing analog ICs in advanced technologies. Besides, instead of using the overdrive voltage to decide the operating bias, the inversion coefficient (*IC*) design methodology [4], [5] can span the operating point from weak (WI), moderate (MI) to strong inversion (SI), continuously. Therefore, sEKV offers a powerful feature for low-power circuit designs, in which a transistor operating point is often pushed closer to MI. However, the essential sEKV parameters related to technology node, device dimensions, materials, etc., are not available directly from the PDK and need to be extracted either from measured data or data generated from the PDK. In the past, the parameters are extracted manually either from the measurement or PDK [6], which ends up with a time-consuming engineering process. Hence, this paper presents an open-source Python-based parameter extractor [7], namely sEKV-E, which automatically and efficiently obtains the parameters from given *I-V* curves.

II. THE SIMPLIFIED EKV MODEL

In the sEKV model, the transfer characteristic I_D-V_G of a MOSFET in saturation is given by [8]

$$\frac{V_G - V_{T0} - nV_S}{nU_T} = 2q_s + \ln q_s \tag{1a}$$

$$q_s = \frac{\sqrt{4IC + (1 + \lambda_c IC)^2} - 1}{2}, \tag{1b}$$

where V_{T0} is the threshold voltage without short-channel effects, V_S is the source-to-bulk voltage ($V_S = 0\,\mathrm{V}$ for the rest derivation), $U_T = k_B T/e$ is the thermal voltage with the Boltzmann constant k_B and the elementary charge e, and q_s is the normalized inversion charge at the source. The term of q_s can be expressed by the inversion coefficient (*IC*) and a parameter λ_c accounting for the velocity saturation (VS). $IC = I_D/I_{spec}$ is a measure of the inversion level (WI: $IC \leq 0.1$, MI: $0.1 < IC \leq 1$, and SI: $1 < IC$), where

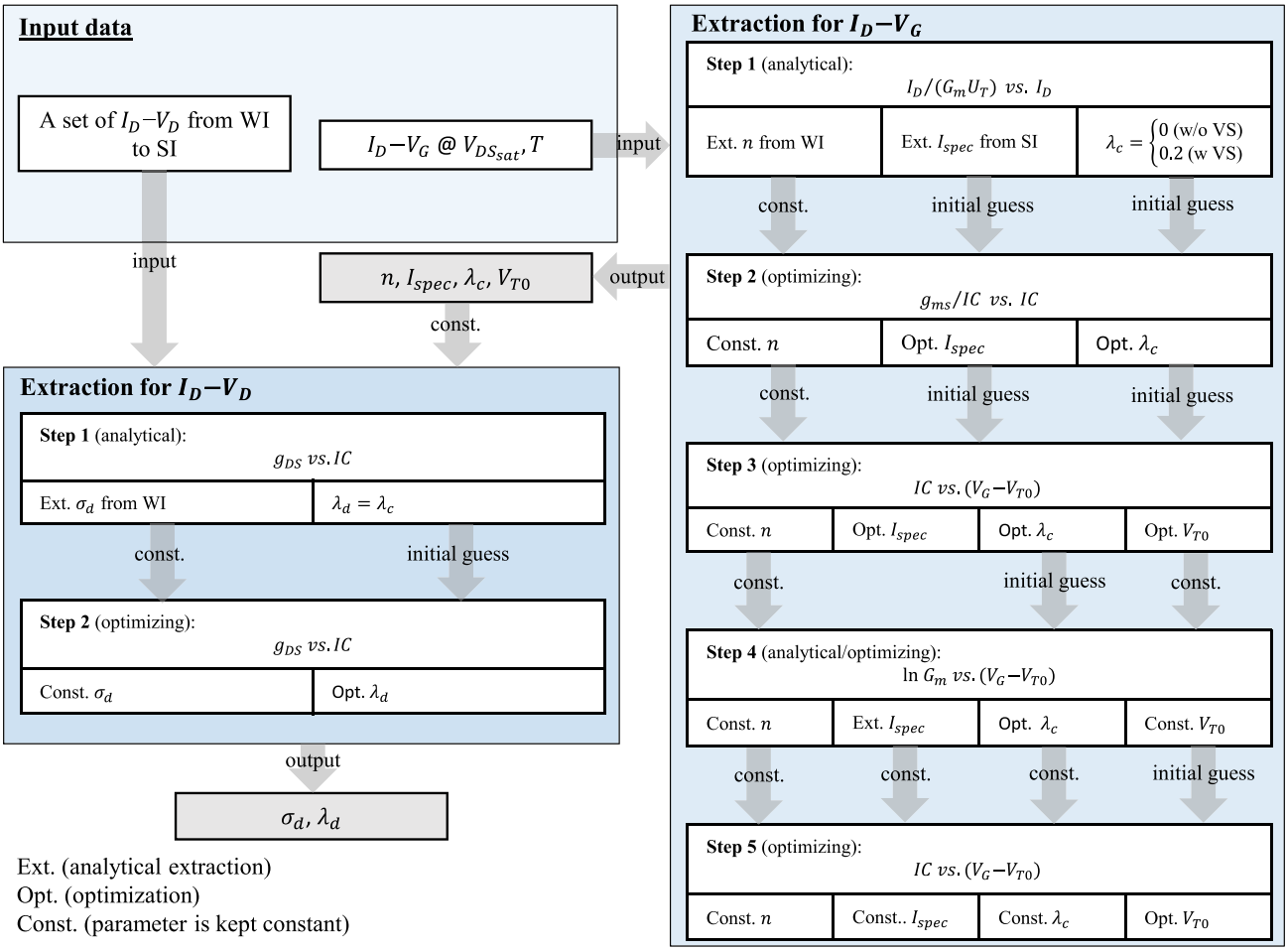

FIGURE 1. The workflow of the automated extraction tool for simplified EKV parameters. The extraction starts from *Input data*, *Extraction for* I_D-V_G, and finally *Extraction for* I_D-V_D. The parameters passed from one block to another either be kept constant or be the initial guess for the optimizer. The grey blocks highlight the outputted parameters.

$I_{spec} = 2n\mu_0 C_{ox} U_T^2 W/L = I_{spec\square} W/L$ is the specific current with the slope factor n, low-field mobility μ_0, the oxide capacitance C_{ox}, and device width W and length L. Thanks to the log-linear inversion-charge relation [9], the model has continuity from the subthreshold to the region above V_{T0}. From (1) we see that only four parameters (n, I_{spec}, V_{T0}, λ_c) are required to describe I_D-V_G from WI to SI continuously.

On the other hand, the output characteristic I_D-V_D in saturation is described by the first-order approximation ($I_D \approx G_{DS}(V_D + V_M)$) with the Early voltage V_M. When a down-sized transistor suffers from the drain-induced barrier lowering (DIBL) effect, the output conductance G_{DS} can be derived using the chain rule as [10]

$$G_{DS} \triangleq \frac{\partial I_D}{\partial V_D} = \frac{\partial I_D}{\partial V_T}\frac{\partial V_T}{\partial V_{DS}} = (-G_m)(-\sigma_d), \tag{2}$$

where $V_T = V_{T0} - \sigma_d V_{DS}$ includes a first-order model of DIBL. The link between G_{DS} and transconductance G_m is built in (2), therefore G_{DS} can be rewritten by expanding G_m as

$$g_{DS} = \frac{G_{DS}}{G_{spec}} = \frac{\sigma_d}{n}\frac{\sqrt{(\lambda_d IC + 1)^2 + 4IC} - 1}{\lambda_d(\lambda_d IC + 1) + 2} \tag{3}$$

with $G_{spec} = I_{spec}/U_T$. It should be noted that theoretically, λ_d is equal to λ_c. However, they are extracted separately from the output and transfer characteristics, λ_c is slightly larger than λ_d since the extraction of λ_c is influenced by the mobility degradation due to vertical field. Nevertheless, in sEKV, the first-order estimation on G_{DS} for short devices having the DIBL effect requires only two parameters, σ_d and λ_d.

III. EXTRACTION METHODOLOGY

Fig. 1 presents the extraction flow of the SEKV-E, which takes the single I_D-V_G at saturated V_{DS} ($V_{DS_{sat}}$) and a set of I_D-V_D from WI to SI as the input, and outputs the sEKV parameters for a device with the dimension W/L and at the certain T and back-gate/body voltage. The concept of the parameter extraction methodology is (i) using the direct extraction to generate initial guesses and (ii) applying multi-stage optimization. Within this scope, as shown in Fig. 1, the optimization issue such as overfitting is minimized, while the physical meaning of parameters remains. It should be noted that during the optimization the bounds of the parameters are defined physically; the I_{spec} and V_{T0} are positive values, and λ_c is between 0 and 1. The extraction methodology is divided into two parts with respect to I_D-V_G and I_D-V_D.

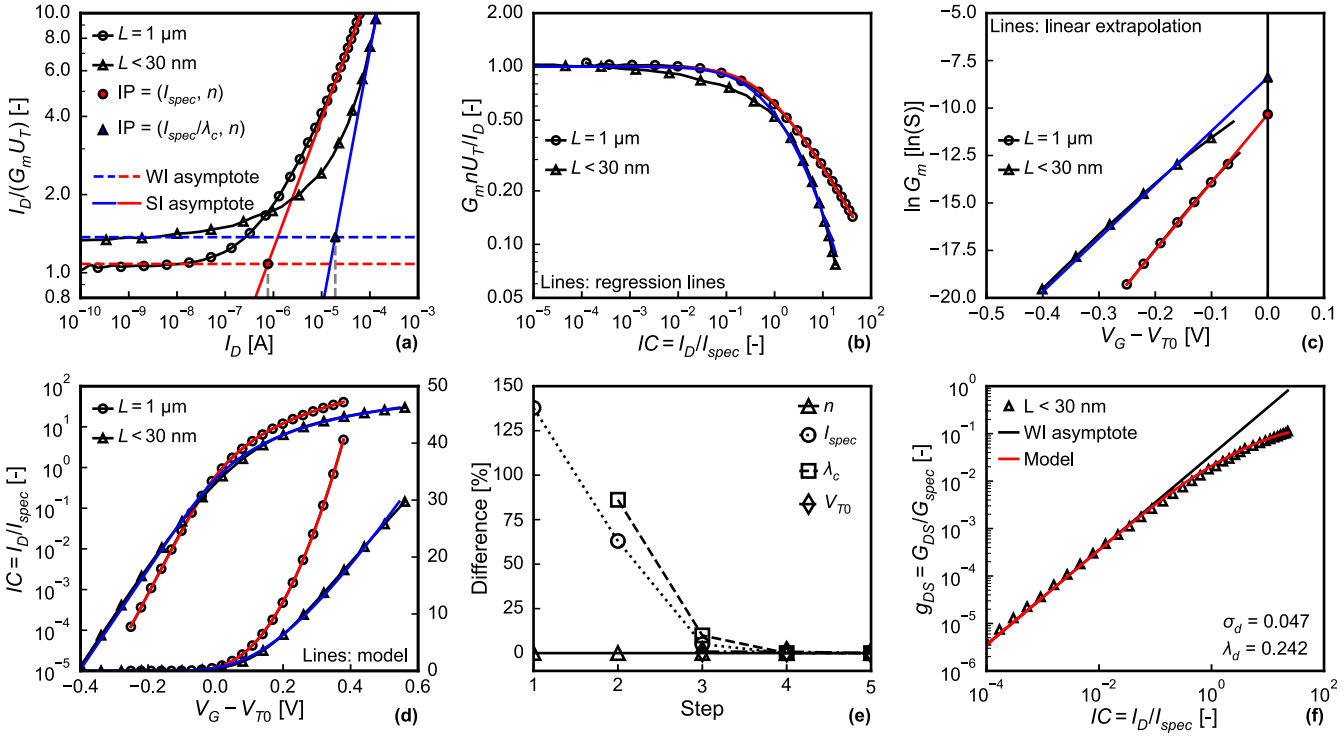

FIGURE 2. Parameter extraction processes of the SEKV-E from I_D-V_G (a-e) and I_D-V_D (f) aspects, where devices are from a commercial 22 nm FDSOI platform, measured at 300 K, biased in saturation ($V_{DS} = 0.8$ V), and at $V_{back} = 0$ V. (a) Step 1: the slope factor n is extracted from an asymptote in WI (horizontal lines), which has an intersection point (IP) with an asymptote in SI. (b) Step 2: Optimization on I_{spec} and λ_c via (4) (c) Step 4: Extraction of I_{spec} without λ_c influence, where I_{spec} is extracted from an intercept on y-axis. (d) Step 5: re-optimization on V_{T0} and comparison between sEKV model with extracted parameters and measurements. (e) Difference for each parameter of a short device at every step in comparison to its final result. (f) Extraction of normalized output conductance g_{DS} at $V_{DS} = 0.8$ V. Black line is an asymptote in WI for extracting σ_d.

A. EXTRACTION FOR I_D-V_G

Fig. 2(a-d) demonstrate the extraction process for a long ($W/L = 1\,\mu m/1\,\mu m$) and a short ($W/L = 0.3\,\mu m/ < 30\,nm$) device from a commercial 22 nm FDSOI process [11] and characterized at room temperature. The short device has the minimal length of such technology. First, according to [6], the normalized source transconductance is given by

$$\frac{g_{ms}}{IC} = \frac{G_m n U_T}{I_D} = \frac{\sqrt{(\lambda_c IC + 1)^2 + 4IC} - 1}{IC[\lambda_c(\lambda_c IC + 1) + 2]}. \tag{4}$$

When a device is biased in WI, (4) is reduced to unity thanks to $\lambda_c IC \ll 1$. The term n can be defined from the flat region, i.e., subthreshold regime, of $I_D/(G_m U_T)$ in Fig. 2(a). On the contrary, as a device works in SI, (4) becomes

$$\left.\frac{G_m n U_T}{I_D}\right|_{SI} = \begin{cases} \frac{1}{\sqrt{IC}} \text{ (without VS)} \\ \frac{1}{\lambda_c IC} \text{ (with VS)} \end{cases} \tag{5}$$

By taking the log on (5), the SI asymptotes shown in Fig. 2(a) for devices without/with VS are given by

$$\log\left(\frac{I_D}{G_m U_T}\right)\Big|_{SI} - \log(n) = \begin{cases} \frac{1}{2}\left(\log(I_D) - \log(I_{spec})\right) \\ \log(I_D) - \log\left(\frac{I_{spec}}{\lambda_c}\right) \end{cases} \tag{6}$$

correspondingly. On top of that, as shown in Fig. 2(a) the intersection point (IP) of the n and the SI asymptote results in the value of I_{spec}. It should be noted that, in (6), the IP with the presence of VS has the value of I_{spec}/λ_c on the horizontal axis. Although λ_c can not be obtained at the first step, measuring the slope of SI asymptote tells whether the device suffers the VS. Due to (6), the SI asymptote should have the slope of 1 for a device influenced by the VS, λ_c is set to 0.2 by default. Otherwise, λ_c is set to 0 for turning off the VS in the model. Thereby, I_{spec} can be roughly estimated for the later non-linear least squares process. Second, the I_{spec} and λ_c from the 1st step are taken as the initial guesses and optimized in the 2nd step by (4), as shown in Fig. 2(b). Up to this point, only V_{T0} remains unknown, which is simply extracted by fitting I_D-V_G via (1) in the 3rd step.

Until now, four parameters (n, I_{spec}, V_{T0}, λ_c) are obtained. Nonetheless, the fraction of I_{spec} to λ_c ($I_{spec}/\lambda_c = nWC_{ox}v_{sat}U_T$) is a constant, where v_{sat} is the saturation velocity. It easily leads to optimization issues. Hence, I_{spec} should be extracted without λ_c. As shown in Fig. 2(b), λ_c mainly impacts a short device in SI, the transconductance efficiency ($G_m n U_T/I_D$) rapidly degrades in comparison to a long device. It suggests that I_{spec} can be redefined when a device operates below the threshold voltage. By having the equation of

$$\ln G_m = \frac{V_G - V_{T0}}{nU_T} + \ln\left(\frac{I_{spec}}{nU_T}\right), \tag{7}$$

I_{spec}, in the fourth step, is extracted accurately from the intercept of the line in Fig. 2(c). The λ_c is therefore optimized again via (4). Finally, V_{T0} is optimized again via (1). Consequently, the sEKV model shows a nice agreement

TABLE 1. Extracted parameters for nMOS FDSOI devices at 300 K.

W/L [μm/μm]	n	$I_{spec\square}$ [nA]	λ_c	V_{T0} [V]	σ_d	λ_d
1/1	1.08	912	0.0	0.411	-	-
0.3/ < 0.03	1.37	483	0.285	0.219	0.047	0.242

with the measurement in Fig. 2(d). Fig. 2(e) demonstrates the difference in percentage for each parameter at each step for a short-channel device. The deviations in I_{spec} and λ_c are decreased in the later steps, where the overfitting issue is properly treated. It further approves the extraction methodology adopting the multi-stage fitting optimization. The ultimate result is summarized in Table 1.

B. EXTRACTION FOR I_D-V_D

With four sEKV parameters extracted from I_D-V_G of a short device, the parameters for G_{DS} are extracted in the following two steps. First, since (4) can be reduced to unity as $IC < 0.1$, (2) can be rewritten by $g_{DS} = \sigma_d IC/n$. The term σ_d is easily acquired by doing the linear regression from g_{DS} versus IC, as shown in Fig. 2(f). Secondly, the only unknown term, i.e., λ_d, is optimized via (3). As shown in Fig. 2(f), the sEKV model with extracted σ_d and λ_d nicely agree with the measurement over a wide operation range. Theoretically, λ_d should be equal to λ_c. However, the mobility reduction due to a strong vertical field, which is not included in the sEKV model, influences the extraction of λ_c. Therefore, λ_c (= 0.285), obtained from Section III-A, is slightly larger than λ_d (= 0.242). Nevertheless, in this case, the accurate G_{DS} with respect to inversion status can be predicted.

IV. RESULTS AND DISCUSSION

This section applies SEKV-E to the wide range of technology, temperature, and back-gate voltage (V_{back}) for FDSOI, and the result of G_{DS} modeling is presented. The percent error is used to measure the match between the model and the inputted I_D-V_G to validate the capability of SEKV-E. However, the I_D is not suitable for calculating the error since I_D spans over several orders. Besides, the sEKV model takes the I_D as a variable. Hence, the percent error is defined by $\frac{1}{N}\sum_{i=1}^{N}|(V_{G_{out,i}} - V_{G_{in,i}})/V_{G_{in,i}}|$ with $V_{G_{in}}$ the inputted V_G from the measurement and $V_{G_{out}}$ the outputted V_G from the sEKV model.

Fig. 3 demonstrates the I_D-V_G in saturation of various advanced CMOS technologies, where the low percent error shows that the SEKV-E is universal to different technologies. The extracted parameters are summarized in Table 2. Besides, the transconductance efficiency, or called the current efficiency, is presented in Fig. 4, where the SEKV-E also captures the small signal of devices from different silicon technologies. From the extracted values of n, the 16 nm FinFET technology shows a well electrostatic control in comparison to other presented technologies due to the π gate configuration. On the other hand, the 16 nm FinFET and the 22 nm FDSOI show the higher λ_c than that of 28 nm Bulk because of the shorter channel. However, since the sEKV model originates from the charge-based model for

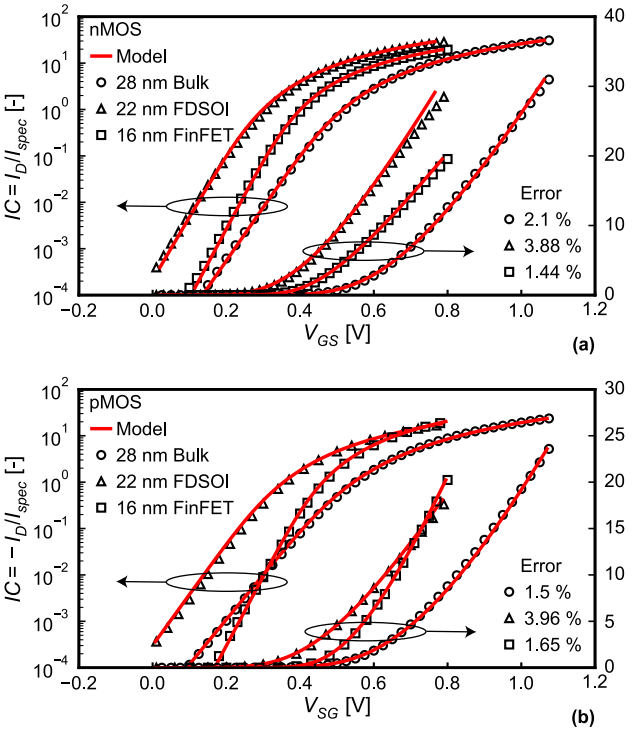

FIGURE 3. The results of applying sEKV-E on the shortest nMOS devices from various advanced CMOS technologies, including 28 nm Bulk ($W/L = 3\,\mu m/30$ nm) [12], 22 nm FDSOI ($W/L = 1\,\mu m/ < 30$ nm), and 16 nm FinFET ($W/L = 58$ nm/16 nm) [13]. The percent error between the measurement and sEKV model is given.

TABLE 2. Summary of sEKV parameters for silicon technologies at 300 K.

Type	Tech.	n	$I_{spec\square}$ [nA]	λ_c	V_{T0} [V]
nMOS	28 nm Bulk	1.46	599	0.271	0.478
	22 nm FDSOI	1.24	446	0.307	0.266
	16 nm FinFET	1.13	1290	0.475	0.366
pMOS	28 nm Bulk	1.74	446	0.253	0.501
	22 nm FDSOI	1.52	468	0.36	0.312
	16 nm FinFET	1.12	995	0.331	0.431

the conventional bulk technology, the quantum correction on charges due to the thin channel thickness (< 10 nm) is not included. Therefore, the simple model, sEKV, becomes a semi-empirical model for the technologies such as FDSOI and FinFET, in which the q_s in (1) behaves like an equivalent term to the bulk CMOS. Nevertheless, from the circuit design perspective, the SEKV-E offers the accurate sEKV model corresponding to the given CMOS technology.

The sEKV parameters have been extracted manually for a 28 nm FDSOI technology and discussed extensively from room temperature down to 3 K in [15]. In contrast, Fig. 5 presents the use of the SEKV-E to extract the parameters from a 22 nm FDSOI technology for each temperature [14]. SEKV-E extracts different parameter sets for each temperature that are summarized in Table 3. The low-temperature effects are nicely captured, such as the subthreshold swing reduction and the increases in the V_{T0} and the mobility.

In fact, the physical model of devices is more complex as the temperature cools down. For instance, the effective mobility strongly varies to the vertical electric field due to the

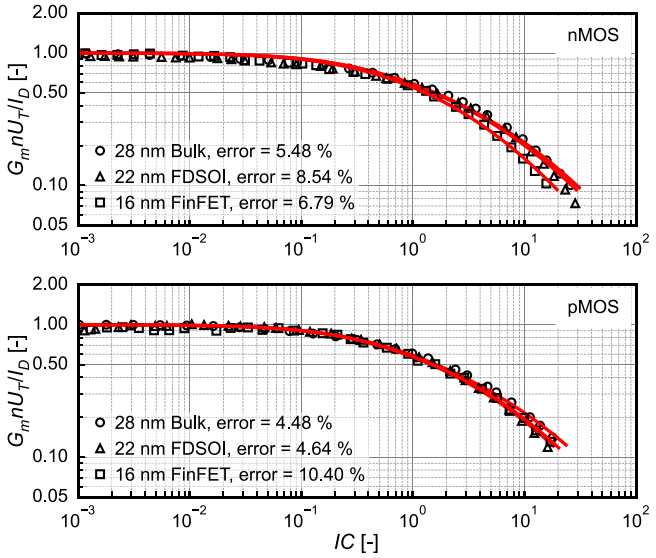

FIGURE 4. The transconductance efficiency versus *IC* showing the shortest nMOS/pMOS devices from 28 nm Bulk ($W/L = 3\,\mu m/30\,nm$) [12], 22 nm FDSOI ($W/L = 1\,\mu m/ < 30\,nm$), and 16 nm FinFET ($W/L = 58\,nm/16\,nm$) [13]. The percent error is defined by $\frac{1}{N}\sum_{i=1}^{N} |(y_{out,i} - y_{in,i})/y_{in,i}|$ with $y = G_m nU_T/I_D$.

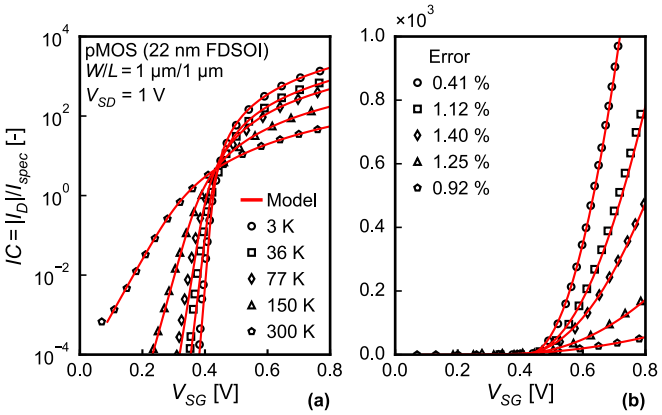

FIGURE 5. Applying SEKV-E to a pMOS device of 22 nm FDSOI technology in saturation with $V_{back} = 0$ V [14] from room temperature down to deep cryogenic temperature. The legend in (b) shows the percent error.

TABLE 3. Extracted sEKV parameters for a pMOS FDSOI ($W/L = 1\,\mu m/1\,\mu m$) at different temperatures.

Temperature [K]	n	$I_{spec_\square}$ [nA]	λ_c	V_{T0} [V]
3	17.68	50	0.0	0.423
36	2.13	97	0.0	0.415
77	1.32	161	0.0	0.4
150	1.19	411	0.0	0.373
300	1.19	1057	0.0	0.313

phonon scattering reduction [14]. Thus, the constant mobility model using low-field mobility μ_0 accounted in I_{spec} is not sufficient at cryogenic temperatures, which makes the sEKV model more empirical. Nonetheless, as more and more cryogenic studies are going on, mainly for the quantum computing applications, the sEKV model potentially meets the need for the cryogenic compact model before the industrial cryogenic PDK is released since the existing PDK is not valid at cryogenic temperatures.

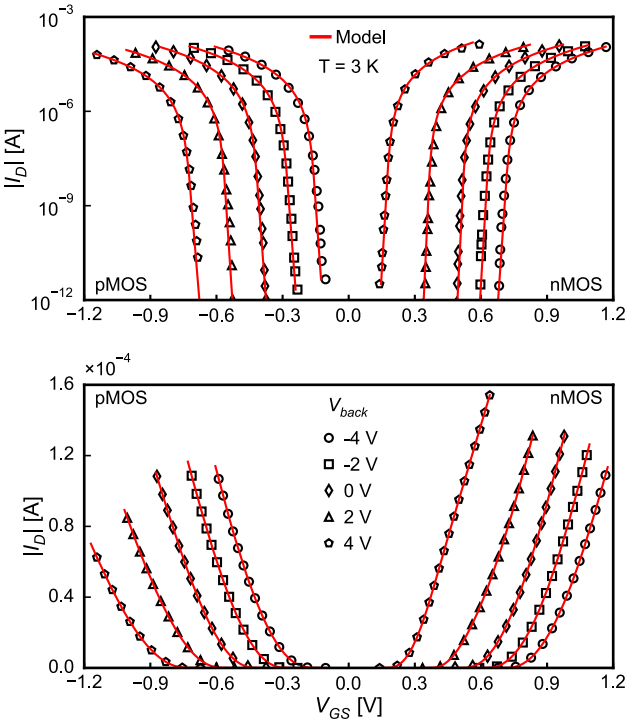

FIGURE 6. The use of SEKV-E on nMOS/pMOS FDSOI devices ($W/L = 1\,\mu m/1\,\mu m$), measured at 3 K with various back-gate voltages V_{back} [14].

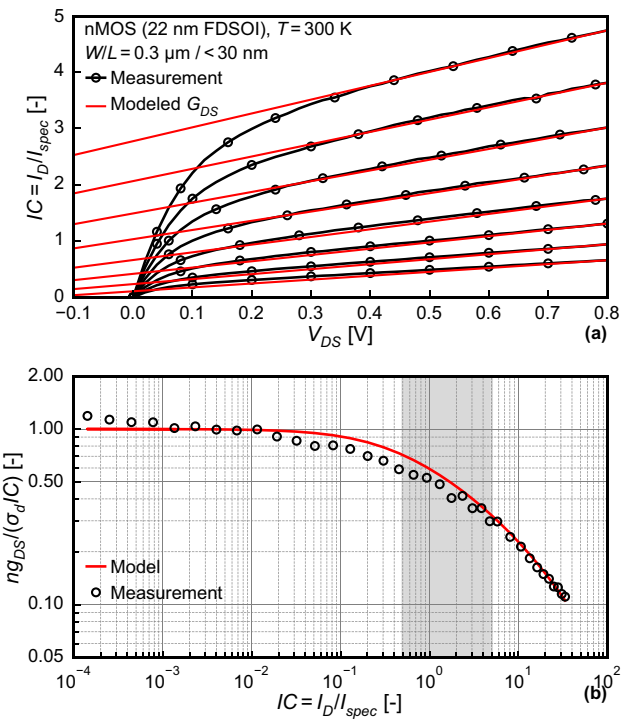

FIGURE 7. The use of SEKV-E on a series of I_D-V_D from WI to SI. (a) *IC* versus V_{DS} with the modeled G_{DS} at $V_{DS} = 0.8$ V. A set of I_D-V_D is measured in the range of $0.5 < IC < 5$, as shown in the gray area in (b). (b) The normalized g_{DS}/IC versus *IC*, where g_{DS} is predicted over a wide operation range.

On the other hand, the advantage of using the FDSOI technology is having freedom of the threshold voltage via modulating the V_{back}. For instance, as V_{back} is increased by

1 V, the threshold voltage of nMOS in saturation is reduced by ≈ 90 mV [14]. Moreover, the experimental results further prove that the effective mobility is increased as the threshold voltage is lowered [14]. The above back-gate effects at 3 K for nMOS and pMOS are also captured by the SEKV-E as shown in Fig. 6. On top of the demonstration presented in this section, the SEKV-E shows the comprehensive ability to extract four parameters from a given I_D-V_G via the sEKV model. SEKV-E is a universal tool to generate a simple design-oriented model in many situations.

Finally, Fig. 7 plots the results of applying the SEKV-E on a set of I_D-V_D that ranges from WI to SI. Fig. 7(a) demonstrates the IC-V_{DS} for the device, operating around MI. The modeled G_{DS} has a nice agreement with the I_D-V_D in saturation regime. Similar to g_{ms}/IC in (4), $ng_{DS}/(\sigma_d IC)$ behaves an unity in deep WI, as shown in Fig. 7(b), where the model with the first-order approximation on the DIBL effect successfully estimates the G_{DS} over a wide operation region.

V. CONCLUSION

This paper presents an open-source Python-based automated parameter extractor for the simplified EKV model, in which only four parameters are needed to predict the I_D-V_G transfer characteristic and two parameters for the I_D-V_D output characteristics, respectively. The analytical extraction and multi-stage optimization are adopted to prevent overfitting issues. Besides, in this work, SEKV-E is applied to a broad range of silicon technologies, temperatures, device dimensions, and back-gate effects. Finally, the work highlights the efficiency and accuracy of the proposed tool, compared to the manual extraction. The tool potentially accelerates IC circuit designs under many scenarios.

ACKNOWLEDGMENT

The authors would like to thank Zhixing Zhao, Steffen Lehmann, and Claudia Kretzschmar from GLOBALFOUNDRIES Germany for providing 22 FDX® test structures.

REFERENCES

[1] B. Sheu, D. L. Scharfetter, P.-K. Ko, and M.-C. Jeng, "BSIM: Berkeley short-channel IGFET model for MOS transistors," *IEEE J. Solid-State Circuits*, vol. SSC-22, no. 4, pp. 558–566, Aug. 1987, doi: 10.1109/JSSC.1987.1052773.

[2] T. Poiroux *et al.*, "Leti-UTSOI2.1: A compact model for UTBB-FDSOI technologies—Part I: Interface potentials analytical model," *IEEE Trans. Electron Devices*, vol. 62, no. 9, pp. 2751–2759, Sep. 2015, doi: 10.1109/TED.2015.2458339.

[3] T. Poiroux *et al.*, "Leti-UTSOI2.1: A compact model for UTBB-FDSOI technologies—Part II: DC and AC model description," *IEEE Trans. Electron Devices*, vol. 62, no. 9, pp. 2760–2768, Sep. 2015, doi: 10.1109/TED.2015.2458336.

[4] C. Enz, F. Chicco, and A. Pezzotta, "Nanoscale MOSFET modeling: Part 2: Using the inversion coefficient as the primary design parameter," *IEEE Solid-State Circuits Mag.*, vol. 9, no. 4, pp. 73–81, Nov. 2017, doi: 10.1109/MSSC.2017.2745838.

[5] W. Sansen, "Analog CMOS from 5 micrometer to 5 nanometer," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, 2015, pp. 1–6, doi: 10.1109/ISSCC.2015.7062848.

[6] C. Enz, F. Chicco, and A. Pezzotta, "Nanoscale MOSFET modeling: Part 1: The simplified EKV model for the design of low-power analog circuits," *IEEE Solid-State Circuits Mag.*, vol. 9, no. 3, pp. 26–35, Aug. 2017, doi: 10.1109/MSSC.2017.2712318.

[7] "SEKV-E." [Online]. Available: https://gitlab.com/moscm/sekv-e (Accessed: May 5, 2022).

[8] C. C. Enz and E. A. Vittoz, *Charge-Based MOS Transistor Modeling: The EKV Model for Low-Power and RF IC Design*. Hoboken, NJ, USA: Wiley, 2006.

[9] Y. Taur, "On the log-linear inversion-charge relation for MOSFET modeling," *IEEE Trans. Electron Devices*, vol. 69, no. 1, pp. 427–429, Jan. 2022, doi: 10.1109/TED.2021.3124861.

[10] M.-A. Chalkiadaki, "Characterization and modeling of nanoscale MOSFET for ultra-low power RF IC design," Ph.D. dissertation, Dept. Comput. Sci., EPFL, Lausanne, Switzerland, 2016.

[11] R. Carter *et al.*, "22nm FDSOI technology for emerging mobile, Internet-of-Things, and RF applications," in *Proc. IEEE Int. Electron Devices Meeting (IEDM)*, 2016, pp. 2.2.1–2.2.4, doi: 10.1109/IEDM.2016.7838029.

[12] A. Beckers, F. Jazaeri, and C. Enz, "Characterization and modeling of 28-nm bulk CMOS technology down to 4.2 K," *IEEE J. Electron Devices Soc.*, vol. 6, pp. 1007–1018, 2018, doi: 10.1109/JEDS.2018.2817458.

[13] H.-C. Han, F. Jazaeri, A. D'Amico, A. Baschirotto, E. Charbon, and C. Enz, "Cryogenic characterization of 16 nm FinFET technology for quantum computing," in *Proc. IEEE 51st Eur. Solid-State Device Res. Conf. (ESSDERC)*, 2021, pp. 71–74, doi: 10.1109/ESSDERC53440.2021.9631805.

[14] H.-C. Han *et al.*, "Back-gate effects on dc performance and carrier transport in 22 nm fdsoi technology down to cryogenic temperatures," *Solid-State Electron.*, vol. 193, Jul. 2022, Art. no. 108296, doi: 10.1016/j.sse.2022.108296.

[15] A. Beckers, F. Jazaeri, H. Bohuslavskyi, L. Hutin, S. De Franceschi, and C. Enz, "Characterization and modeling of 28-nm FDSOI CMOS technology down to cryogenic temperatures," *Solid-State Electron.*, vol. 159, pp. 106–115, Sep. 2019, doi: 10.1016/j.sse.2019.03.033.

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