

Received 16 November 2021; revised 27 January 2022 and 17 February 2022; accepted 20 February 2022. Date of publication 25 February 2022; date of current version 9 March 2022.

Digital Object Identifier 10.1109/OJCAS.2022.3154062

Optimization of Quantized Analog Signal Processing Using Genetic Algorithms and μ -Law

QINGNAN YU^{® 1,2} (Member, IEEE), TONY CHAN CARUSONE^{® 1} (Fellow, IEEE), AND ANTONIO LISCIDINI^{® 1} (Senior Member, IEEE)

¹Department of Electrical and Computer Engineering, University of Toronto, Toronto, ON M5S 3G4, Canada

²Analog Devices Canada, Toronto, ON M5G 2C8, Canada

This article was recommended by Associate Editor B. D. Sahoo.

CORRESPONDING AUTHOR: T. C. CARUSONE (e-mail: tony.chan.carusone@isl.utoronto.ca)

This work was supported in part by Analog Devices Canada and in part by the Natural Sciences and Engineering Research Council (NSERC) of Canada.

ABSTRACT Digital mismatch calibration for quantized analog (QA) signal processing is proposed for the first time. Since the proposed calibration mechanism does not require uniform QA slicer levels, nonuniform quantization can be applied to improve the system performance. We propose two methods utilizing the genetic algorithm and μ -law to find non-uniform slicer levels offering superior performance compared to uniform levels. Simulations show that for a QA amplifier consisting of 32 slices, the signal-to-noiseand-distortion ratio (SNDR) under a multitone input can be doubled by adjusting only the quantization levels while maintaining the same structure and same power, compared to uniform quantization levels that provide 54 dB of SNDR.

INDEX TERMS Quantized analog (QA), digital calibration, adaptive linear combiner (ALC), non-uniform quantization, peak-to-average power ratio (PAPR), genetic algorithms, μ -law.

I. INTRODUCTION

Quantized analog (QA) signal processing is a technique that decomposes the signal into multiple portions, where each portion is processed by an independent signal path. Unlike analog-to-digital converters (ADCs), which convert analog signals into digital form, a QA amplifier converts the input signal into both liquid digital "bits" and analog residues [1]. Compared to an analog amplifier, a QA amplifier has an expanded dynamic range (DR) because its compression point can be higher than the voltage supply [2]. Furthermore, the DR of a QA amplifier can be tuned by adjusting the overlap between the adjacent slices, making it suitable for reconfigurable RF receiver applications. For example, the QA receiver front-end in [1] has a reconfigurable DR, and its 1-dB compression point can be tuned from -8.5 to 10.5 dBm under a 0.8-V supply.

QA signal processing has three essential blocks, as shown in Fig. 1(a). The first block is the slicer, whose job is to determine which portion of the input signal each slice shall process. The slicing of the input signal can be realized by adding an offset voltage at the input of each path. Depending on the input signal level and the offset of each slice, some slices carry the liquid digital "bits" by saturating to ground or the supply voltage while others carry the analog residue [1]. Thus, the QA signal after the slicer is carried in both digital and analog forms. Further processing of the QA signal after the slicer may include filtering and digitization. Finally, the combiner adds the signal from each path together. A digital combiner has significant advantages over an analog combiner because the latter suffers from the DR limitation imposed by the supply voltage, whereas the DR of a digital combiner is limited by the number of bits available. Therefore, it is desirable to include an ADC before the combiner to allow for digital recombination, assuming that the system ultimately requires digital signal processing, for example, in wireless receiver applications.

Although the structure of QA signal processing with backend ADCs is akin to that of a folding ADC [3], several important differences exist. First, the folding amplifier creates a piecewise-linear input-output characteristic whose gain polarity changes every fold. By contrast, the QA amplifier does not "fold" the signal; instead, it performs a



FIGURE 1. (a) Existing QA signal processing structure and (b) proposed QA signal processing structure with adaptive output recombination and slicer optimization.

"slicing" operation whereby the input-output characteristic is monotonic. Second, a coarse ADC is not required in the QA structure. Third, folding ADCs often require preceding sample-and-hold (S/H) circuits to alleviate the problem of frequency multiplication inherent to the folding operation [4], as well as to synchronize the folding path with the coarse ADC path [5]. However, in a QA amplifier with ADCs, there is no systematic delay mismatch, so the S/H operation is not required prior to the ADCs. Hence, QA signal processing can take advantage of continuous-time (CT) ADCs, such as CT delta-sigma ADCs, with benefits like inherent anti-aliasing [6].

There are two major shortcomings in all the existing works on QA signal processing, which use uniformly distributed slicer levels and unweighted adders for output recombination [1], [2], [7], [8]. The first is that the slicer levels, in reality, will inevitably deviate from the desired uniform distribution due to mismatch. The work in [1] argues that the mismatches can be averaged by having enough overlap between adjacent slices. However, enforcing a large overlap of QA units hinders the DR expansion; thus, the QA amplifier cannot be exploited to its full potential. The second is



FIGURE 2. Adaptive linear combiner for quantized analog signal processing.

that uniform slicing is not necessarily optimal for all input scenarios because it neglects the statistical characteristics of the signal completely. As shown in Fig. 1(b), this work proposes digital algorithms that act on the QA slicer and the combiner to address these shortcomings. In Section II, we propose an all-digital calibration method using an adaptive linear combiner (ALC) that can correct the QA slicer mismatch by acting solely on the combiner. Then, in Section III, we introduce optimization algorithms based on the genetic algorithm (GA) and the μ -law algorithm to find non-uniform slicer levels that offer performance superior to uniform levels for different input statistics.

II. ADAPTIVE OUTPUT RECOMBINATION

The QA slicer performs the slicing and the amplification of the partially quantized signal, both of which are adversely affected by the mismatch in the sub-amplifiers. Fig. 2 shows the system model of the QA amplifier with the digital calibration block using the ALC, which is implemented in MATLAB, preceded by ideal 10-bit ADCs. The ADC resolution is chosen such that the thermal noise of the OA amplifier is at least 10 dB higher than the ADC quantization noise, as we will see later in this section. The QA amplifier is implemented using inverter amplifiers in 28nm CMOS technology. The transistor V_T mismatch results in random variations in both the inverter threshold and gain. The offset variation (threshold variation) occurs when the PMOS and the NMOS V_T values move in the same direction, whereas the gain variation occurs when the V_T values move in opposite directions [8]. As a result, the threshold variation directly translates to variations in the QA slicer levels, while the gain variation results in non-uniform gain among the QA signal paths.

The ideal QA amplifier small-signal gain along with the Monte Carlo results are shown in Fig. 3, where the QA amplifier has 18 slices, and the voltage offset is $\Delta V =$ 47 mV. Transistor mismatch models are used in the QA amplifier and the number of Monte Carlo trials is 100. As shown, the mismatch results in greater ripples in the QA amplifier gain, which deteriorates the system's linearity. The percentage gain variation increases from 1.3% to 9.6% due to mismatch. This necessitates a calibration mechanism that



FIGURE 3. (a) Ideal QA amplifier gain (N = 18) (b) Monte-Carlo QA amplifier gain with mismatch (N = 18).

can smoothen the gain ripples and improve the linearity of the QA amplifier. The aim of this section is to demonstrate that the ALC with the LMS algorithm can digitally calibrate for this mismatch.

A. ADAPTIVE LINEAR COMBINER USING THE LMS ALGORITHM

Let *N* be the number of QA amplifier slices, and *X* be the column vector containing all the digital QA outputs from all slices:

$$X = [x_1 \ x_2 \cdots x_i \cdots x_N]^T$$

The ALC performs a weighted sum of the QA outputs using the weight vector:

$$W = [w_1 \ w_2 \cdots \ w_i \cdots \ w_N]^T$$

and produces a single output:

$$y = X^T W \tag{1}$$

The weight vector W is obtained using the LMS algorithm, which is commonly used in adaptive systems due to its computational efficiency, simple implementation and robustness [9]. The reference signal for the LMS is either a known sequence during foreground calibration, or in data communication applications may be decision-directed for background calibration [10].



FIGURE 4. Monte-Carlo QA amplifier gain with mismatch after calibration (N = 18).



FIGURE 5. SNDR and THD histograms with 100 seeds before and after calibration.

Although the precise resolution requirement of the ALC cannot be accurately determined without a detailed design, it can be reasonably estimated following the resolution of the ADCs. To prevent degrading the quantization noise floor of the QA output, the number of bits used in the ALC shall not be lower than that of the ADCs. The simulation results presented hereafter use 10-bit resolution for the ALC.

B. MISMATCH CALIBRATION

Foreground calibration is used to train the ALC weights. The training signal is a 0.3 V_{pp} sinusoid at 2.66 MHz. Fig. 4 shows the QA amplifier gain after calibration with 100 Monte Carlo trials. The ALC significantly reduces the QA amplifier gain ripple by tuning the summation weight of each slice digitally for the input range covered by the training signal. The maximum percentage gain variation is reduced from 9.6% to 4.1%. Thus, the ALC can be seen as a block that linearizes the QA amplifier gain by counteracting the non-linearity introduced by random mismatch.

The quantitative improvements are summarized by histograms in Fig. 5. The LMS algorithm minimizes the mean-squared error between the ALC output and the reference signal, which contains both thermal noise and distortion. The SNDR in the ideal case is thermal noise limited and is degraded by distortion due to mismatch in the practical case. Hence, we expect the SNDR to be thermal noise limited after calibration if the ALC sufficiently reduces the gain ripple. This can be confirmed in Fig. 5(a), where the SNDR after calibration reach the same value as the ideal

Pre-calibration

Post-calibration

50



FIGURE 6. QA amplifier (N = 18) gain without mismatch before and after calibration using the ALC.



٥

-20

-40

-60

case, which is 55.4 dB. On the other hand, since the harmonic distortions do not have a hard limit, the total harmonic distortion (THD) values after calibration may have a small variance, but they should all be lower than the noise power, as shown in Fig. 5(b). Interestingly, more than half of the trials after calibration have lower THD than the ideal case. These marginal improvements in linearity are obtained with completely random variations in the inverter threshold and gain. This suggests that the performance of the QA amplifier can be improved with non-uniform quantization spacing, which will be investigated in Section III.

The proposed calibration algorithm operates in the foreground. The limitation of foreground calibration is that it does not track temperature variations continuously. There are two possible ways to overcome this. One is to perform foreground calibration periodically, for example, in certain applications where the system needs to be re-calibrated at wake-up [11], [12]. In applications where the system is never taken offline, it can be calibrated first using a known reference before switching to the decision-directed mode whereby the reference is obtained from the output decisions [10].

Although the proposed calibration method is in the digital domain, the same principle is applicable to QA structures with analog recombination where the signal does not need to be digitized. For example, the ALC can be realized by common-source amplifiers with tunable gate bias voltages [13]. Thus, in principle, the mismatch in the QA amplifier can nonetheless be calibrated without using ADCs.

C. COMPENSATION FOR QA AMPLIFIER GAIN **COMPRESSION**

Besides mismatch calibration, the ALC can also serve as a compensation for gain compression so that any QA amplifier could benefit from it, whether the mismatch requires calibration or not. Fig. 6 shows the QA amplifier gain without mismatch before and after calibration using a 0.7 V_{pp} training signal, which has a larger amplitude to explore the input range where the gain rolls off, causing large-signal distortion. It is important to note that although the offsets are uniformly spaced, the QA amplifier gain before calibration is not perfectly uniform due to uneven overlap among the slices. For example, the first and last slices in the inverter

amplifier array have less adjacent slices, resulting in less overlap and lower small-signal gain for the highest and lowest input signal levels. Fortunately, this gain roll-off can be compensated by the ALC due to its ability to digitally adjust the gain of each slice. As shown, the gain after ALC calibration is flatter for the entire input range covered by the training signal. This creates a much sharper roll-off. In other words, the ALC can be seen as a digital non-linearity correction that reverses the gain compression of the QA amplifier, or indeed anywhere in the analog signal path.

The quantitative improvement is shown in the output spectrum in Fig. 7, where the test signal is a 0.7 V_{pp} tone at 3.38 MHz and the input full-scale of the QA amplifier is 0.8 V_{pp} . The gain compression results in significant harmonic distortions, which are then suppressed by the ALC. The SNDR improvement is from 43 dB to 61 dB (by 18 dB). The THD is reduced from -43 dB to -66 dB (by 23 dB).

III. QUANTIZATION LEVEL OPTIMIZATION

Analog front-ends are expected to handle various input scenarios due to the growing demand for multistandard wireless receivers [14]-[18]. The drawback of uniform quantization, which is used in all the prior works on QA signal processing [1], [2], [7], [8], is that it hinders the QA slicer from being optimized for different scenarios. Uniform quantization, even with adaptive DR [1], only takes into account the input amplitude and ignores the statistical characteristics of the signal entirely. In many applications, we expect the signal to be non-uniformly distributed over the input range, affording opportunities for non-uniform quantization. For example, it is well-known that orthogonal frequency-division multiplexing (OFDM) signals have very high peak-to-average power ratios (PAPR), which means that samples of the signal are mostly concentrated in a much smaller range than the maximum amplitude. The idea of non-uniform quantization is not foreign as it has been studied extensively for ADCs. For example, the Lloyd-Max (LM) algorithm [19] can determine the SQNR-optimal threshold levels of an ADC given the input probability density function (PDF). Also, several other works proposed algorithms to find the BER-optimal quantization levels for ADC-based wireline receivers [20]-[22]. However, it is important to note that in



FIGURE 8. QA amplifier behavioral model for quantization level optimization.

this work, "quantization" is the slicing of the input signal by the QA slicer, and the "quantization levels" determine which portion of the input signal each slice shall process. It is important to distinguish QA slicer quantization, also known as liquid digital decomposition [1], from ADC quantization, which is fully digitization. Therefore, the optimal QA slicer (quantization) levels do not necessarily correlate with the ADC quantization levels provided by those algorithms.

A. THE GENETIC ALGORITHM

This work considers the SNDR as the cost function for the quantization level optimization. Although gradient-based algorithms are popular candidates for many optimization problems, the SNDR performance space of the QA quantization levels contains local extrema that could potentially trap a gradient-based optimizer. Moreover, the quantization levels of the QA amplifier are ultimately controlled by digitalto-analog converters (DACs) in the circuit implementation. Consequently, their voltage values are discrete variables, for which gradient-based algorithms are not best suited. The most primitive discrete variable optimizer is an exhaustive search, which examines all possible combinations of the variables to locate the global extrema. However, the complexity of the performance space makes an exhaustive search impractical because the search space is N-dimensional, where N is the number of slices. Hence, we require a discrete variable optimizer that is time-efficient and performs well for cost functions containing local extrema.

One promising candidate satisfying the criteria listed above for QA quantization level optimization is the GA [23], which is an evolutionary algorithm inspired by the law of natural selection. GAs have been applied in analog design for automated circuit synthesis [24], [25] and finding optimal circuit coefficients for wireline receiver analog front-ends [26]. Moreover, GAs have the advantage of not having to rely on assumptions about the performance landscape, which in this case varies considerably based on the operative scenario, especially for wireless applications. In this work, we use the GA as a global optimizer for various test cases. The behavioral model of the QA system for the GA optimization is shown in Fig. 8. To accelerate the GA, the inverter amplifiers are modelled using tanh functions fit to simulations in a 28nm CMOS technology as described in Appendix A, and



FIGURE 9. QA amplifier (N = 32) quantization levels before and after the GA optimization for eight-tone input when the SNDR is noise-limited.



FIGURE 10. QA amplifier (N = 32) quantization levels before and after the GA optimization for sinusoidal input when the SNDR is noise-limited.

the ADCs are modelled as unity gain buffers. We let $v_{os,i}$ be the offset voltage added to the input of the *i*th slice. The vector notation for all the offset voltages is:

$$V_{os} = \begin{bmatrix} v_{os,1} & v_{os,2} \cdots & v_{os,i} \cdots & v_{os,N} \end{bmatrix}^{T}$$

The genes of the GA are V_{os} vectors and the cost function is SNDR. When evaluating the SNDR, the GA assumes that the ALC weights are determined by the LMS algorithm for each vector V_{os} and fixed after convergence. To accelerate the simulations, the outcome of the LMS algorithm is found using the quadratic programming algorithm described in Appendix B. A detailed description of the GA is provided in Appendix C.

B. INPUT SIGNAL SETUP

We consider two practical scenarios in wireless communication receivers where highly non-uniform input distributions arise. First, we construct an input with a peak amplitude of $0.707 V_{pp}$ using eight equal amplitude sinusoidal tones. The PAPR is 12 dB, which is similar to a typical OFDM signal, and the input PDF is shown in Fig. 9. It can be observed that the signal content is concentrated in a much smaller region than the peak-to-peak swing. The second scenario is a single-tone sinusoidal input, which emulates a narrow-band blocker. With the same peak-to-peak amplitude of $0.707 V_{pp}$, the sinusoid is more likely to be sampled at its peak, and its PDF is higher at the two ends, as shown in Fig. 10. Since the two input scenarios have very different statistical



characteristics, we expect the GA to produce very different level distributions.

C. INTUITION BEHIND NON-UNIFORM LEVEL DISTRIBUTION

We can first qualitatively set expectations of how nonuniform level distributions can improve the SNDR of the QA amplifier assuming it is thermal noise limited, using the LM algorithm [19] as an analogy. The LM algorithm minimizes the quantization noise power of an ADC by condensing the levels where the input PDF is higher so that the quantization error is less for the more frequently arising signal levels. For the signal levels where the PDF is lower, the LM algorithm allows the instantaneous quantization error to be higher because it has less impact on the overall SQNR.

It is important to note that the QA amplifier does not digitize the signal like an ADC because it produces a combination of liquid bits and analog residues. Hence, the LM algorithm, which assumes full digitization, is not suitable for SNDR optimization of the QA amplifier. Nevertheless, the same intuition can be applied to explain why non-uniform quantization could be advantageous for the QA amplifier. For the thermal noise limited case, the SNDR can be maximized by reducing the noise for signal levels where the PDF is higher while allowing higher noise elsewhere. Therefore, we expect the optimized quantization levels to be more closelyspaced in the high PDF regions, affording the QA amplifier higher gain at these signal levels so that the input-referred noise (IRN) is lowered. One challenge is that non-uniform level spacing will result in considerable gain variation, since less-frequently arising input signal levels will experience lower gain through the QA amplifier. Fortunately, the ALC can digitally correct for this gain variation. In what follows, we quantify the improvement of such optimization.

D. GA OPTIMIZATION FOR THERMAL NOISE LIMITED SNDR

The SNDR of the QA amplifier could be limited by either distortion or thermal noise. Therefore, it is important to study the two scenarios separately. The small-signal distortion of the QA amplifier depends on the overlap, which is controlled by the total number of slices [1]. For the simulations presented hereafter, the number of slices used in the QA amplifier are 32 and 16, in order to emulate a noise limited scenario and a distortion limited scenario, respectively. We first consider the case where the SNDR is limited by thermal noise. The QA amplifier has 32 slices (N = 32), and the IRN of each unsaturated slice has a total integrated power of $1.98 \times 10^{-7} V^2$.

1) EIGHT-TONE INPUT

The GA is initialized with uniform quantization levels, and the level spacing is chosen from an exhaustive search to maximize the SNDR before the optimization. The SNDR adaptation is shown in Fig. 11(a). The SNDR improvement is from 54.3 dB to 58.0 dB (by 3.7 dB) over 200 generations



FIGURE 11. QA amplifier (N = 32) GA adaptation for (a) eight-tone input (b) sinusoidal input.



FIGURE 12. QA amplifier (N = 32) gain with uniform and non-uniform (genetic) quantization levels under eight-tone input when SNDR is noise-limited (a) pre-ALC (b) post-ALC.

of the GA. The initial and final quantization levels are shown in Fig. 9.

As expected, the GA concentrates the quantization levels so that the QA amplifier gain is higher where the input PDF is higher, as shown in Fig. 12(a). Although the resulting QA amplifier gain is non-linear, it is corrected by the digital ALC as shown in Fig. 12(b). This confirms the prediction that the optimal levels shall be distributed such that the IRN is lower for signal levels where the input arises more frequently.

2) SINUSOIDAL INPUT

The GA adaptation for the sinusoidal input scenario is shown in Fig. 11(b). The SNDR improvement is from 62.2 dB to 63.9 dB (by 1.7 dB) over 200 generations of the GA. The initial and final quantization levels are shown in Fig. 10.

In contrast to the eight-tone input, a sinusoid is more likely to be sampled at its peaks, so we expect the optimized quantization levels to produce higher gain near the peaks of the input signal, as shown in Fig. 13(a). Similar to the eight-tone case, the non-linearity of the QA amplifier gain is corrected by the ALC, as shown in Fig. 13(b).

E. GA OPTIMIZATION FOR DISTORTION LIMITED SNDR

We now consider the case where the SNDR of the QA amplifier is limited by distortion caused by the gain ripple in the input-output transfer characteristics. Although this distortion can be reduced by increasing the overlap between the slices [2], the penalty is either a reduction of the input



FIGURE 13. QA amplifier (N = 32) gain with uniform and non-uniform (genetic) quantization levels under sinusoidal input when SNDR is noise-limited (a) pre-ALC (b) post-ALC.



FIGURE 14. QA amplifier (N = 16) GA adaptation for (a) eight-tone input (b) sinusoidal input.



FIGURE 15. QA amplifier (N = 16) quantization levels before and after the GA optimization for eight-tone input when the SNDR is distortion-limited.

range or the use of impractically large number of slices, which inevitably results in substantial chip area and design complexity (e.g., 100 as done in [1]). Thus, the possibility of using non-uniform quantization to reduce the gain ripple becomes very attractive because it does not necessarily compromise the input range expansion of the QA amplifier. To emulate a distortion-limited scenario, the number of QA slices is reduced to 16 to increase the gain ripple and the simulations are performed with noise sources turned off.

1) EIGHT-TONE INPUT

The GA improves the SNDR from 64.3 dB to 71.7 dB (by 7.4 dB), as shown in Fig. 14(a). It is important to note that noise is completely neglected in the simulation so the SNDR values only reflect the signal to distortion power ratio. The initial and final quantization levels are shown in Fig. 15.



FIGURE 16. QA amplifier (N = 16) gain with uniform and non-uniform (genetic) quantization levels under eight-tone input when SNDR is distortion-limited (a) pre-ALC (b) post-ALC.



FIGURE 17. QA amplifier (N = 16) quantization levels before and after the GA optimization for sinusoidal input when the SNDR is distortion-limited.



FIGURE 18. QA amplifier (N = 16) gain with uniform and non-uniform (genetic) quantization levels under sinusoidal input when SNDR is distortion-limited (a) pre-ALC (b) post-ALC.

We expect the optimal quantization levels to be distributed such that the post-ALC gain of the QA amplifier has as little ripple as possible, especially for the signal levels where the input arises more frequently, as shown in Fig. 16.

2) SINUSOIDAL INPUT

The SNDR adaptation is shown in Fig. 14(b). The SNDR improvement is from 68.8 dB to 79.9 dB (by 11.1 dB). Again, this SNDR value only reflects the signal to distortion power ratio. The initial and final quantization levels are shown in Fig. 17. Similar to the eight-tone scenario, the GA-optimized levels are distributed such that the post-ALC QA amplifier gain has as little ripple as possible, despite the fact that the pre-ALC gain is non-linear, as shown in Fig. 18.



TABLE 1.	Comparison between GA optimization and $\mu\text{-law}$ optimization for noise
limited SND	IR.

Input	PAPR [dB]	SNDR Uniform	SNDR GA	SNDR µ-law	Optimal µ
		[dB]	[dB]	[dB]	
8-tone	12	54.3	58.0	57.7	10.67
Sinusoid	3	62.2	63.9	63.0	-1.67

F. µ-LAW OPTIMIZATION

Although the GA is a powerful algorithm that can optimize the OA quantization levels and improve the performance significantly, it still suffers from the time complexity because it requires the evaluation of the cost function for a large number of candidate V_{os} distributions. The fundamental challenge is the complexity of the N-dimensional search space of V_{os} . This motivates the need for a heuristic that can constrain the search space. Through application of the GA, we notice that the QA amplifier SNDR (noise-limited) is improved by concentrating the quantization levels in the region where the input PDF is high. This insight allows us to reduce the dimensionality of the optimization search space. Specifically, µ-law is a coding algorithm originally proposed for companding audio signals in digital transmission with only one free parameter [27]. We propose a modified μ -law to parameterize the compression or expansion of the QA quantization levels resulting in performance similar to that achieved by global optimization using the GA, but without running a long GA simulation.

The proposed μ -law search method is a two-dimensional parameter sweep to find the SNDR-optimal quantization levels. The first parameter is μ , which controls the degree of logarithmic compression or expansion. First, a uniform level distribution between -1 and 1 is created:

$$U_{os} = \left[u_{os,1} \, u_{os,2} \cdots \, u_{os,i} \cdots \, u_{os,N} \right]^T$$

Then the distribution is compressed or expanded by:

$$v_{os,i} = \delta_{max} \cdot \begin{cases} \operatorname{sgn}(u_{os,i}) \frac{(1+\mu)^{|u_{os,i}|} - 1}{\mu}, & \mu > 0\\ u_{os,i}, & \mu = 0 \\ \operatorname{sgn}(u_{os,i}) \frac{\ln(1-\mu|u_{os,i}|)}{\ln(1-\mu)}, & \mu < 0 \end{cases}$$

where δ_{max} sets the degree of linear compression and it equals to the maximum value in the V_{os} array. Note that equation (2) logarithmically compresses the quantization levels when $\mu > 0$, and expands the quantization levels when $\mu < 0$. Thus, the SNDR of the QA amplifier can be evaluated as a function of μ and δ_{max} . Since there are only 2 parameters, an exhaustive search of all reasonable values of μ and δ_{max} can be performed to find their global optimum.

The same SNDR simulation setup as the GA is used to evaluate the 2D search surface for μ -law optimization. The SNDR performance surfaces for the thermal noise limited cases are shown in Fig. 19, and the results are summairzed in Table 1 in comparison with the GA. It is expected that the GA, which is a global optimizer, will provide more optimal



FIGURE 19. QA amplifier (N = 32) SNDR (noise-limited) μ -law search surface with (a) eight-tone input (b) sinusoidal input.

results than the μ -law 2D search because μ -law operates on a restricted performance surface. In other words, it is possible that the SNDR-optimal levels do not precisely correspond to the μ -law logarithmic compression or expansion. However, the μ -law 2D search is much more efficient despite using an exhaustive search. Each 2D search surface shown in Fig. 19 only requires the SNDR to be evaluated 256 times, compared to 8000 required by the GA global optimization. Further reductions in the complexity of the optimization may be obtained by applying more efficient algorithms on the 2D search surface, such as simulated annealing, particle swarm, or a GA, to find the best values for μ and δ_{max} .

In comparison with the GA, which is a global optimizer, the proposed μ -law method is a heuristic to achieve similar results using less time. It is reasonable to assume that the GA will work for many other possible operative scenarios that are not yet analyzed because it is a global optimizer which does not rely on information about the performance space. However, the same assumption cannot be made for μ law. The μ -law method is proposed to reduce the complexity of optimization for the scenarios which we have considered so far.

G. OPTIMIZATION UNDER VARYING INPUT POWER

The key benefit of QA signal processing is that the DR can be reconfigured to fit different input scenarios. This is demonstrated using measurement results in [1]; specifically, by increasing the quantization level spacing, the 1-dB compression point of the QA amplifier increases faster than the noise figure. However, the QA topology in [1] only allows the quantization levels to be uniformly distributed because the offset voltages are generated using a resistive ladder. In what follows, we quantify the improvement obtained with nonuniform quantization in comparison with what the existing QA topology allows.

Fig. 20 shows the relationship between SNDR and input power under 3 optimization settings, for a QA amplifier with 32 slices, each having an IRN of $1.98 \times 10^{-7} V^2$. The input to the QA amplifier is an eight-tone signal, and the full-scale is defined as the spacing between the maximum and minimum v_{os} , which is equal to 1 V_{pp} .



FIGURE 20. QA amplifier (N = 32) optimization under three different settings.

The "Uniform Optimized" setting emulates the existing QA topology in [1], where the quantization levels are allowed to be compressed or expanded while maintaining a uniform distribution. This allows the QA amplifier to take advantage of both the low-noise configuration and the high compression point configuration. The low-noise configuration is when the level spacing is minimized to maximize the QA amplifier gain, and the high compression point configuration is when the level spacing is maximized to expand the input range. This allows the relationship between the SNDR and the input power to have a slope less than 1, as shown in Fig. 20.

Both the "µ-law Optimized" and the "GA Optimized" settings provide approximately 3 dB SNDR improvement compared to the "Uniform Optimized" setting at high input power. This two-fold improvement in SNDR is equivalent to saving half of the power consumption. As the input power drops, the optimized SNDR using non-uniform levels slowly approaches the "Uniform Optimized" SNDR because as the level spacing reduces, in the extreme case, all slices would be overlapping with each other, and the QA amplifier practically becomes a single amplifier. In other words, both uniform and non-uniform quantization levels approach the same distribution when all the slices are overlapped for the low-noise configuration.

H. HARDWARE COMPLEXITY OF NON-UNIFORM LEVEL GENERATION

Although non-uniform quantization may require extra hardware complexity to allow each offset voltage to be adjusted individually, its SNDR performance boost should not come with notable penalty on either power consumption or design effort. For wireless communication applications where the system needs to be calibrated periodically, the offset voltages can be set during the calibration phase and remain static afterwards. Hence, these offset voltages can be generated by low power, medium resolution DACs that can be easily designed without any stringent bandwidth requirements. One candidate is a resistor string DAC with *N* outputs, each one provides the DC bias point for a sub-amplifier [8]. This allows all the bias voltages to be generated by a single DAC which consumes little static power. Furthermore, it would be unnecessary to make the DAC resolution finer than the IRN of each slice. This work assumes 10-bit resolution for the offset added to each line.

I. RECONFIGURATION TIME

Assuming that the input PDF for the common operative scenarios can be stored in the firmware, we can use the proposed optimization algorithms to obtain the V_{os} distribution for each input PDF so that there is a one-to-one relationship between each PDF and the optimized V_{os} . The initial ALC weights are also unique for each V_{os} since they are determined using the quadratic programming method as in Appendix B. Hence, the optimized V_{os} along with the ALC weights for the common input scenarios can be stored in a look-up table using the input PDF as the keys. Thus, the reconfiguration time of the QA quantization levels can be reasonably estimated by the time it takes to obtain the input PDF. In this work, the signal PDF for each scenario is obtained using 1000 samples. For example, assuming that a baseband ADC has a sampling rate of 200 MSPS, then 5 µs is required to obtain the input PDF, which is much less than the 0.2 ms transmission time interval size for hybrid automatic repeat request in 5G mission-critical communication applications [28].

IV. CONCLUSION

An all-digital calibration method using the ALC with the LMS algorithm is introduced to correct for the mismatch effects in the QA front-end. Since the calibration algorithm does not require uniform quantization for the QA amplifier, non-uniform quantization can be applied to achieve better system performance. The optimal quantization levels can either be obtained by global optimization using the GA or closely approximated using the modified μ -law as a heuristic. Compared to the existing QA topologies, all of which adopt uniform quantization, the proposed optimization algorithms can achieve 3 dB higher SNDR by taking advantage of non-uniform quantization under a multitone input.

APPENDIX A QA AMPLIFIER BEHAVIORAL MODELING USING HYPERBOLIC TANGENT FUNCTIONS

A behavioral model for the CMOS inverter amplifier is constructed to shorten the simulation time, particularly for the proposed optimization algorithms. Since the optimizers in this work only consider the DC characteristics of the QA amplifier, the inverter amplifier can be modelled by fitting mathematical functions into the DC voltage transfer characteristics obtained from SPICE simulations.

The fitting function is a combination of T hyperbolic tangent functions. Let x and y be the input and output voltage of the behavioral inverter amplifier. The fitting function is:

$$y = \sum_{i=1}^{T} p_i \tanh\left(q_i(x-c)\right) + d \tag{3}$$



FIGURE 21. (a) QA amplifier DC voltage transfer characteristics comparison with tanh behavioral model (b) QA amplifier DC gain comparison with tanh behavioral model.

where $Q = [q_1 \ q_2 \ \cdots \ q_i \ \cdots \ q_T]$ is a user defined vector controlling the sharpness of each tanh function and $P = [p_1 \ p_2 \ \cdots \ p_i \ \cdots \ p_T]$ along with *c* and *d* are determined from parameter fitting.

An inverter amplifier is first designed in 28nm CMOS technology, with both PMOS and NMOS devices having W = 280nm, L = 30nm and fingers = 16. The behavioral model used in this work consists of T = 5 hyperbolic tangent functions and $Q = -[10\ 15\ 20\ 25\ 30]$. The arrived-at fitting parameters are: $P = [0.7281\ -1.597\ 1.997\ -0.6\ -0.02731]$, c = 0.4683 and d = 0.5023. The fitted function, along with the inverter voltage transfer characteristics obtained from SPICE simulation, is shown in Fig. 21(a). The resulting small-signal gain of the behavioral model in comparison with SPICE simulation is shown in Fig. 21(b).

APPENDIX B OBTAINING THE ALC WEIGHTS USING QUADRATIC PROGRAMMING

Let x be the variable representing the input voltage to the QA amplifier; let f(x) be the voltage transfer function of one QA amplifier slice and let g(x) be the overall voltage transfer function of the entire QA amplifier consisting of N slices, then:

$$g(x, W) = \sum_{i=1}^{N} w_i \cdot f(x + v_{os,i})$$
(4)

where $v_{os,i}$ and w_i are the offset voltage and ALC weight of each slice, respectively. Then the small-signal gain of the QA amplifier is the first derivative of g(x, W) with respective to x:

$$h(x, W) = \frac{\partial g(x, W)}{\partial x} = \sum_{i=1}^{N} w_i \cdot f'(x + v_{os,i})$$
(5)

Let G be the desired DC gain of the QA amplifier and let ε be the error between the desired gain and the actual gain:

$$\varepsilon(x, W) = h(x, W) - G \tag{6}$$

We can take *L* samples of the gain error $\varepsilon(x, W)$ over the entire input range of *x* and calculate the total squared gain

VOLUME 3, 2022

error:

$$\sum_{l=1}^{L} \left[\varepsilon(x_l, W) \right]^2 = \sum_{l=1}^{L} \left[h(x_l, W)^2 - 2h(x_l, W)G + G^2 \right]$$
(7)

The goal is to find the vector W containing the ALC weights such that equation (7) is minimized. We can drop the constant term in equation (7) and express the remaining terms as:

$$\rho(W) = \sum_{l=1}^{L} \left[h(x_l, W)^2 - 2h(x_l, W)G \right]$$
(8)

$$= \sum_{l=1}^{L} \left[\sum_{i=1}^{N} w_i \cdot f'(x_l + v_{os,i}) \right]^2$$
(9)

$$-2G\sum_{l=1}^{L}\sum_{i=1}^{N}w_{i}\cdot f'(x_{l}+v_{os,i})$$
(10)

We notice that $\rho(W)$ can be reduced to the form of the quadratic optimization problem:

$$\rho(W) = \frac{1}{2} W^T A W - B^T W \tag{11}$$

where A is an $N \times N$ matrix whose values are given by:

$$A_{i,j} = 2\sum_{l=1}^{L} f'(x_l + v_{os,i}) f'(x_l + v_{os,j})$$
(12)

and B is a column vector with N rows:

$$B_{i} = 2G \sum_{l=1}^{L} f'(x_{l} + v_{os,i})$$
(13)

The solution to finding the minimum of (11) can be obtained by solving $W = A^{-1}B$ or using the dedicated quadratic programming algorithms in MATLAB if additional constraints on W are needed.

APPENDIX C

IMPLEMENTATION OF THE GENETIC ALGORITHM FOR QUANTIZATION LEVEL OPTIMIZATION

Fig. 22 explains the GA used to optimize the quantization levels of the QA amplifier. The algorithm has five steps in total. Step 1 is choosing the initial parent(s). A parent is a vector V_{os} containing the offset voltages added at the input of each slice. If the GA is in its first cycle, the parent is one single uniform V_{os} ; otherwise, the parents are 3 survivors from the previous generation. Step 2 is the generation of the new V_{os} population through crossover, mutation and adding new random individuals. Crossover is the exchange of genetic information between the parents to generate offsprings. Each pair of the three parents generates one offspring through crossover. Let $V_{os,p1}$ and $V_{os,p2}$ be a pair of parents and let B_r be a vector containing N random boolean values with equal probability of 0 and 1. The offspring generated from crossover is:

$$V_{os,c} = B_r \odot V_{os,p1} + B_r \odot V_{os,p2} \tag{14}$$



FIGURE 22. GA procedure for optimization of the QA amplifier quantization levels.

Each of the three parents also generates 8 offsprings through mutation, which is modelled by adding Gaussian random variables to all elements in the parent V_{os} . The standard deviation of the Gaussian mutation is 2 mV. Moreover, 10 completely random V_{os} are added to the pool of offsprings in order to explore other points in the search surface. Thus, a new population of V_{os} is formed by combining the 3 parents, 3 offsprings from crossover, 24 offsprings from mutation and 10 new random individuals. The evaluation of the new population happens in two separate steps. In step 3, the ALC weights W corresponding to each V_{os} is obtained using the quadratic programming method as described in Appendix B. Then in step 4, the entire population is evaluated by the cost function SNDR. It is important to note that during the evaluation of SNDR, the ALC weights are fixed because they are pre-calculated in step 3. Finally, step 5 is the selection of the survivors based on the SNDR. The top 3 candidates with the highest SNDR are selected to be the parents of the next generation. The algorithm then goes back to step 2 and continues iteratively.

REFERENCES

- J. Musayev and A. Liscidini, "A quantized analog RF front end," *IEEE J. Solid-State Circuits*, vol. 54, no. 7, pp. 1929–1940, Jul. 2019.
- [2] J. Musayev and A. Liscidini, "Quantised inverter amplifier," *Electron. Lett.*, vol. 54, no. 7, pp. 416–418, 2018.
- [3] R. Van de Plassche, Integrated Analog-to-Digital and Digital-to-Analog Converters. Boston, MA, USA: Springer, 1994.
- [4] Y. Li and E. Sanchez-Sinencio, "A wide input bandwidth 7-bit 300-MSample/s folding and current-mode interpolating ADC," *IEEE J. Solid-State Circuits*, vol. 38, no. 8, pp. 1405–1410, Aug. 2003.
- [5] H. Pan and A. A. Abidi, "Signal folding in A/D converters," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 51, no. 1, pp. 3–14, Jan. 2004.
- [6] T. Caldwell, D. Alldred, R. Schreier, H. Shibata, and Y. Dong, "Advances in high-speed continuous-time delta-sigma modulators," in *Proc. IEEE Custom Integr. Circuits Conf.*, 2014, pp. 1–8.

- [7] J. Musayev and A. Liscidini, "Quantized analog RX front-end for SAW-less applications," in *Proc. IEEE 44th Eur. Solid State Circuits Conf. (ESSCIRC)*, 2018, pp. 306–309.
- [8] J. Musayev, "Integrated circuits for quantized analog signal processing," Ph.D. dissertation, Dept. Electr. Comput. Eng., Univ. Toronto, Toronto, ON, Canada, Nov. 2018.
- [9] D. G. Manolakis, V. K. Ingle, and S. M. Kogon, *Statistical and Adaptive Signal Processing*. Norwood, MA, USA: Artech House Publ., 2005.
- [10] Z. Ding, "Adaptive filters for blind equalization," in *Digital Signal Processing Fundamentals*, V. K. Madisetti and D. B. Williams, Eds. Boca Raton, FL, USA: CRC Press, 1999.
- [11] M. Ding et al., "A 2.4GHz BLE-compliant fully-integrated wakeup receiver for latency-critical IoT applications using a 2-dimensional wakeup pattern in 90nm CMOS," in Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC), 2017, pp. 168–171.
- [12] K.-D. Hwang and L.-S. Kim, "A 5 Gbps 1.6 mW/G bps/CH adaptive crosstalk cancellation scheme with reference-less digital calibration and switched termination resistors for single-ended parallel interface," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 61, no. 10, pp. 3016–3024, Oct. 2014.
- [13] Y.-L. Luo, A. Ershadi, R. Rady, K. Entesari, and S. Palermo, "A powerefficient 20–35 GHz MZM Driver with programmable linearizer in 28nm CMOS," in *Proc. Opt. Fiber Commun. Conf. Exhibition (OFC)*, 2021, pp. 1–3.
- [14] Y. Wang, L. Ye, H. Liao, R. Huang, and Y. Wang, "Highly reconfigurable analog baseband for multistandard wireless receivers in 65-nm CMOS," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 62, no. 3, pp. 296–300, Mar. 2015.
- [15] B. J. Thijssen, E. A. M. Klumperink, P. Quinlan, and B. Nauta, "30.4 A 370tW 5.5dB-NF BLE/BT5.0/IEEE 802.15.4-compliant receiver with >63dB adjacent channel rejection at >2 channels offset in 22nm FDSOI," in *Proc. IEEE Int. Solid State Circuits Conf. (ISSCC)*, 2020, pp. 466–468.
- [16] M. Jeong et al., "A 65nm CMOS low-power small-size multistandard, multiband mobile broadcasting receiver SoC," in Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC), 2010, pp. 460–461.
- [17] R. Oneţ, M. Neag, I. Kovács, M. D. Ţopa, S. Rodriguez, and A. Rusu, "Compact variable gain amplifier for a multistandard WLAN/WiMAX/LTE receiver," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 61, no. 1, pp. 247–257, Jan. 2014.
- [18] J. Kim and J. Silva-Martinez, "Low-power, low-cost CMOS directconversion receiver front-end for multistandard applications," *IEEE J. Solid-State Circuits*, vol. 48, no. 9, pp. 2090–2103, Sep. 2013.
- [19] S. Lloyd, "Least squares quantization in PCM," *IEEE Trans. Inf. Theory*, vol. 28, no. 2, pp. 129–137, Mar. 1982.
- [20] Y. Lin et al., "A study of BER-optimal ADC-based receiver for serial links," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 63, no. 5, pp. 693–704, May 2016.
- [21] R. Narasimha, M. Lu, N. R. Shanbhag, and A. C. Singer, "BERoptimal analog-to-digital converters for communication links," *IEEE Trans. Signal Process.*, vol. 60, no. 7, pp. 3683–3691, Jul. 2012.
- [22] L. Wang, Y. Fu, M. LaCroix, E. Chong, and A. C. Carusone, "A 64Gb/s PAM-4 transceiver utilizing an adaptive threshold ADC in 16nm FinFET," in *Proc. IEEE Int. Solid State Circuits Conf. (ISSCC)*, 2018, pp. 110–112.
- [23] D. E. Goldberg, Genetic Algorithms in Search, Optimization and Machine Learning. Reading, MA, USA: Addison-Wesley, 1989.
- [24] H. Shibata and N. Fujii, "Analog circuit synthesis by superimposing of sub-circuits," in *Proc. IEEE Int. Symp. Circuits Syst.*, vol. 5, 2001, pp. 427–430.
- [25] W. Kruiskamp and D. Leenaerts, "DARWIN: Analogue circuit synthesis based on genetic algorithms," *Int. J. Circuit Theor. Appl.*, vol. 23, no. 4, pp. 285–296, 1996.
- [26] S. Shahramian et al., "30.5 a 1.41pJ/b 56Gb/s PAM-4 wireline receiver employing enhanced pattern utilization CDR and genetic adaptation algorithms in 7nm CMOS," in Proc. IEEE Int. Solid- State Circuits Conf. (ISSCC), 2019, pp. 482–484.
- [27] B. Smith, "Instantaneous companding of quantized signals," *Bell Syst. Tech. J.*, vol. 36, no. 3, pp. 653–710, 1957.
- [28] K. I. Pedersen, G. Berardinelli, F. Frederiksen, P. Mogensen, and A. Szufarska, "A flexible 5G frame structure design for frequencydivision duplex cases," *IEEE Commun. Mag.*, vol. 54, no. 3, pp. 53–59, Mar. 2016.





QINGNAN YU (Member, IEEE) received the B.A.Sc. (High Hons.) and M.A.Sc. degrees in electrical engineering from the University of Toronto, Toronto, ON, Canada, in 2018 and 2021, respectively.

From 2016 to 2017, and in 2020, he was an intern with Analog Devices, Toronto, where he was involved in high speed analog-to-digital converter designs. In 2021, he returned to Analog Devices, where he is currently working as an Analog Integrated Circuit Design Engineer. His

research interests include system optimizations and digital algorithms for analog signal processing.



ANTONIO LISCIDINI (Senior Member, IEEE) was born in Tirano, Italy, in 1977. He received the Laurea (*summa cum laude*) and Ph.D. degrees in electrical engineering from the University of Pavia, Pavia, Italy, in 2002 and 2006, respectively.

He was a summer Intern with National Semiconductors, Santa Clara, CA, USA, in 2003, studying poly phase filters and CMOS low-noise amplifiers. From 2008 to 2012, he was an Assistant Professor with the University of Pavia and a Consultant with Marvell Semiconductors, Pavia,

in the area of integrated circuit design. In 2012, he moved to the Edward S. Rogers Sr. Department of Electrical and Computer Engineering, University of Toronto, Toronto, ON, Canada, where he is currently an Associate Professor. In 2019, he has become Consultant with Huawei Technology Group in the area of RFIC for optical communication. His research interests are focused on analog mixed signal interfaces with particular emphasis on the implementations of transceivers and frequency synthesizers for wireless-wireless-wireless-wireless.

Dr. Liscidini was a recipient of the Best Student Paper Award at the IEEE 2005 Symposium on VLSI Circuits, a co-recipient of the Best Invited Paper Award at the 2011 IEEE CICC and Best Student Paper Award at the 2018 IEEE ESSCIRC. He is currently an Associate Editor of IEEE Open Journal of Solid State Circuit Society and IEEE Solid State Circuit Letters. He has served as an Associate Editor for the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—PART II: EXPRESS BRIEFS from 2008 to 2011 and 2017 to 2018 and as a Guest Editor for the IEEE JOURNAL OF SOLID-STATE CIRCUITS in 2013 and 2016 and the Guest Editor of the IEEE RFIC VIRTUAL JOURNAL in 2018. He has been a member of the ISSCC TPC from 2012 to 2017, the ESSCIRC TPC from 2010 to 2018, and a member of the CICC TPC since 2019. Between 2016 and 2018, he has been a Distinguished Lecturer of the IEEE Solid-State Circuit Society.



TONY CHAN CARUSONE (Fellow, IEEE) received the Ph.D. degree from the University of Toronto in 2002.

He is a Professor with the Department of Electrical and Computer Engineering, University of Toronto. He has also been a Consultant to industry in the areas of integrated circuit design and digital communication since 1997 and is currently the Chief Technology Officer of Alphawave IP Group, Toronto, Canada. He coauthored the popular textbooks *Analog Integrated Circuit Design*

(along with D. Johns and K. Martin) and *Microelectronic Circuits*, 8th edition (along with A. Sedra, K.C. Smith and V. Gaudet). He was Editorin-Chief of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS II: EXPRESS BRIEFS in 2009. He coauthored the Best Student Papers at the 2007, 2008, and 2011 Custom Integrated Circuits Conferences, the Best Invited Paper at the 2010 Custom Integrated Circuits Conference, the Best Paper at the 2005 Compound Semiconductor Integrated Circuits Symposium, the Best Young Scientist Paper at the 2014 European Solid-State Circuits Conference, and the Best Paper at DesignCon 2021. He was an Associate Editor for the IEEE JOURNAL OF SOLID-STATE CIRCUITS from 2010 to 2017. He was a Distinguished Lecturer for the IEEE Solid-State Circuits Society from 2015 to 2017 and has served on the Technical Program Committee of several IEEE conferences, including the International Solid-State Circuits Conference from 2016 to 2021. He is currently the Editor-in-Chief of the IEEE SOLID-STATE CIRCUITS LETTERS.