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# IGZO-TFT-PDK: Thin-Film Flexible Electronics Design Kit, Standard Cell and Design Methodology

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**ABSTRACT** With the increasing demand for transparent/flexible displays, healthcare sensors, and robotics, there is a need to advance the development of thin-film transistors (TFTs) manufacturing and large-scale circuits. This paper has proposed an IGZO-TFT-PDK to aid the educators and research community to explore the circuit design space of dual-gate IGZO-TFT devices. To solve the tensile force-induced current variation problem in IGZO-TFT devices, an omni-directional device and its layout template with a compensation methodology that mitigates its variation are proposed. A layout template is also proposed to speed up the design development flow of both analog and digital IGZO-TFT circuits. Based on the proposed layout template, a tensile force-insensitive standard cell library is proposed. We have implemented a 32-bit carry select adder to validate the usability of the standard cell library.

**INDEX TERMS** Thin-film transistors, IGZO-TFT, electronics, process design kit, standard cell library, open-source.

## I. INTRODUCTION

THE DEMANDS for thin-film transistors (TFTs) have become prominent in transparent/flexible displays, healthcare sensors, and robotics due to their material flexibility and cheap manufacturing costs [1]–[4]. However, due to the lack of open-source platform for GaZnO (IGZO) TFT technology process, its related development in circuit design has been relatively slow compared to its CMOS counterparts. Therefore, an open-source process design kit (PDK) and a basic standard cell library should be made available to accelerate the learning curve of individuals in adopting new technology.

Besides the absence of open-source PDK for the community, there are also several design challenges in using these TFT devices for flexible electronics before they can be broadly developed in the next generation of IoT and wearable products [5], [6]. TFT devices have been commonly limited to one type of device (n-type or p-type) due to their choice of semiconductor materials [7], [8]. It is challenging for circuit designers to directly use the existing CMOS design methodologies to design TFT-based circuits. In addition, due to the use of the flexible substrate, TFT circuits are usually subjected to tensile forces, causing variation in the channel current. Therefore, the need for a more robust TFT device will be very critical for the success of large-scale, highly integrated flexible electronics.

This paper has identified the problems in the studies of the TFT circuit design and has proposed an

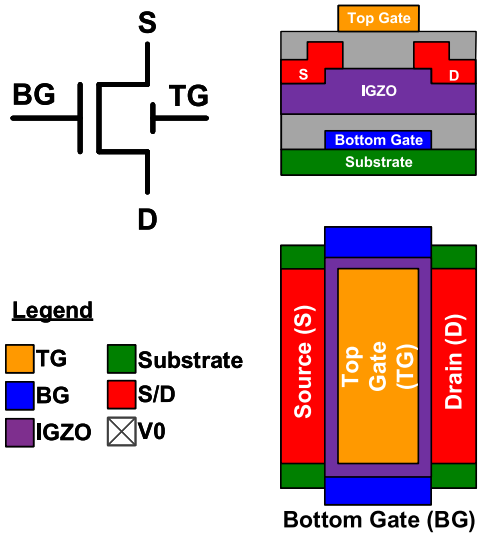


**FIGURE 1.** The schematic and graphical representation of a single IGZO-TFT device.

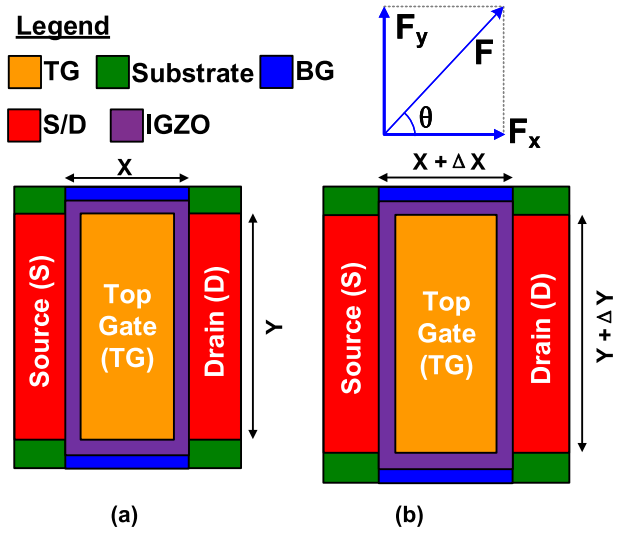


**FIGURE 2.** Illustration of IGZO-TFT and Poisson deformation caused by a tensile force. Top profile of the dual-gate IGZO-TFT device (a) without and (b) with a tensile force.

IGZO-TFT-PDK[1], that aids the design flow. The proposed IGZO-TFT PDK provides design files in GDS and LEF format, a series of scripts, and physical verification files which are commonly used in commercial EDA tools like Cadence Innovus, Virtuoso, and Mentor Calibre. To solve the tensile force-induced current variation problem in IGZO-TFT devices (Fig. 1), an omni-directional device and its layout template with a compensation methodology that mitigates its variation are proposed. Furthermore, a layout template is proposed to speed up the design development flow of both analog and digital IGZO-TFT circuits. Based on the proposed layout template, a tensile force-insensitive standard cell library is proposed. Educators and researchers can conduct IGZO-TFT circuit studies or design with the proposed open-source PDK and develop IGZO-TFT circuits on a larger scale.

The rest of this paper is organized as follows. Section II identifies the tensile force acting on the IGZO-TFT devices, causing huge variation in the device. It also details the design of an omni-directional IGZO-TFT device. Section III reviews the recent development of the open-source PDKs and discusses the content of our proposed IGZO-TFT PDK and standard cell library. Section IV discusses the design of the layout template for IGZO-TFT devices and how it can be used to develop the standard cell library. Section V discusses the design of a 32-bit carry select adder to validate the usability of the standard cell library. Section VI concludes this paper.

## II. CHALLENGES WITH IGZO-TFT DEVICE AND PROPOSED STRUCTURE

### A. TENSILE FORCE-INDUCED CURRENT VARIATION IN IGZO-TFT DEVICE

The IGZO-TFT devices on the flexible substrate are subjected to tensile forces, causing a large variation in their electrical performance [9], [10]. According to the Poisson effect [11], the ratio of the transverse deformation ($\varepsilon_t$) and the axial deformation ($\varepsilon_a$) of the material can be derived as

$$\nu = -\varepsilon_t/\varepsilon_a = -F_t/F_a, \tag{1}$$

where $\nu$ is a constant determined by the physical characteristics of the material. This constant also equates to the ratio of the transverse component force ($F_t$) and the axial component force ($F_a$). The deformations caused in both directions can change the carrier mobility and threshold voltage of the IGZO-TFT channels. As illustrated in Fig. 2, a tensile force $F$ on an IGZO-TFT device in an arbitrary direction can be decomposed into component forces in $x$ and $y$ directions ($F_x$ and $F_y$), where $x$ direction refers to the direction parallel to the channel while $y$ direction refers to the direction perpendicular to the channel. Both component forces cause deformation (expansion or contraction) to the channel, changing the carrier mobility and threshold voltage in the corresponding direction. With the first-order approximation similar to [12], the relationship between the carrier mobility and threshold voltage with an arbitrary tensile force can be expressed as:

$$\mu = \mu_0 + \alpha F_x \tag{2}$$

$$V_{TH} = V_{TH0} + \beta F_x, \tag{3}$$

$$F_x = F\cos\theta - \nu F\sin\theta, \tag{4}$$

where $\mu$ and $V_{TH}$ are the carrier mobility and threshold voltage under a tensile force respectively while $\mu_0$ and $V_{TH0}$ are their original values when the tensile force is not applied to the IGZO-TFT device. $\theta$ refers to the acute angle value between the channel direction and the tensile force $F$. $\alpha$ and $\beta$ are constants determined by the physical characteristics of the material only [13].

1. Open-Source Design Kit and Basic Standard Cell Library - https://github.com/SJTU-YONGFU-RESEARCH-GRP/IGZO-TFT-PDK.

The tensile force-induced variation in the carrier mobility and threshold voltage of the IGZO-TFT device can result in variation of the current flowing through the IGZO-TFT channel. Prior study has shown that in specific cases, a change of the tensile force as small as 0.4% can lead to variation in the channel current of 6% [14]. As a result, the robustness and stability of the IGZO-TFT circuit are severely influenced by the tensile forces. These challenges have a direct impact on the timing closure of the large-scale IGZO-TFT-based digital design circuits, increasing the duration of the design cycle and the circuit's functionality risk. There have been studies on the Corbino circular transistor [15] to address the tensile force resilient TFT transistor designs but it is hard to scale down the circular shape due to lithography constraints in nanometer scale.

### B. OMNI-DIRECTIONAL IGZO-TFT DEVICE

To address the aforementioned challenges, several new types of IGZO-TFT device structure and new fabrication methods, such as dual-gate (DG) IGZO-TFT structures [16], [17], circular structure [18], dual-layer process [19], ultra-thin substrates [20], [21], mesh and strip patterning of device layers [22] and placing the devices close to the neutral bending plane [23], have been proposed to minimize the performance variations of IGZO-TFTs. However, most of these methods require complex fabrication methods, which will dramatically increase the manufacturing cost. We have yet to see any method that can well attenuate the mechanical effect under a purely tensile-force-loading condition.

Fig. 2 illustrates the dual-gate IGZO-TFT device, in which a bottom gate and a top gate can be controlled independently. The bottom gate of the IGZO-TFT device controls the IGZO-TFT channel similar to the gate terminal in a conventional n-type CMOS device. The top gate of the IGZO-TFT device can regulate the threshold voltage. The voltage bias on the top gate induces the change in the threshold voltage of the IGZO-TFT device, allowing additional control on the device's channel conductivity. Therefore, the utilization of the dual-gate structure gives the IGZO-TFT device the potential for higher stability compared to the single-gate structure.

Based on the dual-gate IGZO-TFT device, an omni-directional IGZO-TFT device design structure [12] offers a cost-effective method with minimized fabrication cost but compatibility for both bending and stretching conditions, minimizing the tensile force-induced drain current variation in the IGZO-TFT device. The layout of the omni-directional IGZO-TFT device is illustrated in Fig. 3 The omni-directional IGZO-TFT device consists of four IGZO-TFT devices connected in parallel, where the same terminals are connected except for the top gate terminals. Each top gate terminal is controlled independently to minimize the tensile force-induced drain current variation.

The effect of a tensile force on the carrier mobility and the threshold voltage is opposite in its transverse and axial direction. The effect of tensile forces along $x$ or $y$ directions

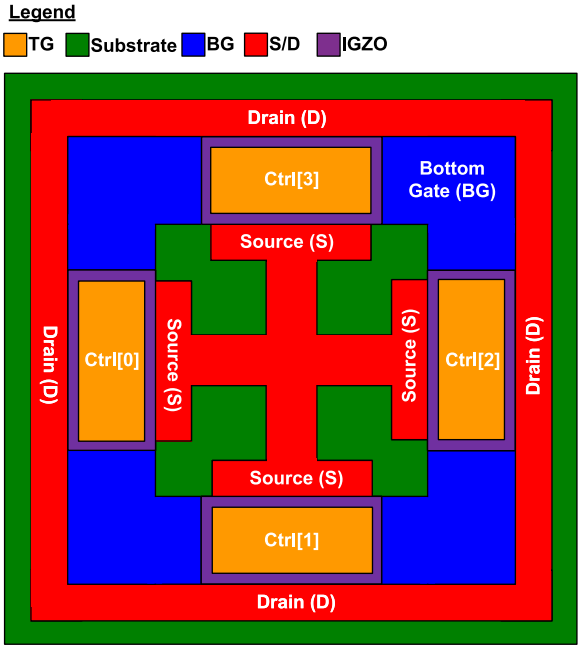


**FIGURE 3.** Graphical layout representation of the omni-directional IGZO-TFT device [12].

to the IGZO-TFT device channel current cancels out with itself, causing zero variation. This direction is the tensile force-insensitive axis of each device and can be represented by its angle with the channel, namely $\theta_t$. According to equation (1-4), $\theta_t$ can be determined as:

$$\theta_t = tan^{-1}\left(\sqrt{\frac{1}{\nu}}\right). \tag{5}$$

The omni-directional IGZO-TFT device allows the reconfiguration of the axis direction by selectively biasing *Ctrl[0]-[3]*.

## III. DEVELOPMENT OF IGZO-TFT PDK

### A. RESEARCH OPPORTUNITIES FOR PDKS WITH EMERGING DEVICES

To fabricate a design in a foundry, it is essential to translate the foundry's proprietary data into a collection of library files and provide programming scripts, which can be used with the commercial electronic design automation (EDA) tools [30]. These library files and programming scripts are collectively known as a process design kit (PDK). With the tight intellectual property (IP) control on PDKs, the academic and research groups are extremely limited in their ability to use them.

To overcome the aforementioned problem, open-source process design kit (PDK) promotes open collaboration among individuals, which allows copying, modifying, and redistributing of the PDK without paying royalties or fees. The first publicly available PDK, FreePDK45, was jointly developed by North Carolina State University (NCSU) and Oklahoma State University (OSU), based on 45nm predictive technology models [31]. Consequently, several

**TABLE 1.** List of open-source PDKs with its associated components.

| Reference | Library Name | Device Type | PDK Node | Company Institution | Circuit | | Layout | |
|---|---|---|---|---|---|---|---|---|
| | | | | | Design | Verification | Design | Verification |
| [24] | Synopsys PDK | CMOS | 14 or 28-<br>32 or 90 nm | Synopsys | Schematic<br>Device Model | Hspice<br>Verilog<br>Verilog-A | Pcell<br>Techfile | DRC Rule<br>LVS Rule<br>PEX |
| [25] | Cadence GPDK | CMOS | 45 or<br>90 or 180 nm | Cadence | Schematic<br>Device Model | Verilog<br>Verilog-A | Pcell<br>Techfile | DRC Rule<br>LVS Rule<br>PEX |
| [26] | APAS Pre-PDK | FinFET | 7 nm | ASU&ARM | Device Model | Spice | Pcell<br>Techfile | DRC Rule<br>LVS Rule<br>PEX |
| [27] | FreePDK15 | CMOS&FinFET | 15 nm | NCSU | Schematic<br>Device Model | Verilog | Pcell<br>Techfile | DRC Rule |
| [28] | FreePDK45 | CMOS | 45 nm | NCSU | Schematic<br>Device Model | Hspice<br>Verilog<br>Verilog-A | Pcell<br>Techfile | DRC Rule<br>LVS Rule<br>PEX |
| [29] | FreePDK15TFET | CMOS&TFET | 15 nm | SJTU | Schematic<br>Device Model | Hspice<br>Verilog<br>Verilog-A | Pcell<br>Techfile | DRC Rule<br>LVS Rule<br>PEX |

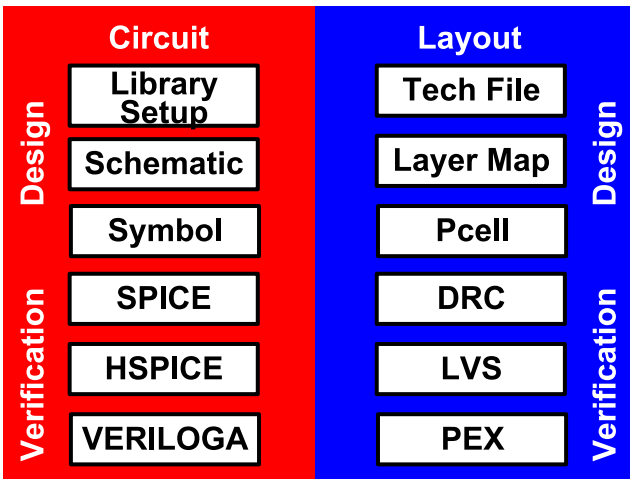


**FIGURE 4.** Basic components of PDK.

open-source PDKs are developed across 7nm to 180nm CMOS technologies, including Synopsys Generic Libraries 14nm, 28/32nm, 90nm [24], [32], Cadence University Program 45nm, 90nm, 180nm [25], ASAP PDK 7nm [26], and FreePDK 15nm [27], and 45nm [28]. There are improved versions of FreePDK with new add-on devices, such as RRAM [33] and MTJ [34], and TFET [29]. Table 1 summarizes the different types of open-source PDKs.

### B. DIFFERENT COMPONENTS OF PDKS

PDK can be broadly classified into four use-case models, i.e., (i) functional design, (ii) functional verification, (iii) physical design, and (iv) physical verification, as shown in Fig. 4. (i) Functional design is a design procedure where a circuit designer uses the circuit symbols and device model files from the PDK to translate a high-level design block into a circuit netlist. (ii) Upon completion of the design, the circuit designer performs functional verification to ensure that the circuit netlist meets the intended specifications. (iii) Subsequently, during the physical design phase, the layout designer draws the physical layout design based on the circuit netlist and the design constraints defined in the technology files, including the layer mapping file, the geometrical definitions, and constraints of each design data layer. (iv) Finally, the physical layout design is verified using physical verification rule files, containing the design rule check (DRC), layout versus schematic (LVS), to ensure that the layout complies with the mask fabrication rules and matches exactly with the netlist. 0

### C. IGZO-TFT PDK AND STANDARD CELL LIBRARY

To provide more opportunities for colleges, universities, and research institutions to design large-scale, highly integrated flexible electronics, this paper presents an open-source IGZO-TFT PDK and standard cell library, which fully support the design flow from schematic to layout and verification. The IGZO-TFT device supports Cadence Virtuoso layout and Mentor Calibre physical verification, which simplifies the IGZO-TFT circuit design flow.

In particular, as illustrated in Fig. 2, the IGZO-TFT device in the IGZO-TFT-PDK adopts a dual-gate TFT structure, in which a bottom gate and a top gate can be controlled independently. The schematic and its corresponding layout representation of a TFT IGZO device in the proposed IGZO-TFT PDK are illustrated in Fig. 1. Thus, the next section focuses on the design methodology of the omni-directional IGZO-TFT layout template and standard cell library for analog and digital circuit design, respectively.

## IV. PHYSICAL DESIGN OF OMNI-DIRECTIONAL DEVICES AND STANDARD CELLS

### A. OMNI-DIRECTIONAL IGZO-TFT LAYOUT TEMPLATE

The physical design of omni-directional transistor (Fig. 3) aims to minimize the local tensile force-induced current variation, which is highly suitable for small-scale analog circuit design. However, since the *Ctrl[0]* to *Ctrl[3]* control signal

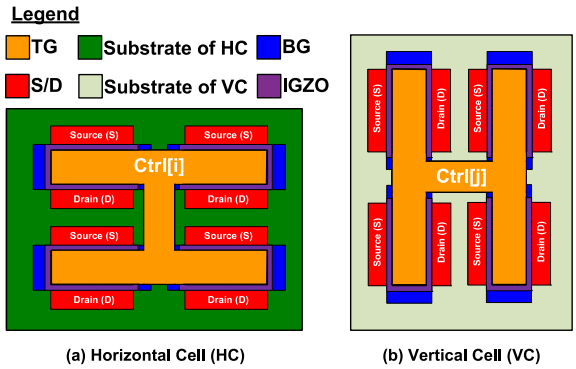


**FIGURE 5.** Graphical representation of layout template for the IGZO-TFT Device. (a) Vertical cell (VC) and (b) Horizontal cell (HC).

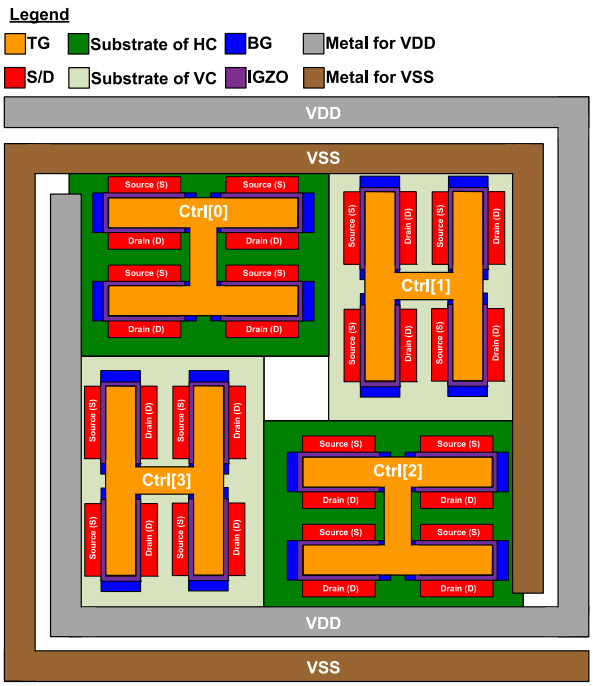


**FIGURE 6.** Graphical layout representation of a omni-directional IGZO-TFT standard cell design.

pins are being decentralized to each group of transistor, it is not very suitable for the digital standard cell design as it will result in complex routing congestion. Therefore, in this work, we proposed to use centralize the control signal pins as shown in Fig. 5. Fig. 5 illustrates the graphical representation of layout template for the omni-directional IGZO-TFT devices, namely the horizontal cell (VC) and the vertical cell (VC). The layout of both VC and HC has a cell height of 9 tracks (9T). As shown in Figs. 5(a) and (b), the IGZO-TFT devices within a VC have vertical channel directions while the IGZO-TFT devices within a HC have horizontal channel directions. VC and HC share the same input and output pins, circuitry function, and IGZO-TFT device sizing scheme.

Fig. 6 illustrates the graphical representation of an omni-directional IGZO-TFT device implemented with the layout template (Fig. 5). Within the omni-directional IGZO-TFT

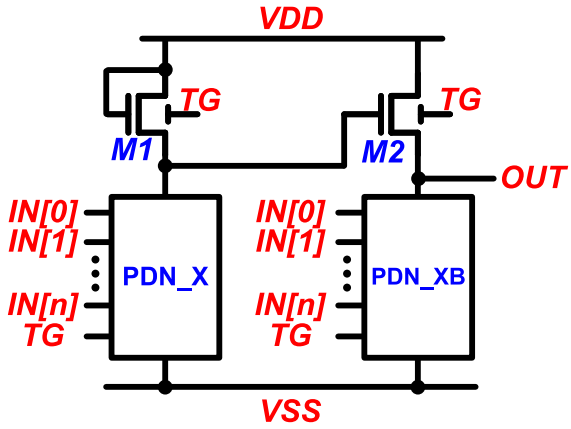


**FIGURE 7.** Illustration of the NMOS-logic-like Standard cell schematic design.

device, 2 VCs are located at the top-left and bottom-right corner while the 2 HCs are located at the top-right and bottom-left corner. It is worth noting that the layout symmetry of these cells can be mirrored along the x- or y-axis so long as the channel direction remains unchanged. To allow sufficient headroom for routing, the height of the overall omni-directional standard cell is 19T. The power rails of the omni-directional standard cell are arranged in a staggering manner, allowing an easier placement using cell flipping technique such that each cell is able access to *VDD* and *VSS* without causing DRC "short" errors. The cells share the same data input and output pins except for the top gate pins. These top gates are controlled individually with *Ctrl[0]* to *Ctrl[3]* signal pins. These signal pins control the channel conductivity, mitigating the variation of channel current caused by tensile forces. Therefore, the proposed IGZO-TFT layout template allows engineers to design a more consistent and robust physical design and verification, which makes it more easier for standard cell's characterization.

### *B. DESIGN METHODOLOGY OF OMNI-DIRECTIONAL STANDARD CELL*

Since IGZO-TFT devices are commonly limited to one type of device, the traditional standard cell topology involving both p-type and n-type devices is not applicable for IGZO-TFT. To address this challenge, a new design methodology is required to implement the IGZO-TFT omni-directional standard cells using the layout template. For each logic function, both VC and HC adopt a two-stage pseudo-nmos-like architecture illustrated in Fig. 7. Compared with traditional pseudo-nmos logic [35], the proposed architecture utilizes a second stage to boost the output range. The first stage of a sub cell is comprised of a resistive IGZO-TFT device *M1* with its bottom gate connected to *VDD* permanently and a pull-down network *PDN-X*. The logic function of *PDN-X* is identical to the logic function of the sub cell. The second stage consists of an IGZO-TFT device *M2* and a complementary pull-down network *PDN-XB*. The bottom gate of *M2* is connected to the output node of the first stage *N0*.

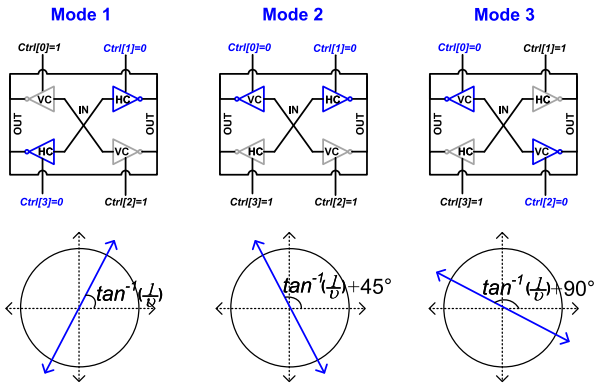


**FIGURE 8.** Three operating modes of the omni-directional standard cell and corresponding directions of force-insensitive axis.

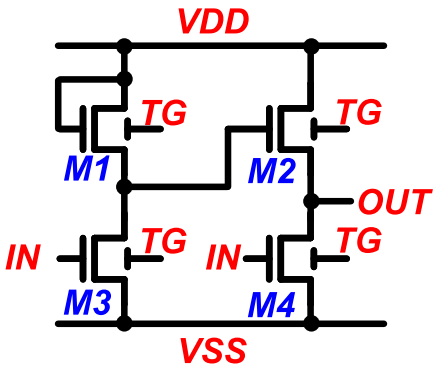


**FIGURE 9.** Design of an omni-directional IGZO-TFT inverter.

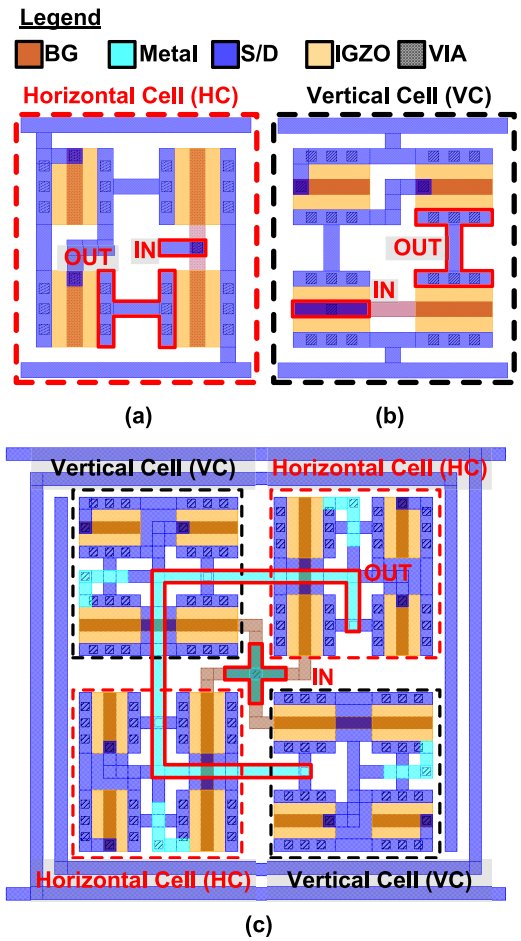


**FIGURE 10.** Physical layout of an omni-directional IGZO-TFT inverter.(a) Horizontal Cell (HC), (b) Vertical Cell (VC) and (c) Omni-directional IGZO-TFT Inverter.

The top gate of all the IGZO-TFT devices within the sub cell is connected to a common node *TG*. *IN[0]-[n]* are the data input pins and *OUT* is the data output pin.

As illustrated in Fig. 8, the omni-directional standard cell provides three different compensating modes for the arbitrary tensile force, each with a different tensile force-insensitive axis direction. The three modes are distinguished by the voltage bias at the control pins *Ctrl[0]-[3]* within the omni-directional standard cell. Thus, the variation in channel current within each standard cell can be minimized locally without affecting the overall performance at the top level. The omni-directional standard cell with globally connected and controlled top gates can be used to form larger digital circuits that are robust against tensile forces.

The working principle of this standard cell architecture is as follows.

**Mode1:** For an input pattern, if the *TG* pin has a logic level of "0" and the output of the logic function is "0", *PDN-X* is turned "ON" while *PDN-XB* is turned "OFF". Thus *N0* is discharged to a low voltage, turning *M2* "OFF". At the same time, output node *OUT* is discharged to *VSS* by *PDN-XB*.

**Mode2:** If the *TG* pin has a logic level of "0" and the output of the logic function is "1", *PDN-X* is turned "OFF" while *PDN-XB* is turned "ON". Thus, *N0* is charged to *VDD* by *M1*. *M2* is turned "ON" by *N0*, charging *OUT* to *VDD*.

**Mode3:** If the *TG* pin has a logic level of "1", the sub cell is turned "OFF".

### *C. EXAMPLE OF OMNI-DIRECTIONAL IGZO-TFT INVERTER DESIGN*

#### 1) SCHEMATIC DESIGN

An example of an omni-directional IGZO-TFT inverter and its layout are shown in Figs. 9 and 10, respectively. The IGZO-TFT devices within VC have vertical channels, while the IGZO-TFT devices within HC have horizontal channels. Both VC and HC adopt the standard cell design methodology proposed in Section IV-B, where IGZO-TFT devices *M1* and *M2* comprise the first stage while IGZO-TFT devices *M3* and *M4* comprise the second stage. When the input signal *IN* transits from *VSS* to *VDD*, IGZO-TFT device *M2* is turned "ON", pulling *N0* down. Thus IGZO-TFT device *M3* is turned "OFF" by *N0* while *M4* is turned "ON" by *IN*. As a result, output node *OUT* is pulled down to *VSS*. When *IN* transits from *VDD* to *VSS*, IGZO-TFT device *M2* and *M4* are turned "OFF", thus *N0* is pulled up by *M1*. As a result, IGZO-TFT device *M3* is turned "ON", pulling *OUT* to *VDD*.

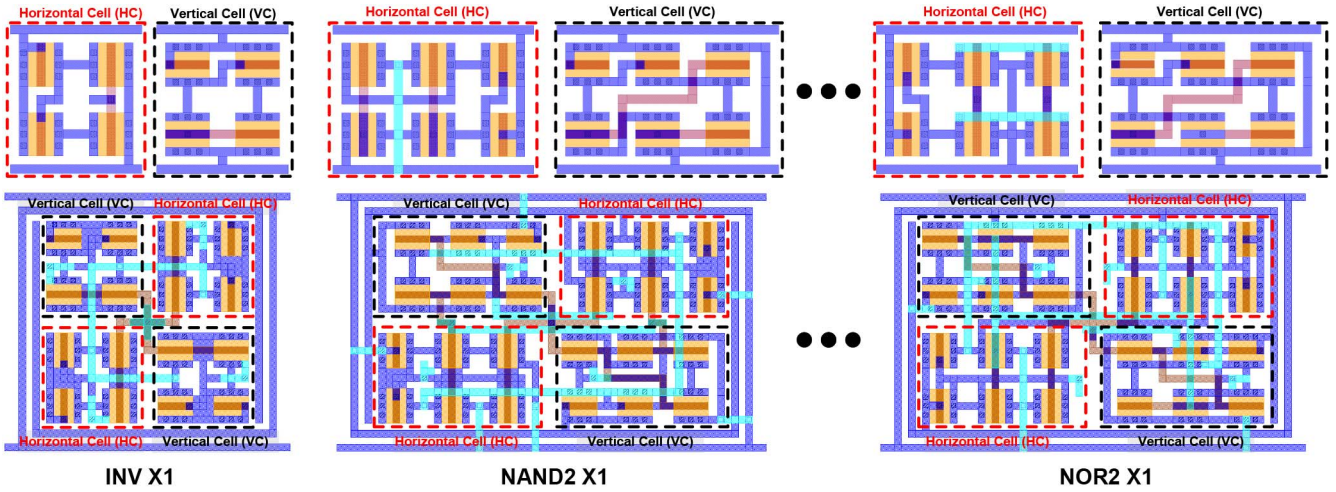


FIGURE 11. The proposed omni-directional IZGO-TFT standard cell library.

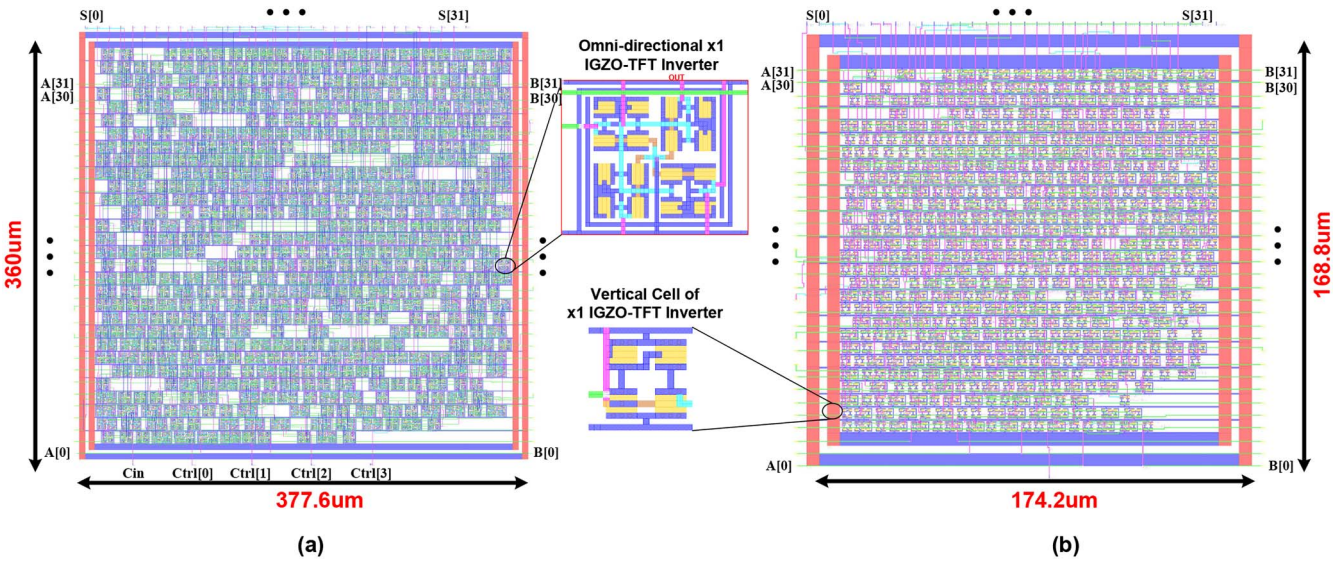


FIGURE 12. Layout of the 32-bit carry-select adders implemented with (a) omni-directional standard cells. (b) vertical sub cells.

### D. IGZO-TFT STANDARD CELL LIBRARY

Based on the aforementioned layout template, an omni-directional IGZO-TFT standard cell library is proposed, which includes more than 40 standard cells, with distinct functions NAND2, NAND3, NOR2, NOR3, AOI21, and D-Flip-Flop and so on with four driving strengths ($\times 1$, $\times 2$, $\times 4$, and $\times 8$). The standard cell library is implemented with Cadence Virtuoso and provides GDS and LEF file support for the full back-end digital design flow. An example of the physical layout design for various standard cells is illustrated in Fig. 11.

## V. CASE STUDY

To verify the proposed omni-directional standard cell library, a 32-bit carry-select adder has been implemented and the physical layout design is presented in Fig. 12(a). The carry-select adder is implemented with Cadence Innovus using the proposed IGZO-TFT standard cell library. This experiment has validated the compatibility of the proposed IGZO-TFT standard cell library. To assess the area penalty due to the proposed standard cell library using the layout template mentioned in Section IV-A, an additional 32-bit carry-select adder with the same architecture has been implemented with the VCs only. Fig. 12(b) has shown the 32-bit carry-select adder using VCs only.

TABLE 2. Resources comparison of the 32-bit carry-select adder implemented with omni-directional standard cells and traditional standard cells.

| | Omni-directional adder | Single-height adder |
|---|---|---|
| Standard Cell Numbers | 544 | 544 |
| Area ($\mu m^2$) | 135,936.00 | 29,404.96 |
| Standard Cell Height | 19T | 9T |

A comparison of the hardware resources of the two adders is given in Table 2. Comparing both designs, the 32-bit full adder implemented with 19T omni-directional standard cells incurred an additional 362.29% area. However, this trade-off

is essential to ensure the stability of the circuit under different conditions of tensile force.

## VI. CONCLUSION

To conclude, we believe that our proposed PDK will empower researchers to develop innovative large-scale electronic circuits, and educators can allow students to gain insight into emerging technologies. To solve the tensile force induced current variation problem in IGZO-TFT devices, an omni-directional device and its layout template with a compensation methodology that mitigates its variation is proposed. A layout template is also proposed to speed up the design development flow of both analog and digital IGZO-TFT circuits. Based on the proposed layout template, a tensile force-insensitive standard cell library is proposed. We have implemented a 32-bit carry select adder to validate the usability of the standard cell library. In the near future, we expect to continue to refine this TFT PDK with advanced design and verification supports, and IP designs in upcoming versions.

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