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# Analog and Mixed Signal Circuit Design Techniques in Flexible Unipolar a-IGZO TFT Technology: Challenges and Recent Trends

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**ABSTRACT** Advancements in the field of flexible electronics have enabled many novel applications such as wearables, flexible large-area displays, and textile-based sensor systems. A widely used semiconductor material for flexible electronics is amorphous indium gallium zinc oxide (a-IGZO). When compared to other semiconductors suitable for flexible technologies, this material is attractive for its higher mobility, better bias stability and improved uniformity. This paper presents an overview of current trends in analog and mixed signal circuit design and in architectures for a-IGZO TFT based sensor systems. We highlight the specific design challenges associated with the main sub-blocks found in sensors and bio-signal acquisition systems based on a-IGZO TFT technologies: front-end amplifiers and data converters. We then present an overview of several state-of-the-art sensor systems based on a-IGZO TFTs and their applications. Finally, conclusions are drawn, and a roadmap for the future development of analog and mixed signal circuit design in a-IGZO TFT is presented.

**INDEX TERMS** a-IGZO TFT, analog circuits, mixed signal circuits, flexible electronics, flexible wearable systems.

## I. INTRODUCTION

THE FIELD of electronics has witnessed a transformation phase in the recent years, due to the rapid growth of wearables and ubiquitous sensors and the advent of Internet of Things (IoT). Flexible electronics is increasingly recognized as a key enabler for novel sensor applications due to its low-cost, light weight, ultra-thin and large-area form factor, conformability and mechanical flexibility. The inherent flexible nature of the substrates in these technologies can be leveraged in applications requiring conformability, bendability, foldability and stretchability. A typical application example that can strongly benefit from flexible electronics is the domain of flexible and conformable wearable devices for wellness and healthcare monitoring.

Amorphous indium gallium zinc oxide (a-IGZO) [1] is considered to be one of the best options for implementing flexible electronic systems due to its comparatively higher mobility, large area uniformity, compatibility with low temperature processing and good bias stability, among flexible devices. The stability of a-IGZO TFTs is much greater than that of hydrogenated amorphous silicon (a-Si:H) and organic TFTs and is comparable to that of polycrystalline silicon (poly-Si) TFTs [2]. Moreover, a-IGZO devices have shown bendability upto 25 μm radius without damage [3]–[5] and can be stretched more than 200% [6]. Additionally, TFT scaling is possible in IGZO due to its amorphous nature [7], as grain boundaries will not interplay with the dimensions of the transistor and hence, TFTs can be scaled down to very short dimensions. a-IGZO TFT technology has also demonstrated high yield and integration capability, e.g., compared to organic TFTs. Indeed, integration of more than 50,000 devices (n-type TFTs and resistors) has been reported [8]. Thus, the a-IGZO TFT technology represents a good compromise between performance, technology reliability and cost.

However, when compared to mainstream silicon electronics, the physical properties of flexible a-IGZO TFTs still give rise to many challenges at circuit and system level, which can be summarized as follows:

1) Large flicker noise and high noise corner frequency [9] compared to silicon;
2) Lower power efficiency than silicon due to the lower mobility;
3) Parameter variability;
4) Unipolar devices with only n-type TFTs available;
5) Difficulty in interfacing with silicon-based circuits.

The large flicker noise and high noise corner frequency makes chopping less effective and increase low-frequency noise in amplifiers. The low intrinsic gain and the unavailability of complementary devices make high gain amplifiers difficult to realize and result in reduced accuracy when using negative feedback to overcome variability issues. These and other issues translate into the necessity of unconventional circuit and system design approaches for a-IGZO TFT circuits, as the well-known design techniques developed for complementary circuits cannot be applied. Hence, a circuit design approach considering specific technology constraints is mandatory.

There has been a strong research and industrial effort in a-IGZO TFT technology applications related to large area displays [10]–[13], flexible X-ray imagers [14]–[16], touchscreen tags [17]–[19], Radio Frequency Identification (RFID) [20], [21], Near Field Communication (NFC) tags [22]–[25], machine learning processing engines [26] and flexible microprocessors [8] in the last few years. This research was mainly focused on circuits and systems where the TFTs are used as switches, due to various challenges observed when trying to implement analog functions.

Recent advancements in processing technology have resulted in improved a-IGZO TFT performance, enabling more demanding applications [7]. As a consequence, novel applications can be envisioned using this technology, such as: physiological monitoring by wearable flexible health patches [27]–[30], temperature sensors [31], [32], display-integrated fingerprint sensors [33]–[35] and piezoelectric pressure sensing [36], [37]. However, analog and mixed signal circuit design in a-IGZO TFT technologies has not reached maturity yet.

Thus, in this paper we will present an overview of challenges and the recent trends in the design of a-IGZO TFT circuits. Several techniques that have been experimentally validated to improve analog and mixed signal designs are presented. In Section II, an introduction of a-IGZO TFT technology is provided. In Section III, we explain how technology limitations translate to challenges at the circuit and system design level when implementing analog and mixed-signal functions. Some of the state-of-the-art design approaches for a-IGZO TFT front-end amplifiers are presented in Section V. Furthermore, data conversion techniques recently implemented in a-IGZO TFT technology are discussed in Section VI. Section VII provides an overview of some of the sensor systems demonstrated using a-IGZO TFTs and their applications. Finally, we draw some conclusions and outline some future research directions in the field of analog and mixed-signal circuit design with a-IGZO TFT technology.

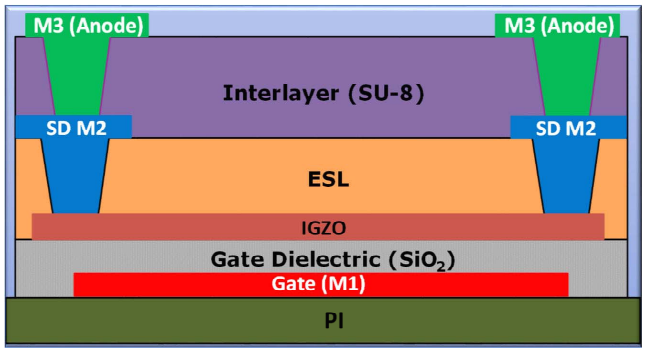



**FIGURE 1.** A simple bottom-gate a-IGZO TFT stack.

## II. A-IGZO TFT TECHNOLOGY

Fig. 1 shows the cross section of a typical single-gate a-IGZO TFT [38], [39]. It is based on Etch Stop Layer (ESL) approach. The device is fabricated by depositing different layers on top of a flexible substrate. The stack consists of three metal layers, an a-IGZO layer, dielectric layers (gate, ESL) and a passivation layer (interlayer). The maximum processing temperature is 350°C. a-IGZO TFTs typically show charge carrier mobility ($\mu$) of 15-20 $cm^2/V.s$, while the threshold voltage ($V_T$) varies between 0-2 V. Better speed performance compared to ESL TFT technology can be achieved by using self-aligned stacks, where the overlaps between gate, source and drain, and the parasitic capacitance that they cause, are minimized [12], [40]–[42]. The processing temperature of a-IGZO TFTs typically ranges between 150°C and 350°C. However, room temperature fabrication of a-IGZO TFT has also been reported [1], [43].

The device architecture of a-IGZO TFTs is an active field of research with many stack variants reported [44]. The device stack can either be bottom gate [45] or top gate [46], depending on deposition of gate electrode with respect to semiconducting layer. In the case of bottom gate devices, the gate electrode is below the semiconducting layer, while in top gate devices, the gate electrode is above the semiconducting layer. The TFT stack could further be categorized in coplanar [40] or staggered [47] topologies depending on source/drain contacts position with respect to the accumulated channel. In coplanar TFT stacks, source/drain contacts are on the same plane as the channel, while in staggered TFT stacks, source/drain contacts are on the opposite side of the channel. The performance of TFT device can be improved using double gate [48], [49] architectures. Indeed, the presence of an extra gate helps to control the channel more effectively, increasing the transconductance when front and back gate are shorted together. Alternatively, the second gate can be used to control via electric biasing the TFT threshold, a feature that can be extremely useful to

improve circuit behavior. To reduce channel length, non-planar TFT stack, such as such as vertical TFTs (VTFTs) or quasi-vertical TFTs (QVTFTs) have also been reported [50]–[54]. The use of different materials in the TFT stack and their effects on the electrical and mechanical performance of the device, along with the stability have been extensively investigated [55], [56]. The choice of the gate dielectric is an important factor for the performance of a TFT. The quality of the interface between gate insulator and channel has indeed a strong influence on the stability and the carrier mobility of the TFT, by controlling the charge trap density [55]. The most commonly used gate dielectric is aluminium oxide ($Al_2O_3$), which has comparatively high relative permittivity of 9.5, and provides a high-quality interface with a-IGZO [55]. Besides $Al_2O_3$, hafnium oxide ($HfO_x$), titanium oxide ($TiO_x$), silicon oxide ($SiO_2$) and silicon nitride ($SiN_x$) are also used as gate dielectrics.

TFT devices with high performance in terms of mobility and stability have been reported [57]–[59]. The typical supply voltage of a-IGZO TFTs ranges between 5-30 V, however recently a-IGZO TFTs operated at 1 V or less have been described [60], [61]. The nominal transition frequency ($f_T$) of these devices lies in the MHz regime [62]. However, scaling of channel length below the micrometer regime and minimizing the overlap capacitances has made possible to reach $f_T$ in the range of GHz [63], [64]. Recent reports have documented further scaling of IGZO TFTs channel lengths down to 160 nm [65] and 32 nm [66].

## III. CIRCUIT AND SYSTEM CHALLENGES

The physical properties of a-IGZO TFTs and their processing give rise to many challenges at circuit and system level, which are summarized here below.

### A. LOW FREQUENCY NOISE

The low-quality interface between dielectric and semiconductor, together with mobility fluctuation results in large low-frequency noise (1/f or flicker noise) in thin film transistors [9]. This 1/f noise component is the dominant noise contribution for bio-signal acquisition front-ends owing to the low frequency content of biomedical signals. Hence, low-frequency noise mitigation is the foremost challenge in designing bio-signal acquisition front-ends. Flicker noise can be suppressed by using chopping [67], but at the cost of larger bandwidth requirements. It can be decreased by increasing device area as well, which increases the input parasitic capacitance, reducing the input impedance. Discrete time circuit techniques such as auto-zeroing and correlated double sampling can also be exploited to mitigate 1/f noise [67]. However, such techniques require large capacitors which are difficult to integrate in a-IGZO TFT technology with acceptable yield, at the state-of-the-art.

### B. POWER EFFICIENCY

One of the main limitations of a-IGZO TFTs is their mobility, which is one to two order of magnitude smaller than mainstream silicon field effect transistors. Low mobility results in low transconductance ($g_m$) of the devices, which consequently limits the small-signal intrinsic gain ($g_m r_o$) and $f_T$. Moreover, the large oxide thickness in a-IGZO TFTs results in limited gate electrostatic control over the channel, which ultimately leads to larger supply voltages, even lower transconductance and more pronounced channel length modulation. Together with the considerable parasitic capacitances observed in non-self aligned TFTs, from the circuit design perspective, this results in low gain-bandwidth product (GBW) and low efficiency in terms of speed versus needed power.

### C. VARIABILITY

The low process temperature (compared to silicon fabrication), which is the enabler of mechanical flexibility, and the low-cost manufacturing of a-IGZO TFTs, result in large parameter variability and in poor intrinsic matching between identical neighboring devices. This has a particularly strong impact on analog circuit techniques and analog to digital conversion, which typically take advantage of the good matching offered by silicon technologies. If high accuracy a-IGZO TFT circuitry is required in an application, then system techniques like calibration might need to be applied.

### D. UNIPOLAR NATURE OF DEVICES

Complementing n-type a-IGZO TFTs with another material p-type TFTs on flexible substrates is quite challenging due to diffiAculties with hybrid integration [68]–[71]. The unipolar nature of the devices in a-IGZO TFT technology makes it difficult to exploit commonly used CMOS circuit techniques. Consequently, active loads with simple configuration and low transistor count are not available in unipolar technologies. The low intrinsic gain and the unavailability of complementary devices limit the achievable gain with unipolar a-IGZO TFT based amplifiers, which makes feedback architectures less useful.

### E. INTERFACES WITH SILICON-BASED CIRCUITS

Circuits consisting of a-IGZO TFTs generally require a high supply voltage due to thicker dielectrics, while state-of-the-art silicon-based integrated circuits are operated at supply voltages below 1 V. This inherent difference in supply voltage domains makes interfacing of flexible circuits with silicon based circuits in hybrid systems quite challenging.

Recent advances in technology have resulted in some fruitful results in the direction of low voltage flexible technologies. Recently, TFTs operating at 1-V or lower supply voltages have been reported [60], [61]. However, complex circuits built with such devices have still not been demonstrated. Some research groups have reported IGZO TFTs [72] which achieve low voltage operation (< 2 V) using an electrolyte as gate dielectric. The low voltage operation of electrolyte-gated TFTs is due to the large capacitance provided by the electrolyte [73]. However, electrolyte-gated

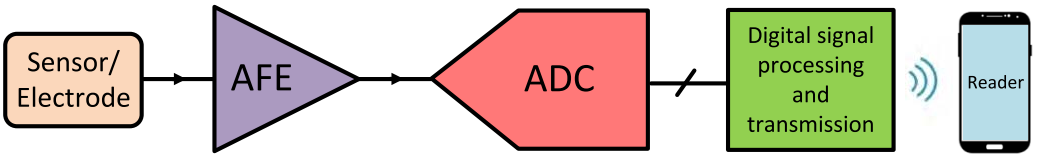



**FIGURE 2.** General architecture of a sensor acquisition system.

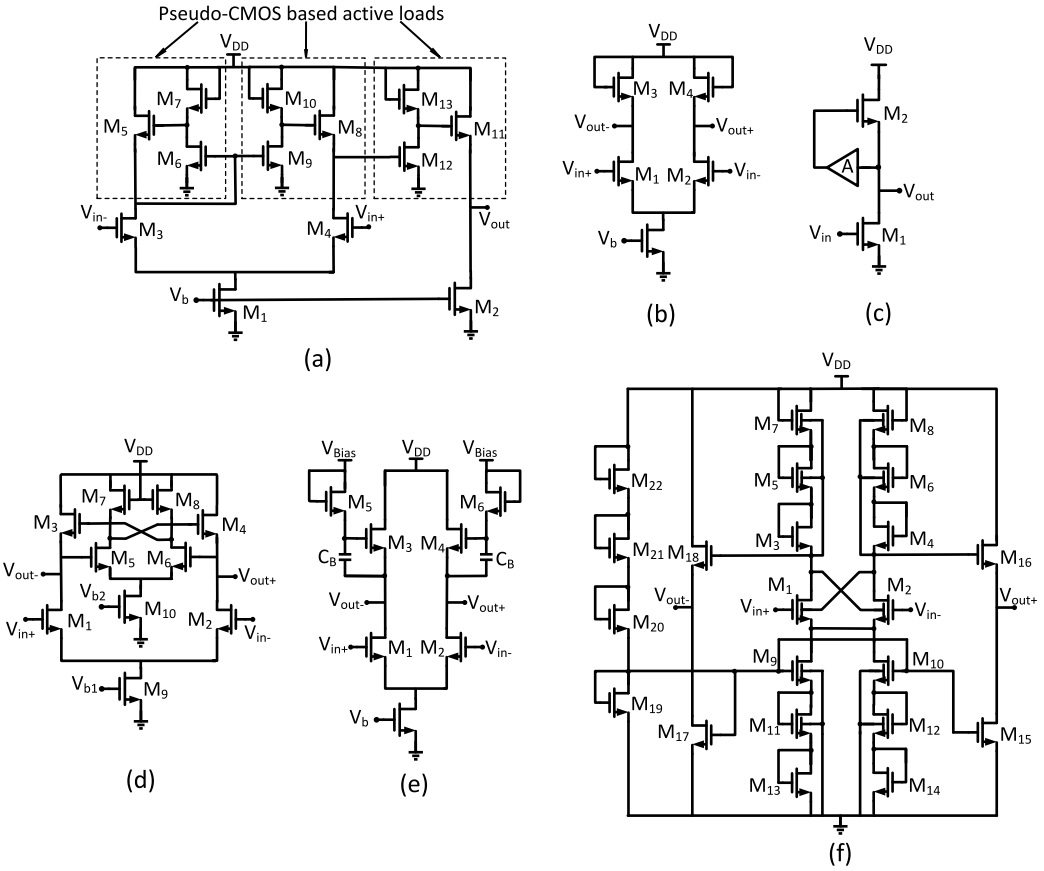



**FIGURE 3.** Different types of state-of-the-art a-IGZO TFT amplifiers. (a) Pseudo CMOS load amplifier [74], (b) Diode connected load amplifier, (c) Single ended positive feedback common source amplifier, (d) Differential positive feedback amplifier [31], (e) Bootstrap load amplifier [75], (f) Modified diode load amplifier [76].

TFTs have large parasitic capacitances, which results in reduced device speed.

## IV. ARCHITECTURE OF SENSOR ACQUISITION SYSTEMS

A typical implementation of a sensor acquisition system is shown in Fig. 2. The full acquisition chain comprises a sensor or electrode, an analog front-end (AFE), an analog to digital converter (ADC), a digital signal processing and transmission block, and a reader. The external analog quantity is picked by an electrode, or converted to the electric domain by a sensor. The sensor or electrode output is generally small, hence, amplification through an AFE is required. Conversion to digital representation is essential before transmitting signals to a reader device (e.g., smart phone), to increase noise immunity during transmission. This digital conversion and transmission process is performed by an ADC, digital signal processing and a transmission block.

The AFE is the most crucial analog building block, which is inevitably present in almost all sensor systems. The next section deals with the design techniques of front-end amplifiers based on a-IGZO TFTs.

## V. A-IGZO TFT BASED AMPLIFIERS

As mentioned in Section III, a-IGZO TFTs are only n-type. Different types of amplifiers depending on load configurations have been reported in a-IGZO TFTs. They can be broadly classified considering their load topologies among amplifiers in which the load mimimcs a p-type device behavior (often called pseudo-CMOS amplifiers) and amplifiers that exploit an n-type load (often supported by some output-impedance enhancement technique).

Fig. 3(a) shows the circuit schematic of a pseudo CMOS amplifier [74]. It consists of a pseudo-CMOS load, comprising 3 TFTs as shown in the enclosed box. The basic idea in this topology is to put an inverter in front of an n-type device

**TABLE 1.** Comparison of the state-of-the-art a-IGZO TFT amplifiers.

| | [77] | [28] | [31] | [78] | [79] | [75] | [80] | [76] | [74] |
|---|---|---|---|---|---|---|---|---|---|
| Amplifier topology | Diode connected load | Diode connected load | Positive feedback | Positive feedback | Positive feedback | Bootstrap load | Bootstrap load | Modified diode load | Pseudo CMOS load |
| Channel length [μm] | 6 | 15 | 15 | 15 | - | 15 | - | 15 | - |
| Supply voltage [V] | 5 | 10 | 20 | 15 | 6 | 10 | 20 | 20 | 5 |
| Maximum gain [dB] | 18.7 | 22 | 62.4 | 31.1 | 19 | 22.8 | 34 | 30 | 22.5 |
| Bandwidth [kHz] | 108 | 3 | - | - | 25 | 0.185-3.3 | 5 | 0.15 | 5.6 |
| Power dissipation [μW] | 900 | 32 | 104 | 87 | 6780 | 52 | 576 | 188.4 | 160 |

to obtain a transistor that behaves in a similar way to a p-type device. Although this solution tries to circumvent the unavailability of p-type TFTs, it requires very careful transistor sizing, exploiting accurate models, to enable stable operation.

The most conventional n-type load amplifier topology in a-IGZO TFT technology is the diode connected load amplifier [27], [28], [32], [75], [77]. It is popular due to its minimalistic design. A differential implementation of this topology is shown in Fig. 3(b). As the small-signal gain is given by a ratio of transconductances of TFTs ($\frac{g_{m1}}{g_{m3}}$), this topology in general, is less sensitive to parameter variability. In some applications, the gain of one stage may not be sufficient and hence cascading two stages may be required [27], [28], [75]. The availability of a dual gate a-IGZO TFT technology may enable further variations of the diode connected load amplifier topology [32]. The second gate of the device may be used to improve performance [81], e.g., the second gate can be connected to the source of the TFT to increase the output resistance. For input driver TFTs, the gates can be shorted together to improve the transconductance.

Another very common circuit technique which is employed in a-IGZO TFT amplifiers [29], [31], [78], [79], [82] is the use of a local positive feedback, shown in Fig. 3(c). The small-signal gain of this topology can be written as:

$$G = \frac{g_{m1}}{g_{m2}(1-A)} \tag{1}$$

If we design $A$ such that $|A| < 1$, then, the gain of this amplifier is enhanced by the factor $\frac{1}{1-A}$ compared to a diode connected load amplifier.

A TFT implementation of this gain enhancement technique is schematically presented in Fig. 3(d), for a fully differential amplifier [31]. The auxiliary amplifier consisting of TFTs $M_{5-8}$ and $M_{10}$ is used to provide the gain $A$: this reduces the $v_{gs}$ of the load TFTs $M_{3-4}$ and thus boosts the output impedance, increasing the gain. Ensuring the stability of the amplifier in presence of variations is crucial for this type of design in a-IGZO TFT technology, and is a design concern when using auxiliary amplifiers in positive feedback to boost the gain.

Another variant of the gain enhancement technique shown in Fig. 3(b) is displayed in Fig. 3(e), which is also known as a bootstrapped load amplifier [75], [80]. It uses a load comprising $M_3$ and $M_5$ with a bootstrapping capacitor $C_B$. The peculiarity of this load configuration is that, at low frequencies, $M_3$ acts as a diode-connected load offering a smaller gain, while at high frequencies, the capacitor $C_B$ shorts the gate of $M_3$ with its source, providing a zero-$V_{GS}$ load, and consequently higher gain. According to this simple analysis, this amplifier has a band-pass response, which is especially suited to biomedical applications, where the inherent DC electrode offset needs to be rejected. The band-pass response is also beneficial to avoid amplifier saturation due to mismatch and thus excessive offset. One major disadvantage of this amplifier topology is that it requires large bootstrapping capacitors $C_B$, and hence large area, due to two reasons. The first reason is that a large $C_B$ is required to realize low high-pass frequencies. Secondly, the capacitor $C_B$ and the parasitic capacitance from the gate of $M_3$ to ground form a capacitive divider. Hence, $C_B$ should have a very small impedance, to provide an effective zero-$V_{GS}$ load, i.e., to effectively short the gate and source of $M_3$.

Fig. 3(f) shows another n-type load amplifier design which is based on load enhancement and a positive feedback techniques [76]. The load configuration consists of the diodes $M_3$, $M_5$ and $M_7$ with top gates of diodes $M_5$ and $M_7$ connected to the source of $M_3$. This specific arrangement of load diodes increases the output resistance of $M_5$, consequently increasing the DC gain. The output resistance is given indeed by the expression:

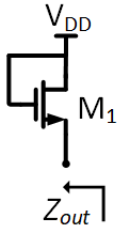
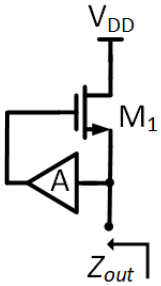
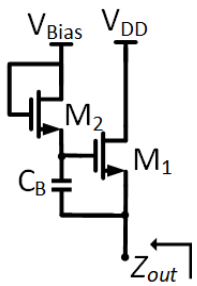
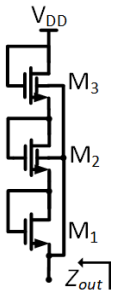
$$R_{out} = \frac{1}{g_{m7}} + \frac{1}{g_{m5}}(1+\eta) + \frac{1}{g_{m3}}(1+\eta)^2 \tag{2}$$

where, $\eta$ corresponds to the threshold modulation coefficient due to the second gate biasing, and $g_{m3}$, $g_{m5}$, $g_{m7}$ are the transconductances of $M_3$, $M_5$ and $M_7$ respectively. In the same amplifier, a partial positive feedback is also implemented by cross coupling the top gates of the input driver TFTs $M_1$ and $M_2$. This enhances both transconductance and gain. A buffer with a source follower configuration ($M_{16}$ and $M_{18}$) is also implemented at the output. Although, this peculiar arrangement of the load diode TFTs increases the gain, it also increases the sensitivity to mismatch and variations. This amplifier is also susceptible to input offset due to large gain at DC, which may result in amplifier saturation. Another drawback of this amplifier topology is its limited output swing due to large stack of TFTs.

Although, a-IGZO TFT based amplifiers are generally used in low frequency applications, there have been some reports, where large GBW amplifiers implemented with TFTs having few MHz $f_T$ have been demonstrated [83]–[88].

An overview of some state-of-the-art amplifiers in a-IGZO TFT technologies which compares several performance indicators is shown in Table 1.

**TABLE 2.** Different types of active load topologies for a-IGZO TFT based amplifiers.

| Load topologies |  |  |  |  |
|---|---|---|---|---|
| $Z_{out}$ | $\frac{1}{g_{m1}}$ | $\frac{1}{g_{m1}(1-A)+g_{ds1}}$ | $\frac{1}{g_{m1}(1-A_f)+g_{ds1}}$ where, $A_f = \frac{sR_{off,2}C_B}{1+sR_{off,2}C_B}$ | $\frac{1}{g_{m3}} + \frac{1}{g_{m2}}(1+\eta) + \frac{1}{g_{m1}}(1+\eta)^2$ |
| No. of Elements | 1 TFT | 1 TFT and a feedback amplifier | 2 TFTs and a capacitor | 3 TFTs in double gate technology |
| Pros | Robust | High output impedance | High output impedance with band pass response | High output impedance |
| Cons | Low output impedance | Stability concern | Large capacitor | Large voltage headroom |

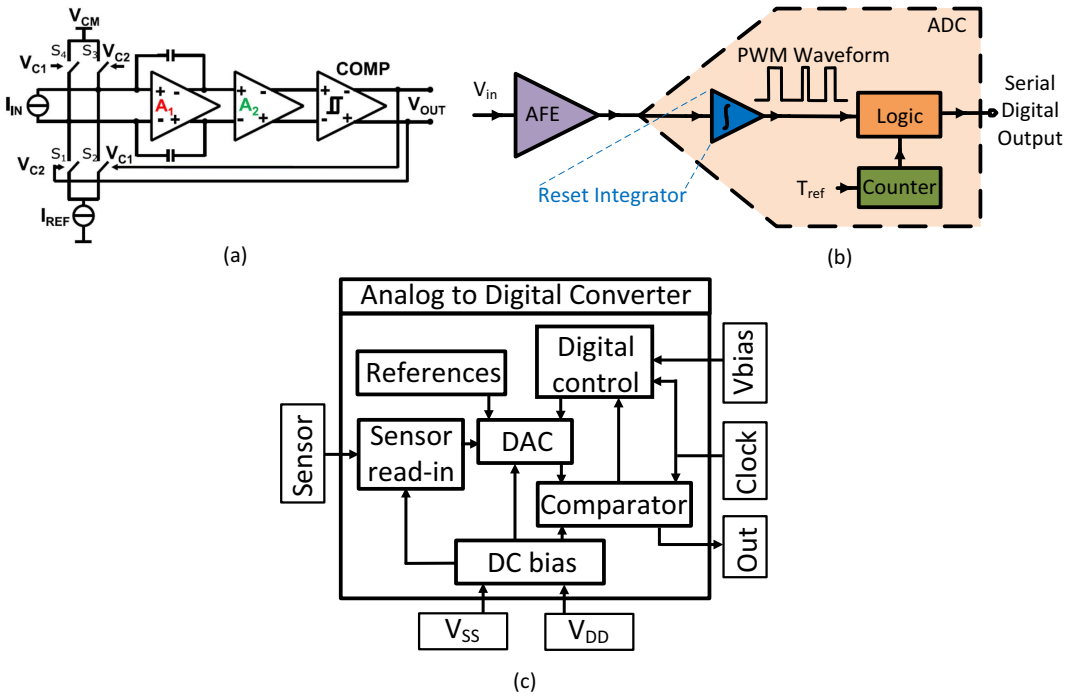



**FIGURE 4.** a-IGZO TFT based data converter architectures. (a) Asynchronous delta sigma modulator [31], (b) Reset integrator based ADC [27], (c) C-2C SAR ADC [32]. (a) Copyright 2017 IEEE. Reprinted with permission from [31].

Table 2 summarizes various active load topologies using n-type devices in a-IGZO TFT technology. It also compares their output impedance ($Z_{out}$), the number of elements required to realize the active load, and the main pros and cons of each circuit block.

## VI. DATA CONVERTERS BASED ON A-IGZO TFT TECHNOLOGY

The next block in the signal acquisition chain (Fig. 2) after the amplifier is the data converter. It is required to convert the analog signal at amplifier's output to a digital (multi-bit discrete time) or binary (two-level pulse-width modulated) representation, which ensure robustness against interferers during transmission. As discussed in Section IV, in the former case one typically speaks of an ADC. Fig. 4 shows some of the data converter architectures reported in a-IGZO TFT technology. The important sub-blocks of these architectures are further illustrated in Fig. 5.

One of the first reported data converters [31] in a-IGZO TFT technology is shown in Fig. 4(a). It has an asynchronous delta sigma modulator (ADSM) architecture. Thus, it converts an input current signal to an output pulse-width

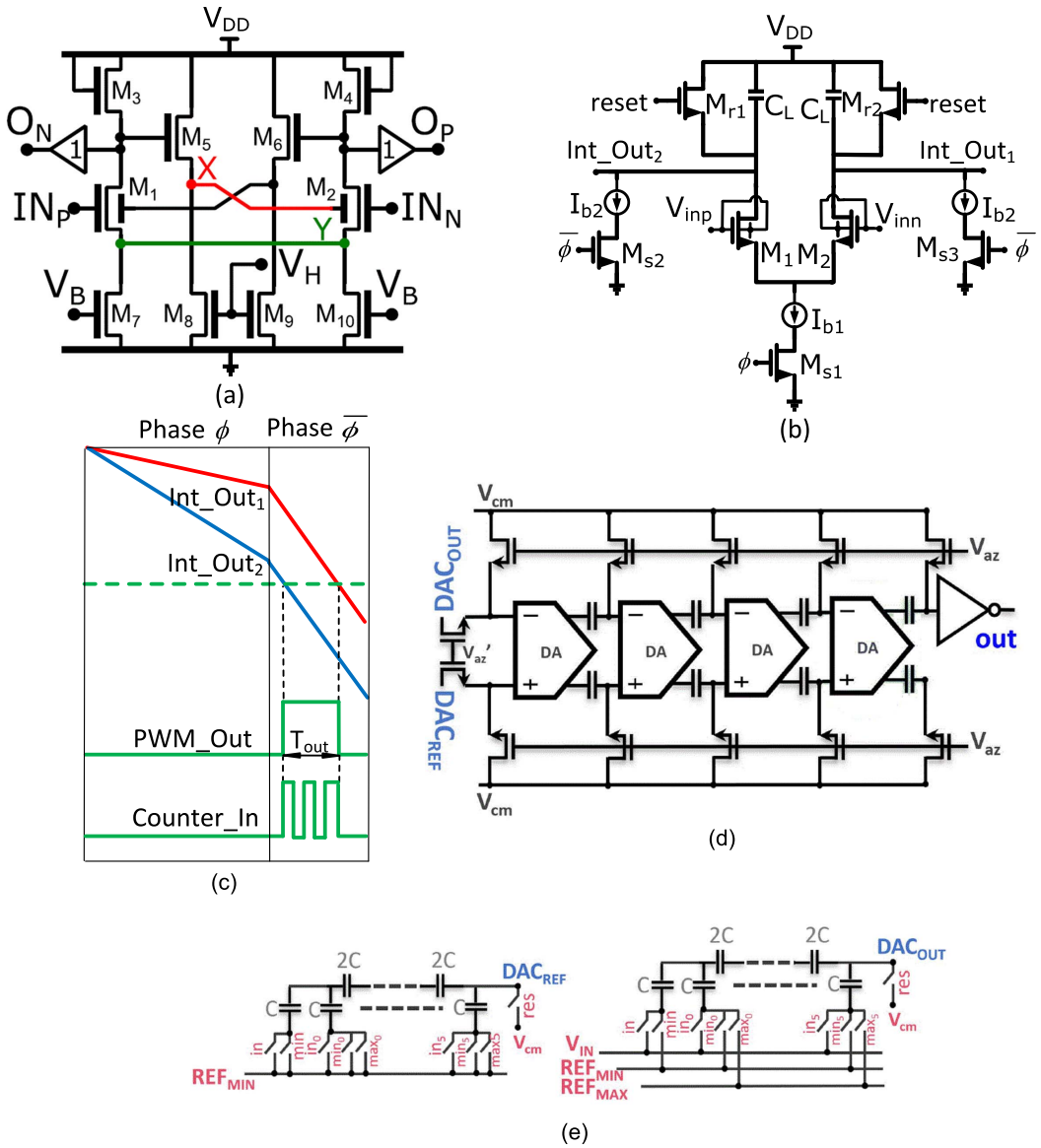



**FIGURE 5.** Implementation details of a-IGZO TFT based data converter architectures. (a) Schematic of the comparator used in ADSM [31], (b) Schematic of the reset integrator [27], (c) Timing diagram of the reset integrator based ADC [27], (d) Schematic of the comparator used in C-2C SAR ADC with offset cancellation [32], (e) Schematic of the C-2C DAC in SAR ADC [32]. (a) Copyright 2017 IEEE. Reprinted with permission from [31], (d-e) Copyright 2018 IEEE. Reprinted with permission from [32].

modulated (PWM) signal. It comprises a loop filter, a pre-amplifier, a comparator with tunable hysteresis, and a current steering digital to analog converter (DAC). Thanks to the loop filter and feedback arrangement, the time average of the output binary signal equals the input current. This data converter is not time sampled and thus does not introduce a quantization error. Besides, it is built using an oscillator whose frequency is modulated by the input current, and this ensures an inherent oversampling of the input signal, which improves accuracy in the transformation to the time domain [89]. The amplifier used as core of the loop filter ($A_1$) is already shown in Fig. 3(c). The filter is completed with feedback capacitors to realize a current integrator (Fig. 4(a)). The comparator preamplifier ($A_2$) is a diode connected load amplifier. The top gates of the input pair are connected to the output of the opposite branches, realizing a limited positive feedback that increases the transconductance and hence enhances gain. The pre-amplifier is used to boost the loop filter's limited output swing. Fig. 5(a) shows the schematic of the comparator. The top gates of the input TFTs $M_1$ and $M_2$ are cross coupled through level shifters $M_5$, $M_8$ and $M_6$, $M_9$ to create a positive feedback with loop gain larger than one. The desired hysteresis of the comparator, which is caused by the positive feedback, can be tuned by the bias voltage $V_H$. The 1-bit DAC consists of the reference current $I_{REF}$ and the switches $S_{1-4}$. The ADSM can also been considered as an asynchronous oscillator whose frequency is modified by the input current.

The ADSM experimentally demonstrates a maximum signal to noise ratio (SNR) of 55 dB, spurious free dynamic

range (SFDR) of 55 dB and signal to noise-plus-distortion ratio (SNDR) of 50 dB in 10-Hz bandwidth. A maximum SNR of 44 dB, SNDR of 40 dB and SFDR of 55 dB, are obtained in 300-Hz bandwidth. The performance of this ADSM is the state-of-the-art among a-IGZO TFT technology based data converters. The power dissipation of the full system is 2 mW. The area occupied by the ADSM is 27.9 $mm^2$.

Another way to convert a signal to PWM representation is the use of a reset integrator. It has the disadvantage of losing the inherent oversampling due to the self-oscillation of the ADSM, but it has the advantage of being far simpler, more compact and potentially lower power. Fig. 4(b) shows the block diagram of a reset integrator based ADC [27]. It consists of a reset integrator, a logic block and a counter. The reset integrator is used to convert the input signal to a binary PWM signal, i.e., to a time-domain representation. The rationale behind the time domain processing is that a-IGZO TFT technology does not have stable voltage references which are required in most of the data converter architectures, while processing signals in time domain requires a time reference which can be easily obtained by suitable division of 13.56-MHz NFC (or HF RFID) carrier. Indeed, in this work [27], the PWM signal is transformed to a digital word quantizing the PWM with the help of a counter and suitable logic, providing a serialized output. The circuit schematic of the reset integrator is shown in Fig. 5(b), while its timing waveform is shown in Fig. 5(c). The reset integrator operates in two phases: in first phase $\phi$, a signal dependent discharging of the load capacitors $C_L$ takes place, while in the other phase $\bar{\phi}$, a constant current $I_{b2}$ discharges the capacitors. The two phase integration is used to improve the linearity of the reset integrator, by providing a constant signal slope at the comparator inputs. The integrator outputs are periodically reset to $V_{DD}$. The discharge of the reset integrator output branches ($Int\_out_{1,2}$) is monitored by comparators. Based on the timing instants at which $Int\_out_{1,2}$ cross a given threshold, a PWM output of pulse width $T_{out}$ is generated (Fig. 5(c)), which is proportional to the differential input signal.

The reset integrator based ADC in [27] has been experimentally validated with the full sensor interface, which is discussed in Section VII.

Considering now a traditional Nyquist analog to digital converter with digital time-sampled output, Fig. 4(c) shows a C-2C SAR ADC presented in [32], [90]. The main sub-blocks of the ADC are a comparator, a DAC, a bias circuit and a digital control sub-block. A sensor interface is added at the input of the ADC. The block level diagram of the comparator is shown in Fig. 5(d). It is built of cascading differential amplifiers (DA) implemented with double gate TFTs and using a diode connected load topology. Buffers are also placed at the output stage after the comparator. Auto-zeroing is used at each comparator stage to cancel the offset. The operation of offset cancelation takes place in two phases. $V_{az}$ is high in the first phase, which resets all the input nodes of the DAs to $V_{cm}$. The capacitors store the output offset. In the second phase, the comparator inputs are connected to the inputs to be compared. The common mode voltage $V_{cm}$ at half rail is generated using a voltage divider based on diode connected TFTs.

Fig. 5(e) shows the two 6-bit C-2C capacitor networks that implement the DAC. One C-2C network is connected to the input signal $V_{IN}$ from sensor while the other network is used to obtain the comparator's reference value from the minimum reference ($REF_{MIN}$) for the operation range of the sensor. The C-2C DAC architecture is chosen for its compactness and simplicity, and for the fact that ensures sufficient linearity for the 6-bit quantizer that is discussed in this work. The use of a second C-2C network to generate the comparator reference alleviates inaccuracies caused by charge injection due to switching and by interferers. A digital control block is also implemented to control C-2C network and comparator's offset cancelation.

The experimental characterization of the 6-bit C-2C SAR ADC yields an SNDR of 35.9 dB with a sampling rate of 26.67 S/s. The power dissipation of the analog part is 73 μW. The area occupied by the ADC is 1.5 $cm^2$. A similar ADC with different flavor of a-IGZO TFT technology is presented in [91].

## VII. SENSOR ACQUISITION SYSTEMS BASED ON A-IGZO TFTS

The advancements in a-IGZO TFT processing technology have resulted in applications beyond digital systems, that exploit implementation of complex functionalities by integrating different circuit blocks. In this section, we will present some of the examples of state-of-the-art a-IGZO TFT based systems that have successfully demonstrated various applications. Two a-IGZO TFT based temperature sensors have been demonstrated in [31], [32]. Furthermore, wearable physiological monitoring systems have been shown in [27]–[30].

Reference [31] showed one of the first a-IGZO TFT based temperature sensor. The architecture of the system is shown in Fig. 4(a). The full system consists of the ADSM based on a-IGZO TFTs presented in Fig. 4(a) and described in Section VI, and two thin-film thermistors fabricated on a Polyethylene Naphthalate (PEN) substrate. The micrograph of the ADSM on flexible foil is shown in Fig. 6(a). The experimental results are shown in Fig. 6(b). An accuracy of 0.54°C in 100 ms integration time is achieved, while a maximum full range error of 2.3°C is obtained after 3 points calibration. The total power dissipation is 2 mW. The ADSM provides a binary PWM representation of the sensed temperature, but no digital code.

Another temperature sensor based on a-IGZO TFTs is presented in [32]. It is based on a 5-bit version of the C-2C SAR ADC topology shown in Fig. 4(c) and discussed in Section VI. Fig. 6(c) shows the foil micrograph of the full temperature sensor. It consists of a C-2C SAR ADC and 4 reference tunable resistors using source drain metal layers to generate the reference voltages. The system is demonstrated

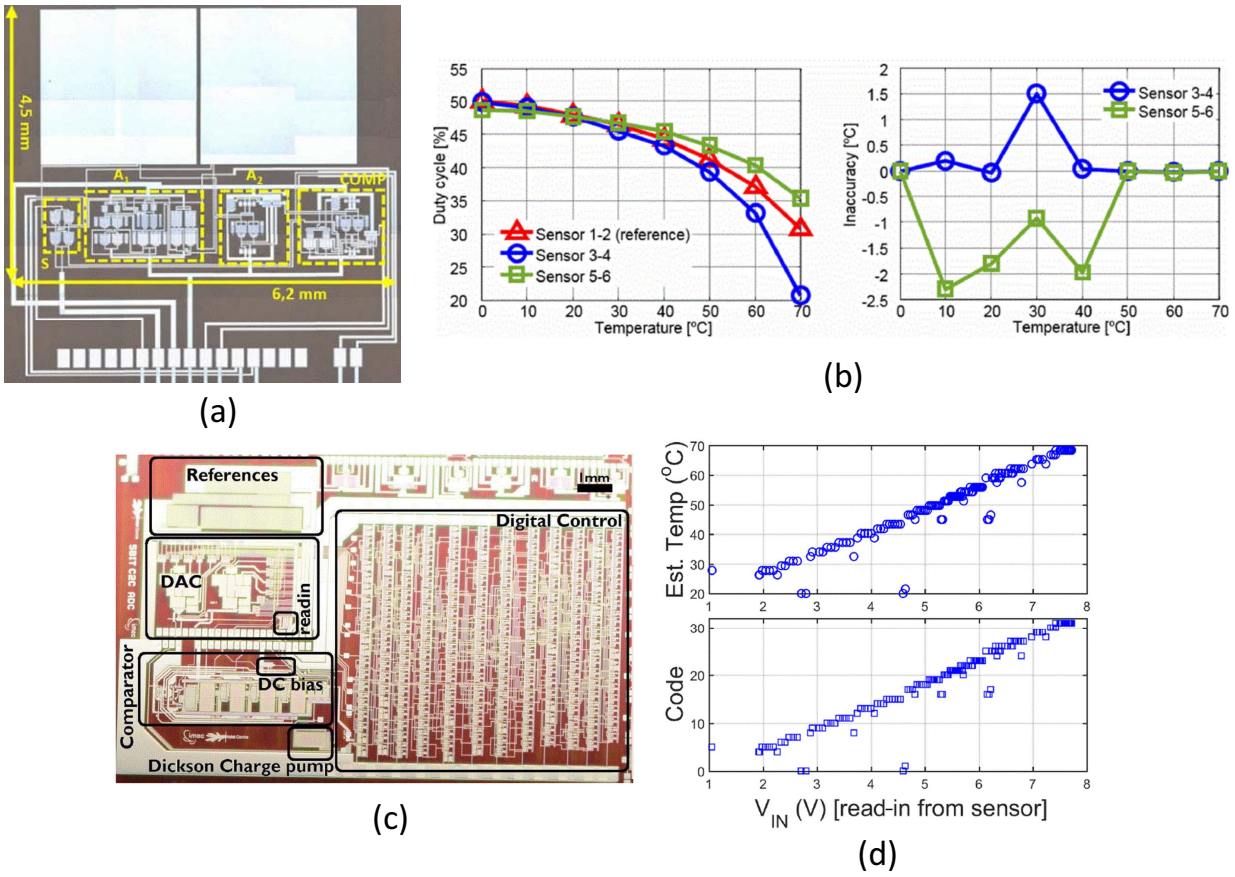



**FIGURE 6.** Temperature sensors based on a-IGZO TFTs. (a) Foil micrograph of ADSM presented in [31], (b) Duty cycle vs temperature and inaccuracy vs temperature characteristics of the temperature sensor presented in [31], (c) Foil micrograph of the system presented in [32], (d) Output digital code and temperature estimate from sensor's analog input. (a-b) Copyright 2017 IEEE. Adapted with permission from [31], (c-d) Copyright 2018 IEEE. Adapted with permission from [32].

**TABLE 3.** Comparison of the state-of-the-art a-IGZO TFT sensor systems.

| | [31] | [32] | [29] | [28] | [30] | [27] |
|---|---|---|---|---|---|---|
| Architecture | ADSM | C-2C SAR ADC | Amplifier with FDM | Amplifier with Reset Integrator | SE CS Amplifier | Reset Integrator based ADC |
| Input domain | Current | Current | Voltage | Voltage | Voltage | Voltage |
| Sensing mechanism | Temp. sensitive resistor | Temp. sensitive resistor | Electrode | Electrode | Electrode | Electrode |
| Output type | PWM | Digital | Analog | PWM | Analog | Digital |
| Application | Temp. sensor | Temp. sensor | EMG | HR | EMG | ECG |
| Integrated noise [$\mu V_{rms}$] (BW) | - | - | 31.4 (500 Hz) | 186.3 (200 Hz) | - | 8 (100 Hz) |
| Supply voltage [V] | 20 | $V_{DD}$ = 15 $V_{BIAS}$ = 30 | 26 | 10 | 5 | $10^a$ & $5^b$ |
| Power dissipation [mW] | 2 | 245 | 1.3 | 0.052 | 0.008 | $0.28^a$ & $15.4^b$ |
| Area [$mm^2$] | 27.9 | 150 | 11.2 | 52.5 | $900^c$ | 123.4 |

$^a$Analog $^b$Digital $^c$Estimated from [30]

with a printed Negative Temperature Coefficient (NTC) sensor on a separate Polyimide (PI) foil. The measured temperature sensing performance is shown in Fig. 6(d), which shows the digital output code of the system in response to NTC sensor's input signal. It also shows the estimated non-calibrated temperature. The power dissipation of the system is 245 mW.

One of the first reported physiological monitoring system based on a-IGZO TFTs is the electromyogram (EMG) interface described in [29]. The system consists of four chopper amplifiers driven at four different frequencies, whose differential outputs are summed in the current domain on a single pair of wires, to realize a frequency division multiplexing (FDM). Fig. 7(a) shows the foil micrograph of one EMG acquisition circuit, while Fig. 7(b) shows the positions of electrodes and the acquired EMG signal during *in-vivo* experiment. The front-end achieves an input referred noise of 31.4 $\mu V_{rms}$ in 500-Hz bandwidth, 29.6-M$\Omega$ input impedance and 41-dB SNR. The total power consumption is 1.3 mW. This design necessitates a silicon IC to implement analog to digital conversion.

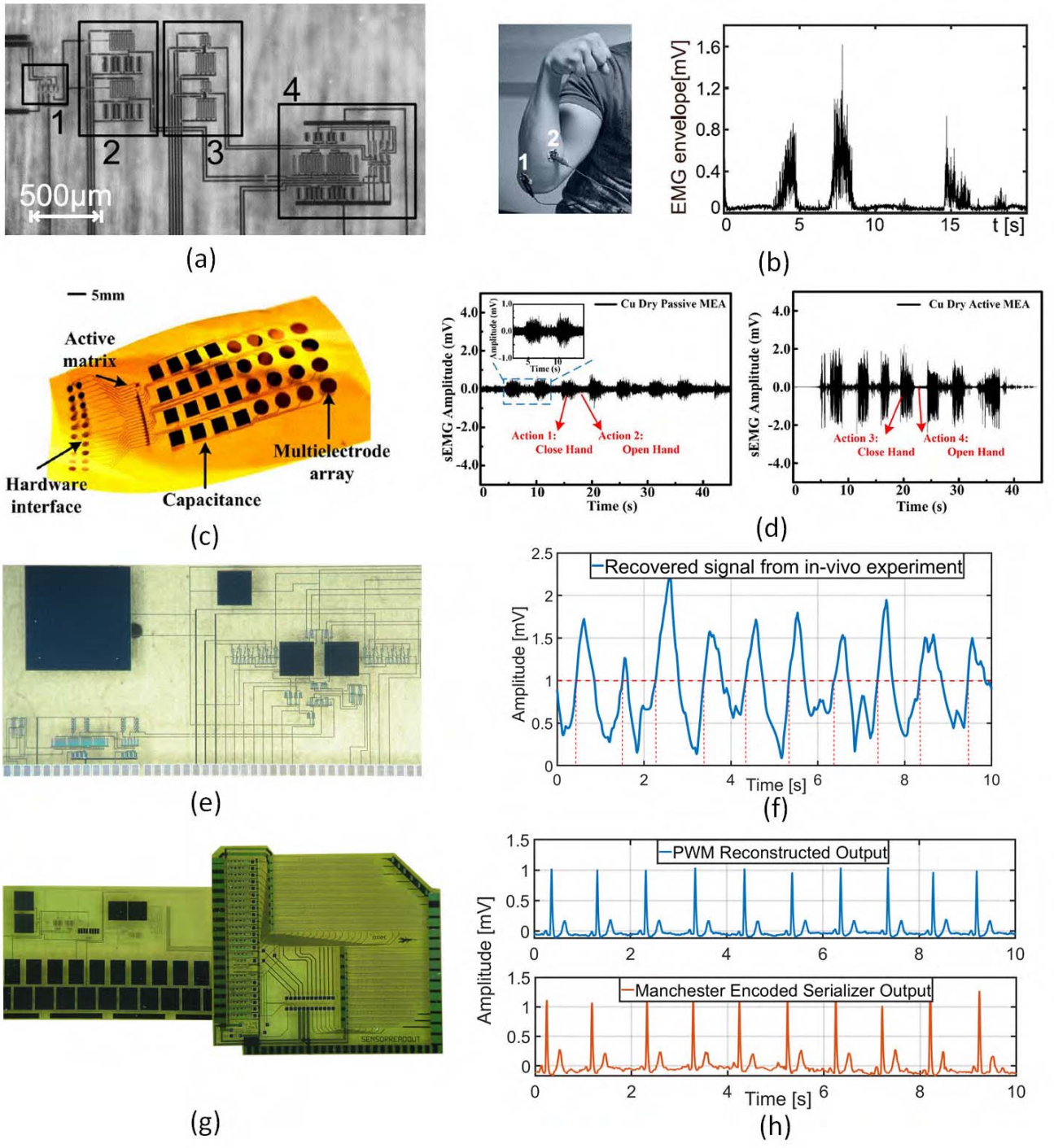



**FIGURE 7.** Bio-signal monitoring systems based on a-IGZO TFTs. (a) Foil micrograph of the EMG front-end presented in [29], (b) Acquired EMG signal [29], (c) 4 × 4 sEMG sensor array [30], (d) sEMG acquired through passive MEA and active MEA, (e) Foil micrograph of the HR readout presented in [28], (f) Acquired HR signal from reconstructed PWM [28], (g) Micrograph of the flexible ECG patch [27], (h) Acquired ECG signal from the output PWM and Manchester encoded output [27]. (a-b) Copyright 2018 IEEE. Reprinted with permission from [29], (c-d) Copyright 2020 IEEE. Adapted with permission from [30], (e-f) Copyright 2018 IEEE. Adapted with permission from [28].

Fig. 7(c) shows a surface EMG (sEMG) multielectrode array (MEA) based on a-IGZO TFTs [30]. It consists of $4 \times 4$ array of single ended (SE) common source (CS) amplifiers. The MEA achieves gain of 15 dB in 480-Hz bandwidth with supply voltage of 5 V. The power dissipation of a single CS amplifier is 8 μW. Fig. 7(d) shows the sEMG signal acquired during *in-vivo* experiment using a passive and active MEA. The recorded SNR of passive and active MEA is 24.7 dB and 35.4 dB, respectively. This MEA demonstrates the large area character of the technology enabling multiple electrodes, but

it does not provide multiplexing and requires other building blocks such as filters, ADC, DSP etc. to complete the full signal acquisition chain. The spatial resolution (pitch) of the MEA is 4 mm, which might impact its clinical applicability.

Another example of physiological monitoring system is the HR readout interface on flexible foil presented in [28] and shown in Fig. 7(e). It is able to convert the input signal to a PWM representation using a reset integrator. The system experimentally demonstrates a low-frequency gain of 25 ms/V with an input referred noise of 186.3 $\mu V_{rms}$ in 200-Hz bandwidth. The total power consumption of the interface is 52 $\mu$W. Fig. 7(f) shows an *in-vivo* experiment demonstrating measurement of the heartbeat of a person. This interface is very power efficient but it is lacking the digital output representation (i.e., in bits), which is required to be compatible with most standard wireless transmission systems. Moreover, the integrated input referred noise is too high to perform most bio-signal measurements.

An evolution of this concept, aiming to demonstrate an intelligent healthcare patch based on a-IGZO TFTs that is compatible with the NFC wireless communication standard, is demonstrated in [27]. This work exploits a digitization strategy using a time reference, that can be derived from the NFC carrier, without the need for a voltage reference. The ECG signal is amplified, transformed to PWM representation using a reset integrator (Section VI) and quantized by a counter to provide the digital output in the format of a 105.9 kb/s Manchester encoded serial bit stream (Fig. 4(b)). The analog front-end in this system has an input-referred noise of 8 $\mu V_{rms}$ in 100-Hz bandwidth. Moreover, the system has 67.4-dB common mode rejection ration (CMRR), 58.9-dB power supply rejection ratio (PSRR) and 16.5-M$\Omega$ input impedance at 50 Hz with 1 kHz chopping. The power dissipation of the analog subsystem is 280 $\mu$W, while the digital subsystem consumes 15.4 mW. Fig. 7(g) shows the foil micrograph of the system, while Fig. 7(h) demonstrates *in-vivo* experiments showing the ECG reconstructed from the PWM and from the Manchester encoded output bitstream. To the best of authors' knowledge, this is the first and only demonstrated physiological signal acquisition system in flexible a-IGZO TFTs on foil providing a digital serial output bit stream compatible with the NFC standard. The system implements digital signal processing on the flexible foil, which increases the overall power dissipation of the system considerably due to the power-hungry nature of unipolar logic. Moreover, it is a single channel system which does not fully leverage the large area character of flexible technologies.

Apart from temperature sensing and physiological monitoring applications, a-IGZO TFT based circuits have been used in other applications such as radiation sensing [82], magnetosensory applications [92], space applications [93], gamma ray detection [94], $NO_2$ gas sensing [95] etc. Moreover, IGZO TFTs have also been utilized as sensing devices in an aqueous medium for applications such as biosensing [96], virus detection [97], and artificial DNA detection [98] etc.

## VIII. CONCLUSION AND FUTURE PERSPECTIVES

Advances in flexible a-IGZO TFT processing technologies have enabled the implementation of complex circuits and architectures to realize various flexible sensors systems. Emerging applications of the Internet of Things (IoT) such as wearable textiles, wearables for diagnostics and sports, sensing of physical quantities distributed on surfaces, NFC tags etc. may benefit from this fabrication strategy.

a-IGZO TFT based amplifiers show a continuous trend to realize high-gain amplifiers with novel load topologies while using only n-type TFTs. The performance of these amplifiers has reached the point where they can be used in demanding low-noise applications like continuous physiological signal monitoring. Recently, there has also been an effort to realize larger bandwidth amplifiers, which could be used, e.g., in potential RF applications, also exploiting the impressive improvements in terms of $f_T$ at device level.

The research in the field of data converters based on a-IGZO TFTs is still in its infancy: only few data converters have been presented in literature. Realizing a data converter in the absence of complementary devices, voltage and current references, and using a technology that is affected by large parasitic capacitance and mismatch is indeed quite challenging. A clear trend is to prefer time-domain conversion approaches, as time references at the state-of-the-art are easier to implement (in RFID or NFC platforms) than their voltage or current counterparts.

Some significant achievements have been demonstrated in complete sensor acquisition systems based on a-IGZO TFTs as discussed in Section VII. However, there is still a long way to go, before being able to realize the vision of fully flexible sensors on foil integrating all parts of the signal processing chain, including wireless data transmission. The true potential of flexible technologies which lies in the large area character, flexibility and conformability has thus not been exploited entirely.

In terms of future perspective, research in the area of TFT device processing and architecture should open up new possibilities for circuit designs offering lower supply voltage, faster devices and better noise performance. The mobility of present day a-IGZO TFTs is limited, however, operation frequencies can be increased by scaling the TFTs dimensions and lowering parasitic capacitance. Apart from that, realization of reliable and well-matched integrated passive components like capacitors and resistors would be an important asset to enable better data conversion on foil. Low supply voltage is also key to enable easier and efficient integration between TFTs on flexible foil and silicon integrated circuits, which is an interesting possibility to embody applications requiring speed, power-efficient digital processing and wireless communication together with flexible form factor.

From the circuit design and system architecture perspective, a very important and rather unexplored domain in flexible smart sensors is power management. Although many groups are working on flexible batteries, more research on

voltage regulators, fast rectifiers for efficient RF energy harvesting in RFID platforms, current and voltage references, etc. is essential to design and realize smart sensors that integrate their energy sources, an achievement that would be of paramount practical importance.

Non-conventional data processing approaches such as analog classifiers, neuromorphic computing, machine learning, compressed sensing and stochastic computing, which have been reported in other flexible technologies [99]–[102], are still unexplored in a-IGZO TFT technologies. The use of such approaches at system level might ensure system robustness against device variability [102], and also minimize the number of physical interconnects needed to interface a large number of sensors to the external world [101].

The demonstrators which have been shown in a-IGZO TFT technologies so far, still need to be commercialized, which, in turn, requires technology scalability. Nevertheless we think that advancements in the field of a-IGZO TFT technologies will play an important role in fulfilling societal needs with unprecedented solutions.

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