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Comparison of High-Order Programmable Mismatch Shaping Bandpass DEM Implementations Applicable to Nyquist-Rate D/A Converters

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ABSTRACT Non-shaping dynamic element matching (DEM) randomization schemes are widely adopted for wideband Nyquist-rate digital-to-analog converters (DACs) within transmitter architectures. Here, randomization translates the mismatch-induced distortion into white noise from dc to $F_s/2$ range. However, the DAC performance for various bands within the Nyquist range cannot be improved using non-shaped DEMs as their inherent structure cannot be made programmable. Conversely, mismatch-shaping DEMs can be made tunable to shape the DAC errors over various signal bands, which makes them suitable for wireless transmitter applications. This paper presents the design methodology for high-order mismatch-shaping DEM architectures suitable for wideband Nyquist DACs. The challenge in designing high-order DEM structures for Nyquist DACs is to make them programmable to cover various signal bands within the Nyquist range and to operate them at high-frequencies demanded by the applications. Moreover, the stability of the high-order loop-filter within the DEM and its implementation cost is of great concern. This work details techniques to design programmable, stable, and hardware efficient high-order DEM structures for wideband Nyquist DACs. The DEM structures are implemented on an UltraScale+ FPGA device for prototyping and validation. Furthermore, the DEM design operation is validated by obtaining the measurement results interfacing with a 5-bit analog DAC.

INDEX TERMS Bandpass, current-steering, DEM, Nyquist-DAC, programmable.

I. INTRODUCTION

HIGH-SPEED, wideband Nyquist-rate D/A converters are necessary components in wireless transmitters to cover various operational bandwidths for different radio standards, while maintaining high spectral purity in the presence of in-band interference. Spurious-free-dynamic-range (SFDR) and intermodulation-distortion (IMD) are key parameters to measure the DAC performance over a narrow or wideband. The non-idealities within the DAC circuit causes static and dynamic errors [1], which significantly deteriorates the digital-to-analog converter (DAC) SFDR and IMD performance over the Nyquist-band. Non-linearity due to component mismatches can be alleviated by the use of dynamic element matching (DEM) logic in Nyquist DACs. This work discusses high-order DEM architectures that are suitable for wideband Nyquist-rate D/A converters. The major challenge in designing the DEM architectures for Nyquist DACs is to make them programmable and to maintain their stability over the full Nyquist range for higher orders. In this case, programmability is required in the higher-order DEM structures to deliver good mismatch performance over a wide range of signal bandwidths to

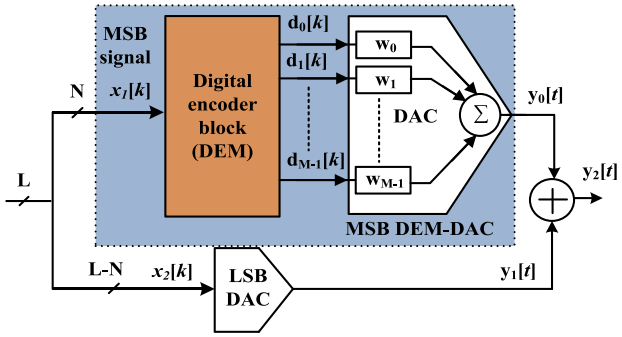

FIGURE 1. Dynamic element matching (DEM) block employed in the MSB path of the segmented Nyquist DAC.

cover various radio standards. A further challenge is to make high-order DEMs operational at the faster speeds required by high-speed Nyquist DACs.

This work details techniques to design programmable, stable, and hardware efficient DEM structures using high-orders suitable for wideband Nyquist DACs. A segmented Nyquist DAC divided into two sub-DACs consisting of a thermometer-decoded most significant bit (MSB) DAC and a binary-weighted least significant bit (LSB) DAC is shown in Fig. 1. The digital DEM block is connected to the MSB-DAC section that spectrally shapes errors within the DAC at low frequencies. The MSB-DAC mismatch errors dominate over the LSB-DAC section degrading linearity performance.

The foreground/background techniques presented in [2]–[5] helps to mitigate the impact of static mismatch errors within DAC at low frequencies. However, these techniques are not effective in mitigating DAC errors at high frequencies. Moreover, they involve complex static calibrations using analog and digital circuitry. Randomization techniques [6]–[9], select the DAC elements in pseudorandom fashion and translate the distortion tones into white noise. This results in a flat spectrum across the entire Nyquist band. Therefore, randomization is a widely used technique for wideband Nyquist DACs. However, with an increase in the mismatch error on the DAC elements, randomization increases the noise floor leading to in-band signal-to-noise and distortion (SNDR) degradation. The data-weighted-averaging (DWA) [10] scheme is an inherent first-order lowpass mismatch-shaping DEM, however, its element selection pattern repeats in a periodic fashion introducing idle tones appearing in the in-band portion of the spectrum. In time-interleaved DAC architectures [11], the extent of image suppression depends on the gain and clock phase matching among the internal DACs. The local oscillator in a mixing DAC [12] introduces switching time disparities, which result in additional sources of delay and duty-cycle errors, reducing the DAC's dynamic performance. In [13], [14], the authors adopt a hybrid DAC which consists of a Nyquist-rate MSB-DAC and an over-sampled delta-sigma ($\Delta\Sigma$) LSB-DAC. Here, the LSB-DAC operates at a much higher speed than the MSB-DAC section which is used to correct MSB-DAC errors. The architecture also requires off-chip manual calibrations. Moreover, to meet the $\Delta\Sigma$ modulator quantization noise requirements, the architecture needs to employ various noise cancellation techniques. Additionally, the hardware complexity and the power consumption required for this architecture are significant. In [15], the author uses a new mismatch-noise-cancellation (MNC) technique that adaptively measures and cancels both amplitude and timing errors resulting in better SFDR/IMD. However, the MNC technique cannot utilize 12% of the first Nyquist-band near $F_s/2$ due to the aliasing from the decimation filter's transition band, which reduces the accuracy of this technique.

The inherent structure of the non-shaping DEM such as randomization cannot be made programmable which means the DAC performance over a particular band within the Nyquist range cannot be improved. However, noise-shaping DEMs such as vector-feedback (VF) [16], tree-structure (TS) [16], and butterfly-shuffler (BS) [16] can shape the mismatch errors for any choice of frequency locations based on the employed loop-filter characteristics. This error can be shaped over a narrow/wide bandwidth to improve the in-band dynamic performance of the DAC. The mismatch error performance of the noise-shaped vs non-shaped DEM structures is discussed later in Section V.

The work presented in [17] discusses a 6^{th} order mismatch-shaping bandpass VF-DEM field-programmable gate array (FPGA) realization. As an advancement, we present the FPGA design implementation, validation and comparison of the 6^{th} order bandpass VF, TS, and BS DEM architectures applicable to wideband Nyquist-rate D/A converters. The DEM architectures are realized onto an FPGA device for a 5-bit MSB-DAC using System-Generator for DSP (Sys-Gen)/Vivado tools. The DEM structures hardware resources and speed performances are compared using an UltraScale+ FPGA device. In this work, the DEM architectures are designed to be programmable so that the filter order can be selected to '2', '4' or '6'. The different choice of filter order selection allows shaping of the mismatch errors over a narrow or wideband for any choice of the centre-frequency location. This work demonstrates that for a 12-bit segmented DAC, the lowest in-band SFDR and IMD3 is $\geq$ 88dB and $\geq$ 80dB respectively for various configurations of the DEM logic operation evaluated over the Nyquist band. Moreover, the DEM design operation is validated by obtaining the measurement results interfacing with a 5-bit analog DAC.

The paper is organized as follows: Section II overviews the DEM-DAC operation for a Nyquist DAC. The section also details the VF, TS and BS DEM structure operating principle and overviews their implementation. Section III describes the technique to improve speed performance and efficient realization of the high-order filter in the DEM structures. Section IV provides the implementation details and the comparison of the VF, TS and BS DEM structures using the XILINX Sys-Gen/Vivado tool onto an UltrasScale+

FPGA device. Section V presents the FPGA hardware implementation results of the DEM architectures. These results are based on different filter order selections, various selections of centre-frequency locations and operational bandwidth choices. Section VI presents the measurement results of the DEM realized onto the FPGA board interfacing with a 5-bit unary-weighted current-steering DAC (CS-DAC). Finally, the conclusion and future work is presented in Section VII.

II. DEM-DAC OPERATION

The general diagram of a DEM structure employed in the MSB path of the segmented Nyquist DAC is shown in Fig. 1. A L-bit segmented DAC is split into a N-bit thermometer-decoded MSB-DAC and a $(L-N)$ bit binary-weighted LSB-DAC. The output of the MSB DEM-DAC $y_0[t]$ and the LSB-DAC $y_1[t]$ are combined to form $y_2[t]$. The DEM structure in the MSB path consists of a digital-encoder block, which drives an N-bit unary DAC. The DAC is made up of M elements, where $M = 2^N$. The amplitude value of the elements within the DAC is represented as w_0, $w_1 \ldots w_{M-1}$.

The digital-encoder block converts a N-bit MSB signal $x_1[k]$ to a set of 1-bit signals, which are used to control the elements in the DAC. The digital-encoder block produce digital bits based on the $x_1[k]$ value and the DAC converts these digital bits into a discrete analog output on each conversion cycle. If the amplitude value of all DAC elements is equal, then the DAC's input-output follows a linear relationship resulting in no distortion in the DACs spectrum. However, mismatches within the DAC elements causes the DAC transfer characteristics to be non-linear and induce distortion. The key principle of the DEM-DAC is that the digital-encoder block exerts control over the selection of the DAC elements, deterministically selecting different permutations that de-correlate the error term from an input signal. This helps to minimize the mismatch errors and eliminates the distortion tones from the output spectrum resulting in better DAC dynamic performance. The VF, TS and BS DEM architectures are widely used noise-shaping solutions in $\Delta\sum$ DACs, however, this work explores their use for wideband Nyquist-rate D/A converters.

A. VECTOR-FEEDBACK (VF) DEM

A modified VF-DEM adopted by Sun in [18] is shown in Fig. 2. VF-DEM is more hardware efficient as compared to the conventional VF-DEM since it does not require a minimization block. It consists of a vector-quantizer (VQ), a subtractor, and a bank of mismatch-shaping loop-filters. For an N-bit and M-level (where $M = 2^N$) DAC, the thick line in the figure denotes the signal containing M vector signals in parallel. The output of the VQ $d_v[k]$ is a vector containing a 1-bit signal, which is fed back (global feedback) and gets subtracted from $x_1[k]$. The resulting error $S_e[k]$ is then passed through a noise-transfer function (NTF) $NTF(z)$. The $NTF(z)$ equation is stated in Section III. The NTF output acts as an input to the VQ. The VQ selects the appropriate

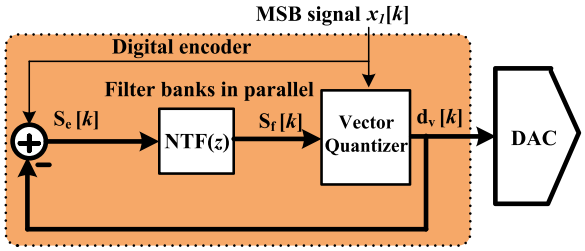

FIGURE 2. Hardware efficient modified VF-DEM.

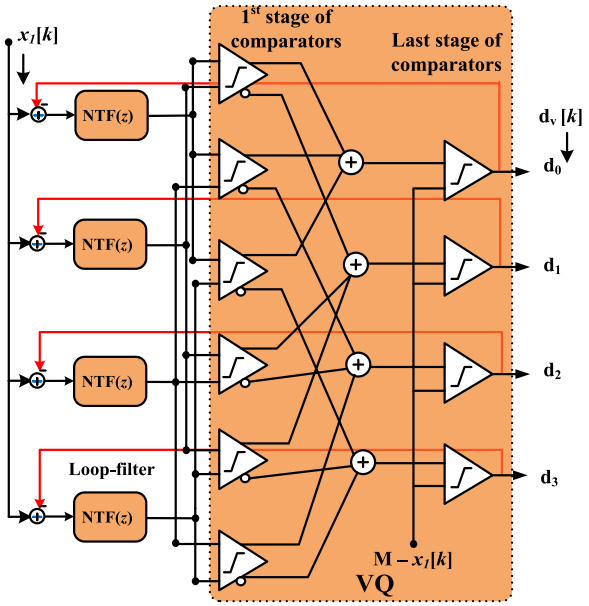

FIGURE 3. A modified VF-DEM hardware realization for a 2-bit unary-weighted DEM-DAC (red line highlights global feedback connection).

number of DAC elements from its input $S_f[k]$ with priority given to the largest value of the element based on $x_1[k]$.

The hardware realization of the modified VF-DEM proposed in [19] is adopted in this work and shown in Fig. 3 using a 2-bit (4-level) DAC example. The design consists of four subtractors, and four loop filters in parallel. The VQ is implemented using a bank of six comparators and four adders in the first stage, and four comparators in the final stage. For this case, the first stage of comparator banks gives ranking to the four loop filters based on their output value. The highest rank will be given to the filter with the larger output value and the second-highest rank will be given to the second largest output value of the filter and so forth. The output of comparator banks in the first stage is then combined using four 2-bit adders. The final stage of the comparator bank sets the appropriate number of comparators output to '1' based on the MSB segment value with priority given to the largest output value of the adder. For an N-bit and M-level DAC, the total number of comparators required are $(M^2 + M)/2$. The number of comparators required in the first stage is $(M^2 - M)/2$, and the remaining number of comparators in the final stage are M. The M n-bit adders

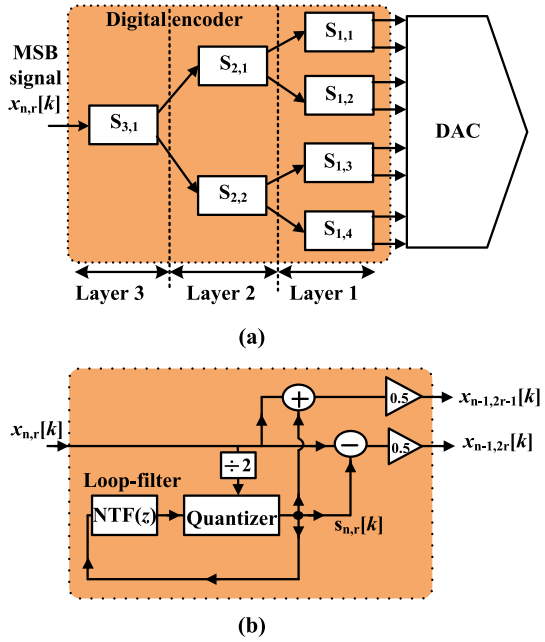

FIGURE 4. (a) TS-DEM implementation for a 3-bit unary-weighted DAC. (b) The general form of a 'switching block'.

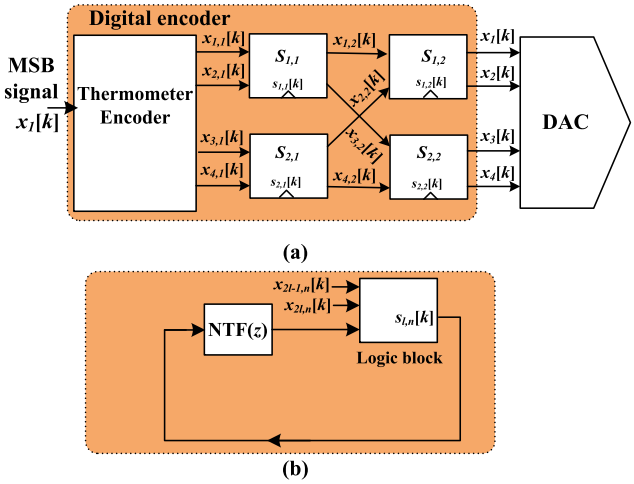

FIGURE 5. (a) A BS-DEM implementation for a 2-bit unary-weighted DAC. (b) Swapper cell implementation within the BS-DEM.

are required to add outputs of the first stage comparators, where $n = log_2(M)$.

B. TREE-STRUCTURED (TS) DEM

An example of a 3-bit TS-DEM implementation adopted by Welz and Galton in [16] is shown in Fig. 4(a). This implementation consists of three layers of digital devices called 'switching blocks' each of which is labelled $S_{n,r}$ where n denotes the layer number and r denotes the position of the switching block in the layer. The general form of the switching block is shown in Fig. 4(b). The switching block divides its input $x_{n,r}[k]$ amongst its two outputs named $x_{n-1,2r-1}[k]$ and $x_{n-1,2r}[k]$ as shown in the figure. Each switching block internally generates a switching sequence $s_{n,r}[k]$ based on the input and the value from the loop-filter. The switching sequence $s_{n,r}[k]$ is also controlled by a pseudorandom PN sequence.

Additionally, each of the switching blocks must obey the number conservation rule where the sum of the outputs must be equal to the inputs and each output must not violate the range (0 to 2^{n-1}). Furthermore, when the input of the switching block $x_{n,r}[k]$ is even then $s_{n,r}[k]$ is even and if it is odd then $s_{n,r}[k]$ is odd. If the switching block generates a L^{th}-order shaped switching sequence $s_{n,r}[k]$, which is uncorrelated from the $s_{n,r}[k]$ of the other switching blocks, then the DAC's mismatch error will be L^{th}-order shaped sequence. The hardware realization of the switching block requires an EX-OR gate, adders, multipliers, mux logic and delay elements in the filter bank.

C. BUTTERFLY-SHUFFLER (BS) DEM

A BS DEM is proposed by Adams and Kwan and presented in [20]. The block diagram of a BS for a 2-bit unary-weighted DEM-DAC is shown in Fig. 5(a). The digital-encoder block consists of a thermometer-encoder and M-swapper cells, which are labelled $S_{l,n}$ and positioned in a matrix with $l = 1 \ldots 2^{N-1}$, $n = 1 \ldots N$, corresponding to row and column numbers, respectively. To provide enough switching combinations to shape the mismatch error in the DAC, $M/2$ swapper cells are arranged in N layers, where M is the number of elements in an N-bit DAC. The MSB signal is thermometer-decoded and separated into pairs of signals. Each signal pair is then connected to a two-input swapper cell. The final layer of switching cells provide the control signals to the analog DAC. The input and output sequences of each swapper cell are 1-bit sequences; the values of each are taken to be $1/2$ and $-1/2$ at sample times when the sequence is high and low, respectively. The logic to implement a swapper cell is shown in Fig. 5(b). It consists of a logic block that can be implemented using a mux, a subtractor and a shaping filter. For a swapper cell block $S_{l,n}$, a swapping sequecnce $s_{l,n}[k]$, generated internally is based on two inputs $x_{2l-1,n}[k]$ and $x_{2l,n}[k]$.

At each sample time k, each swapper cell determines its outputs by routing its inputs either straight-through or swapped. For example the output of $S_{1,1}$ block from Fig. 5(a) can be written as

$$x_{1,2}[k] = \frac{1}{2}\big[x_{1,1}[k] + x_{2,1}[k] + s_{1,1}[k]\big],$$
$$x_{3,2}[k] = \frac{1}{2}\big[x_{1,1}[k] + x_{2,1}[k] - s_{1,1}[k]\big] \quad (1)$$

where $s_{1,1}[k]$ is called a swapper sequence. This sequence is generated within the swapper block $S_{1,1}$ and is restricted to be 0 when $x_{1,1}[k] = x_{2,1}[k]$ and ± 1 otherwise. When $s_{1,1}[k] = \pm 1$, the sign of the swapper sequence determines whether the swapper cell inputs are routed straight through or swapped. When $s_{1,1}[k] = 0$, both swapper cell inputs are the same; therefore, both outputs are the same regardless of how the swapper cell routes its inputs. The switching sequence

generated within the swapper block is shaped, therefore, the DAC output spectrum is shaped as well.

The VF, TS and BS DEMs can be used to shape DAC errors, however, these architectures have specific advantages and disadvantages. The VF-DEM is a simple structure for realization, however, the DEM logic grows exponentially as the number of DAC bits are increased. Moreover, the global feedback (red line shown in Fig. 3) in this structure makes it difficult to use DSP techniques (pipelining and retiming) to improve the speed of the DEM design. The BS-DEM architecture requires more swapper cells as compared to switching blocks in a TS-DEM for the same number of bit implementations. Both of these DEM architectures do not have global feedback, therefore they can be easily pipelined at a higher level to improve the speed performance.

III. PROGRAMMABLE LOOP-FILTER IN DEM STRUCTURES

While the DEM architecture governs parameters like speed, scalability, latency, and logic area, it is the loop-filter that ultimately controls the mismatch shaping. The following subsections detail how loop-filter characteristics are designed using a simple pole-zero placement technique for different orders. It also details how programmability and high-speed operation of the high-order filter is achieved by splitting it into several stages. The programmable filter is designed to be independent of architecture, allowing the VF, TS, and BS DEM architectures to employ the same loop-filter structure.

A. FREQUENCY-RESPONSE OF PROGRAMMABLE LOOP-FILTER

An L^{th} order notch filter desired frequency response can be obtained using (2) by optimal placement of the combination of poles and zeros in the Z-plane. The numerator and denominator part of (2) represents the complex-conjugate zeros and the complex-conjugate poles respectively, where r is the radius of the poles. The NTF that goes within the DEM structures is given by $\frac{1-H(z)}{H(z)}$. Figure 6 shows the placement of complex-conjugate zeros and poles of the 6$^{\text{th}}$ order IIR notch filter at $F_s/8$ centre-frequency. Here, the complex conjugate zeros that are placed with an angle θ on the unit-circle determines the centre-frequency of the filter. The locations of the complex-conjugate poles align with their complex-conjugate zeros and are placed within the unit-circle using $r < 1$ to ensure the stability of the filter.

$$H(z) = \left[\frac{1 - 2\cos\theta\ z^{-1} + z^{-2}}{1 - 2r\cos\theta z^{-1} + r^2 z^{-2}}\right]^L. \tag{2}$$

The programmable coefficient values for various filter orders, i.e., 2, 4 and 6 at $F_s/8$, $F_s/4$ and $3F_s/8$ centre-frequency are obtained using (2). The choice of centre frequency dictates the approximate placement of the pole-zero locations. From this, we can now obtain the notch type magnitude response over a narrow or wideband for any choice of the centre frequency. For orders 4 and 6, a narrow bandwidth is achieved by moving the zeros closer to the centre frequency; conversely moving the zeros away from the centre frequency widens the bandwidth. The movement of the poles along the radius r determines the depth of the notch giving the desired attenuation. The final pole-zero locations are determined by considering the trade-off between stability and attenuation. This is done by iteratively evaluating pole-zero locations to provide a set of coefficients that result in a stable filter with the desired response. For example, using the pole-zero placement method, the magnitude and phase response for 2$^{\text{nd}}$, 4$^{\text{th}}$ and 6$^{\text{th}}$ order IIR notch filters at $F_s/8$, $F_s/4$ and $3F_s/8$ centre-frequency is shown in Fig. 7(a), (b) and (c) respectively. Here, a notch is obtained over 5%, 10% and 20% of the F_s using 2$^{\text{nd}}$, 4$^{\text{th}}$ and 6$^{\text{th}}$ order IIR notch filters respectively. The pole-zero locations on the unit circle are also shown for 2$^{\text{nd}}$, 4$^{\text{th}}$ and 6$^{\text{th}}$ order IIR notch types in Fig. 7(a), (b) and (c) respectively.

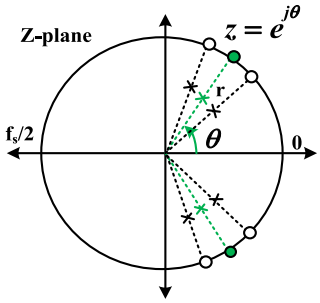

FIGURE 6. 6$^{\text{th}}$ order IIR notch filter complex conjugate poles and zeros in the z-plane for Fs/8 centre-frequency.

TABLE 1. 6$^{\text{th}}$ order h(z) filter coefficients for $3f_S/8$ centre-frequency.

Numerator coefficients						
1	3.5841	6.4312	7.6839	6.4312	3.5841	1
Denominator coefficients						
1	2.9846	4.4582	4.6461	3.6111	1.9582	0.5314

B. HIGHER-ORDER PROGRAMMABLE LOOP-FILTER DESIGN

The implementation of a stable high-order programmable IIR loop-filter within the DEM structure is critical. As the order of the filter increases, so does the complexity of the implementation. Furthermore, for a fixed-point implementation, effects such as coefficient quantization, rounding errors, overflow and stability have to be carefully considered. The numerator and denominator coefficients of the 6$^{\text{th}}$ order IIR notch filter designed for $3F_s/8$ centre-frequency using (2) are tabulated in Table 1 and the associated frequency-response is shown in Fig. 7(c). The 6$^{\text{th}}$ order NTF coefficients for $3F_s/8$ centre-frequency obtained from Table 1 are shown in Table 2. The realization of the NTF using Direct-Form (DF) structure has a -4 to $+8$ range of coefficient values, which means that a fixed-point implementation requires larger bit widths leading to increased hardware. Moreover, if each sample within the filter gets multiplied using larger coefficient values, this can cause data to overflow, leading to filter instability. A 6$^{\text{th}}$

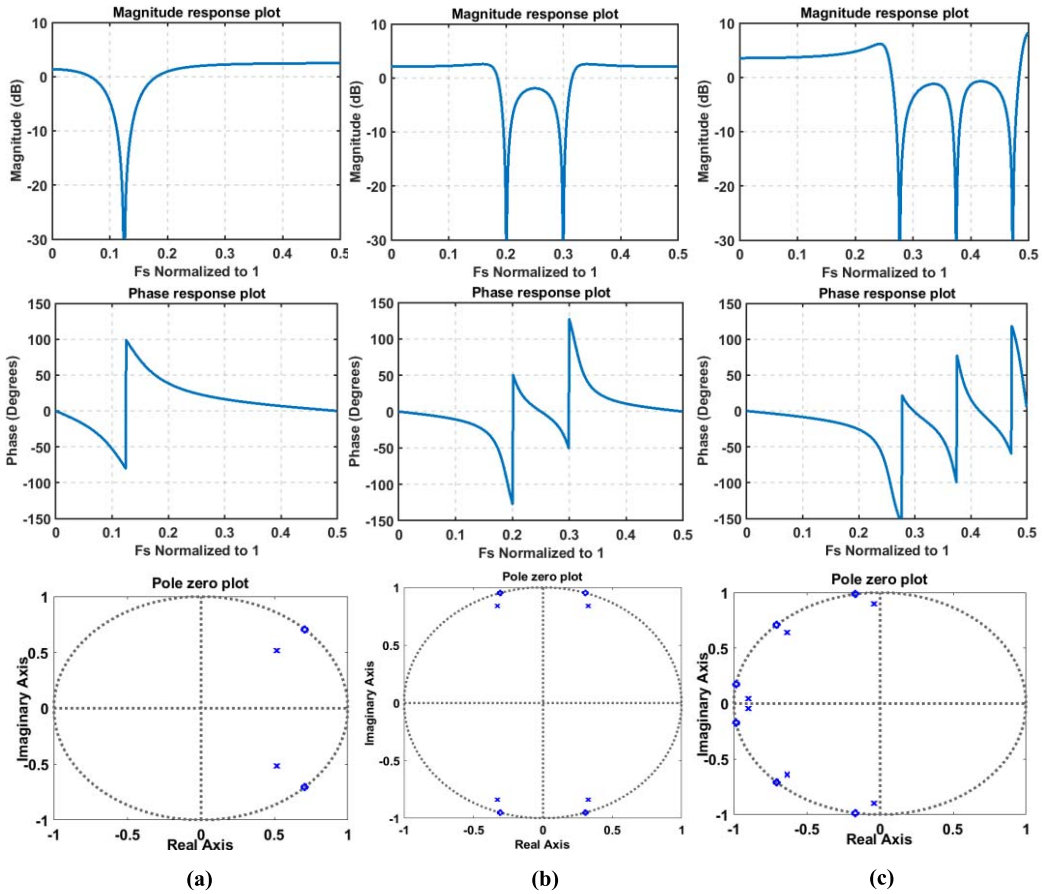

FIGURE 7. The magnitude, phase and pole-zero plot for the (a) 2nd, (b) 4th and the (c) 6th order IIR notch filters at centre-frequency $F_S/8$, $F_S/4$, and $3F_S/8$ respectively.

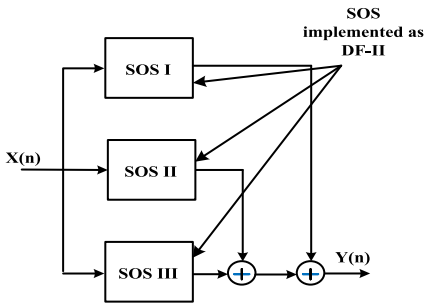

FIGURE 8. 6th order filter arranged as three SOS in parallel.

TABLE 2. 6th order NTF coefficients for $3f_S/8$ centre-frequency.

Numerator coefficients						
0	-0.5994	-1.9730	-3.0378	-2.8201	-1.6258	-0.4686
Denominator coefficients						
1	3.5841	6.4312	7.6839	6.4312	3.5841	1

order NTF realization using DF structure is not a suitable choice of implementation considering stability, high-speed operation and hardware efficiency.

Higher-order DEM filter implementations for oversampling converters are often based on a cascaded filter format;

TABLE 3. 6th order filter decomposition into 3 SOS stages.

SOS stages	Numerator coefficients			Denominator coefficients		
SOS I	0	-0.1645	-0.1928	1	1.4099	1
SOS II	0	-0.1838	-0.1829	1	1.9904	1
SOS III	0	-0.2511	-0.0928	1	0.1838	1

however, an alternative way is to use an equivalent parallel structure. In this work, we split the 6th order NTF into three second-order stages (SOS). The three SOS are then arranged in parallel as shown in Fig. 8. The overall transfer function of the three SOS in parallel is equivalent to the 6th order NTF. Each SOS is implemented as a hardware efficient Direct-Form II (DF-II) structure. As compared to the cascaded form, the parallel arrangement of SOS offers better timing performance by reducing the critical path delay. This enables high-speed operation of the DEM suitable for Nyquist DACs. Moreover, the SOS are less sensitive to quantization effects and requires a lower number of bits to represent the coefficients resulting in reduced hardware. The SOS stages coefficients shown in Table 3 have a significantly smaller range from ± 2 as compared to the coefficient values for the DF implementation shown in Table 2. The reduced range of the coefficient values for each SOS stage enables the realization of higher-order filters using lower bit widths

in the signal paths, while also introducing less quantization errors. The total number of multipliers required for the 6th order NTF using DF implementation is 12. However, using a parallel arrangement of SOS requires 9 multipliers, which helps to reduce the hardware complexity. In addition, the three SOS arranged in parallel enables modification of the 6th order NTF to order 2, 4 or 6 by selecting the number of SOS stages in the filter.

It can be noted that the frequency-response characteristics of the loop-filter dictate the mismatch error shaping of the DAC. This results in a DAC spectrum analogous to the employed loop filter's frequency-response characteristics within the DEM structure. Additionally, the arrangement of the SOS in a high-order filter either as a cascade or parallel decides the speed performance of the DEM design.

IV. DEM FPGA HARDWARE IMPLEMENTATION

The DEM architecture's hardware for the upper five MSB DAC bits is realized in XILINX's Sys-Gen tool using in-built adders, multipliers, delay elements and M-code blocks targeting the UltraScale+ FPGA device. The Sys-Gen implementation of the VF, TS and BS DEM structure's are illustrated in Fig. 9 (a), (b) and (c) respectively. For each DEM architecture, the word lengths of the programmable coefficients ($C_0 \ldots C_8$) and the data paths within the DEM filter were chosen to be 10 and 11 bits respectively, which is sufficient to achieve low round-off noise and maintain accuracy.

For a 5-bit VF-DEM, the output of the VQ is 32 parallel 1-bit digital signals ($d_0 \ldots d_{31}$) containing 1's and 0's. Each 1-bit digital signal is gained by the gain block in the feedback path. The 5-bit output of the gain block gets subtracted from the 5-bit MSB code using a subtractor and the 6-bit output is fed to the filter block. The VQ is implemented using an M-code block, which performs 496 comparisons on the 11-bit 32 filter outputs ($F_0 \ldots F_{31}$). The comparators generate a one-bit signal internally. For example, using the first comparator, if $F_0 \geq F_1$ the comparator sets $w_1 = 1$ and $\overline{w_1} = 0$, otherwise, $w_1 = 0$ and $\overline{w_1} = 1$ which is illustrated in Fig. 9(a). The comparator outputs are combined using 32 5-bit adders realized using M-code. The adder outputs ($Y_0 \ldots Y_{31}$) are compared using the final stage of comparators that constitute 32 comparators to produce a final digital output.

In the case of the 5-bit TS-DEM, 32 switching blocks are arranged in five layers as shown in Fig. 9(b). The input/output bit widths of switching blocks change from Layer 5 to Layer 1 as can be seen from the figure. The switching block realization uses an Ex-OR gate, M-code block, adders, subtractors, gain blocks and $NTF(z)$ including bit widths is shown in Fig. 9(d). A two-input Ex-OR gate operates on the LSB of the input signal and a constant 0 to produce '1' or '0' output. The 11-bit output (S_f) of the loop-filter and a 1-bit output (x_{lsb}) of the Ex-OR gate is fed to the logic block (implemented in M-code) that outputs a 1-bit signal S_k. Here, if $S_f \leq 0$ and $x_{lsb} = 1$, then $S_k = -1$, else if $S_f > 0$ and $x_{lsb} = 1$, then $S_k = 1$, otherwise $S_k = 0$. The adder, subtractor and the gain block input/output widths are dependent on the bit widths (L) of the input signal to the switching block based on the layer number. For a 5-bit BS-DEM, 80 swapper-cell blocks are arranged in five layers as shown in Fig. 9(c), each layer consisting of 16 blocks. The 5-bit MSB is converted to a thermometer code, which acts as input to the BS-DEM.

The realization of the swapper cell is depicted in Fig. 9(e). The logic block within the swapper cell is realized using M-code block, whereas the $NTF(z)$ is realized using adder, multiplier and delay elements. Each swapper cell has a 1-bit two inputs and a 1-bit two outputs. At each sample time k, each swapper cell determines its outputs by routing its inputs either straight-through or swapped based on $S_{l,n}$ value. A 6th order NTF within the DEM architectures is implemented as three SOS in parallel as shown in Fig. 9(f). Each SOS is implemented using a DF-II structure, which requires 3 adders, 3 multipliers and 2 delay elements. The bit widths for each SOS are also shown. The FPGA logic resources and speed performance of the 5-bit VF, TS and BS DEM architectures are compared in Table 4. The BS-DEM requires more DSP blocks as compared to the VF and TS DEM structures due to the increased number of swapper cells. The TS-DEM design utilizes fewer LUT's as compared to the VF-DEM as it does not require a large number of comparators. The critical path delay for VF, TS and BS DEMs after synthesizing using design constraints is 11.25ns, 10.5ns and 13ns respectively. This means that the VF, TS and BS DEM can operate up to 88.8MHz, 95.2MHz and 76.9MHz clock frequency respectively. Table 4 also gives an estimated ND2 equivalent gate count based on the synthesized DEM results where the logic size is dominated by the number of multipliers (DSPs) within the DEM filter designs. In this work, we did not target the optimization of the multiplier logic as we targeted a fully programmable coefficient approach. The TS-DEM structure is more advantageous as compared to VF and BS DEM structures concerning speed and logic. Moreover, the TS-DEM structures speed performance can be improved by employing DSP techniques such as pipelining and retiming. Therefore, this architecture is more suitable for high-speed Nyquist-rate D/A converters.

TABLE 4. 6th order tunable bandpass DEM structures comparison.

DEM architectures	DSP's	LUT's	Registers	Delay (ns)	Est. ND2 Eqv.
VF-DEM	288	12515	2112	11.25	~1.04M
TS-DEM	288	5281	2232	10.5	~0.81M
BS-DEM	720	12528	5280	13.0	~1.91M

V. FPGA IMPLEMENTATION RESULTS

This section presents the implementation results of the TS-DEM structure using the FPGA synthesis flow as shown in Fig. 10. Initially, the DEM design is realized using XILINX's Sys-Gen tool. The Sys-Gen IP block is then integrated into the Vivado tool. Verilog RTL code is written for the top-level

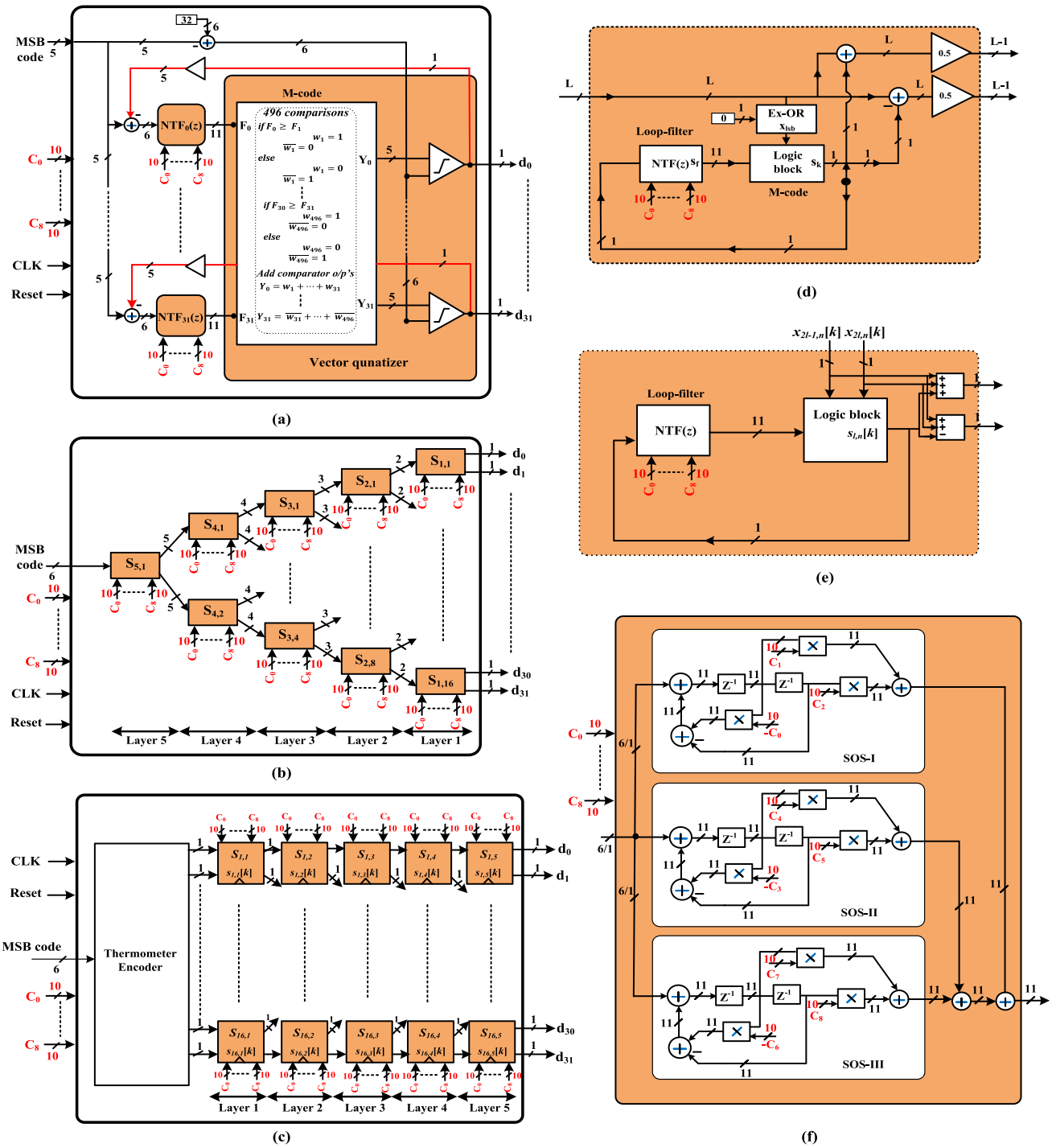

FIGURE 9. (a) The 5-bit programmable VF-DEM Sys-Gen realization. (b) The 5-bit tunable TS-DEM Sys-Gen realization. (c) The 5-bit programmable bandpass BS-DEM Sys-Gen implementation. (d) Sys-Gen realization of a switching block within TS-DEM. (e) Swapper-cell block realization within BS-DEM. (f) 6^{th} order NTF realization as three SOS in parallel with each SOS implemented using a DF-II structure.

DEM module that contains I/O's, main FPGA clock, reset pin, hard-coded coefficient values and a sub-module that passes data to the DEM design. A sinusoidal input tone is quantized to a 12-bit level and this quantized code is split into a 5-bit MSB and a 7-bit LSB code. The 5-bit MSB-DAC code to the DEM design is stored in the random-access-memory (RAM) on the FPGA board and then passed through the DEM design. The top-level DEM module is synthesized targeting the UltraScale+ ZCU104 MPSOC board using design constraints.

To obtain the dynamic performance results at the 12-bit level, the output of the 5-bit MSB DEM-DAC is combined with an ideal 7-bit binary-weighted LSB-DAC. Single and dual-tone FFT results are obtained for TS-DEM using

different filter orders, various choices of centre-frequency locations and operational bandwidth. Dual-tone IMD performance is based on two tones that are placed ±5% around the centre-frequencies. The DEM design operates at a 75MHz clock, which is obtained by dividing the main FPGA clock (300MHz) by 4. A 0.5% Gaussian distributed mismatch error is used on the DAC elements. The F_s is normalized to 1 for single/dual-tone plots.

A. SECOND-ORDER BANDPASS DEM RESULTS (NARROW BANDWIDTH)

The mismatch-shaping bandpass DEM results for filter order 2 are presented by selecting only one SOS from the three parallel SOS. The second-order on/off TS-DEM single and dual-tone spectrum for a 12-bit Nyquist DAC at $F_s/8$ centre-frequency is shown in Fig. 11(a). The input tone is chosen close to $F_s/8$ and the performance is evaluated over 5% of F_s. The min, max and average SNDR, SFDR and IMD3 results for 2nd order on/off TS-DEM using 100 MC runs at $F_s/8$, $F_s/4$, and $3F_s/8$ centre-frequencies are tabulated in Table 5. The table show that the SFDR and IMD3 performance of the DAC improves ∼14dB and ∼10dB respectively over a narrow-band for the 2nd order TS-DEM enabled case.

TABLE 5. 2nd order TS-DEM on/off SNDR, SFDR and IMD3 results for a 12-bit DAC at $F_S/8$, $F_S/4$, and $3F_S/8$ using 100 MC runs.

At $F_s/8$ centre-frequency							
	Ideal	DEM off			DEM on		
(dB)	Avg.	Min.	Max.	Avg.	Min.	Max.	Avg.
SNDR	84.5	71.76	79.19	76.02	80.18	82.33	81.37
SFDR	96	73.55	86.59	81.00	91.99	96.01	94.28
IMD3	96	66.78	86.50	74.82	86.09	88.56	87.47
At $F_s/4$ centre-frequency							
	Ideal	DEM off			DEM on		
(dB)	Avg.	Min.	Max.	Avg.	Min.	Max.	Avg.
SNDR	84.5	61.30	74.26	68.37	79.56	81.72	80.88
SFDR	96	62.88	79.19	72.40	92.50	97.10	94.8
IMD3	96	61.84	83.79	71.89	80.86	83.86	81.80
At 3 $F_s/8$ centre-frequency							
	Ideal	DEM off			DEM on		
(dB)	Avg.	Min.	Max.	Avg.	Min.	Max.	Avg.
SNDR	84.5	71.09	79.81	75.53	81.19	82.43	81.76
SFDR	96	73.18	86.99	79.25	92.98	97.28	95.52
IMD3	96	68.01	86.88	76.75	87.15	90.00	88.91

B. FOURTH-ORDER BANDPASS DEM RESULTS (MEDIUM BANDWIDTH)

Here, the mismatch-shaping bandpass DEM results for filter order 4 are presented by selecting two SOS out of the three parallel SOS. The 4th order on/off TS-DEM single and dual-tone spectrum for a 12-bit Nyquist DAC at $F_s/4$ centre-frequency is shown in Fig. 11(b). The input tone is chosen close to $F_s/4$ and the performance is evaluated over 10% of F_s. Table 6 shows ∼12dB and ∼10dB improvement in the SFDR and IMD3 performance respectively using 100 MC runs at $F_s/8$, $F_s/4$, and $3F_s/8$ centre-frequencies for the 4th order TS-DEM enabled case. In the case of the $F_s/4$ centre-frequency location, with the DEM, turned off, the SFDR and IMD degradation are worse when compared to $F_s/8$ and $3F_s/8$ centre-frequencies. This is due to the distortion tones that fall within the in-band and are removed by the DEM logic when it is turned on.

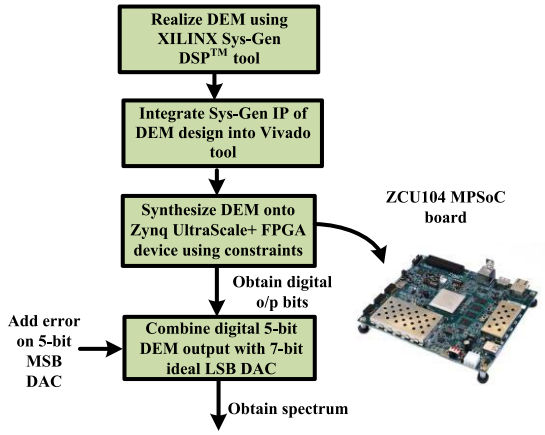

FIGURE 10. DEM design FPGA implementation flow.

TABLE 6. 4th order TS-DEM on/off SNDR, SFDR, and IMD3 results for a 12-bit DAC at $F_S/8$, $F_S/4$, and $3F_S/8$ using 100 MC runs.

At $F_s/8$ centre-frequency							
	Ideal	DEM off			DEM on		
(dB)	Avg.	Min.	Max.	Avg.	Min.	Max.	Avg.
SNDR	81.5	71.82	76.84	74.49	73.21	75.31	74.55
SFDR	96	74.51	83.70	79.11	90.68	92.34	91.85
IMD3	96	61.05	83.79	78.36	85.03	88.06	86.88
At $F_s/4$ centre-frequency							
	Ideal	DEM off			DEM on		
(dB)	Avg.	Min.	Max.	Avg.	Min.	Max.	Avg.
SNDR	81.5	63.08	72.69	68.92	74.88	77.78	76.54
SFDR	96	64.29	78.76	72.59	86.48	92.11	89.90
IMD3	96	65.90	81.79	72.04	80.29	82.32	81.37
At 3 $F_s/8$ centre-frequency							
	Ideal	DEM off			DEM on		
(dB)	Avg.	Min.	Max.	Avg.	Min.	Max.	Avg.
SNDR	81.5	69.70	78.72	73.85	74.12	76.64	75.28
SFDR	96	71.73	84.60	77.97	91.24	94.00	93.62
IMD3	96	67.93	86.40	78.35	85.81	95.00	89.50

C. SIXTH-ORDER BANDPASS DEM RESULTS (WIDE BANDWIDTH)

The mismatch-shaping bandpass DEM results for filter order 6 are presented by selecting all three SOS in parallel. The 6th order on/off TS-DEM single and dual-tone spectrum for a 12-bit Nyquist DAC at $3F_s/8$ centre-frequency is shown in Fig. 11(c). The SNDR, SFDR, IMD3 results for 6th order on and off TS-DEM using 100 MC runs at $F_s/8$, $F_s/4$, and $3F_s/8$ centre-frequencies are tabulated in Table 7. The tables show that the SFDR and IMD3 performance of the DAC improves ∼12dB and ∼10dB respectively over a wide band for the TS-DEM 'on' solution.

The Sys-Gen/Vivado simulation results for the VF and BS DEM has similar performance as that of TS-DEM for

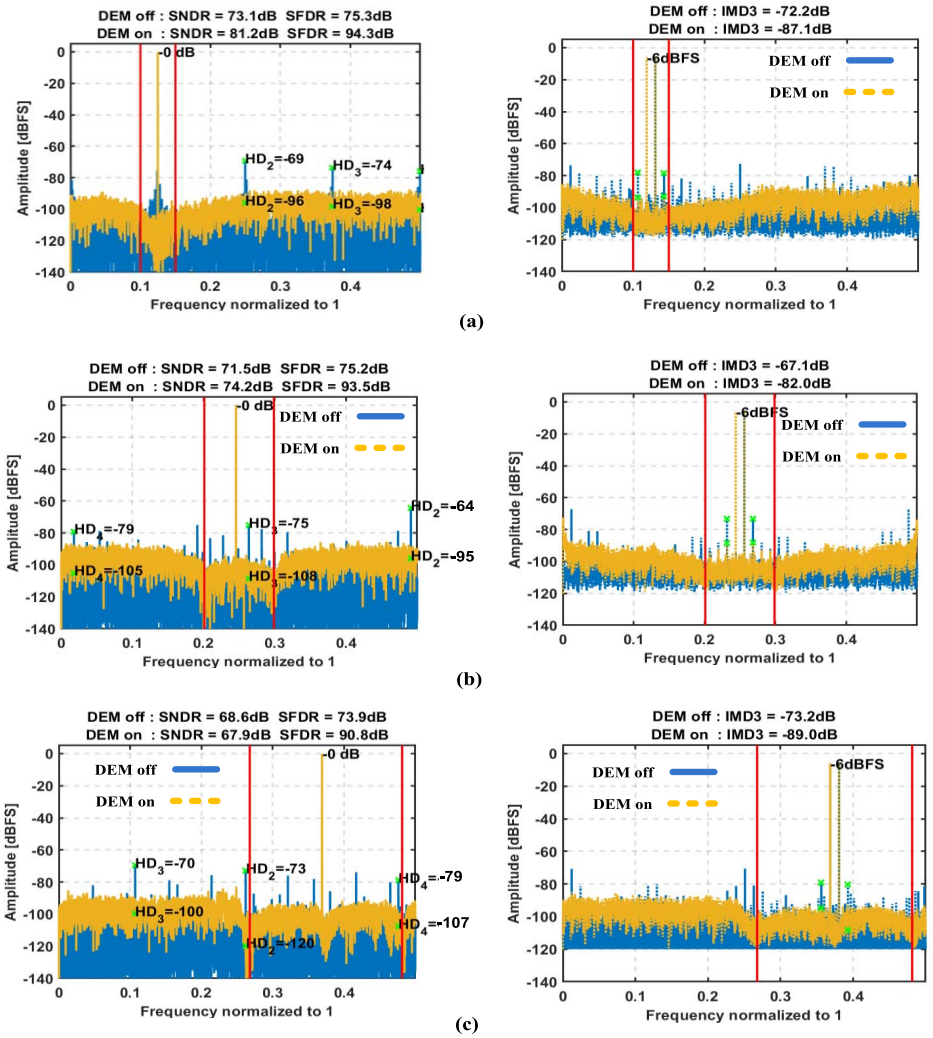

FIGURE 11. Single and dual tone spectrums for the DEM order selected to (a) 2 (narrow bandwidth), (b) 4 (medium bandwidth), (c) 6 (wide bandwidth) at $F_S/8$, $F_S/4$, and $3F_S/8$ centre-frequencies respectively using a 12-bit Nyquist DAC.

an order 2, 4 and 6 using the same number of bits and the same amount of mismatch error on the DAC elements. This is due to the same filter that is employed in the three DEM structures with the same bit widths in the data paths.

D. NOISE-SHAPED VS NON-SHAPED DEM PERFORMANCE

The mismatch error shaping bandpass DEM results for various filter orders are presented in the above sections. The random DEM on/off SNDR, SFDR, and IMD3 results using 100 MC runs at $F_s/8$, $F_s/4$, and $3F_s/8$ centre-frequencies are tabulated in Table 8. Here, the sigma of mismatch on DAC elements is 0.5% and the performance is evaluated over 20% of *Fs*. The results for the non-shaped DEM shown in Table 8 show the degradation in SNDR when compared to the SNDR values for the noise-shaped DEM in Table 7. This is due to pseudorandomly selecting the DAC elements that result in the increased noise floor for non-shaped DEM. Moreover, the 6th order mismatch shaping DEM average SFDR, and IMD numbers shown in Table 7 are ∼3dB better than the numbers shown for random (non-shaped) DEM in Table 8.

TABLE 7. 6th order TS-DEM on/off SNDR, SFDR and IMD3 results for a 12-bit DAC at $F_S/8$, $F_S/4$, and $3F_S/8$ using 100 MC runs.

At $F_s/8$ centre-frequency							
	Ideal	DEM off			DEM on		
(dB)	Avg.	Min.	Max.	Avg.	Min.	Max.	Avg.
SNDR	77.5	67.51	74.95	71.60	66.96	69.74	68.38
SFDR	96	70.19	83.89	77.83	88.22	92.00	90.21
IMD3	96	66.91	82.12	75.5	85.06	89.48	87.27
At $F_s/4$ centre-frequency							
	Ideal	DEM off			DEM on		
	Avg.	Min.	Max.	Avg.	Min.	Max.	Avg.
SNDR	77.5	61.71	73.20	68.15	68.81	69.97	69.44
SFDR	96	62.24	81.27	72.27	89.08	92.00	90.79
IMD3	96	63.34	74.28	71.60	80.64	83.50	82.01
At $3F_s/8$ centre-frequency							
	Ideal	DEM off			DEM on		
	Avg.	Min.	Max.	Avg.	Min.	Max.	Avg.
SNDR	77.5	68.02	74.81	72.55	66.46	69.44	68.20
SFDR	96	70.19	84.93	78.77	88.27	91.75	89.84
IMD3	96	66.24	79.93	71.72	85.31	92.00	89.57

TABLE 8. Non-shaped DEM on/off SNDR, SFDR and IMD3 results for a 12-bit DAC at $F_S/8$, $F_S/4$, and $3F_S/8$ using 100 MC runs.

At $F_s/8$ centre-frequency							
	Ideal	DEM off			DEM on		
(dB)	Avg.	Min.	Max.	Avg.	Min.	Max.	Avg.
SNDR	77.5	69.71	75.76	72.86	62.16	67.33	64.64
SFDR	96	72.49	85.26	78.52	86.08	88.67	86.58
IMD3	96	69.22	81.72	74.98	79.55	88.39	83.40
At $F_s/4$ centre-frequency							
	Ideal	DEM off			DEM on		
	Avg.	Min.	Max.	Avg.	Min.	Max.	Avg.
SNDR	77.5	63.05	73.21	68.63	62.75	67.28	64.44
SFDR	96	65.91	83.09	72.87	86.09	89.24	87.72
IMD3	96	63.38	77.87	75.15	77.16	84.62	79.50
At $3F_s/8$ centre-frequency							
	Ideal	DEM off			DEM on		
	Avg.	Min.	Max.	Avg.	Min.	Max.	Avg.
SNDR	77.5	68.30	73.70	71.34	62.10	67.21	64.63
SFDR	96	72.49	83.05	77.95	84.68	88.90	86.89
IMD3	96	66.24	82.42	75.93	83.16	90.00	86.08

VI. DEM-DAC MEASUREMENT RESULTS

This section provides the measurement results of the higher-order DEM design onto an FPGA board interfacing with a 5-bit CS-DAC. Fig. 12 shows the measurement set-up diagram that includes an FPGA evaluation board (ZCU104 MPSOC), an adapter, a DAC board, a data capture card, and a Personal-Computer (PC). The DEM logic is realized onto the UltraScale+ FPGA board. The input code to the DEM design is stored using FPGA RAM. An adapter connects the FPGA evaluation board and the DAC board. A 5-bit (32-element) unary-weighted CS-DAC [21] designed for low F_s (1MHz) is used to interface with the DEM solution. The CS-DAC is implemented using UMC 90nm CMOS technology. Each CS_{rc} cell delivers $\sim$30μA current to 500Ω external resistive load to produce a 0.48V output swing. The digital core logic is driven by a 1V supply whereas the analog circuitry uses a 1.2V supply. The chip is designed using 2.5V pads I/O's that interface to an external FPGA board through the adapter as shown in Fig. 12. The DEM design on the FPGA board and the analog DAC operates at the same clock frequency, i.e., CLK1. The analog output data from the DAC is captured using a National-Instruments data acquisition card.

Fig. 13(a) and (b) shows the 6^{th} order TS-DEM on/off spectrum (wideband performance) at $F_s/8$ and $3F_s/8$ centre-frequency respectively connected to the analog-DAC using the measurement set-up. The on/off TS-DEM spectral results for order 2 (narrowband performance) is shown in Fig. 13(c) at $F_s/8$. The F_s is normalized to 1 for the plots. Here, the measured analog output of the 5-bit MSB DEM-DAC is combined with an ideal 7-bit binary-weighted LSB-DAC section. The spectral shaping results using the measurement set-up for various filter order and different choice of centre-frequency locations does match with the synthesized DEM implementation results shown in Section V demonstrating that the DEM logic operation significantly improves spectral performance. Moreover, distortion tones over the Nyquist band are significantly reduced for the DEM enabled case.

VII. CONCLUSION AND FUTURE WORK

Nyquist DACs employed in transmitters demand high-speed and programmable DEM structures to alleviate mismatch errors over a full Nyquist range. In this paper, mismatch-shaping bandpass DEM architecture suitable for wideband Nyquist-rate D/A converters have been explored. The work presented implementation, validation and comparison of the VF, TS, and BS architectures using an UltraScale+ FPGA device. This work showed how programmability and improved performance for the high-order filter within the DEM logic can be achieved by splitting it into several stages and arranging them in parallel. Moreover, splitting the high-order filter into stages reduces the hardware complexity and introduces less quantization errors. In addition, the loop filter's frequency-response characteristics are designed using a simple pole-zero placement technique for different orders. As compared to VF DEM, the TS and BS DEM architectures do not have global feedback, therefore they can be more easily pipelined to improve the speed performance. The TS-DEM structure is more suitable to Nyquist-rate DACs as compared to VF and BS DEM structures regarding the speed of operation and logic area.

The FPGA implementation is chosen in this work for prototyping and validation of the DEM design, however, migrating the DEM implementations to ASIC is expected to increase speed by a factor of 2-3x and is scalable to lower nanometre CMOS nodes. The FPGA implementation results demonstrated that for a 12-bit Nyquist DAC, the lowest in-band SFDR and IMD3 is $\geq$ 88dB and $\geq$ 80dB respectively for various configurations of the DEM operating at a 75MHz clock frequency. The VF, TS and BS DEM structures have similar spectral performance for the same number of bit implementations due to the same loop-filter structure employed within. Furthermore, the DEM spectral performance is validated at a 12-bit level by obtaining measurement results by interfacing with an analog CS-DAC.

Since the VF-DEM has a global feedback feature, the TS and BS structures are more suitable for higher speeds of operation as pipelining can be inserted between each sub-layer segment. This reduces the critical path to the 'switching block' section. Further techniques such as unfolding loops to shorten the critical path are complicated by the quantizer in the signal path. However, pipelining using multistage bit reduction methods have been shown in [14], while other methods such as retiming and pipelining with quantizer loops [22], [23] are a way forward. Future work will investigate DEM design techniques applicable to Nyquist DACs operating at GHz speeds.

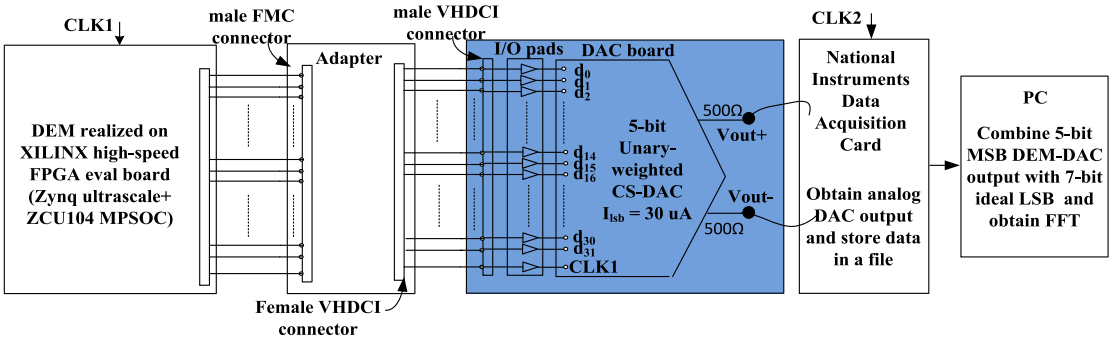

FIGURE 12. A 5-bit DEM-DAC measurement set-up diagram.

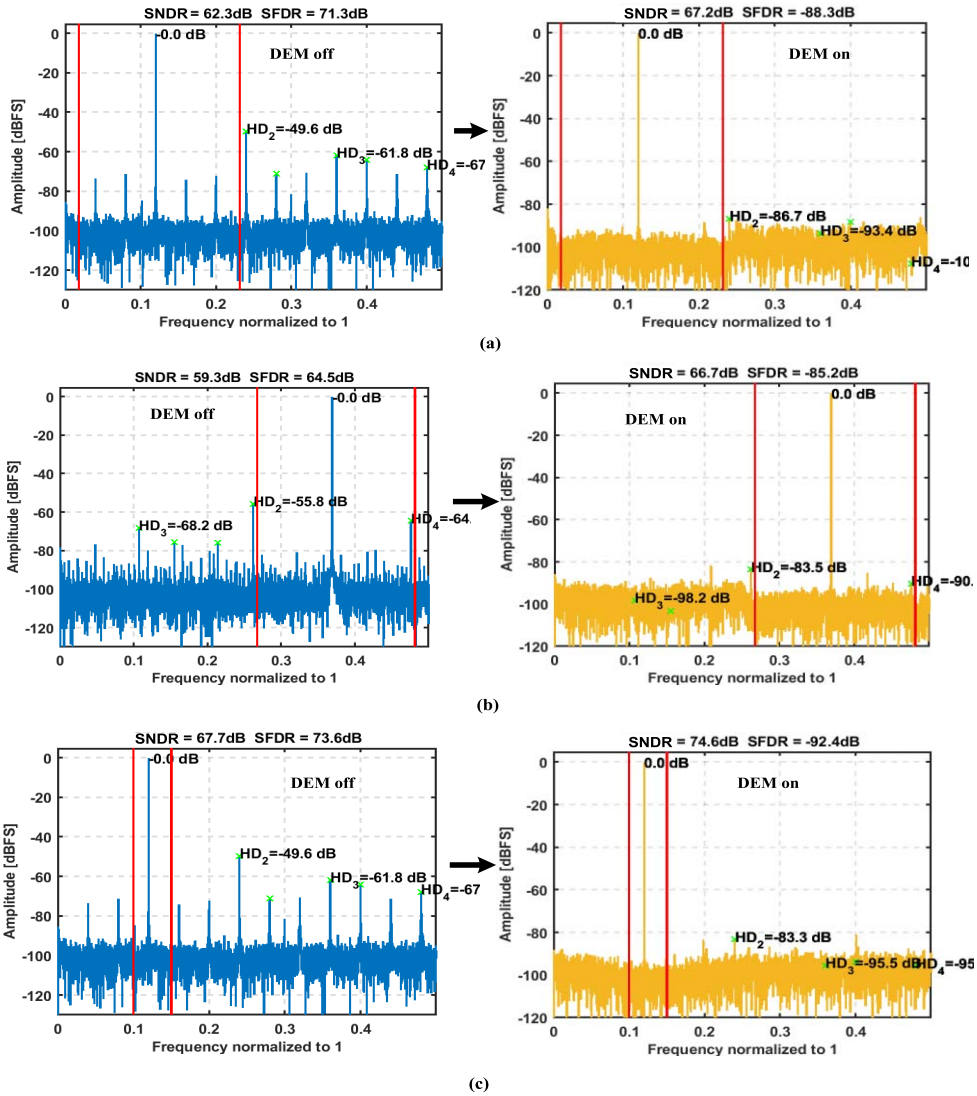

FIGURE 13. FFT results using measurement set-up for 6^{th} order TS-DEM at (a) $F_S/8$, (b) $3F_S/8$ center-frequency. (c) FFT results for 2^{nd} order TS-DEM at $F_S/8$ using the measurement set-up.

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