IEEE Open Journal of
Circuits and Systems

Received 25 August 2020; revised 18 December 2020 and 6 February 2021; accepted 7 February 2021. Date of publication 12 February 2021; date of current version 4 March 2021.

Digital Object Identifier 10.1109/OJCAS.2021.3058654

A Complementary Ring Mixer Driven by a Single-Ended LO in 22-nm FD-SOI CMOS for *K* and *Ka*-Bands

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This article was recommended by Associate Editor V. Chen.

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This work was supported by the Federal Ministry for Economics and Energy (BMWi) and by the State of Saxony through subcontract from GLOBALFOUNDRIES Dresden Module One within the framework Important Project of Common European Interest (IPCEI).

ABSTRACT This article presents a double-balanced up-conversion ring mixer based on complementary switches operating at millimeter-wave frequencies. Complementary-switching relieves the mixer from the need for a differential Local-Oscillator (LO) signal, simplifying the design and improving the circuit performance. A prototype, capable of operation between 18 GHz and 32 GHz, is implemented in a 22 nm FD-SOI CMOS technology offering n- and p-type transistors with comparable performance. Furthermore, the presented circuit also exploits the back-gate control voltage offered by the process to minimize the transistors threshold voltage, reducing the minimum LO power required to saturate the mixer gain. Measurements showed a conversion gain of –5.5 dB, an output power at 1 dB gain compression (o1dBCp) of –7 dBm, and a Radio-Frequency (RF) bandwidth of 10 GHz. These results were demonstrated for an LO power of 3 dBm at 23.5 GHz or 28 GHz, a DC power of 2.2 mW, and all the mixer ports matched to 50 Ω. The active area of the chip is 0.11 mm^2, the smallest so far demonstrated for ring mixers. These performances translate in the best-reported figure of merit, which relates gain, RF up-converted power, and required DC and LO power.

INDEX TERMS 22 nm FD-SOI, 5G, complementary switches, K-band, Ka-band, low power, millimeter-wave integrated circuits, RF CMOS, ring mixer, up-conversion.

I. INTRODUCTION

THE FIFTH-GENERATION mobile-communication standard (5G) achieves data rates above 10 Gbps using carrier frequencies in the *Ka*-band (26.5 GHz – 40 GHz). Depending on the actual world region, 5G uses different bands at millimeter-waves. Therefore, multi-band frontends are necessary to support the standard. Besides, broadband transceivers operating at *K*-band (18 GHz – 27 GHz) are also employed for the Industrial, Scientific, and Medical (ISM) unlicensed band and in automotive systems [1]. Finally, all these applications require the processing of the exchanged data.

Fully-Depleted (FD) Silicon-On-Insulator (SOI) Complementary Metal-Oxide-Semiconductor (CMOS) technologies offer compact transistors size, and above-300-GHz maximum-oscillation (f_{max}) and transit (f_t) frequencies. It is then possible to co-integrate in FD-SOI technologies Very-Large-Scale Integration (VLSI) digital circuits with millimeter-wave transceivers. For these reasons, FD-SOI processes play a dominant role in the realization of 5G systems. Furthermore, the latest FD-SOI technologies provide strain-engineered pMOS with performance comparable to those of the nMOS transistors [2], [3]. Recently, millimeter-wave circuits have been realized in FD-SOI CMOS processes, such as power amplifiers [3], low-noise amplifiers [4], broadband amplifiers [5], down-conversion mixers [6], phase shifters [7].

Up-conversion mixers are key components in transceivers. As discussed in [8]–[12], active mixers, such as those based on Gilbert cells, provide high conversion gain for reduced

LO power while requiring dc dissipated power (P_{DC}) and high voltage supply. On the contrary, passive mixers, such as ring mixers, do not dissipate dc power and are capable of larger linearity and broader bandwidth of operation. The former is useful in transmitters, while the latter is beneficial in multi-standard systems. The main drawbacks of passive mixers are the lower conversion gain and the higher required LO power than their active counterparts.

This work exploits the comparable performance of n- and pMOS transistors offered by a 22 nm FD-SOI CMOS technology to implement an up-conversion ring mixer based on complementary-switches and operating with a single-ended LO signal. In the presented design, the LO drives during its positive phase an nMOS pair and on its negative phase a pMOS one. Mixers based on complementary switching have been presented in the past [13]–[18]. In these works, a differential LO signal drives transistor gates (*T*-gates) formed by nMOS and pMOS connected in parallel, aiming at an LO leakage reduction. This work extends previous research demonstrating a ring mixer based on complementary switches where a differential LO signal is unnecessary. Furthermore, operation at millimeter-wave frequencies of this circuit class is achieved for the first time. Experimental characterization confirmed the mixer functionality with a sufficient gain and LO isolation for 5G mobile communications. In systems where a balun at the LO port is unnecessary, chip size and losses of the LO signal are reduced, and issues due to the imbalance between the differential LO signals are eliminated. The presented design solution exploiting both LO phases, and avoiding the power losses of baluns, reduces the LO power required to saturate the mixer gain, addressing one of the most significant limitations of this architecture. Furthermore, if different bands have to be supported, this approach enjoys the advantage of not requiring the challenging design of a wideband balun. Finally, the demonstration of circuits operating at millimeter-wave frequencies and implemented in deep sub-micrometer CMOS technology nodes paves the way to co-integrating VLSI digital and RF system blocks.

The manuscript is organized as follows: Section II outlines the major features of the process employed for this circuit implementation, Section III presents the proposed architecture together with its circuit analysis, Section IV gathers the experimental methods and results, while Section V concludes the work with a comparison against state of the art.

II. MM-WAVE IC TECHNOLOGY AND PASSIVE COMPONENTS

The mixer was implemented in a 22 nm FD-SOI CMOS technology offered by GLOBALFOUNDRIES under the trademark *22-FDX* [2]. The employed metal stack has nine copper levels labeled from the bottom to the top $M_{1,2}$, C_{1-5}, J_A, O_I, plus an additional top aluminum layer L_B [2], [6]. A thin buried oxide layer isolates the fully-depleted transistors from the low-resistivity substrate, decreasing the capacitive parasitics [2], [4]. One of the key features of

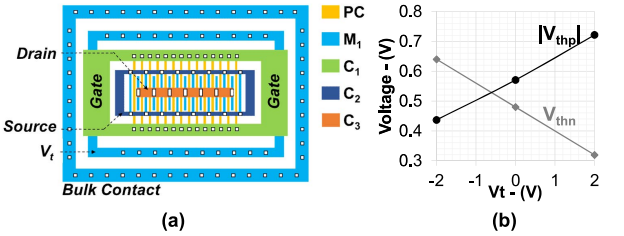

FIGURE 1. (a) Millimeter-wave transistor layout used in this work. The gate has a double contact to reduce the parasitic resistance, while the source and drain are accessible directly above the active area [19]. PC labels the gate polysilicon; (b) simulated n- and pMOS transistors threshold voltages $V_{thn,p}$ versus the back-gate control voltage V_t.

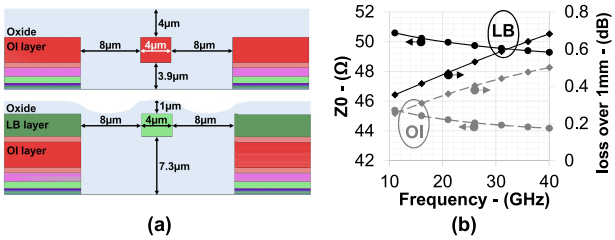

FIGURE 2. (a) Cross-section view of the L_B (top) and O_I (bottom) transmission lines; (b) simulated characteristic impedance Z_0 and attenuation over 1 mm of the O_I (gray) and L_B (black) lines

the *22-FDX* is its f_{max} of 371 GHz and 299 GHz, and its f_t of 347 GHz and 242 GHz of the super-low-threshold-voltage nMOS and pMOS transistors, respectively [2]. Such performance is reached thanks to the FD-SOI architecture, the strain-engineered channel, and the reduced gate resistance [2]. Figure 1(a) illustrates the transistor layout used in this work. The device is formed by 24 fingers of 20 nm length and 900 nm width. The minimum channel length of the process ensures the maximum transistor speed [19]. In contrast, the total transistor width W has been chosen according to mixer-design considerations described in the next section. The technology also provides a back-gate node to tune the threshold voltages V_{th} of the transistors. Figure 1(b) shows the simulated V_{th} for both n- and p-MOS versus the control voltage V_t.

Transmission lines were implemented with the signal conductors in the O_I or L_B layers, while the ground was sustained by lateral walls and a plane below the signal conductor. The ground plane was realized within C_1, and slotting was used to reduce the line losses [20]. Finally, the cross-section dimensions were optimized to have a characteristic impedance Z_0 close to 50 Ω and to fulfill the process metal density rules without metal fillers, avoiding the consequent Q-factor reduction as in [4]. Figure 2(a) shows the cross-section of the transmission lines. The L_B line suffers from higher losses than the O_I one because of the reduced conductivity and thickness of the signal conductor [6]. This is confirmed in Fig. 2(b), which presents the simulated line losses over 1 mm and the characteristic impedance of the transmission lines. As sketched in Fig. 2(a), the wafer IC passivation shows profiles with depressions where the

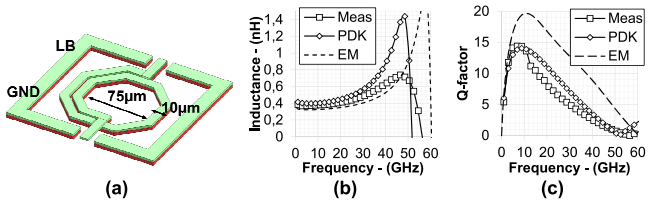

FIGURE 3. (a) 3D-View of the inductor used in this work together with its inductance (b) and Q-factor (c). Measurement (Meas), simulation with PDK model (PDK), and simulation without fillers with EM tool.

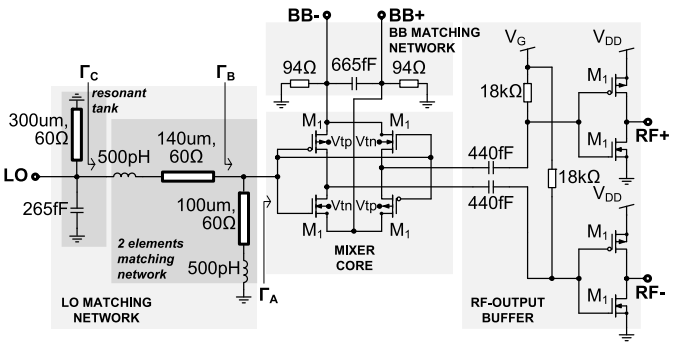

FIGURE 4. Circuit schematic of the presented CMOS up-conversion ring mixer.

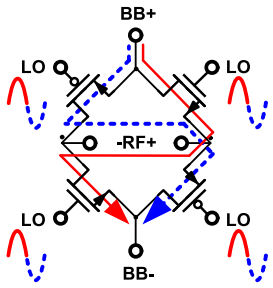

FIGURE 5. Proposed complementary ring-mixer architecture employing a single-ended LO signal.

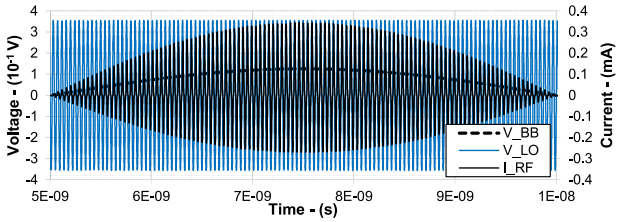

FIGURE 6. Time-domain simulation of the differential baseband voltage at 100 MHz (V_BB) and single-ended local-oscillator voltage at 23.5 GHz (V_LO) together with the current at 23.4 GHz flowing in a 100 Ω resistor connected at the RF port of the circuit in Fig. 5.

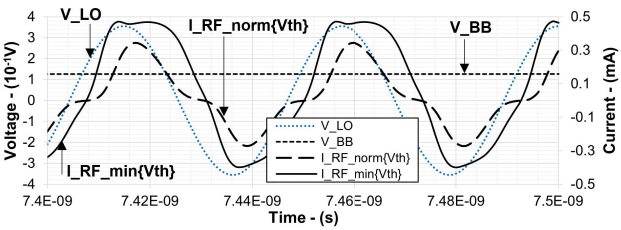

FIGURE 7. Time-domain simulation of the differential baseband voltage at 100 MHz (V_BB) and single-ended local-oscillator voltage at 23.5 GHz (V_LO) together with the current at 23.4 GHz flowing in a 100 Ω resistor connected at the RF port of the circuit in Fig. 5. The comparison between transistors operating in nominal and minimal threshold voltage is also shown.

Lj metal is not present. The irregular passivization profile translates into a more difficult description of the L_B line cross-section with respect to the O_I one, increasing the uncertainty on the line simulation. In-house measurements have shown deviations up to 10% from the simulated Z_0. In spite of these considerations, L_B lines have been used to route the BaseBand (BB) signals, which are more robust against these limitations due to their significantly lower frequency, leaving the O_I lines available for the other signals.

The *22-FDX* Product-Development-Kit (PDK) provides alternate-polarity metal-finger capacitors *apmom* superior in terms of Q-factor (15% better) and area (one fourth) than custom-made metal-oxide-metal multi-plate capacitors [4], [21]. Finally, the PDK inductors are suited for RF and millimeter-wave designs. Figure 3(a) illustrates the inductor used in this work, while Fig. 3(b) compares its measured inductance against simulation with the PDK model and electromagnetic (EM) tool. Finally, Fig. 3 presents the same comparison for the component Q-factor. The PDK model is based on de-embedded measurements, and it is more accurate than the EM simulation, where metal fillers were neglected to reduce the calculation effort. The measured inductance and Q-factor are 500 pH and 5 at 30 GHz, while the Self-Resonance Frequency (SRF) is 55 GHz. Simulations have shown that minor deviations against the PDK model are due to the custom ground-signal-ground interface.

III. CIRCUIT ARCHITECTURE AND ANALYSIS

Figure 4 presents the schematic of the mixer. The circuit is formed by the mixer core, the LO matching network, the RF output buffers, and the baseband matching network.

A. MIXER CORE

The mixer core consists of four transistors, two pMOS and two nMOS, used as switches. The LO signal drives all transistor gates, activating on its positive phase the nMOS devices and on its negative phase the pMOS ones, as Fig. 5 sketches. Each of the pairs is used to connect the BB (input) port to the RF (output) port, alternating the polarity of the RF signal when the phase of the LO changes.

To highlight the mixer operation, Figures 6 and 7 show the time-domain simulations of LO and BB voltages together with the current flowing into a 100 Ω resistor when connected at the RF port. During the positive LO phase, the nMOS switches are closed while the pMOS ones open, so the BB signal is transferred to the RF port while a positive current flows into the load resistor. On the contrary, during the negative LO phase, the pMOS switches are closed, and the BB signal appears at the RF port inverted in sign. Consequently, the RF current changes sign with the LO

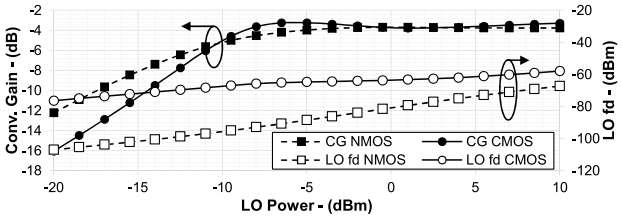

FIGURE 8. Comparison between the simulated open-voltage up-conversion conversion gain (CG) and LO feed-through (fd) for an nMOS ring mixer and the CMOS ring mixer presented in this work for the same device size, when the LO is at 23.5 GHz, and the BB signal is at 100 MHz with –20 dBm power. Layout parasitics are not included while the transistor threshold voltage is minimized via the back-gate signal.

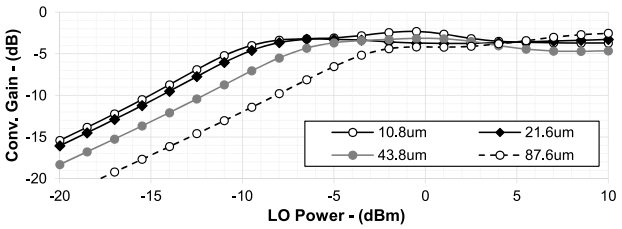

FIGURE 9. Comparison between the simulated open-voltage conversion gain of the CMOS ring mixer core presented in this work for a switch transistor width W between 10.6 μm and 87.6 μm, when the LO is at 23.5 GHz, and the BB signal is at 100 MHz with –20 dBm power. Layout parasitics are not included while the transistor threshold voltage is minimized via the back-gate control.

signal. Figure 7 compares the RF current in case of nominal and minimal transistor threshold voltages, tuned via the back-gate contact (Fig. 1): a higher RF current, and hence conversion gain, is obtained for a given LO amplitude when the threshold voltage is minimized.

The presented complementary solution is more efficient than conventional transistor-monopolarity ring mixers since both LO phases are used for the frequency conversion. Figure 8 confirms this showing the comparison between the simulated conversion gains of an nMOS ring mixer against the CMOS mixer presented in this work for the same device size when the LO is a 23.5 GHz and the BB signal is at 100 MHz with –20 dBm power. The conversion gain of the presented mixer saturates at –7.5 dB LO power, while that of the nMOS one at –3 dB. Moreover, the simulation does not include the losses of the balun required to generate the differential LO, which drives the nMOS mixer, neither the possible phase and amplitude imbalance of the balun paths. On the other hand, the simulation of the presented complementary mixer not requiring a balun is closer to real-implementation performance. Finally, Fig. 8 also illustrates the LO feed-through, or leakage, to the RF port for the two circuits. Although the nMOS mixer shows higher levels of isolation thanks to the differential LO signals, the presented mixer still retains isolation above 60 dB, highlighting that the complementary design and the body biasing do no entail a substantial degradation of the LO-to-RF isolation.

Three types of losses have to be considered in this type of passive mixer: (a) those arising from the switches L_{SW} not providing a perfect short or open impedance in their ON and OFF states; (b) the losses relative to the mixing process L_{MX}; (c) those due to layout parasitics. The devices sizing aims at the minimization of L_{SW}. When transistors are used as switches, their ON and OFF impedance $Z_{\rm ON}$ and $Z_{\rm OFF}$ are approximated as [8]:

$$Z_{\rm ON} \approx R_{ds,\rm ON} \approx \frac{L}{W\sigma}, \qquad |Z_{\rm OFF}| \approx \frac{1}{\omega L W C_{g,A}} \tag{1}$$

with $R_{ds,\rm ON}$ the drain-source resistance when the device is in saturation, σ the channel conductance, and $C_{g,A}$ the gate capacitance per unit of area. From (1) it can be concluded that a minimum channel length for L is beneficial to both $Z_{\rm ON}$ and $Z_{\rm OFF}$, while a trade-off value exists on the devices width W [8]. The loss limit L_{SW} due to the non-ideal $Z_{\rm ON}$ and $Z_{\rm OFF}$ of each switch is [8], [25]:

$$L_{SW} = 1 + 2\delta^2\left[1 + \sqrt{1 + \left(\frac{1}{\delta}\right)^2}\right], \quad \delta = \left|\frac{Z_{\rm ON}}{Z_{\rm OFF}}\right| \tag{2}$$

where a minimum δ minimizes L_{SW}. As mentioned above, this is achieved with a minimum channel length of the device, while the total switch loss is independent from the channel width assuming a symmetric open and close time for the switches [25]. Nevertheless, the LO power required to saturate the conversion loss (completely switching the transistors between ON and OFF states) decreases for a decreasing W, and associated gate capacitance [25]. The simulation in Fig. 9 confirms the trend. Small transistor widths are also beneficial for the mixer bandwidth, since smaller devices have less parasitic capacitances. On the contrary, a small W increases the difficulty in matching the LO port [25], and reduces the linearity in terms of current driving capabilities of the switches for a given gate-source voltage. A trade-off value of 21.6 μm for W has been chosen to satisfy at the same time bandwidth, linearity, and LO power requirements. Simulations have shown that for these device dimensions, the $R_{ds,\rm ON}$ of n- and pMOS devices are 4.0 Ω and 9.2 Ω, respectively, for grounded drain and source nodes and for an LO voltage amplitude of ±1 V. For identical conditions, the gate capacitances $C_G = LWC_{g,A}$ are 11.6 fF and 12.8 fF for n- and pMOS transistors. L_{SW} for the n- and pMOS switches calculated at 30 GHz are then 0.15 dB and 0.38 dB. The small employed channel length and the associated low parasitics produce these relatively low values of L_{SW} [8].

The losses of the mixing process in the case of open load can be calculated from the relation between the RF and BB signals [26]:

$$v_{RF}(t) = \frac{g_p(t) - g_n(t)}{g_p(t) + g_n(t)} v_{BB}(t) = m(t) v_{BB}(t) \tag{3}$$

with $g_p(t)$ and $g_n(t)$ the conductance of p- and nMOS at a time t. Figure 10 presents the simulated $g_p(t)$ and $g_n(t)$ for the devices used in this work with the value of LO voltage amplitude and device dimensions mentioned above. The two functions are delayed by half LO period T_{LO}, while the peak conductance of the n-type device is 9% higher than the p-type

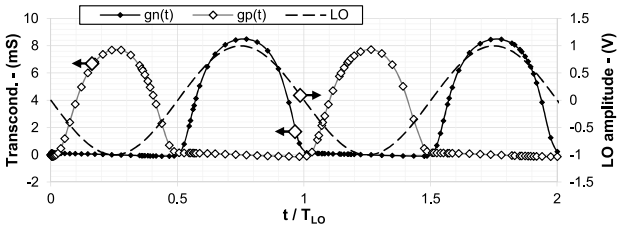

FIGURE 10. Simulated conductance of the p- and nMOS transistorsch in Fig. 5, $g_p(t)$ and $g_n(t)$, versus time normalized to the LO period.

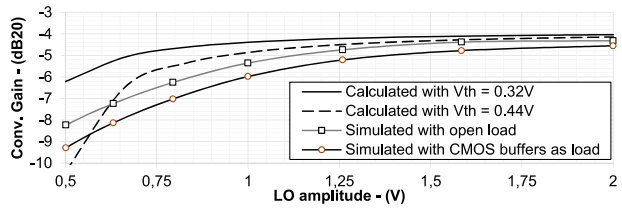

FIGURE 11. Open-load conversion gain calculated with (5) and $|V_{thn,p}|$ of 0.32 V and 0.44 V covering the case of nMOS and pMOS mixers biased at minimum threshold voltage, respectively. The simulated conversion gain of the presented mixer core when the load is an open, and when it is the input impedance of the CMOS buffers, is also shown.

counterpart. In these conditions, the approximation $g_n(t) \approx g_p(t - T_{LO}/2)$ holds, and the relation between RF and BB signals reduces to [26]:

$$v_{RF}(t) \approx \frac{g(t) - g(t - T_{LO}/2)}{g(t) + g(t - T_{LO}/2)} v_{BB}(t) = m(t) v_{BB}(t) \qquad (4)$$

while the voltage conversion gain of the mixer core, which accounts for the losses of the mixing process, G_C given by the Fourier transform of $m(t)$ evaluated at the LO frequency is [26]:

$$G_C = \frac{2}{\pi}\sqrt{1 - r^2}, \qquad r = \frac{V_{th}}{A_{LO}} \qquad (5)$$

where V_{th} is the transistors threshold voltage and A_{LO} the amplitude of a sinusoidal LO signal with dc component equal to zero. This switching condition is called *break-before-make*, and the LO amplitude needs to overcome the transistors threshold voltage to saturate the mixer gain [26]. Furthermore, in this operation mode, the transistor gates and mixer LO port are dc grounded simplifying the component integration into the front-end, while the minimization of the transistors threshold voltage via the back-gate potential ensured low required the LO power. Figure 11 compares the simulated G_C of the mixer core against (5) evaluated for $|V_{thn,p}|$ of 0.32 V and 0.44 V covering the case of all-nMOS and all-pMOS mixers biased at minimum threshold voltage, respectively. The G_C of the proposed mixer, simulated with PDK transistor models and open load, is well predicted by (5) for sufficiently high LO voltage amplitude. Figure 11 also presents the simulated G_C when the mixer core is loaded with the CMOS output buffers described in Section III-D, showing minimal deviation with respect to the case of open load. This result is achieved thanks to the high input impedance of the buffers. Finally, (5) highlights that the LO amplitude, and hence power, required to

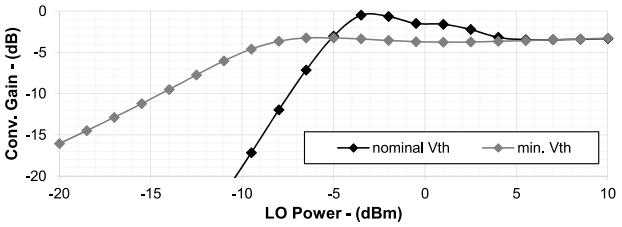

FIGURE 12. Comparison between the simulated open-voltage conversion gain of the CMOS ring mixer core presented in this work for nominal and minimal transistors threshold voltage (V_{th}), when the LO is at 23.5 GHz, and the BB signal is at 100 MHz with –20 dBm power. Layout parasitics are not included.

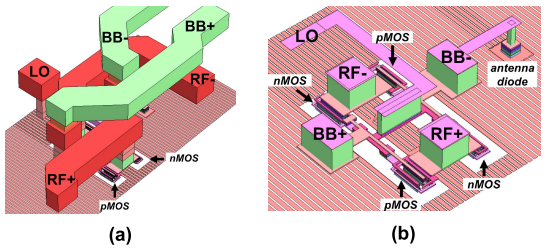

FIGURE 13. Layout 3D-view of the mixer core in Fig. 5: (a) view of the top metals (L_B, O_I) where the global routing of BB, LO, RF signals is implemented; (b) view of the lower metals where the transistor interconnections are realized.

saturate the conversion gain decreases for a decreasing the threshold voltage. The back-gate potentials of the transistors have been thus biased in agreement with (Fig. 1(b)) to minimize V_{th}. Figures 7 and 12 illustrates the impact of V_{th} on the mixer response. Furthermore, reducing the threshold voltages acting on the back-gate potentials makes unnecessary the biasing of the MOS gates at their threshold voltage to maximize the conversion gain to $2/\pi$. Hence, the gate potential can be grounded, avoiding, in turn, dc-decoupling capacitors and associated losses for the LO port [9], [10].

Figure 13(a) shows the 3D-view of the transmission lines reaching the mixer core, while Fig. 13(b) illustrates the transistor interconnections. An H-tree layout distributes the LO signal uniformly to the transistor gates, while the symmetric arrangement of RF and BB routing ensures uniform parasitics around the transistors. At the best of the authors' efforts, the LO signal loss due to layout parasitics within the mixer core is 2 dB, while 1.3 dB and 0.7 dB affected the BB and RF distribution, respectively.

B. BASEBAND MATCHING NETWORK

The baseband port is matched with a first-order Resistor-Capacitor (RC) filter implemented with two 94 Ω n^+ polysilicon silicided resistors (*npcres*) in parallel to the single-ended BB ports, plus a 665 fF *apmom* capacitor connected between them. For a given resistance in parallel to the single-ended BB ports, a higher capacitance value reduces the bandwidth of the BB signal. For differential excitation at the BB port and the chosen capacitance and resistors value, the –3 dB corner frequency of the differential voltage across the capacitor is 5 GHz, which in turn sets the maximum up-converted RF band of the mixer to 10 GHz.

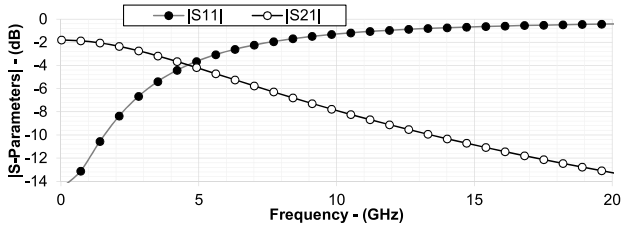

FIGURE 14. Response of the baseband matching network simulated with PDK models for a differential excitation. Layout parasitics are not included.

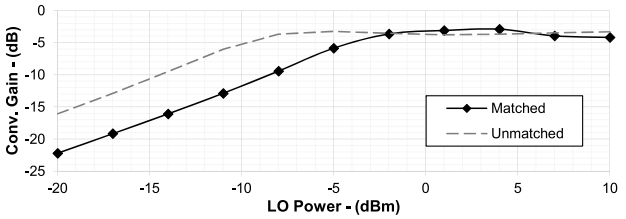

FIGURE 15. Comparison between the simulated open-voltage conversion gain of the ring mixer presented in this work when the LO port is matched and unmatched, and for a LO signal at 23.5 GHz and a BB signal at 100 MHz with –20 dBm power. Layout parasitics are not included while the transistor threshold voltage is minimized via the back-gate signal.

Towards dc, the differential impedance at the BB port is 94 Ω, a trade-off value between matching, bandwidth, and conversion gain. The voltage at the baseband port is proportional to the value of this resistor; values above 50 Ω increase the conversion gain while deteriorating the matching. Although several mixer implementations do not match the BB port to maximize the conversion gain, signal ringing on this port could occur, deteriorating the transceiver's performance where the mixer is employed, especially for BB frequencies in the GHz range as in this work. The simulated filter response is shown in Fig. 14: the minimum insertion loss of the network is 2 dB.

C. BROADBAND LO MATCHING NETWORK

When the mixer is integrated into transceivers, low LO power required to saturate the mixer gain, and matching for the LO port contribute to the system performance. It is challenging to generate high power at high frequency. At the same time, a large mismatch of the LO port can affect other frontend blocks, for example, when the local-oscillator drives mixers in quadrature through passive networks. A trade-off exists between the LO matching and the LO power which saturates the conversion gain. The switching MOS transistors, forming the ring mixers, are controlled by their gate-source voltage rather than by the power injected into the LO port. Being the MOS gate impedance mostly capacitive, for a fixed generator power, a higher voltage appears on the switching transistor gates in case of mismatching, and consequently a lower LO power is required to saturate the mixer gain when compared to the case of matched LO port. The simulation in Fig. 15 confirms the trend. Indeed, high voltages on the switching MOS gates can also be obtained by resonating their capacitance with inductive elements, but the approach is viable only for a fixed LO frequency [11].

Although the presented mixer does not require matching at the LO port to operate stand-alone, and it would show superior efficiency in terms of LO power requirements in case of mismatching at this port (Fig. 15), in practice, the LO matching ensures the correct functionality of the frontend where the mixer is integrated. In detail, the LO matching is critical in 5G massive Multiple-Input-Multiple-Output (MIMO) systems, where several mixers share the LO signal, and mismatching at one mixer LO port could disturb the operation of the other components. Hence, a LO matching network useful to support multiple 5G bands has been designed. Moreover,

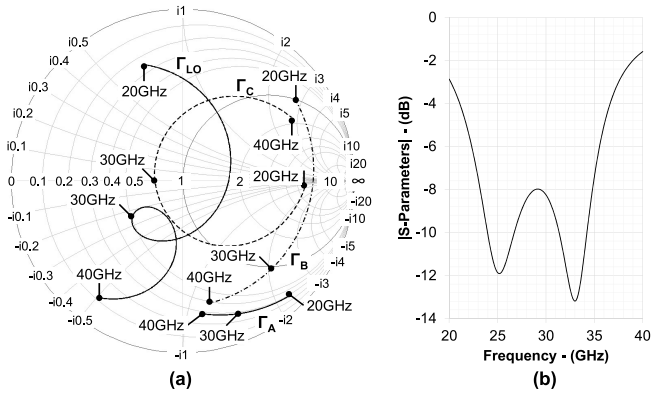

FIGURE 16. Smith representation of the simulated impedance annotated in Fig. 4, and simulated S-Parameter magnitude of the scattering parameter at the LO port.

the presented approach is also a proof of concept for a general broadband-matching technique. The matching network consists of capacitors and inductors plus O_I lines to physically separate them, enabling the layout (Fig. 4). At its core, the matching network is formed by a two-element section that matches the impedance at the center of the frequency band of interest, and by an inductor-capacitor tank that resonating folds the scattering parameter around the Smith-chart center. As described in [23], [24], broadband matching is achieved in this way by exploiting the different impedance (or admittance) shown at different frequencies by the same passive elements due to resonance effects. Figure 16(a) illustrates the Smith representation of the impedance seen at the sections of the LO matching network implemented in the mixer (Fig. 4). Simulations after parasitics extraction indicated that the time-averaged impedance versus the LO phase seen at Section III-A towards the mixer core (Γ_A) is $14\,\Omega + (j\omega\,70\,\text{fF})^{-1}$. The design of the two-element inductive network follows the conventional approach where the 50 Ω-constant circle of the Smith chart is reached with a parallel inductance, while the second inductor matches the imaginary part of the impedance. The scattering parameter at Section III-C is now over an almost full circumference, and matching is achieved in the middle of the frequency band of interest. Finally, the anti-resonant circuit formed by the 265 fF capacitor and 300 μm line (=120 pH), resonating at 28 GHz, transforms the impedance at Section III-C as if it

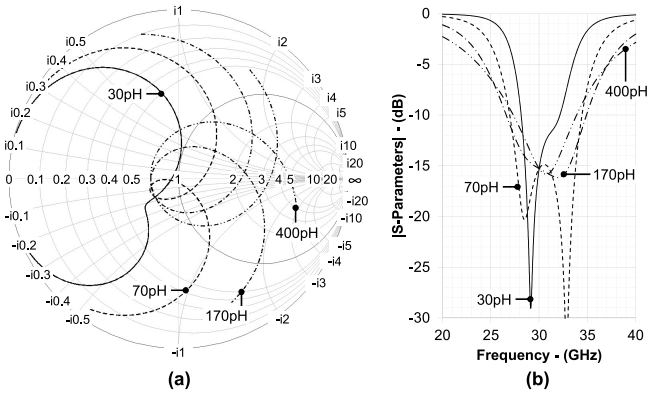

FIGURE 17. Simulated Smith representation and S-Parameter magnitude of the impedance at the LO port for different inductance and capacitance of the resonant tank (Fig. 4) resonating at 30 GHz. Only the inductance values are annotated, while the capacitance is adjusted to keep the resonance frequency at 30 GHz.

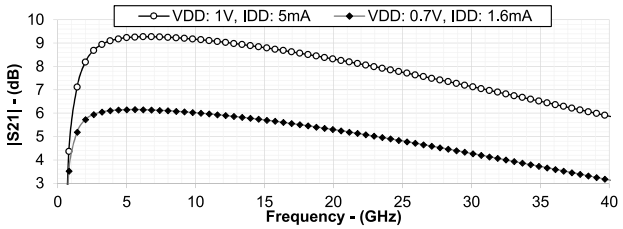

FIGURE 18. Simulated CMOS-output-buffer small-signal gain $|S_{21}|$ versus frequency for V_{DD} of 0.7 V and I_{DD} of 1.6 mA (Transistors in weak-inversion), and for V_{DD} of 1 V and I_{DD} of 5 mA (Transistors in saturation). Layout parasitics are not included.

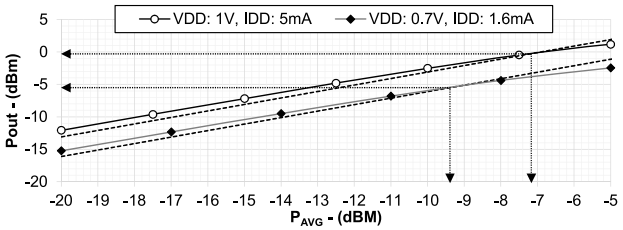

FIGURE 19. Simulated CMOS-output-buffer output power versus the generator available power P_{AVG} for V_{DD} of 0.7 V and I_{DD} of 1.6 mA (transistors in weak-inversion), and for V_{DD} of 1 V and I_{DD} of 5 mA (transistors in saturation). Layout parasitics are not included.

was connected to a parallel inductor for frequencies below the resonance and as if connected to a parallel capacitor for frequencies above the resonance. This folds the scattering parameter around the center of the Smith chart, ensuring a broadband matching. Indeed, multiple inductor-capacitor combinations could have been used to design the resonant tank for a fixed frequency of resonance. Figure 17 shows the simulated impedance at the LO port for a target resonance of 30 GHz and with ideal LC components for the tank. For an increasing value of inductance, the folding of the scattering parameter around the Smith-chart center (Fig. 17(a)) and the frequency band of the matching (Fig. 17(b)) broadens. Components SRF and layout feasibility set then the chosen LC pair for the circuit implementation. Finally, in condition of perfect matching, the losses of the LO matching-network are 1.1 dB at 23.5 GHz and 1.4 dB at 28 GHz. At 23.5 GHz, each inductor loses 0.3 dB, the capacitor 0.1 dB, and the remaining 0.4 dB are lost into the interconnecting transmission lines. Similar breakdown of the losses among the components take place at 28 GHz. Indeed, the longer the transmission lines and the bigger the inductors, the higher are the signal losses.

D. OUTPUT BUFFERS

CMOS output buffers are employed to increase conversion gain, output power, isolation from RF to LO and BB ports, and to ensure output matching towards 50 Ω loads. The transistors of the buffers are sized with minimum length to have maximum transconductance and minimum gate capacitance for a given device-width *W*. The output buffer resistance is 67 Ω, while the output buffer capacitance is 30 fF (=180 Ω at 30 GHz) for a p- and nMOS width of 21.6 μm. These values are almost constant over the frequency range of interest, ensuring a broadband matching condition. RC first-order high-pass filters connect the mixer core to the buffers. A 440 fF *apmom* capacitor and an 18 k Ω n^+ polysilicon un-silicided resistors (*opnpcres*) realize a –3 dB lower-corner frequency of 20 GHz, a value beneficial to improve the isolation between RF and BB ports. The input impedance of the buffer is 25 Ω + j115 Ω at 30 GHz, offering a high-impedance load to the mixer core useful for the conversion gain. The voltage supply of the buffer V_{DD} is 0.7 V, while the gate potential V_G is 0.35 V, which corresponds to a bias drain current of 1.6 mA and power consumption of 1.12 mW per buffer. In the chosen bias point, the transistors operate in the sub-threshold region, also called weak-inversion region [22], since the transistors V_{GS} is 0.35 V while their threshold voltages $|V_{thn,p}|$ is close to 0.5 V. In weak inversion, the relation between drain current and gate-to-source voltage is approximated by an exponential relation [22], which increases the transistors transconductance and gain with respect to the operation in saturation region for a given bias drain current, while it decreases the linearity. Hence, the sub-threshold biasing enables higher efficiency in terms of gain to required dc power [22]. Figures 18 and 19 summarize the effect showing the simulated small- and large-signal behavior of the buffer for the two operation modes: in weak inversion, the peak gain and the output-power in 1 dB gain compression are 6 dB and –5.5 dBm for a P_{DC} of 1.12 mW, while in saturation 9.2 dB and 0 dBm are obtained with 5 mW. These results correspond to an efficiency in terms of gain to dc power consumption of 5.35 dB/mW for the sub-threshold, and 1.84 dB/mW for the saturation. Same trend is observed for the output power once converted in linear scale.

E. TOTAL CONVERSION-GAIN CALCULATION

The total power conversion gain of the mixer is expressed in dB notation by:

$$G_{Mx} \approx G_C + 10\log_{10}\left(\frac{R_{C,in}}{R_{C,out}}\right) + G_{buf} - L_{BB} - L_{par} - L_{SW} \quad (6)$$

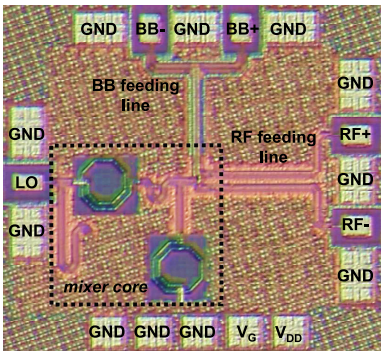

FIGURE 20. Chip micro-photograph of the presented CMOS up-conversion ring mixer. The chip dimensions are 0.83 mm per 0.76 mm, while the core area is 0.11 mm^2.

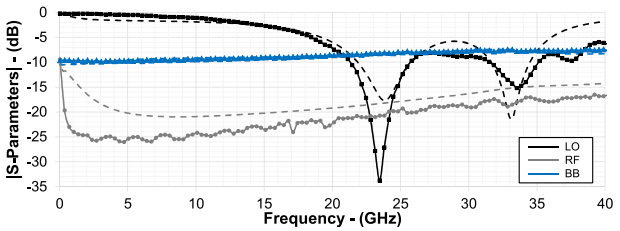

FIGURE 21. Measured (solid) and simulated (dashed) single-ended scattering parameters magnitude at the mixer ports.

where $R_{C,in}$ and $R_{C,out}$ are the input and output mixer-core impedance evaluated at the BB and RF frequency (3 dB), G_{buf} is the output buffer gain (5 dB), L_{BB} is the baseband filter insertion loss (2 dB), and L_{par} are the signal losses due to layout parasitic (4 dB). Equation (6) evaluated with the simulated design values predicts a mixer power gain of –3.5 dB, a value in agreement with the measurement results presented in the next section.

IV. MEASUREMENTS METHODS AND RESULTS

Figure 20 shows the micro-photograph of the mixer. The circuit was characterized with wafer probing; the presented results include the losses of pads and on-chip transmission lines used to reach the mixer. The supply voltage of the mixer buffers V_{DD} was 0.7 V, while their total bias current I_{DD} was 3.2 mA (1.6 mA per buffer).

Figure 21 presents the single-ended S-Parameters of the mixer ports measured and simulated for a reference impedance of 50 Ω. The scattering parameter of the RF port was below –15 dB from 1 GHz to 40 GHz, while that of the LO port was below –8 dB from 20 GHz to 38 GHz. Finally, the matching of the BB port was below –9 dB from dc until 15 GHz.

Two signal generators and a spectrum analyzer realized the measurement setup for the conversion gain. The generators provided the BB and LO signals, while the spectrum analyzer captured the up-converted RF signal, as Fig. 22 illustrates. An off-chip balun fed the BB signal differentially to the mixer, while a second balun combined the differential up-converted RF outputs. A power meter was used to calibrate the setup, de-embedding the losses of the cables and baluns

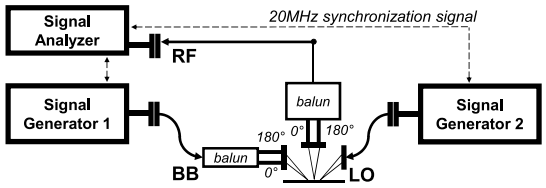

FIGURE 22. Measurement setup used to characterize the mixer conversion gain.

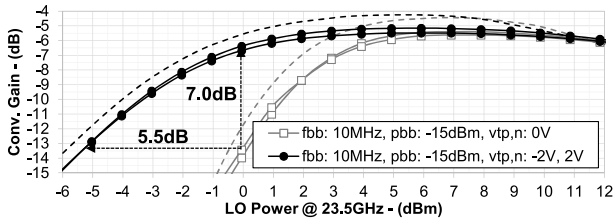

FIGURE 23. Measured (solid) and simulated (dashed) conversion gain of up and low sidebands versus LO power for nominal (grounded back-gate control voltages) and minimum transistors threshold-voltages.

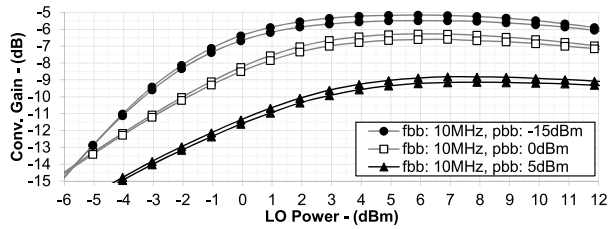

FIGURE 24. Measured conversion gain of up and low sidebands versus LO power for different BB power (*pbb*).

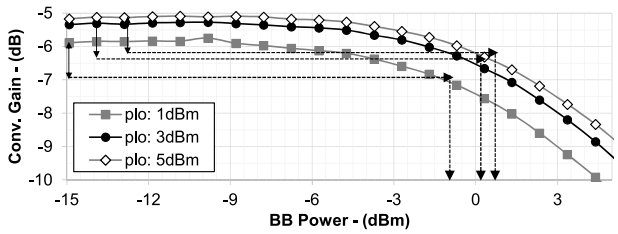

FIGURE 25. Measured conversion gain of the up sidebands versus the BB power *pbb* for different LO power *plo* at 23.5 GHz.

used to connect instruments and probes. Finally, the probes losses were known from direct measurements available in their data-sheet.

Figure 23 shows the measured and simulated conversion gain for both high and low sidebands when the BB signal was –15 dBm (*pbb*) at 10 MHz (*fbb*), and the LO power (*plo*) varied from –6 dBm to 12 dBm at 23.5 GHz. The measured saturated conversion gain was –5.5 dB for an LO of 3 dBm. Furthermore, the results compare the conversion gain for nominal and minimal threshold voltages of the transistor. In agreement with (5), a reduced LO power is necessary to saturate the conversion gain when the threshold voltage is minimized. For this reason, the remaining mixer characterization was performed at the minimum threshold voltage.

TABLE 1. State of the Art of Up-Conversion Ring Mixers Operating at or Close-To the *K*- and *Ka*-Band

Ref.	RF BW (GHz)	LO freq. (GHz)	LO pwr. (dBm)	Gain (dB)	LO-RF* (dB)	EVM† (%)	o1dBCp (dBm)	P_{DC} (mW)	Area+ (mm^2)	Key features	BB* (dB)	LO* (dB)	FOM ×100	Tech.
[9]	35	32.5	10	–15	25	19.9	–12	0	0.15	gate bias. for LO reduct.	no	no	0.02	0.18 μm CMOS
[10]	68	60	0	-3	35	3.9	–11	6	0.12	weak inv. plus IF buffer	n.a.	no	0.56	0.9 μm CMOS
[11]	10	28	8	–8.5	44	2.1	–2.7	0	0.20	LO boosting via res.	no	no	1.12	0.18 μm CMOS
[12]	19	28	3	1.5	45	5.6	–17	2.75	1.12	buffers on BB port	n.a.	no	0.59	0.18 μm CMOS
This	10	23.5 | 28	3	–5.5	29	6.3	–7	2.2	0.11	sing.-end. LO + RF buffer	–10	–35	1.34	22 nm FD-SOI

*: isolation, +: core area, *: matching, †: $EVM_{LO\_Leakage}$.

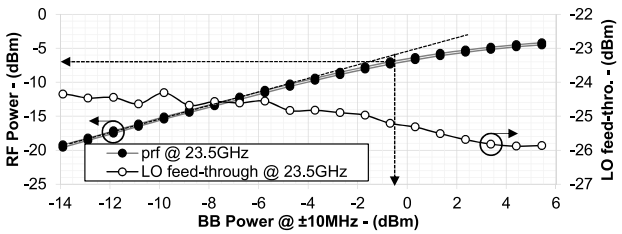

FIGURE 26. Measured up-converted RF and LO feed-through power leakage at the RF port versus *pbb* at 10 MHz when *plo* is 3 dBm.

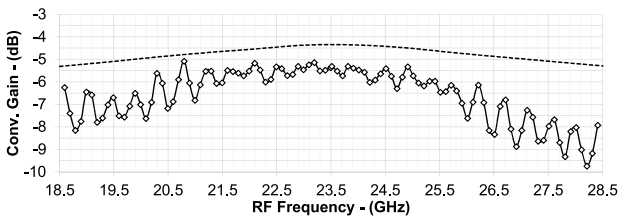

FIGURE 27. Measured (solid) and simulated (dashed) conversion gain versus RF frequency.

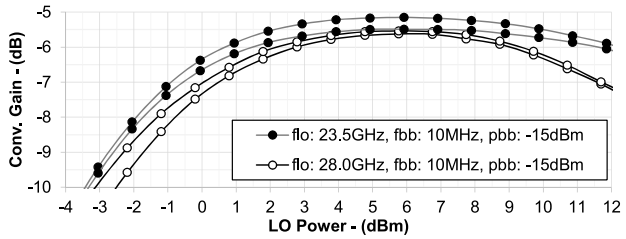

FIGURE 28. Measured conversion gain of up and low sidebands versus LO power at 23.5 GHz and 28 GHz.

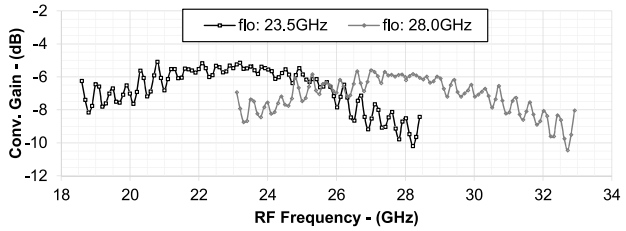

FIGURE 29. Measured conversion gain versus RF frequency when the LO frequency (*flo*) is 23.5 GHz or 28 GHz.

The mixer linearity is presented in Figs. 24 and 25, where the measured conversion gain versus BB power is shown for different LO power. Due to the non-linearities of the mixer, the conversion gain drops for increasing BB power. Moreover, the BB power that compresses the conversion gain by 1 dB (*BB1dBcp*) increases with the LO power. Finally, Fig. 26 presents the measured RF power and LO feed-through leakage when the BB power is swept. A *BB1dBcp* of –0.5 dBm, an RF power of –7 dBm, and an LO isolation of 29 dB were measured when the LO power was 3 dBm. Measurements of the stand-alone off-chip balun used to combine the RF differential signals indicated that the phase imbalance between the balun paths is 2 degrees. Since the adopted mixer measurement technique is based on a power budget between the mixer ports, the balun phase imbalance could not be de-embedded from the presented results. The 2 degrees phase imbalance translates in a maximum measurable isolation of 29 dB, assuming a sinusoidal differential signal at the RF port.

Figure 27 presents the frequency response of the mixer for an LO tone at 23.5 GHz. The measured –3 dB frequency band is 10 GHz, in agreement with the response of the BB matching network (Section III-B). Figure 28 shows the comparison between the conversion gain for an LO at 23.5 GHz and at 28 GHz versus the LO power, while Fig. 29 presents the comparison versus the RF frequency. The conversion gain decreases for an increasing LO and RF frequency due to a higher impact of the parasitics. Finally, measurements of the stand-alone baluns indicated that the ringing on the conversion-gain response away from the LO carrier originated from the uncompensated phase-unbalance of the baluns, being the measurement method again based on a power budget between the mixer ports.

V. CONCLUSION

This work demonstrated the first up-conversion ring mixer where the comparable performance of the n- and p-type transistors are employed to implement the switching functionality without using differential LO signal at millimeter-wave frequencies. The mixer is implemented in a 22-nm FD-SOI technology and targets ISM and 5G applications between 18.5 GHz and 32.5 GHz, covering the *K* and *Ka*-bands. Furthermore, the back-gate control voltage of the transistors has been used to minimize the transistors threshold voltage, reducing, in turn, the LO power required to saturate the conversion gain of the mixer. The circuit has been described highlighting the main features of the technology employed in the design, while the circuit analysis has been also provided demonstrating an estimation of the gain in agreement with the measurement results. Finally, a simple broadband matching network has been proposed for the LO port together with design guidelines. The experimental characterization

demonstrated a saturated conversion gain of –5.5 dB for an o1dBCp of –7 dB and an RF bandwidth of 10 GHz, when the LO power is 3 dB at 23.5 GHz or 28 GHz and the dc power consumption is 2.2 mW.

Table 1 summarizes the demonstrated results and compares them against the state of the art of up-conversion ring mixers operating at or close-to the *K* and *Ka*-band. For direct comparison, a Figure-Of-Merit (FOM) can be defined as [11]:

$$\mathrm{FOM} = \frac{10^{\frac{Gain}{10}} \times 10^{\frac{o1dBCp}{10}}}{10^{\frac{plo}{10}} + \frac{P_{\mathrm{DC}}}{1mW}} \tag{7}$$

The presented mixer demonstrated the highest FOM thanks to the approach described in this work, and although that both BB and LO ports are matched. As it is shown in the manuscript, if these ports are unmatched, higher conversion gains are reached for lower LO and dc powers, at the price of compromising the functionality of the frontend where the mixer is integrated. A relevant metric to evaluate the mixer usability in a complete transmitter is the ratio between the LO-power leakage on the RF port, $P_{LO\_Leakage}$, divided by the RF power P_{RF}. This power ratio, in fact, contributes to the Error Vector Magnitude (EVM) of the transmission. The EVM due only to the LO-power leakage is [27]:

$$\mathrm{EVM}_{LO\_Leakage} = \sqrt{\frac{P_{LO\_Leakage}}{P_{RF}}} \tag{8}$$

The EVM metric enables comparing designs requiring different LO power and capable of delivering distinct RF power to highlight the real impact of the LO leakage on the transmitter performance, which the stand-alone LO isolation metric is not capable of capturing. The mixer presented in this work shows performance in line with the state of the art, although being penalized by the uncompensated phase imbalance of the balun used for the measurement on the RF port. The 3GGP consortium defines in the TS 38.101-1 specification an EVM below 17.5% and 3.5% for QPSK and 256-QAM 5G transmissions, respectively. Transmitters using the presented mixer will support even the more demanding 5G EVM requirements thanks to conventional LO-leakage-cancellation approaches [28]. Finally, the chip occupation area of the presented circuit is also the smallest so far reported, and it is mostly dominated by the matching network used to support multiple LO frequencies and multiple communication standards.

REFERENCES

[1] V. Issakov *et al.*, "Wideband resistive ring mixer for automotive and industrial applications in 0.13μm CMOS," in *Proc. IEEE German Microw. Conf.*, Munich, Germany, 2009, pp. 1–4.

[2] S. N. Ong *et al.*, "A 22nm FDSOI technology optimized for RF/mmWave applications," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, Philadelphia, PA, USA, 2018, pp. 72–75.

[3] O. El-Aassar and G. M. Rebeiz, "A compact pMOS stacked-SOI distributed power amplifier with over 100-GHz bandwidth and up to 22-dBm saturated output power," *IEEE Solid-State Circuits Lett.*, vol. 2, no. 2, pp. 9–12, Feb. 2019.

[4] L. Gao, E. Wagner and G. M. Rebeiz, "Design of E- and W-band low-noise amplifiers in 22-nm CMOS FD-SOI," *IEEE Trans. Microw. Theory Techn.*, vol. 68, no. 1, pp. 132–143, Jan. 2020.

[5] P. V. Testa, D. Fritsche, S. Schumann, W. Finger, C. Carta, and F. Ellinger, "110 GHz travelling-wave amplifier in 22 nm FD-SOI CMOS," in *Proc. IEEE Asia Pac. Microw. Conf. (APMC)*, Kuala Lumpar, Malaysia, 2017, pp. 406–409.

[6] P. V. Testa, V. Rieß, C. Carta, and F. Ellinger, "An inductorless 60GHz down-conversion mixer in 22nm FD-SOI CMOS technology," in *Proc. 14th Eur. Microw. Integr. Circuits Conf. (EuMIC)*, Paris, France, 2019. pp. 152–155.

[7] P. V. Testa, L. Szilagyi, Z. Tibensky, C. Carta and F. Ellinger, "A Compact Vector-Sum Phase Shifter for 5G Applications in 22 nm FD-SOI CMOS," in *Proc. IEEE Int. Symp. Radio-Frequency Integration Technol. (RFIT),* Hiroshima, Japan, 2020, pp. 238–240.

[8] F. Ellinger, "26.5-30-GHz resistive mixer in 90-nm VLSI SOI CMOS technology with high linearity for WLAN," *IEEE Trans. Microw. Theory Techn.*, vol. 53, no. 8, pp. 2559–2565, Aug. 2005.

[9] J.-H. Chen, C.-C. Kuo, Y.-M. Hsin, and H. Wang, "A 15-50 GHz broadband resistive FET ring mixer using 0.18-μm CMOS technology," in *Proc. IEEE MTT-S Int. Microw. Symp.*, Anaheim, CA, USA, 2010, pp. 784–787.

[10] J.-H. Tsai, "Design of 40–108-GHz low-power and high-speed CMOS up-/down-conversion ring mixers for multistandard MMW radio applications," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 3, pp. 670–678, Mar. 2012.

[11] Y.-H. Lin *et al.*, "A Ka-band high linearity up-conversion mixer with LO boosting linearization technique," in *Proc. 48th Eur. Microw. Conf. (EuMC)*, Madrid, Spain, 2018, pp. 259–262.

[12] J.-H. Tsai, W.-H. Lin, and C.-J. Huang, "Design of 15–34 GHz low-power up-conversion ring mixer using 0.18 μm CMOS technology," in *Proc. IEEE Int. Symp. Radio-Freq. Integr. Technol. (RFIT)*, Taipei, Taiwan, 2016, pp. 1–3.

[13] S. Zhou and M.-C. F. Chang, "A CMOS passive mixer with low flicker noise for low-power direct-conversion receiver," *IEEE J. Solid-State Circuits*, vol. 40, no. 5, pp. 1084–1093, May 2005.

[14] A. Dissanayake, H.-G. Seok, O.-Y. Jung, S.-K. Han, and S.-G. Lee, "A 64 μW, 23 dB gain, 8 dB NF, 2.4 GHz RF front-end for ultra-low power Internet-of-Things transceivers," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, Honolulu, HI, USA, 2017, pp. 184–187.

[15] Y. Liao, N. Mei, and Z. Zhang, "Feedback followed bias generation scheme for complementary passive mixer," *Electron. Lett.*, vol. 54, no. 8, pp. 531–533, Apr. 2018.

[16] K. Kumar, K. R. Raghunath, A. Muraleedharan, J. S. Gaggatur, and G. Banerjee, "A 75-μW 2.4 GHz wake-up receiver in 65-nm CMOS for neonatal healthcare application," in *Proc. 32nd Int. Conf. VLSI Design 18th Int. Conf. Embedded Syst. (VLSID)*, Delhi, India, 2019, pp. 287–292.

[17] I. Nam, B. Kim, and K. Lee, "Single-ended differential amplifier and mixer circuits utilizing complementary RF characteristics of both NMOS and PMOS," in *IEEE MTT-S Int. Microw. Symp. Dig.*, vol. 1. Philadelphia, PA, USA, 2003, pp. A117–A120.

[18] I. Nam, B. Kim, and K. Lee, "CMOS RF amplifier and mixer circuits utilizing complementary characteristics of parallel combined NMOS and PMOS devices," *IEEE Trans. Microw. Theory Techn.*, vol. 53, no. 5, pp. 1662–1671, May 2005.

[19] D. Fritsche, G. Tretter, C. Carta, and F. Ellinger, "Millimeter-wave low-noise amplifier design in 28-nm low-power digital CMOS," *IEEE Trans. Microw. Theory Techn.*, vol. 63, no. 6, pp. 1910–1922, Jun. 2015.

[20] P. V. Testa, G. Belfiore, R. Paulo, C. Carta, and F. Ellinger, "170 GHz SiGe-BiCMOS loss-compensated distributed amplifier," *IEEE J. Solid-State Circuits*, vol. 50, no. 10, pp. 2228–2238, Oct. 2015.

[21] J. Shi *et al.*, "Evolution and optimization of BEOL MOM capacitors across advanced CMOS nodes," in *Proc. IEEE 48th Eur. Solid-State Device Res. Conf. (ESSDERC)*, Dresden, Germany, 2018, pp. 190–193.

[22] D. J. Comer and D. T. Comer, "Operation of analog MOS circuits in the weak or moderate inversion region," *IEEE Trans. Educ.*, vol. 47, no. 4, pp. 430–435, Nov. 2004.

[23] P. V. Testa, C. Carta, B. Klein, R. Hahnel, D. Plettemeier, and F. Ellinger, "A 210-GHz SiGe balanced amplifier for ultrawideband and low-voltage applications," *IEEE Microw. Wireless Compon. Lett*, vol. 27, no. 3, pp. 287–289, Mar. 2017.

[24] X. Xu *et al.*, "A broadband power amplifier for 5G applications in 22 nm FD-SOI CMOS," in *Proc. IEEE Asia-Pac. Microscopy Conf. (APMC)*, Singapore, 2019, pp. 1640–1642.
[25] E. W. Lin and W. H. Ku, "Device considerations and modeling for the design of an InP-based MODFET millimeter-wave resistive mixer with superior conversion efficiency," *IEEE Trans. Microw. Theory Techn.*, vol. 43, no. 8, pp. 1951–1959, Aug. 1995.
[26] A. R. Shahani, D. K. Shaeffer, and T. H. Lee, "A 12-mW wide dynamic range CMOS front-end for a portable GPS receiver," *IEEE J. Solid-State Circuits*, vol. 32, no. 12, pp. 2061–2070, Dec. 1997.
[27] Q. Gu, *RF System Design of Transceivers for Wireless Communications*, New York, NY, USA: Springer, 2010.
[28] C. Lanschutzer, A. Springer, L. Maurer, Z. Boos, and R. Weigel, "Integrated adaptive LO leakage cancellation for W-CDMA direct upconversion transmitters," in *Proc. IEEE Radio Freq. Integr. Circuits (RFIC) Symp.*, Philadelphia, PA, USA, 2003, pp. 19–22.

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