Digital Object Identifier 10.1109/OJCAS.2020.3041108

Introduction to the Special Section on High-Speed Wireline and Optical Communication Circuits and Systems

I. INTRODUCTION

THIS Special Section of the IEEE OPEN JOURNAL OF CIRCUITS AND SYSTEMS is dedicated to a collection of articles on High-Speed Wireline and Optical Communication Circuits and Systems, to promote techniques in both circuit and system levels to tackle various challenges as the data rate keeps increasing and provide insightful guidelines for interconnects in the years to come. This Special Section covers articles in three categories including high-speed transceivers, multitone-modulations, and equalizations.

II. HIGH-SPEED TRANSCEIVERS

There are two articles in high-speed transceivers category. The first article by Wang *et al.* presents a 52-Gb/s quarter-rate source-synchronous PAM-4 receiver in 40-nm CMOS. A single-stage multiple peaking continuous-time linear equalizer along with a 1-tap feedforward equalizer are proposed to improve the BER performance and overall energy efficiency. A ring oscillator based wide bandwidth phase-locked loop is adopted for multiphase clock and data recovery to save power with acceptable phase accuracy. The prototype demonstrates error-free operation with bit efficiency of 0.126 pJ/bit/s/dB while compensating 7.3-dB channel loss at 13 GHz.

The second article by Ho *et al.* describes a 32-Gb/s PAM-4 optical transceiver in 40-nm CMOS. The proposed design incorporates active back termination with automatic impedance tracking and asymmetric feedforward equalizer in its transmitter. The receiver adopts quarter-rate architecture with automatic slicer threshold tracking to improve BER performance, guided by its integrated SS-LMS engine.

III. MULTITONE MODULATIONS

The first article in this category by Salinas-Delgado *et al.* compares two signaling schemes, namely baseband (such as PAM-4 and PAM-8) and discrete multitone modulation in terms of achievable data rate and complexity. Two example channels are considered, one with a smooth frequency response and one with a notch frequency response. The comparison is performed in the context of a DAC/ADC-based link, including for both modulations the effect of crosstalk, AWGN, TX and RX jitter, residual ISI, DAC/ADC quantization noise, and clipping.

The next article by Vatankhahghadim *et al.* then studies discrete multitone modulation for wireline links beyond 100 Gb/s. This article presents behavioral modeling results considering link impairments and shows promise of achieving 200 Gb/s communication with IC blocks that have already been reported in the literature and with a reasonable energy and area efficiency. It also details an experimental procedure to evaluate discrete multitone modulation.

IV. EQUALIZATIONS

The last paper in this Special Section by Dey *et al.* describes low latency, zero overhead DFE burst error correction technique. Without any encoder or decoder latency the proposed technique makes use of the existing precursor ISI to detect and correct error on a burst of data. A prototype with 2-tap DFE in 65-nm CMOS operates at 16 Gb/s and compensates 32 dB of channel loss at Nyquist rate, while consuming 58 mW only. With additional 18 mW, the receiver enables error correction capability that translates to 2-to-6 dB SNR gain depending on the pre-cursor magnitude.

ACKNOWLEDGMENT

The Guest Editors would like to thank all the authors and anonymous reviewers for their efforts and time to ensure high-quality manuscripts under a tight schedule. Finally, they would also like to thank G. Manganaro, the OJ-CAS Editor-in-Chief, for his invaluable guidance and assistance in publishing this Special Section.

PING-HSUAN HSIEH
Department of Electrical Engineering
National Tsing Hua University
Hsinchu 30013, Taiwan
e-mail: phsieh@ee.nthu.edu.tw

CHUN-MING HSU
Intel Labs
Intel Corporation
Hillsboro, OR 97124 USA
e-mail: chun-ming.hsu@intel.com

YUNZHI DONG
High-Speed Mixed-Signal Group
Analog Devices
Wilmington, MA 01887 USA
e-mail: yunzhi.dong@analog.com

PING-HSUAN HSIEH (Member, IEEE) received the Ph.D. degree in electrical engineering from the University of California at Los Angeles, Los Angeles, CA, USA, in 2009.

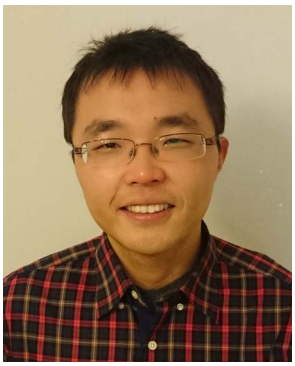
She was with IBM T. J. Watson Research Center, Yorktown Heights, NY, USA, from 2009 to 2011, where she worked on the design of mixed-signal integrated circuits for high-speed serial data communication. In 2011, she joined the Department of Electrical Engineering, National Tsing Hua University, Hsinchu, Taiwan, where she is currently an Associate Professor. Her research interests focus on mixed-signal integrated circuit designs for high-speed electrical data communications, clocking and synchronization systems, and energy-harvesting systems for wireless sensor networks and machine-to-machine applications.

Dr. Hsieh serves as a Guest Editor for the IEEE OPEN JOURNAL OF CIRCUITS AND SYSTEMS and the Technical Program Committees of the IEEE International Solid-State Circuits Conference and the IEEE Asian Solid-State Circuits Conference. She served as an Associate Editor for the IEEE INTERNET OF THINGS JOURNAL from 2014 to 2018.

CHUN-MING HSU received the B.S. and M.S. degrees in electrical engineering from National Taiwan University, Taipei, Taiwan, in 1997 and 1999, respectively, and the Ph.D. degree in electrical engineering and computer science from the Massachusetts Institute of Technology, Cambridge, MA, USA, in 2008. In his Ph.D. thesis, he pioneered the implementation of low-noise digital PLL and demonstrated a 3.6-GHz frequency synthesizer with a 500-kHz bandwidth and $<$ 300-fs jitter.

He is currently a Research Scientist with Intel Labs, specializing in photonic and electrical I/O circuit design as well as link modeling. From 1999 to 2004, he worked with the Industrial Technology Research Institute, Taiwan, as a Circuit Designer for GSM and WCDMA transceivers and was later promoted to management positions. From 2008 to 2014, he was with IBM, East Fishkill, NY, USA, where he worked on decision-feedback equalizer and clock-and-data recovery in IBM's 32- and 45-nm 16–32-Gb/s transceiver IPs for backplane and optical applications.

Dr. Hsu was a co-recipient of the Best Student Paper Award (2nd place) in the 2008 IEEE Radio Frequency Integrated Circuits (RFIC) Symposium and the Best Paper Award in the 2011 IEEE Custom Integrated Circuits Conferences. He also served as a Technical Program Committee Member of the RFIC Symposium.



YUNZHI DONG (Senior Member, IEEE) received the B.S. degree (with Hons.) from Fudan University, Shanghai, China, in 2005, the M.S. degree (*cum laude*) from the Delft University of Technology (TU-Delft), Delft, The Netherlands, in 2008, and the Ph.D. degree from the University of Toronto, Toronto, ON, Canada, in 2012.

He was a Design Intern with Intel, Shanghai, in 2005, NXP Semiconductors, Eindhoven, The Netherlands, from 2007 to 2008, and Granite Semi, Toronto, Canada, from 2011 to 2012. Since 2012, he has been with Analog Devices, Wilmington, USA, where he is working on high-speed data converter circuits and systems.

Dr. Dong received the Top-Talent Scholarship from TU-Delft in 2006, the Fellowship from the University of Toronto in 2008, and the ADI Outstanding Student Designer Award in 2011. He won the Outstanding Industrial Paper Award at 2017 Custom Integrated Circuits Conference. He has been serving as a member of the Technical Program Committee for the Custom Integrated Circuits Conference since 2016 and an Associate Editor for IEEE OPEN JOURNAL OF CIRCUITS AND SYSTEMS since 2019.