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Chaotic Dynamics and FPGA Implementation of a Fractional-Order Chaotic System With Time Delay

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ABSTRACT This article proposes a numerical solution approach and Field Programmable Gate Array implementation of a delayed fractional-order system. The proposed method is amenable to a sufficiently efficient hardware realization. The system's numerical solution and hardware realization have two requirements. First, the delay terms are implemented by employing LookUp Tables to keep the already required delayed samples in the dynamical equations. Second, the fractional derivative is numerically approximated using Grünwald-Letnikov approximation with a memory window size, L, according to the short memory principle such that it balances between accuracy and efficiency. Bifurcation diagrams and spectral entropy validate the chaotic behaviour of the system for commensurate and incommensurate orders. Additionally, the dynamic behaviour of the system is studied versus the delay parameter, τ, and the window size, L. The system is realized on Nexys 4 Artix-7 FPGA XC7A100T with throughput 1.2 Gbit/s and hardware resources utilization 15% from the total LookUp Tables and 4% from the slice registers. Oscilloscope experimental results verify the numerical solution of the delayed fractional-order system. The amenability to digital hardware realization, which is experimentally validated in this article, is added to the system's advantages and encourages its utilization in future digital applications such as chaos control and synchronization and chaos-based communication applications.

INDEX TERMS Chaos, fractional-order systems, FPGA, time-delay.

I. INTRODUCTION

CHAOTIC systems are non-linear dynamical systems that show high sensitivity to initial conditions [1]. A minor change in the system parameters prompts a significant difference in its behaviour. Chaos phenomenon was first discovered by Lorenz during his work on weather prediction, where a butterfly attractor appeared [2]. Chaos phenomenon stands out in many applications such as in communications systems [3], synchronization [4], [5], encryption and pseudo-random generators [6]–[9] and in different fields of science such as chemistry, physics, biology and others [10], [11]. Chaotic systems have been proposed in the form of discrete-time maps and continuous-time differential equations. Discrete-time maps are simpler to implement, but they have lower dimension and time series complexity compared with the continuous-time ones [12]. To employ continuous-time differential equations in digital communication and security applications [13], they must be discretized and solved numerically. Nonlinear time-delayed systems arise inherently in natural systems, e.g., diseases, physiology and population dynamics [14] and artificial systems, e.g., neural networks and control systems [15]. Research works aimed at studying bifurcation, chaos and hyperchaos, and multistability of time-delayed nonlinear systems as well as their control, coupling and synchronization applications [16].

Fractional calculus (FC) is the old mathematical topic that deals with integrations and differentiations for fractional-orders [17]. FC is the generalization of the conventional calculus. Fractional-order differential/integral operators can be obtained using several numerical methods such as Hermite wavelet method [18], spectral-collocation

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method [19], Legendre pseudospectral method [20], Adams-Bashforth-Moulton method [21], linear interpolation method [22], finite difference method [23] and Grünwald-Letnikov (GL) method [21]. The GL definition [24] can be written as follows:

$$ {}_{a}D_{t}^{q}x(t) = \lim_{h\to 0}\left[\frac{1}{h^{q}}\sum_{k=0}^{\left[\frac{t-a}{h}\right]} w_{k}^{(q)}x(t-kh)\right], \tag{1} $$

where q is the fractional-order and the binomial coefficients $w_k^{(q)}$ can be calculated by:

$$ w_0^{(q)} = 1,\ \ w_k^{(q)} = \left(1-\frac{q+1}{k}\right)w_{k-1}^{(q)},\ \ k = 1, 2, 3, \ldots \tag{2} $$

Based on the short memory principle, a modified GL equation was introduced for the possible implementation of the GL operator with length L to reach approximate formula [24]

$$ {}_{t-L}D_{t}^{q}x(t) = \frac{1}{h^{q}}\sum_{k=0}^{L} w_{k}^{(q)}x(t-kh), \tag{3} $$

where h and L are the step size and window size, respectively.

Many applications employ the FC in the literature taking advantage of the extra degrees of freedom provided by the fractional-order [17]. These applications include but are not limited to bio-impedance [25], [26], health [27], neuron models [28], filters [29], [30] and chaotic systems [31]–[33].

The main advantage of a fractional-order system over its integer-order counterpart is its suitability for describing memory effects and hereditary properties of various processes. Many classic integer-order chaotic systems have been extended to their fractional-order forms [31]. The generalization of delay chaotic systems to fractional-order delay chaotic systems introduced a wider class of fractional-order systems in which the derivative of the unknown state variable at a certain time is expressed in terms of its value at the previous times. Moreover, the next state of the system depends not only upon their present state but also upon all of their past states [34].

Chaotic behaviour was reported in integer and fractional-order nonlinear differential equations with time delay having only one state variable [35], i.e., between $x(t)$ and $x(t-\tau)$. Two-dimensional fractional-order simple delayed memristive chaotic system [36] and fractional-order delayed SBT (a physical memristor using a Sr0.95Ba0.05TiO3 nanometer film), memristive chaotic system [37] and other memristive systems [34], [38] were presented. For higher dimensional systems, few researches extended integer-order systems with time delay to the fractional-order domain. For example, the fractional-order form of the unified chaotic system [39], which switches between Lorenz, Lü and Chen systems according to the parameter setting, was presented in [40]. Other researches extended integer-order systems [41] to the fractional-order domain and introduced time delay in their dynamic equations [42]. Some just introduced time delay in fractional-order systems such as [43] did for fractional-order Chen system [44]. In addition, [45] presented the delayed form of the fractional-order financial system presented in [46] and [47] presented the delayed form of a fractional-order simplified Lorenz system.

These limited studies on fractional-order chaotic systems with time delay focused on numerical simulations without hardware realization. Recently, an analog circuit realization of the double-scroll fractional-order Sprott chaotic system with hyperbolic nonlinearity and time delay using all pass filter circuit model was presented in [48].

There are analog and digital implementations of chaotic systems reported in the literature [49]–[51]. Analog implementation of chaotic systems is considered more challenging than the digital one due to the non-linearity and component tolerances, which can affect the parameters of the chaotic system [50]. Recent researches have built analog active filter-based implementations using frequency domain approximations of the fractional-order derivatives as in [52].

Field Programmable Gate Array (FPGA) is the widespread board that is used to realize chaotic systems due to its assured low power consumption, re-programmability, real-time computing, high speed, and optimized hardware [53]–[55]. Additionally, fractional-order chaotic systems require complex computation algorithms and high dependency on memory. Therefore, FPGA is an appropriate choice for implementing such systems. FPGA is also used in fast prototyping for Application Specific Integrated Circuit (ASIC) [56]–[58]. Some FPGA implementations use software tools to generate the Register Transfer Level (RTL) as LABVIEW and MATLAB Simulink [59], [60]. A new algorithm for the implementation of GL operators based on the linear approximation approach was introduced in [61]. The introduced algorithm reduces the memory dependency of the fractional-order systems [61]. An implementation of the Caputo and the GL fractional-order operators on FPGA was proposed in [62] for different fractional-orders. In [63], another FPGA implementation of the GL operator was presented with different memory window sizes. In addition to this, the hardware implementation of two fractional-order chaotic systems was proposed and validated experimentally. Other FPGA realizations of fractional-order differentiators and integrators were presented based on GL [53], [55] and Adams-Bashforth-Moulton method [51]. The modified versions of the Product Integration (PI) rules were proposed in [32] to facilitate their hardware implementations. Three FPGA implementation methods of the fractional-order operator based on these PI rules were realized and applied on a multi-scroll fractional-order chaotic attractor.

Fractional-order chaotic systems are mainly used in encryption and cryptographic applications as pseudo-random number generators by applying GL method as in [51], [64]. A four-dimensional fractional-order memristor system was implemented on FPGA in [65]. Additionally, variable-order fractional-order chaotic systems were implemented on FPGA

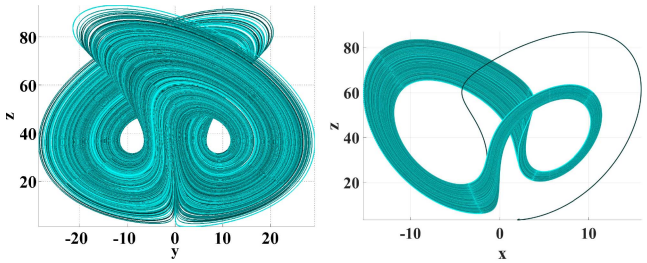


FIGURE 1. Fractional order Liu *et al.* chaotic attractor (a) no delay and (b) with time delay $\tau = 0.008$, $(x_0, y_0, z_0) = (2.2, 2.4, 3.8)$, (a, b, k, c, d)=(10, 40, 1, 2.5, 4).

based on Adams algorithm in [66]. In [67], a new chaotic system was presented using analog and digital circuits.

This article introduces a solution approach for a delayed fractional-order chaotic system , which is amenable to hardware implementation. The investigated system is a delayed fractional-order system, whose fractional-form was proposed by Liu *et al.* [41] and extended to include time delay by Bhalekar and Daftardar-Gejji [42]. The system has the advantages of both fractional-order and delayed chaotic systems: more powerful modelling capabilities, extra degrees of freedom and memory dependency. Numerical simulations are introduced to validate the chaotic behaviour of the system for commensurate and incommensurate orders using bifurcation diagrams and spectral entropy. The amenability to digital hardware realization, which is experimentally validated in this article, is added to the system's advantages and encourages its utilization in future digital applications.

This article is organized as follows: Section II discusses the fractional-order Liu *et al.* chaotic attractor and its delayed version. The dynamic behaviour of the system is studied in Section III, where bifurcation diagrams and spectral entropy are investigated versus the fractional orders. The FPGA implementation of the investigated system is introduced in Section IV with the effect of window size and the delay parameter. Results and discussions for the FPGA utilization are presented in Section V. Finally, Section VI concludes the work.

II. LIU *ET AL.* CHAOTIC ATTRACTOR

The fractional-order chaotic system of Liu *et al.* [41] with a butterfly attractor was proposed in [42]. The dynamical behaviour of the system can be described by:

$$D^{q_1}x = a(y - x), \tag{4a}$$
$$D^{q_2}y = bx - kxz, \tag{4b}$$
$$D^{q_3}z = -cz - dx^2, \tag{4c}$$

where q_1, q_2, and q_3 are the fractional orders, and a, b, k, c, and d are the parameters of the system.

The investigated system in this article is the delayed version of (4) which can be written as follows [42]:

$$D^{q_1}x(t) = a(y(t) - x(t - \tau)), \tag{5a}$$
$$D^{q_2}y(t) = bx(t - \tau) - kx(t)z(t), \tag{5b}$$
$$D^{q_3}z(t) = -cz(t - \tau) - dx(t)^2, \tag{5c}$$

for $t > 0$, while for $-\tau \leq t \leq 0$, $x(t)$ and $z(t)$ are properly initialized. τ is the time delay, which can be considered as an extra control parameter of the system.

The system is solved by using the GL approximation method where (5) can be written as follows:

$$x_i = a\Big(y_{i-1} - x_{i-1-\frac{\tau}{h}}\Big)h^{q_1} - \sum_{j=1}^{L} w_j^{q_1} x_{i-j}, \tag{6a}$$

$$y_i = \Big(bx_{i-1-\frac{\tau}{h}} - kx_{i-1}z_{i-1}\Big)h^{q_2} - \sum_{j=1}^{L} w_j^{q_2} y_{i-j}, \tag{6b}$$

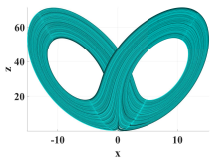
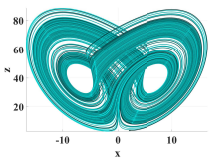
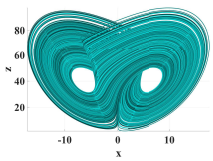
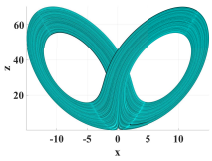
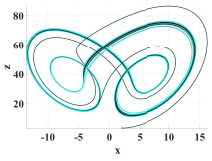
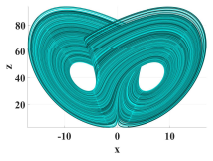
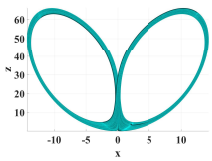
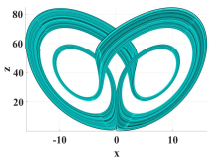
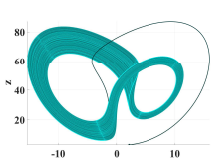
$$z_i = \Big(-cz_{i-1-\frac{\tau}{h}} - d{x_{i-1}}^2\Big)h^{q_3} - \sum_{j=1}^{L} w_j^{q_3} z_{i-j}. \tag{6c}$$

The original system is realized with initial values ($x_0 = 2.2$, $y_0 = 2.4$ and $z_0 = 3.8$), the parameters of the system ($a = 10$, $b = 40$, $k = 1$, $c = 2.5$ and $d = 4$) as in [42], and step size (h) equals to 0.001, with fractional-order parameters ($q_1 = 0.95$, $q_2 = 0.95$ and $q_3 = 0.95$) and window size (L)=30. Figure 1 presents the simulation results of the system employing the GL approximation. Figure 1(a) shows the original system with no delay while Fig. 1(b) shows the delayed system with $\tau = 0.008$, as in [42]. The effect of the fractional-order is detailed in Section III, while the effect of the implementation parameter (window size L) is detailed in Section IV.

III. FRACTIONAL CHAOTIC DYNAMICS

This section further investigates the effect of the fractional-order on the chaotic dynamics of system (6), not only at the fixed values $(0.95, 0.95, 0.95)$. Two chaotic behaviour indicators are used for this purpose: bifurcation diagrams and Spectral Entropy (SE), investigating the qualitative type of the system's solution against an interval of fractional-order(s). Bifurcation diagram classifies the corresponding qualitative type of the post-transient solution into stable, periodic or chaotic versus the system's parameters. The bifurcation diagrams are generated through plotting the value of x time series when it reaches a local maximum x_{max}. SE treats the normalized power distribution in the frequency domain of a time series as a probability distribution and estimates its randomness through Shannon entropy accurately and rapidly without much preprocessing [68]. A larger value of SE indicates a flatter power spectrum, which shows high complexity of the time series and its effectiveness when used in information security applications. When performing Discrete Fourier Transformation (DFT), a large DC offset would often result in a big impulse around frequency 0 Hz and mask out the signals with relatively small amplitude. Thus, for a time series $x(n)$, $n = 0, 1, 2, \ldots, N-1$ of length N, the mean value $\tilde{x}$ is first removed to get $x(n) = x(n) - \tilde{x}$.

TABLE 1. The effect of τ and window size parameters on the chaotic system.

	$L = 10$	$L = 20$	$L = 30$
$\tau = 0.002$			
SE	0.5545	0.4887	0.5532
$\tau = 0.003$			
SE	0.5600	0.1335	0.5512
$\tau = 0.008$			
SE	0.5792	0.5447	0.3790

DFT is given by:

$$X(k) = \sum_{n=0}^{N-1} x(n) e^{-j2\pi nk/N}, \tag{7}$$

where $k = 0, 1, \ldots, N-1$ and j is the imaginary unit. If the power of a discrete power spectrum with the k_{th} frequency is $|X(k)|^2$, then the "probability" of this frequency is defined as:

$$P_k = \frac{|X(k)|^2}{\sum_{k=0}^{N/2-1} |X(k)|^2}, \tag{8}$$

where the summation runs from $k = 0$ to $k = N/2 - 1$ after applying DFT. SE is given by:

$$\text{SE} = \frac{\sum_{k=0}^{N/2-1} |P_k \ln(P_k)|}{\ln(N/2)} \tag{9}$$

where $\ln(N/2)$ is the entropy of completely random signal. In this article, bifurcations are plotted and SE is computed using $N = 9 \times 10^5$ after discarding the first 10^5 iterations.

The bifurcations and SE in Fig. 2(a) are plotted versus q_1, at $q_2 = q_3 = 0.95$ and the rest of the parameters and initial values are the same as in Section II. Figure 2(a) shows the consistency between the two indicators, where SE values increase for the intervals of q_1 that exhibit wide chaotic range in the corresponding bifurcation diagram. Figure 2(b), which investigates the system dynamics when $q_1 = q_2 = q_3 = q$, can be described similarly. Figure 2 indicates that the investigated system exhibits chaotic behaviour for relatively wide ranges of fractional-orders in both incommensurate and commensurate cases. Few special cases of the deduced fractional-order intervals corresponding to chaotic and non-chaotic behaviour from the continuous diagrams in Fig. 2 were mentioned in [42] and agree with our results.

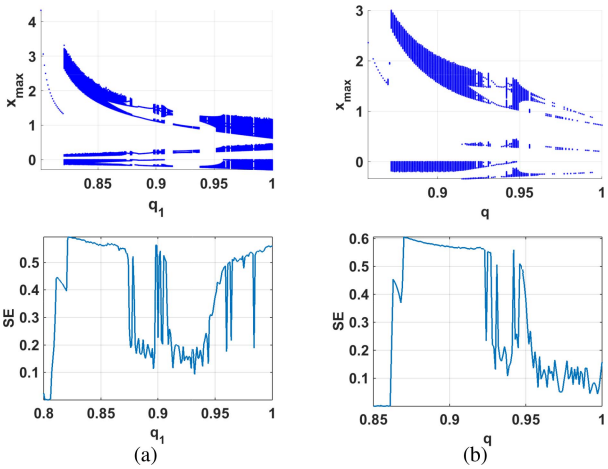


FIGURE 2. Bifurcation diagrams and spectral entropy for (a) incommensurate and (b) commensurate fractional-orders.

IV. FPGA IMPLEMENTATION

In this section, the hardware implementation of the investigated system is introduced. Table 1 shows the effect of the delay parameter (τ) and the window size (L) of the GL on the investigated fractional-order chaotic attractor , fixing the rest of the parameters to the values of Section II. From the shown attractor diagrams and the corresponding SE values, it can be inferred that sudden changes in behavior may occur when changing τ, L, or both. These implementation-dependent variations are not new for chaotic systems and similar variations have been reported before in [12], [69].

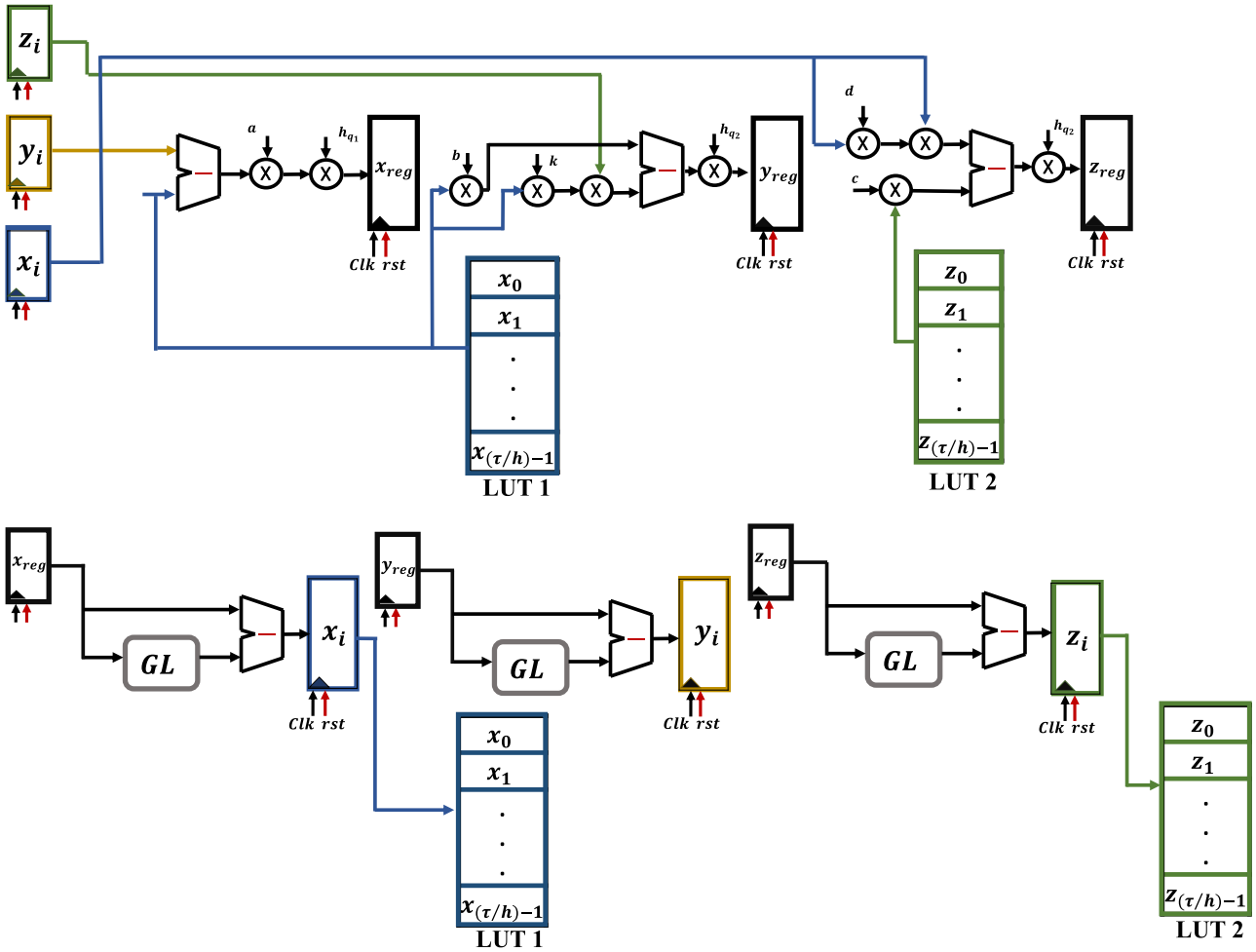


FIGURE 3. FPGA Implementation of the Delayed Fractional-order Liu System.

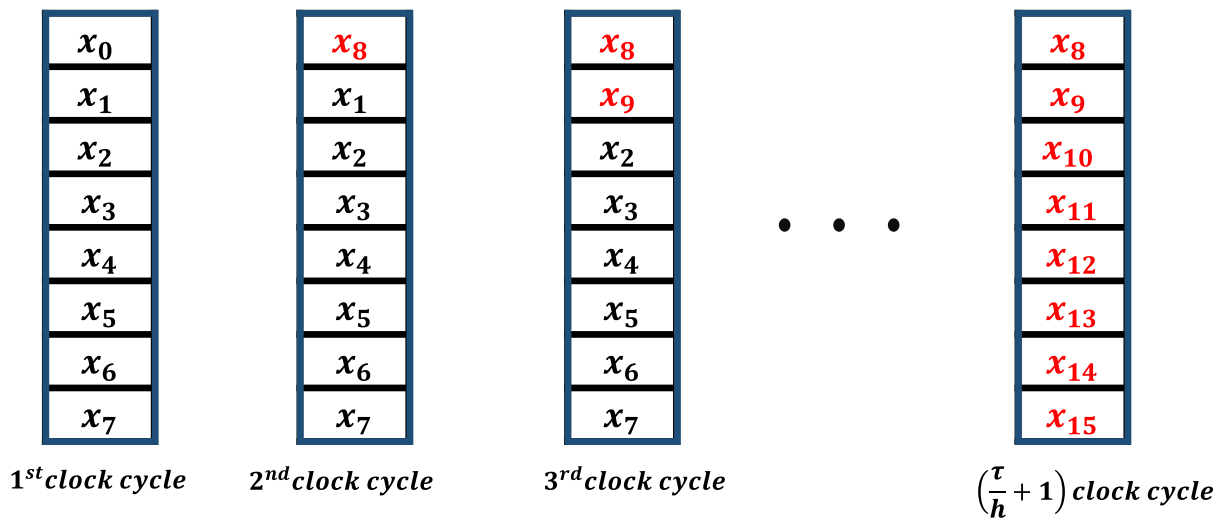
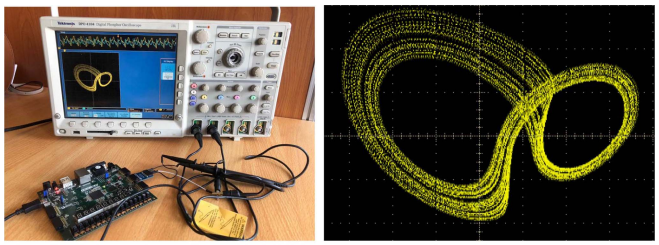


FIGURE 4. LookUp Table (LUT1).

Hence, chaotic behavior must be ensured first using software simulation before proceeding to hardware realization at the same parameter values.

Figure 3 shows the proposed FPGA architecture of the system. The proposed system requires three registers (x, y, and z). Each register is 32-bit divided into 8-bit for the



(a) (b)

FIGURE 5. (a) Experimental setup of the proposed system (b) $x - z$ plane of fractional-order delayed Liu System.

TABLE 2. Hardware resources of delayed fractional-order liu system.

No of LUT	10026 out of 63400
No of slice registers	5139 out of 126800
Clock speed (MHz)	37.577
Throughput (Gbit/sec)	1.2

integer part and 24-bit for the fractional part. Two LUTs are required to save the previous ($\frac{\tau}{h}$) values of (x and z) to properly implement the delayed terms in (6).

The first step in the system implementation is the reset state, where the two LUTs in Fig. 3 are initialized. The three registers (x_i, y_i and z_i) are also initialized as mentioned in Section II at the reset state. The GL block shown in Fig. 3(the lower part) is used to apply the fractional-order calculations as implemented in a previous work [62], [63].

Figure 3 (the upper part) depicts the hardware implementation of the first part of (6), $(a(y_{i-1} - x_{i-1-\frac{\tau}{h}})h^{q_1})$, where the three registers (x_{reg}, y_{reg} and z_{reg}) are updated. Their values are used to calculate the summation $(\sum_{j=1}^{L} w_j^{q_1} x_{i-j})$ using the GL block. Finally, the (x_{reg}, y_{reg} and z_{reg}) outputs and the GL outputs are added to calculate the final values of (x_i, y_i and z_i) that are used to update the LUT as will be explained below.

Taking an example of LUT1 shown in Fig. 3, it is filled with (x_0 to x_7) at the reset state. In the first clock cycle (after reset state), the value (x_0) (see Fig. 4) is used to calculate (x_{reg}). Then, it is used to calculate the final register (x_i) (see Fig. 3). Then the LUT location (0) is updated by the new calculated value (x_8). In the second clock cycle (x_1) will be used, and the first location in the LUT will be updated by the new calculated value (x_9),..., etc. The LUTs will be completely updated after ($\frac{\tau}{h} + 1$) clock cycles as illustrated in Fig. 4 for ($\tau = 0.008$ and $h = 0.001$).

V. RESULTS AND DISCUSSION

The proposed system is implemented using Verilog Hardware Description Language (HDL) on Nexys 4 Artix-7 FPGA *XC7A100T*. Xilinx ISE 14.7 tool is used for simulation. The verification of the proposed system is done by extracting the output from the Verilog code and plotting it using MATLAB. To display the delayed fractional-order system on the Oscilloscope, a digital to analog converter Pmod DAC 2 is used to connect the FPGA with the Oscilloscope.

The Pmod DAC 2 works by taking two digital outputs each of 12-bit and converting them to the analog signal which can be displayed on the Oscilloscope [see Fig. 5(a)]. Figure 5(b) presents the $x - z$ plane of the system displayed on the Oscilloscope DPO 4104.

Table 2 shows the FPGA hardware resources of the proposed implementation of the system. It shows that the system uses 10026 out of 63400 from the LUTs, which is equivalent to 15% from the total LUTs. In addition, 5139 are used out of 126800 from the number of slice registers, which represents 4% from the slice registers. The performance of the system can be evaluated through the throughput, which represents the rate of the output data. It is obtained by multiplying the clock speed with the number of bits of the output which equals to 32-bit. Therefore, the achieved throughput is 1.2 Gbit/sec.

VI. CONCLUSION

An investigation of the chaotic dynamics and an FPGA realization of a delayed fractional-order chaotic system were presented. The presented numerical solution approach is suitable for a digital hardware realization , which balances between accuracy and efficiency. The delay terms were implemented by employing LUTs to keep the required delayed samples in the system equations. Besides, the fractional derivative was numerically approximated using the GL method with a memory window size (L) according to the short memory principle. The chaotic dynamics were investigated through plotting continuous bifurcation diagrams and SE values versus the fractional orders , which validate the chaotic behavior for wide ranges of commensurate and incommensurate orders. The system was shown to exhibit chaotic dynamics for various combinations of the delay parameter (τ) and the window size (L). The system was experimentally realized on Nexys 4 Artix-7 FPGA XC7A100T with throughput 1.2 Gbit/s and hardware resources utilizing 15% of the total LUTs and 4% of the slice registers.

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