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Analysis and Design of a Tri-Level Current-Steering DAC With 12-Bit Linearity and Improved Impedance Matching Suitable for CT-ADCs

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ABSTRACT This paper presents the design of a low-latency, highly linear current-steering DAC for use in continuous-time ADCs. A detailed analysis of equivalent unary-weighted current-steering DAC topologies in terms of mismatch, noise, and output-impedance related distortion is carried out. From this analysis, we propose a tri-level DAC design that achieves 12-bit static linearity and is suitable for implementation in a continuous-time ADC architecture. To reduce output-impedance related distortion, the design combines DAC slice impedance matching with a proposed compensation technique. By incorporating the tri-level DAC in a continuous-time ADC architecture, the technique demonstrates $\sim$ 8dB improvement in DAC dynamic performance at high frequencies over the Nyquist-band at 100MS/s. The DAC has been verified by simulation results in TSMC 1.2V 65nm CMOS technology.

INDEX TERMS Tri-level, current-steering, DACs, thermal noise, DNL, INL, HD3, SFDR.

I. INTRODUCTION

HIGH performance, wide-bandwidth continuous-time ADCs (CT-ADCs) are employed in applications such as cellular/Wi-Fi, video cameras, and automotive radar. In this work, a DAC is employed in the feedforward path of continuous-time-input-pipelined ADC (CTIP-ADC) architecture [1]. The CTIP-ADC as shown in Fig. 1 is a sub-category of CT-ADC. The ADC consists of a continuous time input stage followed by a discrete time backend ADC. The top-level components of the CTIP-ADC are the filter, Flash-ADC/DAC (N-bit), integrating-gain-stage, and a discrete-time backend SAR-ADC (M-bit). CT-ADCs can perform accurate conversion of signals without the need for a large input sampling stage, however they require a highly linear low noise current-steering DAC (CS-DAC) with a linearity specification that matches or exceeds the overall ADC specification. This paper presents the analysis and design of a low-latency high-linearity CS-DAC suitable for a 12-bit, 100MS/s CTIP-ADC architecture as described in [1].

In order to achieve 12-bit ADC performance using 100MS/s sampling rate, the 5-bit (32-level) unary-weighted CS-DAC must fulfill the following key requirements;

1. The DAC must meet the overall linearity performance of the ADC (i.e., 12-bit).
2. A fully differential DAC must be suitable for low-voltage (1.2V) and must have low-noise performance.
3. The DAC decoder logic must have low latency.

Drawing on these requirements, the work analyses three equivalent unary-weighted CS-DAC topologies applicable to

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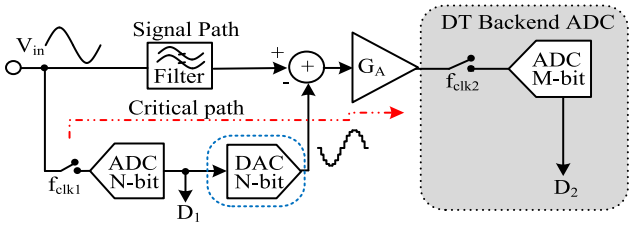

FIGURE 1. CTIP-ADC architecture [1] incorporating the DAC.

the CT-ADC architecture. The analysis focuses on three types of DAC errors these are; random and deterministic mismatch errors due to current-source (CS_{rc}) mismatches [2], thermal noise contributed by the CS_{rc} devices [3], and output-impedance related distortion due to the finite-output-impedance of each CS_{rc} [2]. The DAC in this work drives a resetting integrator gain stage in the CTIP-ADC [1]. The analysis omits the mismatch based timing errors [2] of the individual CS_{rc}s, as the resetting action of the integrator gain stage of the CTIP-ADC negates the timing errors. During the reset phase, the integrator allows the DAC to change its state, while in this reset phase, the CS_{rc}s have sufficient time to settle before the start of the integration process. Consequently, no timing errors will be introduced, as the CS_{rc} outputs would have been settled at the start of each integration phase. The remaining errors introduced will only be due to CS_{rc} and output-impedance mismatches within the DAC. Based on the CS-DAC topologies analysis, we design a tri-level DAC that is suitable for implementation in the CTIP-ADC as shown in Fig. 1. In addition, an approach to improve output-impedance related HD3/SFDR performance of the CS-DAC topologies is presented and applied to the TRI-DAC design.

The rest of the paper is organized as follows: Section II provides an overview of equivalent unary-weighted CS-DAC topologies. Section III provides the analysis and comparison of CS-DAC topologies in terms of thermal noise, static-linearity, and output-impedance related distortion for their equivalent unary-weighted implementation. Section IV provides the design details of the TRI-DAC blocks such as CS_{rc} slice, bias block, and the decoder-logic. The TRI-DAC output-impedance related dynamic performance improvement technique is provided in Section V. In Section VI, the layout implementation and the dynamic performance results of a fully differential TRI-DAC operating at a 100MS/s sampling rate is presented. Finally, Section VII concludes the paper.

II. CS-DAC TOPOLOGIES OPERATION

Unary-weighted CS-DAC topologies are categorized into three types, these are (a) Bi-level DAC (BI-DAC) [4], (b) Complementary DAC (CMP-DAC) [5] and (c) Tri-level DAC (TRI-DAC) [3]. Equivalent 2-bit differential BI-DAC, CMP-DAC and TRI-DAC implementations are shown in Fig. 2(a), 2(b), and 2(c) respectively, where I_{FS} is the full-scale (FS) output current. In this scenario, a 2-bit BI-DAC is implemented with four CS_{rc} slices using nMOS (Sink) devices, and a constant current offset using a pMOS (Source) device on each current output node. The equivalent 2-bit CMP-DAC and TRI-DAC implementation uses four and two CS_{rc} slices respectively. In each of the unit CS_{rc} slices, an nMOS and pMOS (n/p) CS_{rc} device is used to 'Sink' and 'Source' the current respectively. However, as compared to the CMP-DAC, the TRI-DAC unit CS_{rc} slice has an extra 'Dump' state, when activated this forms a path between VDD and GND that contributes no current to the output node.

III. CS-DAC TOPOLOGIES COMPARISON

In this section, the analysis and comparison of CS-DAC topologies is provided in terms of thermal noise, static linearity, and output-impedance related distortion for their equivalent implementations. Based on the conclusions from this analysis, we show why the TRI-DAC topology is chosen for the architecture of Fig. 1.

A. THERMAL NOISE COMPARISON

The noise contribution due to the thermal noise of the CS_{rc} sets the fundamental upper limit for the SNR performance of DACs. Equivalent 2-bit BI-DAC, CMP-DAC, and TRI-DAC thermal noise at each code based on a sinusoidal input signal is shown in Fig. 3(b), 3(c), and 3(d) respectively, along with the DAC output in Fig. 3(a). The CS_{rc}'s in these DAC topologies are assumed to be long channel devices operating in the saturation region.

1) BI-DAC NOISE

The BI-DAC has a constant current noise contribution from the CS_{rc} and offset devices at each code irrespective of the input-code value. For an M-level BI-DAC, the current noise density at the differential output [6] can be expressed as

$$S_{I_{BI-DAC}} = 4kT\gamma I_{FS}\left(\frac{1}{V_{ov,n}} + \frac{1}{V_{ov,p}}\right), \tag{1}$$

where $k = 1.38\text{x}10^{-23}\ J/K$ is the Boltzmann's constant, T is the temperature in Kelvin, $\gamma = 2/3$, $I_{FS} = M.I_{LSB}$, $V_{ov,n}$ and $V_{ov,p}$ are the gate-source overdrive voltages for n/p CS_{rc} device respectively.

2) CMP-DAC NOISE

In the CMP-DAC topology case, the n/p CS_{rc} contributes noise at each code and is constant irrespective of input-code values. As compared to BI-DAC, the CMP-DAC topology requires half the LSB step current to design a unit CS_{rc} slice and removes the need for offset devices. Hence the current noise density at the output is half that of the BI-DAC topology for the same number of bit implementations. Thus the current noise density at the differential output can be expressed as

$$S_{I_{CMP-DAC}} = 2kT\gamma I_{FS}\left(\frac{1}{V_{ov,n}} + \frac{1}{V_{ov,p}}\right). \tag{2}$$

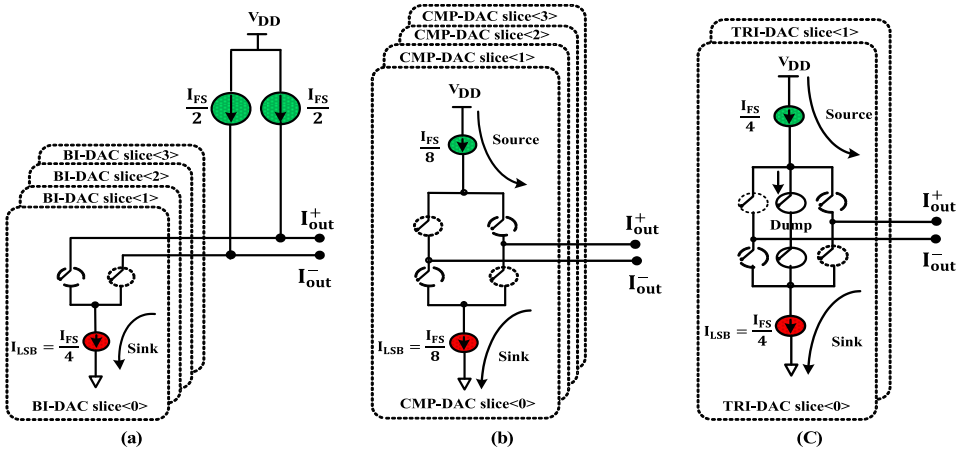

FIGURE 2. Equivalent 2-bit unary-weighted CS-DAC topologies: (a) BI-DAC (b) CMP-DAC (C) TRI-DAC.

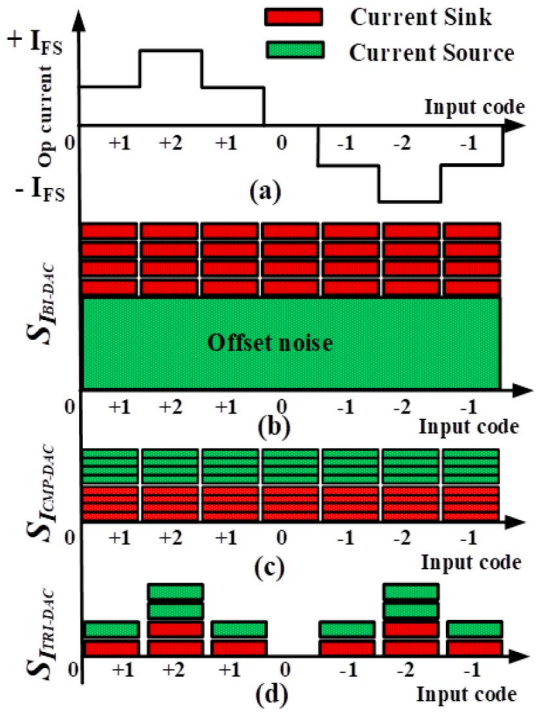

FIGURE 3. (a) 2-bit DAC output, current-noise-density of a 2-bit unary-weighted (b) BI-DAC, (c) CMP-DAC, (c) TRI-DAC.

3) TRI-DAC NOISE

The TRI-DAC CS_{rc} noise varies with the input-code value, with the noise level negligible at mid-code due to no current flowing at the output node. The current noise spectral density for the TRI-DAC is based on the root-mean-square (RMS) value of the input signal at the differential output, which is $1/\sqrt{2}$ of the FS current value. For the TRI-DAC, the code-dependent noise variation corresponds to a full rectified sinusoidal-signal as depicted in Fig. 3(d). Hence the current noise density at the differential output can be formulated as

$$S_{I_{TRI-DAC}} = \frac{2}{\sqrt{2}} kT\gamma I_{FS}\left(\frac{1}{V_{ov,n}} + \frac{1}{V_{ov,p}}\right). \tag{3}$$

The above equations show that the TRI-DAC has improved noise performance compared to the equivalent BI-DAC and CMP-DAC designed for the same number of bits. Moreover, this feature makes it suitable for DAC applications that require improved noise performance at low-level amplitudes [3].

B. STATIC LINEARITY PERFORMANCE

Mismatch within DAC components leads to a degradation in the static linearity performance. In this section, the CS_{rc} mismatch related DNL and INL performance of an equivalent thermometer-decoded BI-DAC, CMP-DAC, and TRI-DAC are compared. To analyze the performance at 12-bit level, a non-ideal 5-bit unary-weighted MSB DAC is combined with an ideal 7-bit binary-weighted LSB DAC.

1) BI-DAC STATIC LINEARITY

For an N-bit BI-DAC consisting of M unary weighted elements where ($M = 2^N$), the maximum RMS DNL (DNL_{RMS}) and maximum RMS INL (INL_{RMS}) can be expressed as [7]

$$DNL_{RMS}(MAX) = \sigma\left(\frac{\Delta I}{I}\right) LSB, \tag{4}$$

$$INL_{RMS}(MAX) = \frac{\sqrt{M}}{2}.\sigma\left(\frac{\Delta I}{I}\right) LSB, \tag{5}$$

where $\sigma(\frac{\Delta I}{I})$ is the relative standard deviation of the unit CS_{rc}.

In order to design a 12-bit BI-DAC with a ±0.5 LSB INL, achieving 99.7% yield, the required relative standard deviation of the unit CS_{rc} [8] can be calculated as

$$\sigma\left(\frac{\Delta I}{I}\right) \le \frac{1}{\sqrt{2^{N+2}}.C} = \frac{1}{\sqrt{2^N}}\frac{0.5}{4.97} = 0.15\%, \tag{6}$$

where N is the DAC resolution and C is an INL yield related coefficient. To obtain 99.7% DAC yield, $C = 4.97$.

Using $\sigma(\frac{\Delta I}{I}) = 0.1\%$, the DNL and INL error is plotted for the BI-DAC using Monte Carlo (MC) simulations and shown in Fig. 4(a). From this plot, the

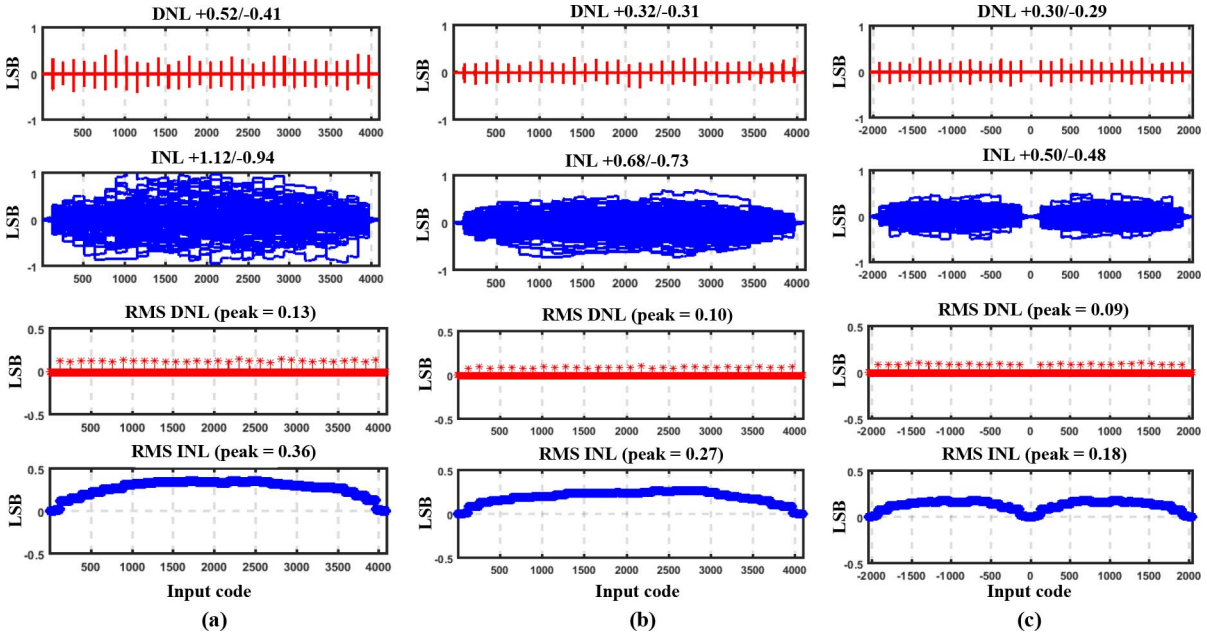

FIGURE 4. 100 MC DNL, INL runs and their RMS plot for a 12-bit (a) BI-DAC, (b) CMP-DAC, and (c) TRI-DAC using MATLAB model.

DNL range is $+0.52/-0.41$ LSB and the INL range is $+1.12/-0.94$ LSB. Fig. 4(a) shows the DNL_{RMS} and INL_{RMS} plot using 100 MC runs. From the plot, the observed maximum DNL_{RMS} is 0.13 LSB and maximum INL_{RMS} is 0.36 LSB at the 12-bit level. Using (4) and (5), the calculated maximum DNL_{RMS} is 0.128 LSB and maximum INL_{RMS} is 0.36 LSB at the 12-bit level. Hence, the mathematical calculations closely match with those obtained from the MC simulation results.

2) CMP-DAC STATIC LINEARITY

For the CMP-DAC topology, the LSB step current of the differential output is the sum of the unit currents I_n and I_p of the n/p CS_{rc} transistors respectively, where I_n and I_p are the independent random variables. Thus the maximum allowable total current deviation $\sigma(\Delta(I_n + I_p)/(I_n + I_p))$ in terms of the relative current deviations $\sigma(\Delta I_n/I_n)$, $\sigma(\Delta I_p/I_p)$ of the n/p CS_{rc} transistors respectively is derived [5] and expressed as

$$\sqrt{\frac{1}{\beta^2}\sigma^2\left(\frac{\Delta I_n}{I_n}\right) + \sigma^2\left(\frac{\Delta I_p}{I_p}\right)} \leq \sigma\left(\frac{\Delta(I_n + I_p)}{I_n + I_p}\right)\frac{(1+\beta)}{\beta}, \tag{7}$$

where $\beta = I_n/I_p$. In the CMP-DAC case, the maximum INL occurs at the mid-code position similar to the BI-DAC. Thus, the maximum DNL_{RMS} and maximum INL_{RMS} can be represented as

$$DNL_{RMS}(MAX) = \sigma\left(\frac{\Delta(I_n + I_p)}{I_n + I_p}\right)LSB, \tag{8}$$

$$INL_{RMS}(MAX) = \frac{\sqrt{M}}{2}.\sigma\left(\frac{\Delta(I_n + I_p)}{I_n + I_p}\right)LSB. \tag{9}$$

According to (6), $\sigma(\Delta(I_n + I_p)/(I_n + I_p))$ should be less than or equal to 0.15% to design a 12-bit CMP-DAC with 99.7% yield and INL error below or equal to 0.5 LSB. Hence, to satisfy this condition, the relative current deviations $\sigma(\Delta I_n/I_n)$, $\sigma(\Delta I_p/I_p)$ of the n/p unit CS_{rc}s are both chosen to be 0.1%. Using (7) and considering $I_n \approx I_p$, the theoretical value for $\sigma(\Delta(I_n + I_p)/(I_n + I_p))$ is 0.07%. Using (8) and (9), the mathematically calculated maximum DNL_{RMS} and maximum INL_{RMS} are 0.09 LSB and 0.25 LSB respectively at 12-bit level. Fig. 4(b) shows the DNL and INL plot for the 100 MC simulations at a 12-bit level. From the plot, the observed DNL range is $+0.32/-0.31$ LSB and the INL range is $+0.68/-0.73$ LSB. Fig. 4(b) shows the DNL_{RMS} and INL_{RMS} plot for the 100 MC simulations at 12-bit level. The observed maximum DNL_{RMS} and INL_{RMS} values from the plot are 0.10 LSB and 0.27 LSB respectively. The values obtained from the MATLAB MC simulation results are in a good agreement with those from the mathematical analysis.

3) TRI-DAC STATIC LINEARITY

In the case of a TRI-DAC topology, mismatch errors contribute from the 'Sink' and 'Source' CS_{rc} devices at each digital input-code in a similar manner to the CMP-DAC. However, the transfer function of the TRI-DAC differs from the CMP-DAC topology due to incorporation of an extra 'dump' mode. The TRI-DAC showing the maximum INL_{RMS} with respect to the input-code is depicted in Fig. 5. It is observed from the figure that due to the zero crossing TRI-DAC, the INL at mid-code is zero and the maximum INL_{RMS} error occurs at $m = \pm M/4$, where m represents the digital input-code.

For an N-bit and a M-level thermometer-decoded differential TRI-DAC, the maximum DNL_{RMS} and INL_{RMS} can

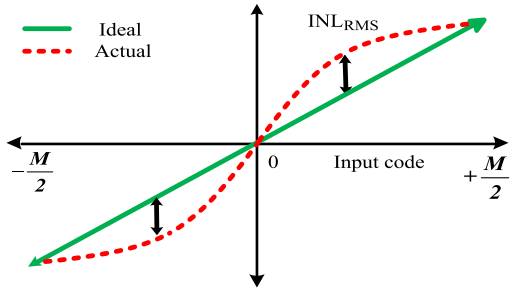

FIGURE 5. An *N*-bit and *M*-level TRI-DAC INL bow diagram.

be formulated and expressed as

$$DNL_{RMS}(MAX) = \sigma\left(\frac{\Delta(I_n + I_p)}{I_n + I_p}\right)LSB, \tag{10}$$

$$INL_{RMS}(MAX) = \sqrt{\frac{M}{8}}.\sigma\left(\frac{\Delta(I_n + I_p)}{I_n + I_p}\right)LSB. \tag{11}$$

Using the same level of mismatch on the n/p unit CS_{rc}s as that of CMP-DAC, the TRI-DAC DNL and INL error plot for 100 MC simulations is shown in Fig. 4(c). From the plot, the observed DNL range is $+0.30/-0.29$ LSB and the INL range is $+0.50/-0.48$ LSB. Fig. 4(c) shows the DNL_{RMS} and INL_{RMS} plot for the 100 MC runs at 12-bit level. The observed maximum DNL_{RMS} and INL_{RMS} from the plot are 0.09 LSB and 0.18 LSB respectively. Using (10) and (11), the calculated maximum DNL_{RMS} and maximum INL_{RMS} are 0.09 LSB and 0.18 LSB respectively at the 12-bit level. These values proved to be in agreement with those obtained from the simulation results. The mismatch analysis presented in this section proves that the TRI-DAC has very good DNL and INL characteristics compared to other CS-DAC topologies for the same number of bit implementations.

C. CS-DACS OUTPUT-IMPEDANCE RELATED HD3 ANALYSIS

The signal-dependent output-impedance degrades HD3/SFDR performance in fully differential DACs at high frequencies. In this section, the code-dependent finite-output-impedance related effects on equivalent unary weighted CS-DACs HD3 performance is analysed at low and high frequency. To make the HD3 analysis easier to follow, the CS-DAC topologies drive an external resistive load. The analysis shows unit CS_{rc} cell output-impedance requirements at low frequencies to achieve desired HD3 performance for high-resolution CS-DAC topologies. Furthermore, the analysis shows an approach to make DACs HD3/SFDR performance signal-independent at high frequencies by employing capacitive matching technique in the DAC unit CS_{rc} cell. For completeness, the analysis is extended to show how a frequency dependent amplifier, which acts as a load for BI-DAC, affects its output-impedance related HD3 performance. A similar analysis is applied to the CMP-DAC and TRI-DAC topologies to derive the HD3 equation with an amplifier load.

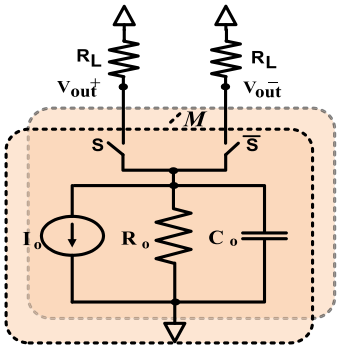

FIGURE 6. BI-DAC simplified model with finite-output-impedance.

TABLE 1. CS-DAC topologies conductance variation at the positive output.

Input code	Output-conductance g^+_{out}		
	BI-DAC	CMP-DAC	TRI-DAC
-2	0	$4g_n$	$2g_n$
-1	g_o	$3g_n + g_p$	$g_n + g_d$
0	$2g_o$	$2g_n + 2g_p$	$2g_d$
+1	$3g_o$	$g_n + 3g_p$	$g_p + g_d$
+2	$4g_o$	$4g_p$	$2g_p$

1) BI-DAC HD3 WITH RESISTIVE LOAD

Consider a BI-DAC model as shown in Fig. 6, which consists of a LSB current I_o in parallel with finite signal-dependent output impedance (Z_o) composed of resistor R_o in parallel with capacitor C_o. In the figure, R_L is the external resistive load, M is the total number of thermometer-decoded DAC elements. In this scenario, the pMOS offset devices are omitted from the analysis and are not shown in Fig. 6. These devices acts as an offset in the signal-dependent impedance characteristic drawn at the positive/negative output node of the BI-DAC and does not influence the DAC HD3 performance. For an N-bit and M-level BI-DAC using a sinusoidal input-signal, the current variation at the positive output node is given as

$$I^+_{out} = I_o\ \frac{M(1 + \sin(\omega t)\ )}{2}. \tag{12}$$

At low frequencies, the DAC unit CS_{rc} cell output-impedance Z_o is dominated by the output-conductance g_o. Its variation at the positive output node of the DAC is given by

$$g^+_{out} = g_o\ \frac{M(1 + \sin(\omega t))}{2}. \tag{13}$$

As an example, the output-conductance variation at the positive output of a 2-bit BI-DAC is tabulated in Table 1. With the load conductance $g_L = 1/R_L$, the output voltage at the positive output node is

$$V^+_{out} = \frac{M\ I_o\ (1 + \sin(\omega t))}{2g_L + Mg_o(1 + \sin(\omega t))}. \tag{14}$$

The Taylor series expansion of (14) is

$$V^+_{out} = \ a_0 + a_1\sin(\omega t) + a_2\sin^2(\omega t) + a_3\sin^3(\omega t) + ., \tag{15}$$

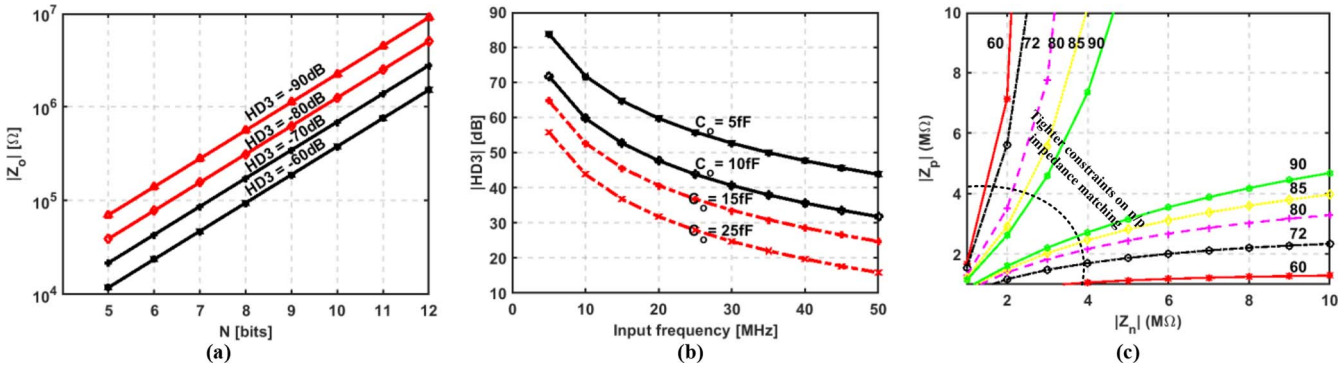

FIGURE 7. (a) Minimal $|Z_O|$ required to achieve specific HD3 for different thermometer DAC bits N with $R_L = 50\Omega$. (b) HD3 vs f_{in} for a 12-bit thermometer-decoded BI-DAC using different C_O values with $R_L = 50\Omega$. (c) $|Z_n|$ and $|Z_p|$ matching requirements for a 12-bit unary-weighted CMP-DAC with $R_L = 50\Omega$.

where $a_0 = \frac{M\ I_o}{2g_L+Mg_o}$, $a_1 = (\frac{M\ I_o}{2g_L+Mg_o})^2 \frac{2g_L}{M\ I_o}$,

$$a_2 = \left(\frac{M\ I_o}{2g_L + Mg_o}\right)^3 \frac{-4g_o g_L}{M\ I_o^2}, a_3 = \left(\frac{M\ I_o}{2g_L + Mg_o}\right)^4, a_4 \cdots$$

Using trigonometric relations for (15) and rearranging the terms results in

$$V_{out}^{+} = a_0 + \left[a_1 + \frac{3}{4}a_3\right]\sin(\omega t) \ + \left[\frac{-(a_2 - a_4)}{2}\right]\sin(2\omega t) + \frac{a_3}{4}\sin(3\omega t) \ + \cdots \tag{16}$$

The HD3 is the ratio of the coefficients of $\sin(\omega t)$ and $\sin(3\omega t)$

$$HD3 = \left|\frac{0.25\ a_3}{a_1 + 0.75a_3}\right|. \tag{17}$$

By placing the coefficients of $\sin(\omega t)$ and $\sin(3\omega t)$ from (15) in (17), the signal-dependent output-impedance related HD3 for BI-DAC yields

$$HD3 = \left|\frac{M^2 {g_o}^2}{(16\ g_L^2 + 16\ g_L\ g_o\ M + 7\ M^2 {g_o}^2\ )}\right|,$$
$$HD3 \propto \frac{M^2 {g_o}^2}{g_L^2}. \tag{18}$$

At low frequencies Z_o is dominated by g_o, therefore the effect of the finite-output-impedance is independent of the signal frequencies as can be seen from (18). It also signifies that the HD3 performance of a high-resolution BI-DAC can be improved by increasing the output-impedance of a unit CS_{rc} cell. Using (18), a low frequency minimal $|Z_o|$ requirement to achieve specific HD3 (-60, $-70-80$, and -90 dB) performance for different number of thermometer-decoded DAC bits is shown in Fig. 7(a) using a 50Ω load. The figure shows that to achieve better HD3 performance for high-resolution BI-DAC, it requires large $|Z_o|$ value.

At high frequencies, Z_o is dominated by $1/j\omega C_o$, where C_o is the effective output-capacitance of a unit CS_{rc} cell. From (18), the HD3 at high frequencies can be obtained by replacing g_o with $j\omega C_o$ as

$$HD3 \propto \left|\frac{M^2\omega^2 C_O^2}{g_L^2}\right| = \left|\frac{4M^2\pi^2 f_{in}^2 C_O^2}{g_L^2}\right|, \tag{19}$$

where $\omega = 2\pi f_{in}$ and f_{in} is the input-signal frequency. Using (19), HD3 versus f_{in} is plotted in Fig. 7(b) for a 12-bit unary-weighted BI-DAC with 50Ω load using different values of C_o (5, 10, 15, and 25fF). The figure shows that the HD3 can be improved at high frequencies by minimizing the effective output capacitance C_o of the DAC unit CS_{rc} cell.

2) CMP-DAC HD3 WITH RESISTIVE LOAD

In the case of the CMP-DAC topology, the n/p CS_{rc} simultaneously 'Sink' and 'Source' the current to the output node. For sinusoidal-input signal the current variation at the positive-output node is

$$I_{out}^{+} = M\left[\frac{I_p(1 + \sin(\omega t)\ )}{2} + \frac{I_n(1 - \sin(\omega t)\ )}{2}\right]. \tag{20}$$

Substituting $I = I_p + I_n$ and $\Delta I = I_p - I_n$ in (20) and re-writing

$$I_{out}^{+} = M\left[\frac{I}{2} + \frac{\Delta I\ \sin(\omega t)}{2}\right]. \tag{21}$$

At low frequencies, output-impedances Z_n and Z_p of the n/p section of CMP-DAC CS_{rc} slice is dominated by g_n and g_p respectively. Therefore, the output-conductance looking into the positive output node is

$$g_{out}^{+} = M\left[\frac{g_p(1 + \sin(\omega t)\ )}{2} + \frac{g_n(1 - \sin(\omega t)\ )}{2}\right], \tag{22}$$

where g_n and g_p are the output-conductance's of the n/p unit CS_{rc}s. In the case of the 2-bit CMP-DAC, the output-conductance variation at the positive output node for different input-codes is tabulated in Table 1. Considering load conductance g_L, the voltage at the positive output node is

$$V_{out}^{+} = \frac{M\ \ (I + \Delta I\ \sin(\omega t)\ )}{2g_L + M(g_p + g_n) + M\ (g_p - g_n)\sin(\omega t)}. \tag{23}$$

Similarly, the voltage at the negative output is

$$V_{out}^{-} = \frac{M\ \ (I - \Delta I\ \sin(\omega t)\ )}{2g_L + M\big(g_p + g_n\big) - M\ \big(g_p - g_n\big)\sin(\omega t)}. \quad (24)$$

From (23) and (24), the differential output voltage is then

$$V_d = V_{out}^{+} - V_{out}^{-} = \frac{2\ Mx\ (2g_L\Delta I + MA\ \Delta I - MBI)}{(2g_L + MA)^2 - (MBx)^2}, \quad (25)$$

where $A = (g_p + g_n)$, $B = (g_p - g_n)$ and $x = \sin(\omega t)$. Expanding (25) using Taylor's series and substituting x and x^3 in (17), the code-dependent output-impedance associated HD3 can be expressed [5]

$$HD3 = \left| \frac{M^2\big(g_n - g_p\big)^2}{\Big(16g_L\big(g_L + M\big(g_n + g_p\big)\big) + M^2\Big(7g_n^2 + 2g_n g_p + 7g_p^2\Big)\Big)} \right|,$$

$$HD3 \propto \frac{M^2(g_n - g_p)^2}{g_L^2}. \quad (26)$$

Equation (26) states that the HD3 performance of the CMP-DAC topology at low frequencies can be improved by employing g_n and g_p matching in a unit CS_{rc} slice. Intuitively, it can be observed from Table 1 that the nMOS unit CS_{rc} conductance (g_n) and pMOS unit CS_{rc} conductance (g_p) should be made equal to make output-conductance equal for each input code at the positive output of the CMP-DAC. Using (26), the required HD3 as a function of $|Z_p|$ and $|Z_n|$ for a 12-bit unary-weighted CMP-DAC driving a 50Ω resistive load is shown in Fig. 7(c). The plot shows that, for a realizable output-impedance values of an nMOS unit CS_{rc} ($\leq$ 4MΩ), HD3 ($\geq$ 70dB) can be obtained, using the tighter matching constraints between $|Z_n|$ and $|Z_p|$. However, these matching constraints become more relaxed for large values of $|Z_n|$ ($\geq$5MΩ).

At high frequencies, Z_n and Z_p of the n/p section of CMP-DAC is dominated by $1/j\omega C_n$ and $1/j\omega C_p$ respectively. In this case, C_n and C_p is the effective output-capacitance of n/p unit CS_{rc} cell of CMP-DAC. From (26), the HD3 at high frequencies can be obtained by replacing g_n and g_p with $j\omega C_n$ and $j\omega C_p$ respectively which can be stated as

$$HD3 \propto \left| \frac{4M^2\pi^2 f_{in}^2\big(C_n - C_p\big)^2}{g_L^2} \right|. \quad (27)$$

It can be noted from (27) that to improve HD3 at high frequencies and to make it signal independent, matching between C_n and C_p is necessary in CMP-DACs unit CS_{rc} slice.

3) TRI-DAC HD3 WITH RESISTIVE LOAD

The HD3 analysis in [5] for CMP-DAC is further developed to enable a complete and thorough analysis of output-impedance related HD3 for TRI-DAC design. The code-dependent output-conductance behavior of the TRI-DAC differs significantly from the BI-DAC and CMP-DAC topology due to incorporation of the 'Dump' switch in a CS_{rc} slice. In an N-bit and M-level thermometer-decoded TRI-DAC, if k is the number of CS_{rc}'s that are turned 'ON' for a given input-code, then there will be $(M/2 - k)$ number of CS_{rc}'s operating in dump mode. The TRI-DAC code-dependent output-conductance variation at the positive output node is shown in Fig. 8 and tabulated in Table 1, where g_d is the dump mode conductance ($Z_d \gg Z_n, Z_p$). Intuitively, it can be observed from both Fig. 8 and Table 1 that g_n, g_p and g_d should be made equal to remove the code-dependent output-conductance variation in the TRI-DAC.

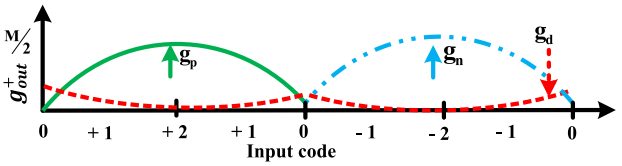

FIGURE 8. Output-conductance variation at the positive output of TRI-DAC.

In order to simplify the HD3 analysis for a TRI-DAC driving an external resistive load, n/p CS_{rc} LSB currents are assumed to be equal, i.e., $I_n \approx I_p = I_{lsb}$. Hence, the current variation at positive the output node of the TRI-DAC can be written as

$$I_{out}^{+} = \frac{MI_{lsb}\sin(\omega t)}{2}. \quad (28)$$

At low frequencies, output-impedances Z_n, Z_p and Z_d of the Sink, Source and Dump mode of TRI-DAC unit CS_{rc} slice is dominated by g_n, g_p and g_d respectively. It can be observed from Fig. 8 that the combination of the n/p output-conductance variation at the positive output forms a full-rectified wave. Therefore, the n/p CS_{rc} output-conductance variation without considering dump conductance is represented as

$$g_{np}^{+} = \frac{M}{2}\left[\frac{A}{\pi} + \frac{B\sin(\omega t)}{2} + \frac{2A}{\pi}\sum_{n=2,4\cdots}^{\infty}\frac{\cos(n\omega t)}{1-n^2}\right], \quad (29)$$

where $A = (g_p + g_n)$, $B = (g_p - g_n)$. From Fig. 8, the signal-dependent dump mode conductance variation of the TRI-DAC at the positive output can be stated as

$$g_d^{+} = \frac{Mg_d}{2}\left[0.36 - \frac{4}{\pi}\sum_{n=2,4\cdots}^{\infty}\frac{\cos(n\omega t)}{1-n^2}\right]. \quad (30)$$

The overall output-conductance looking into the positive output node is the addition of (29) and (30).

$$g_{out}^{+} = \left[\frac{A}{\pi} + \frac{Bx}{2} + 0.36g_d + (A - 2g_d)X\right], \quad (31)$$

where $x = \sin(\omega t)$ and $X = \frac{2}{\pi}\sum_{n=2,4\cdots}^{\infty}\frac{\cos(n\omega t)}{1-n^2}$. To simplify mathematical calculations, X can be further simplified as

$$X = -\frac{2}{\pi}\left(\frac{\cos(2\omega t)}{3} + \frac{\cos(4\omega t)}{15} + \cdots\right). \quad (32)$$

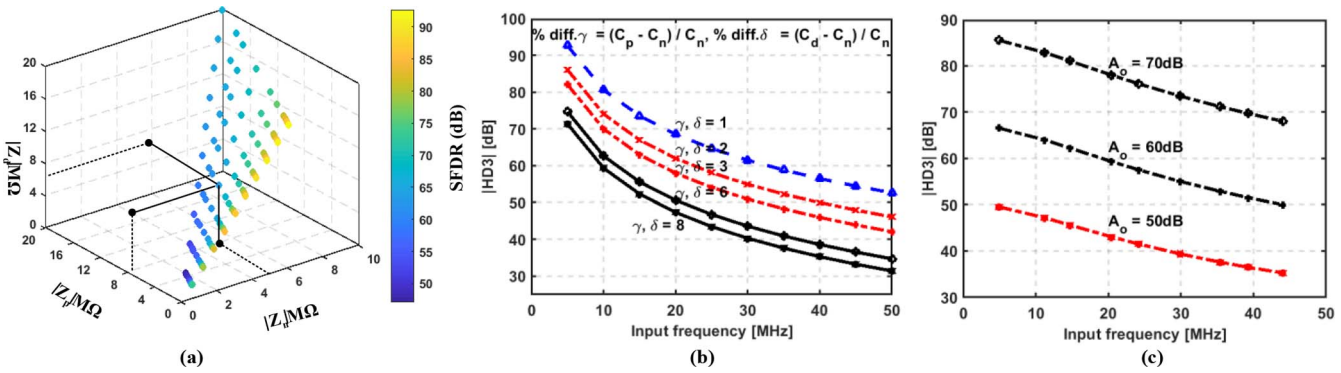

FIGURE 9. (a) A multi-dimensional view using $|Z_n|$, $|Z_p|$, $|Z_d|$ and SFDR for a 12-bit thermometer-decoded TRI-DAC with a $R_L = 50\Omega$. (b) HD3 vs f_{in} and % mismatch γ and δ for a 12-bit thermometer-decoded TRI-DAC with $R_L = 50\Omega$. (c) HD3 vs f_{in} and different A_O(dB) values for a 12-bit unary-weighted BI-DAC with an amplifier load.

Further simplifying (32), using trigonometric formulae and re-writing

$$X = -[0.25 - 0.75x^2 + 0.33x^4]. \tag{33}$$

Substituting (33) in (31) and considering load conductance, the output-conductance at positive output node is

$$g_{out}^{+} = g_L + \frac{MA}{2\pi} + \frac{9Mg_d}{50} - \frac{MC}{8} + \frac{MB}{4}x + \frac{3MCx^2}{8} - \frac{MCx^4}{6}, \tag{34}$$

where $C = (A - 2g_d)$. From (28) and (34), the output voltage at the positive output node is

$$V_{out}^{+} = \frac{\frac{MI_{lsb}x}{2}}{g_L + \frac{MA}{2\pi} + \frac{9Mg_d}{50} - \frac{MC}{8} + \frac{MB}{4}x + \frac{3MCx^2}{8} - \frac{MCx^4}{6}}. \tag{35}$$

Substituting $K = \frac{MI_{lsb}}{2}$, $L = g_L + \frac{MA}{2\pi} + \frac{9Mg_d}{50} - \frac{MC}{8}$, $P = \frac{MB}{4}$, $Q = \frac{3MC}{8}$, $R = \frac{MC}{6}$ in (35) and re-writing

$$V_{out}^{+} = \frac{Kx}{L + Px + Qx^2 - Rx^4}. \tag{36}$$

The Taylor series expansion of (36) is

$$V_{out}^{+}(x) = \left[\frac{K}{L}x - \frac{KP}{L^2}x^2 - \frac{K}{L}\left(\frac{Q}{L} - \frac{P^2}{L^2}\right)x^3 \cdots\right]. \tag{37}$$

Substituting coefficients of x and x^3 from (37) in (17) yields

$$HD3 = \left|\frac{P^2 - QL}{4L^2 + 3QL - 3P^2}\right|,$$
$$HD3 \propto \frac{M^2\left[(g_n - g_p)^2 - \left(g_n^2 + g_p^2 - 32g_d^2 + 2g_ng_p + 14(g_ng_d + g_pg_d)\right)\right]}{g_L^2}. \tag{38}$$

Using (38), a multi-dimensional plot shown in Fig. 9(a) is obtained for a 12-bit thermometer-decoded TRI-DAC with a 50Ω load. The X, Y and Z-axis in the plot represent $|Z_n|$, $|Z_p|$ and $|Z_d|$ values respectively. The color represents the SFDR for a specific value of $|Z_n|$, $|Z_p|$ and $|Z_d|$. As an example, for $|Z_n| = 5\text{M}\Omega$ and $|Z_p|$, $|Z_d|$ equal to 7.5MΩ, the SFDR is close to 70dB. The multidimensional plot illustrates the low frequency $|Z_n|$, $|Z_p|$ and $|Z_d|$ requirements to achieve desired SFDR performance for TRI-DAC. It also signifies that the SFDR performance can be greatly improved by making $|Z_n|$, $|Z_p|$ and $|Z_d|$ closely match in a TRI-DAC unit CS_{rc} slice.

At high frequencies, Z_n, Z_p and Z_d of TRI-DAC is dominated by $1/j\omega C_n$, $1/j\omega C_p$ and $1/j\omega C_d$ respectively. In this case, C_n, C_p and C_d is the effective output-capacitance of unit CS_{rc} cell of TRI-DAC in 'Sink', 'Source' and 'Dump' mode respectively. From (38), the HD3 at high frequencies can be obtained by replacing g_n, g_p and g_d with $j\omega C_n$, $j\omega C_p$ and $j\omega C_d$ respectively as

$$HD3 \propto \left|\frac{M^2\omega^2\left[(C_n - C_p)^2 - \left(C_n^2 + C_p^2 - 32C_d^2 + 2C_nC_p + 14(C_nC_d + C_pC_d)\right)\right]}{g_L^2}\right|. \tag{39}$$

It can be noted from (39) that at high frequencies the HD3 of TRI-DAC can be improved and made signal independent by employing matching between C_n, C_p and C_d in a TRI-DAC unit CS_{rc} slice. Using (39), HD3 versus f_{in} and the percentage mismatch γ between C_n and C_p, the percentage mismatch δ between C_n and C_d is plotted in the Fig. 9(b) for a 12-bit thermometer-decoded TRI-DAC with a 50Ω load. To demonstrate the plot, C_n is chosen to be $70fF$. The plot shows that signal-dependent output-impedance related HD3 for TRI-DAC at high frequencies can be improved by making C_n, C_p and C_d equal in a unit CS_{rc} slice.

4) BI-DAC HD3 WITH AMPLIFIER LOAD

In this section, the output-impedance related HD3 for BI-DAC driving a transimpedance amplifier is derived. The DAC output-impedance model driving a single-ended amplifier is shown in Fig. 10, where Z_F is the feedback impedance and $A(s)$ is the frequency dependent gain of an amplifier. From the figure and by using Kirchhoff's Current Law (KCL), I_{in} is equal to DACs CS_{rc} cell signal-dependent current I_o

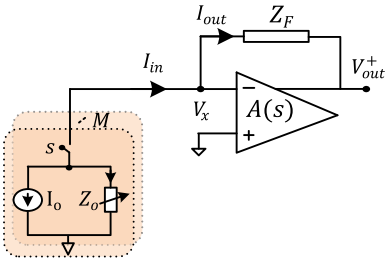

FIGURE 10. BI-DAC output-impedance model driving a single-ended amplifier.

and the current through the code-dependent effective output-impedance Z_o, which can be stated as

$$I_{in} = -\left(0.5MI_o(1+x) + \frac{V_x}{Z_o/0.5M(1+x)}\right). \quad (40)$$

Due to the virtual ground, the current I_{in} is equal to I_{out}. Applying KCL at node V_x

$$-I_{in} + I_{out} = 0. \quad (41)$$

Using I_{in} from (40) and writing for I_{out}, (41) can be written as

$$0.5MI_o(1+x) + \frac{V_x}{Z_o/0.5M(1+x)} + \frac{V_x - V_{out}^+}{Z_F} = 0. \quad (42)$$

At the inverting node of the amplifier, $V_x = -V_{out}^+/A(s)$, and $A(s)$ is represented as

$$A(s) = \frac{A_o}{1 + \frac{j\omega}{\omega_o}}, \quad (43)$$

where A_o is the dc gain of the amplifier, ω_o is the pole frequency in radians. Substituting, $V_x = -V_{out}^+/A(s)$ in (42) and solving for output voltage

$$V_{out}^+ = \frac{0.5MI_o(1+x)\ A(s)}{\frac{0.5M(1+x)}{Z_o} + \frac{(A(s)+1)}{Z_F}}. \quad (44)$$

At low frequency, DACs CS_{rc} cell effective impedance Z_o and the amplifier's feedback impedance Z_F is dominated by conductance's g_o and g_F respectively. Re-writing (44)

$$V_{out}^+ = \frac{0.5MI_o(1+x)\ A(s)}{g_F(A(s)+1) + 0.5Mg_o + 0.5Mg_o x}. \quad (45)$$

Similarly, the output voltage at negative node can be written as

$$V_{out}^- = \frac{0.5MI_o(1-x)A(s)}{g_F(A(s)+1) + 0.5Mg_o - 0.5Mg_o x}. \quad (46)$$

From (45) and (46), the differential output voltage is then

$$V_d = V_{out}^+ - V_{out}^- = \frac{2MI_o x A(s)(Mg_o + (A(s)+1)g_F)}{((A(s)+1)g_F + 0.5Mg_o)^2 - (0.5Mg_o x)^2}. \quad (47)$$

Expanding (47) using Taylor's series and substituting the coefficients of x and x^3 in (17), the output-impedance related HD3 can be expressed

$$HD3 = \left|\frac{M^2 {g_o}^2}{\left(4(2g_F\ (A(s)+1) + Mg_o)^2 + 3M^2 g_o^2\right)}\right|,$$

$$HD3 \propto \frac{M^2 {g_o}^2}{g_F^2\ (A(s)+1)^2}. \quad (48)$$

Intuitively, (48) can be obtained replacing g_L by $g_F.(A(s)+1)$ in (18). Equation (48) states that the HD3 performance of BI-DAC can be improved by increasing DACs output-impedance as well as the frequency dependent gain $A(s)$ of the amplifier. Figure 9(c) shows HD3 versus signal frequency for different A_o values (50, 60, and 70dB) that rolls-off with frequency. In this scenario, $|Z_F| = 500\Omega$ and the amplifier pole frequency f_o is 1MHz. The $|Z_o| = 1M\Omega$, rolls-off with frequency using $C_o = 10fF$. Figure 9(c) shows that the DACs HD3 value increases over the Nyquist band by increasing the dc gain value of the amplifier.

Replacing g_o by $j\omega C_o$ in (48), the HD3 at high frequency can be represented as

$$HD3 \propto \left|\frac{M^2\omega^2 C_O^2}{g_F^2\ (A(s)+1)^2}\right|. \quad (49)$$

5) CMP-DAC HD3 WITH AMPLIFIER LOAD

The HD3 equation for CMP-DAC driving an amplifier load can be obtained using the same procedure as for the BI-DAC topology. The coefficients of x and x^3 are obtained by applying Taylor's series expansion at the differential output voltage of the amplifier. By placing these coefficients in (17), the HD3 can be expressed

$$HD3 = \left|\frac{R_F^2 M^2 (g_n - g_p)^2}{16(A(s)+1)\left((A(s)+1) + M(g_n+g_p)\right) + M^2\left(7g_n^2 + 2g_n g_p + 7g_p^2\right)}\right|,$$

$$HD3 \propto \frac{M^2(g_n - g_p)^2}{g_F^2\ (A(s)+1)^2}. \quad (50)$$

Intuitively, (50) can be obtained by replacing g_L with $g_F.(A(s)+1)$ in (26). The HD3 equation at high frequencies can be stated from (50) as

$$HD3 \propto \left|\frac{M^2\omega^2(C_n - C_p)^2}{g_F^2\ (A(s)+1)^2}\right|. \quad (51)$$

For CMP-DAC with an amplifier load, the HD3 at low frequencies can be improved by g_n and g_p matching, whereas at high frequencies HD3 can be improved by matching C_n and C_p in the DAC unit CS_{rc} slice. The HD3 can also be improved by increasing the frequency dependent gain of the amplifier.

6) TRI-DAC HD3 WITH AMPLIFIER LOAD

The HD3 for TRI-DAC driving an amplifier load can be obtained by referencing the procedures shown for BI-DAC driving an amplifier load and TRI-DAC driving a resistive load. Intuitively, HD3 can be obtained by replacing g_L with $g_F.(A(s)+1)$ in (38) which can be stated as

$$HD3 \propto \frac{M^2\left[(g_n - g_p)^2 - \left(g_n^2 + g_p^2 - 32g_d^2 + 2g_n g_p + 14(g_n g_d + g_p g_d)\right)\right]}{g_F^2(A(s)+1)^2}. \quad (52)$$

TABLE 2. CS-DAC topologies comparison.

Parameter	BI-DAC	CMP-DAC	TRI-DAC
Mismatch	Poor	Medium	Good
Noise	Poor	Medium	Good
Output impedance related HD3/SFDR	Medium (Improves when Z_o is increased)	Medium (Improves when Z_n and Z_p matched)	Medium (Improves when Z_n, Z_p and Z_d matched)

Equation (52) signifies that the HD3 performance can be greatly improved by close matching of g_n, g_p and g_d in a TRI-DAC unit CS_{rc} slice as well as by increasing $A(s)$. The HD3 equation at high frequencies can be obtained from (52) and represented as

$$HD3 \propto \left| \frac{M^2\omega^2\left[(C_n-C_p)^2-\left(C_n^2+C_p^2-32C_d^2+2C_nC_p+14(C_nC_d+C_pC_d)\right)\right]}{g_F^2(A(s)+1)^2} \right|. \tag{53}$$

D. CONCLUSION FROM ANALYSIS OF DAC TOPOLOGIES

The following conclusions can be drawn from the analysis presented in the above sections.

1) The 3-level element selection employed in a unit TRI-DAC exhibits less DNL and INL error compared to the BI-DAC and CMP-DAC topologies for a given level of mismatch and number of bits.
2) Although the TRI-DAC thermal noise is code-dependent; at the maximum code it contributes the same thermal noise as the CMP-DAC; however, at lower signal levels the TRI-DAC contributes significantly less thermal noise than the CMP-DAC and BI-DAC for an equivalent bit implementation.
3) With respect to output-impedance related HD3/SFDR performance, the TRI-DAC is seen to have a signal-dependent output loading effect and this impacts the HD3/SFDR performance; however, this loading effect can be mitigated by matching Z_n, Z_p and Z_d in each unit CS_{rc} slice.

Based on the above conclusions, the TRI-DAC topology is implemented in this work for the CTIP-ADC architecture of Fig. 1. The CS-DAC topologies comparison in terms of their mismatch, thermal noise and output-impedance related HD3/SFDR performance is summarized in Table 2.

IV. TRI-DAC DESIGN

Figure 11(a) shows a 1.2V 100MS/s 5-bit unary-weighted (33-level/16 CS_{rc} slices) tri-level CS-DAC top-level architecture. The TRI-DACs FS differential output current is 2.4mA and the output nodes drive a resetting integrator gain stage in CTIP-ADC design [1]. The TRI-DAC major blocks in include the 16x CS_{rc} slices, the bias circuit and the decoder logic, the design of which are detailed in the following sections.

A. CS-SLICE

The TRI-DAC consists of 16 DAC slices, such that each slice can simultaneously 'Sink' and 'Source' $75\mu A$ of current, to produce a $150\mu A$ differential step current. The TRI-DAC output nodes drive the 600mV common-mode level of the amplifier. From (6), the n/p unit CS_{rc} relative standard deviation should be less than or equal to 0.15% to design a 12-bit TRI-DAC with ± 0.5 LSB INL, achieving 99.7% yield. Furthermore, the gate area of a unit CS_{rc} using the related standard deviation and relevant technology parameters can be expressed [9] as

$$WL = \frac{1}{2\sigma^2\left(\frac{\Delta I}{I}\right)}\left[\left(\frac{2A_{V_t}}{V_{ov}}\right)^2 + \left(A_\beta\right)^2\right]. \tag{54}$$

In this work, the overdrive-voltage (V_{ov}) for the n/p CS_{rc} is 300mV and the nMOS $A_{V_T} = 3.8\text{mV}*\mu\text{m}$, pMOS $A_{V_T} = 3.4\text{mV}*\mu\text{m}$ with $A_\beta = 0.7\%*\mu\text{m}$ for both devices. Using 0.1% standard deviation on both n/p CS_{rc} devices, the initially estimated gate area is $345\mu\text{m}^2$ and $288\mu\text{m}^2$ respectively. The W/L ratio of the n/p CS_{rc} device is determined in such a way that it maintains the required standard deviation and the overdrive voltage on both the devices. Using aspect ratios of $32/10\mu$m and $80/4\mu$m for the n/p CS_{rc} device respectively; the values obtained for $\sigma(\Delta I_n/I_n)$ and $\sigma(\Delta I_p/I_p)$ are 0.12% and 0.13% respectively. The TRI-DAC transistor-level DNL and INL performance results using 100 MC simulations seen in Fig. 11(e) show the DNL/INL is $\leq$0.5 LSB. The obtained maximum DNL_{RMS} and maximum INL_{RMS} are 0.09 LSB and 0.19 LSB respectively. These results are in good agreement with TRI-DAC MATLAB model results and DNL, INL equations as discussed in Section III.

B. BIAS BLOCK AND DECODER LOGIC

The proposed bias circuit is shown in Fig. 11(a). The biasing circuit is divided into two parts 'Global' and 'Local'. The global biasing uses $300\mu A$ of the reference current and a current of $75\mu A$ flow through each parallel branch. Low-voltage-threshold devices are used to implement the biasing circuit to overcome the voltage headroom limitations. A reference branch is designed using 4x larger devices than its replica branches to reduce the effect of mirrored noise. Additionally, the local biasing is divided into two high compliance bias slices for better layout and symmetry. The TRI-DAC decoder logic is driven by the thermometer-decoded outputs of the 5-bit Flash-ADC containing 32 comparators organized as 16 pairs. The pairing of the comparator outputs is shown in Fig. 11(b). Each pair comprises of an 'Upper' and 'Lower' comparator as shown in Fig. 11(c). The outputs U_p and U_n, L_p and L_n of the upper and lower comparators are complementary. To reduce the latency in the feedforward critical path of the CTIP-ADC; the TRI-DAC decoder logic is simply implemented using 2-input NAND gates. The decoder logic truth table is shown in Fig. 11(d). In this design, the use of a simple

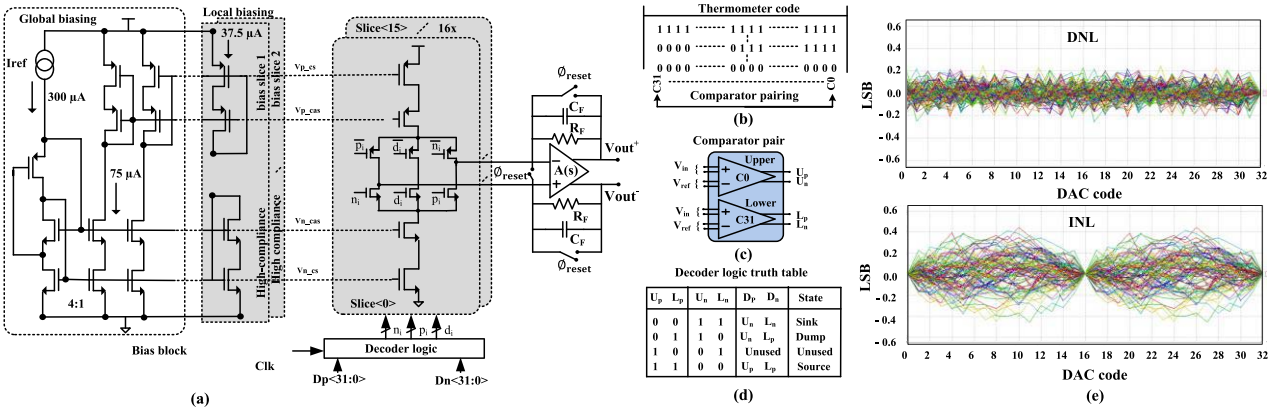

FIGURE 11. (a) TRI-DAC top-level architecture. (b) Pairing of comparators in Flash-ADC. (c) A comparator pair. (d) Decoder logic truth table. (e) TRI-DAC design DNL/INL transistor-level MC runs at 12-bit level.

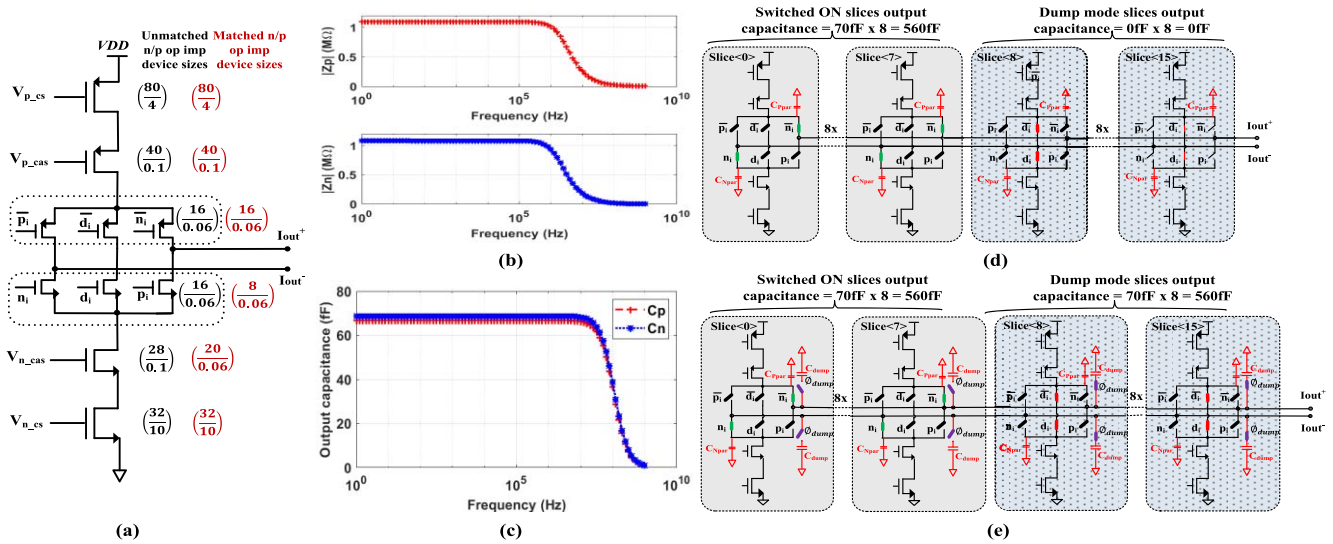

FIGURE 12. (a) Device ratios of unmatched and matched TRI-DAC unit CS_{rc} slice. (b) n/p section output-impedance of a compensated TRI-DAC unit CS_{rc} slice. (c) Output-capacitance of n/p section of a compensated TRI-DAC unit CS_{rc} slice. (d) Uncompensated TRI-DAC (e) Capacitive compensated TRI-DAC.

thermometer-decoded input stage minimizes element transitions and is helpful in reducing dynamic distortion effects such as ISI [10].

V. TECHNIQUE TO IMPROVE OUTPUT-IMPEDANCE RELATED HD3 FOR TRI-DAC

The code-dependent output-impedance behavior of the TRI-DAC differs significantly from the BI-DAC and CMP-DAC topology, which is shown in Section III. Furthermore, it is shown that the TRI-DAC's output-impedance related HD3/SFDR performance can be improved by matching Z_n, Z_p and Z_d in each unit CS_{rc} slice. In this work, the TRI-DAC unit CS_{rc} slice (uncompensated) is initially designed with an n/p section output-impedance of 0.91MΩ and 1.94MΩ respectively. The dynamic performance results of the uncompensated TRI-DAC driving an amplifier is discussed in Section VI. To improve TRI-DAC's HD3/SFDR performance, the impedance matching between the n/p sections is employed within each of the CS_{rc} slice of the TRI-DAC design. This impedance matching is employed at the transistor-level using typical conditions to tune the device sizes with no further calibration over PVT. To achieve close match between the n/p section output-impedance and output-capacitance of the TRI-DAC unit CS_{rc} cell, W/L ratio of the switch devices and cascode's of the n/p section is tuned without disturbing the CS_{rc}'s. Figure 12(a) shows the device ratios for unmatched and matched impedance of a TRI-DAC unit CS_{rc} slice. The matched n/p section output-impedance and output-capacitance for TRI-DAC unit CS_{rc} slice is shown in Fig. 12(b) and (c) respectively. In this scenario, $|Z_n| = 1.08\text{M}\Omega$, $|Z_p| = 1.10\text{M}\Omega$, $C_n = 70fF$ and $C_p = 68fF$.

Even though, the n/p section impedance matching is employed; the output nodes of the TRI-DAC still have a code-dependent variable output loading effect due to the 'Dump' mode. The output-capacitance of a switched 'ON' TRI-DAC unit CS_{rc} slice is approximately 70fF at both output nodes. The 'Dump' state contributes no current to the

output node; hence, the capacitance seen at the output node is zero. In this scenario, the uncompensated TRI-DAC has a code-dependent output-capacitance at the positive/negative output node as can be seen from Fig. 12(d). This signal-dependent capacitance causes distortion in the TRI-DAC and deteriorates its dynamic performance at high frequencies.

In [11], to reduce the code-dependent load effect that causes dynamic glitch variation in a binary-weighted DAC, the capacitors are employed between the latch and the CS_{rc} switch devices. However, in this work, our proposed solution adds a switch $\emptyset_{dump}$ in each TRI-DAC slice to the output nodes in 'Dump' mode to mitigate the code-dependent loading effect. When the slice is switched to 'Dump' mode, $\emptyset_{dump}$ is activated and the capacitive loading at the output becomes C_{dump} as shown in Fig. 12(e). The value of C_{dump} is sized to match the capacitance of an 'ON' unit CS_{rc} slice. In this scenario, the capacitance seen at the positive/negative output node of the compensated TRI-DAC remains at a constant value of 1.12pF (16 x 70fF) for each DAC input-code. In this work, the dump capacitor (C_{dump}) is implemented using an n/p device to mimic the CS_{rc} device parasitic capacitance. The aim is to equalize the DAC capacitive loading for all input codes. This technique improves HD3/SFDR by $\sim$ 8dB at high frequencies as shown by the results in Section VI.

VI. LAYOUT AND SIMULATION RESULTS

The TRI-DAC layout size is 176μm x 372μm, including 16x DAC slices, bias circuitry and decoder-logic as shown in Fig. 13. Each of the 16x slice strips consist of n/p CS_{rc} device, cascodes, switch devices and dump capacitors which has an outline of 163μm x 14μm and maintains the symmetry along its horizontal axis. The dump capacitors using n/p devices are equal in size as that of n/p switch devices; hence, the impact on the area overhead is minimal. The TRI-DAC slice strip contains shorter dummy devices to help with matching and to reduce the shallow-trench-isolation (STI) effects. The local bias section is placed at either side of the 16x DAC slice strip array and connects to the global bias block. The layout includes dummy devices matched to the n/p sensitive devices in each slice. The layout consists of dedicated routing channels to reduce parasitic capacitance and to minimize IR power drop across the full design. The decoder logic in each DAC slice is driven by a separate digital 1.2V supply and isolated rings to minimize the supply noise interference.

The TRI-DAC designed in this work has been verified using transistor-level simulations implemented in TSMC 65nm CMOS technology. The TRI-DAC FS output current is 2.4mA and the power consumption from the blocks including bias, 16x TRI-DAC slices and the decoder logic is 2.55mW (from MSB DAC). The TRI-DAC static linearity simulations show DNL, INL below $\pm$0.5 LSB and the transient simulations show a FS settling time of 355ps including a 28.11ps driver delay.

In this work, the TRI-DAC is employed in the feed-forward path of the CTIP-ADC design [1]. The CTIP-ADC

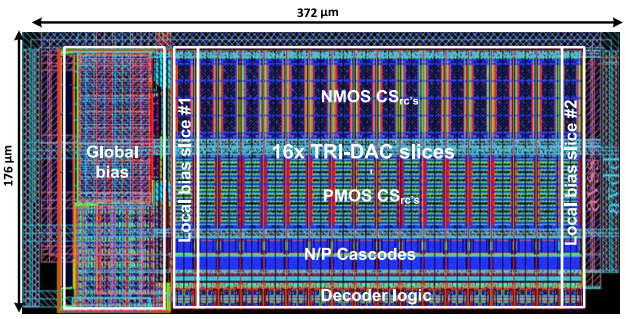

FIGURE 13. Layout of the TRI-DAC.

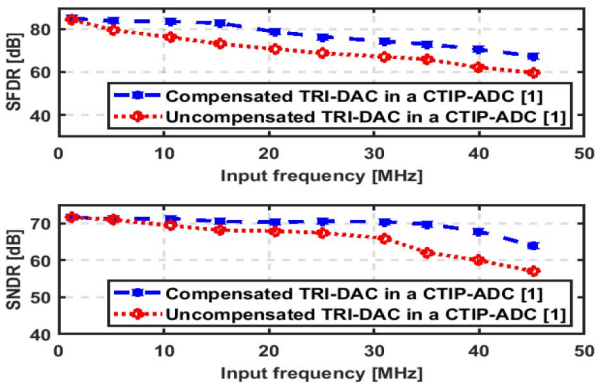

FIGURE 14. SNDR/SFDR versus input-frequency for uncompensated and compensated TRI-DAC employed in a CTIP-ADC design [1].

is implemented using transistor's at SPICE-level in TSMC 65nm technology which consists of all pass filter, 5-bit Flash-ADC, 5-bit TRI-DAC, a resetting integrator gain stage, and a 9-bit back-end SAR-ADC. The TRI-DAC output nodes drive a resetting integrator gain stage detailed in [1]. The resetting integrator is implemented using a feedforward compensated amplifier with $\sim$70dB open loop gain and a 1GHz unity gain frequency. This amplifier has more than one pole and a zero rolls off with $-$40dB for a range of frequencies that allows it to have a smaller unity gain bandwidth than a conventional single pole amplifier. In this scenario, the five MSB bits of Flash-ADC/DAC are combined with seven LSB bits of backend SAR-ADC. The SNDR/SFDR results at 12-bit level for overall CTIP-ADC design by employing uncompensated and compensated TRI-DAC design running at 100MS/s is shown in Fig. 14. The results show an improvement in output-impedance related SNDR/SFDR at higher frequencies over the first Nyquist band for impedance matched and capacitive compensated TRI-DAC employed in the CTIP-ADC architecture [1]. Degradation at higher frequencies occurs as the resetting integrator op-amp is susceptible to offset caused by mismatch of the op-amp input differential pair. This offset is gained by the resetting integrator, which causes the backend ADC to saturate at higher input tones. A solution is to use a scheme like Correlated Double Sampling (CDS) where the op-amp offset is sampled during reset and stored on the integrating capacitors, cancelling the offset effects.

TABLE 3. Comparison with previously published DAC work.

Specifications	[12]	[13]	[14]	[15]	This Work
Bits/Type	14/BI-DAC	12/BI-DAC	14/BI-DAC	14/BI-DAC	5 (12-bit linear)/TRI-DAC
Technology (nm)	180	90	130	180	65
Supply (V)	1.8	2.5 /1.2	1.5	1.8/3.3	1.2
P_{total} (mW)	210	92	28	67.7	2.80[2]
P_{load} (mW)	-	13.36	-	2.5	-
F_s (MS/s)	200	400	200	500	100
BW^{1}_{eff} (MHz)	4	3	10	180	35
$Area^{+}$ (mm^2)	3	0.18	0.9	0.55	0.08[3]
FS current (mA)	16	26.7	10	10	2.4
DNL/INL(LSB)	0.76/1.37	0.3/0.4	0.66/0.64	0.5/0.5	0.3/0.5
SFDR (dBc)	78.1 ~ 42.0	73.6 ~ 50.0	85.3 ~ 48.0	83.7 ~ 68.9	84.8 ~ 67.33
FOM_1	3.12E+02	1.33E+02	5.85E+03	4.35E+04	5.12E+04
FOM_2	6.35E+05	5.13E+06	5.32E+07	2.19E+08	8.46E+08
FOM_3	1.04E+02	7.42E+02	6.50E+03	7.92E+04	6.40E+05
FOM definition	$FOM_1 = \frac{2^N * BW_{eff}}{P_{total}}$		$FOM_2 = \frac{2^{\frac{SFDR^*_{dc}-1.76}{6.02}} * 2^{\frac{SFDR^*_{nyquist}-1.76}{6.02}} * Fs}{P_{total} - P_{load}}$		$FOM_3 = \frac{2^N * BW_{eff}}{P_{total} * Area^{+}}$

[1]Signal bandwidth that retains 70dB SFDR
[2]Approximate power from LSB DAC is included
[3]Approximate LSB DAC area is included
[+]Active area in mm^2
[*]$SFDR_{dc}$/$^*SFDR_{nyquist}$: Best/worst SFDR over the Nyquist band

Table 3 compares the SPICE-level simulation results of the TRI-DAC with measurement results of the previously published state of the art CS-DACs. A straightforward comparison is difficult as operating voltages, FS output current vary across these solutions and often CS-DACs target a resistive load. Although this TRI-DAC sampling rate is lower than reported DACs, the DNL/INL, area, SFDR and figure-of-merit (FOM) performance is seen to be comparable to [12]–[14], and [15]. Furthermore, the output-impedance related HD3/SFDR performance for TRI-DAC is improved using combined impedance matching and capacitive compensation technique over a wide bandwidth without complex analog/digital calibrations. The TRI-DAC design is suitable for operation in low power, low to medium bandwidth applications such as in CT-ADCs and CT-$\Sigma\Delta$ ADCs.

VII. CONCLUSION

In this work, an analysis and design of a thermometer-decoded CS-DAC suitable for CT-ADC architectures is presented. Based on the requirements identified a detailed analysis of the BI-DAC, CMP-DAC, and TRI-DAC topologies in terms of mismatch, noise, and code-dependent output-impedance related distortion is presented. Timing related errors such as ISI and jitter were not included in this analysis as they are mitigated by the use of the resetting integrator. From the analysis, a TRI-DAC topology is chosen for its static-linearity and thermal noise performance benefits over the BI-DAC and CMP-DAC topology. The proposed TRI-DAC is verified using TSMC 65nm simulation results. The design achieves 12-bit static-linearity and low latency with approximately 355ps settling time. The TRI-DAC's thermal noise and mismatch performance design advantages come at the cost of a code-dependent output loading effect. To mitigate this effect a compensation technique is applied that minimizes this non-linear loading effect and improves the output-impedance related dynamic performance over the Nyquist-band. This is verified from the simulation results obtained by employing a capacitive compensated TRI-DAC in the CTIP-ADC architecture.

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