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Impact of Frequency Heterogeneity on Mutually Synchronized Spatially Distributed 24 GHz PLLs

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ABSTRACT This research analyzes the mutual self-organized synchronization of phase-locked loops (PLLs) in the presence of variations in the free-running frequency of a PLL. In contrast to traditional synchronization methods that rely on a reference signal, this study investigates the synchronization dynamics that arise solely from the interactions of PLL nodes within a network. Previous research has proposed theoretical frameworks that can predict the synchronized states of such designs. However, these frameworks do not account for the dynamic behavior that occurs during initial synchronization. To address this gap, this work proposes a constraint that refines the understanding of initial synchronization. The results of this analysis show that there is a maximum detuning between free-running frequencies up to which synchronization is possible. Furthermore, this analysis indicates that detuning not only affects the range of time delays at which stable synchronized states emerge between PLL nodes, but also limits the allowable range of initial phase differences for stable synchronization. In the cases studied, a frequency difference of 1.56 % reduces the probability of achieving stable synchronized states through self-organized synchronization to 73.5 %, while no stable synchronization can be achieved at a frequency difference greater than 2.65 %. The study underscores the critical importance of operating ranges when implementing mutual coupling. In particular, all PLL nodes must have overlapping lock ranges to achieve stable synchronization. It also emphasizes the need for accurate analysis of hold and lock ranges in relation to the time delays between coupled PLL nodes.

INDEX TERMS Synchronization, delay effects, phase locked loops, voltage-controlled oscillators, frequency synchronization, couplings, mutual synchronization, oscillator, frequency synchronization.

I. INTRODUCTION

TIMING synchronization is a crucial aspect in various applications, including communications [1], [2], $[3]$, $[4]$, distributed computing $[5]$, $[6]$, $[7]$, and navigation systems [\[8\]](#page-10-2), [\[9\]](#page-10-3), [\[10\]](#page-10-4). Ensuring a consistent sense of time is essential for coordinating multiple devices or systems to operate effectively. Traditionally, the synchronization of time has been accomplished through hierarchical methods such as Network Time Protocol (NTP) [\[11\]](#page-10-5), [\[12\]](#page-10-6) and Precision Time Protocol (PTP) [\[13\]](#page-10-7), [\[14\]](#page-10-8). However, these methods have been improved and adapted [\[15\]](#page-10-9) in response to a growing need for higher precision, fault tolerance, and scalability. More recently, a new approach to synchronization has been explored, inspired by the flashing of fireflies, the coordinated movements of flocks of birds, or the applause at the end of a performance or speech $[16]$, $[17]$, $[18]$, $[19]$. In this bioinspired concept based on mutual synchronization, spatially distributed entities are able to self-organize their dynamics without the need for hierarchy or central control to establish a precise and robust common time base.

The first technical considerations of mutual synchronization were made in the 1960s in the context of the synchronization of pulse-code modulated signals in telephone networks at Bell Laboratories [\[20\]](#page-10-14), [\[21\]](#page-10-15), [\[22\]](#page-10-16). In this context, stability conditions are formulated for geographically separated, mutually synchronized oscillators, including the effect of timing jitter $[23]$, $[24]$. The search for a generalized expression for stationary synchronized states in networks of mutually synchronized oscillators [\[25\]](#page-10-19), [\[26\]](#page-10-20) was the focus of the 1980s. Theoretical considerations are made on the effect of the time delay between the coupled nodes on the synchronization [\[27\]](#page-10-21), [\[28\]](#page-10-22). The main results of the research group led by Lindsey are summarized in [\[29\]](#page-10-23), which points out that analyzing the mathematical model for finding stationary synchronized states of mutually synchronized oscillator networks in its most general form is difficult to solve. References [\[30\]](#page-10-24) and [\[31\]](#page-10-25) discussed mutual synchronization as a candidate for a data communications network, concluding that this method did not allow for administrationfree operation based on the knowledge available at that time.

On the other hand, studies of biological rhythms and coordinated behavior in nature have found expressions that describe the characteristic behavior of spatially distributed self-organizing rhythms and oscillations [\[32\]](#page-10-26). This mathematical description was simplified by Kuramoto [\[33\]](#page-10-27), which made it exactly solvable. Thus, there has been a remarkable increase in research on mutual oscillator synchronization in recent years, providing valuable insights into the complex self-organizing dynamics of networks with time-delayed nonlinear interactions [\[34\]](#page-10-28), [\[35\]](#page-10-29), [\[36\]](#page-10-30), [\[37\]](#page-10-31). Combining this bio-inspired concept with previous research on mutually synchronized oscillators leads to a more practical implementation using mutually delay-coupled networks of phase-locked loops (PLLs). The resulting theoretical framework for describing mutually time-delayed PLLs, including the nonlinear coupling characteristics of a PLL, is summarized and analyzed numerically in [\[38\]](#page-10-32).

To bring this complex theoretical framework into application, a very good and deep understanding of the underlying properties and limitations is essential. Several research activities have been conducted in recent years to investigate and improve the understanding using concept studies. In this context, crucial aspects such as the critical or maximum delay between two nodes [\[39\]](#page-10-33), time delays where multiple stable synchronized states exist in parallel $[40]$, and how the phase noise is affected by the network topology and the number of coupled nodes [\[41\]](#page-10-35) have been studied. An analysis was made of the impact of introducing a fixed reference in a network of coupled oscillators with mutual time delay [\[42\]](#page-10-36). The findings of these studies have contributed to a better understanding and refinement of the theoretical framework. However, in all of these previous studies, the open-loop freerunning frequencies of each PLL node were calibrated to have the same frequencies prior to analysis. There is also research that considers the effects of heterogeneity in such synchronization concepts. However, this research primarily focuses on the effects of varying time delays. For example, in [\[43\]](#page-10-37) the effects of heterogeneous time delays between coupled nodes were analyzed. Reference [\[44\]](#page-10-38) studied the effect of asymmetric delays between two nodes. In $[45]$, this analysis was extended to four fully digital delay-locked PLLs in ring topology. The mean value of the time differences between the nodes was kept constant, so that only the phase differences are affected.

The objective of this work is to address the effect of different open-loop free-running PLL frequencies on mutual time-delayed synchronization. Ongoing studies have shown that it is important to understand the effect of component tolerances, during design and implementation as they can prevent successful synchronization [\[44\]](#page-10-38), [\[46\]](#page-10-40), [\[47\]](#page-10-41). The most sensitive component in a PLL system with respect to tolerances such as process, voltage or temperature (PVT) variations is the oscillator used and its free-running frequency [\[48\]](#page-11-0), [\[49\]](#page-11-1). Therefore, this article analyzes the effects of different open-loop free-running PLL frequencies and how variations in frequency response of the oscillator affect mutual synchronization.

The concept of mutual self-organizing synchronization has significant advantages in several state-of-the-art applications, especially in the field of real-time multi-sensor data fusion systems [\[50\]](#page-11-2), [\[51\]](#page-11-3), by providing a highly accurate time reference for, e.g., precise localization. Practical applications of this technology are found in areas such as environmental monitoring [\[52\]](#page-11-4), [\[53\]](#page-11-5) and autonomous vehicles [\[54\]](#page-11-6), [\[55\]](#page-11-7). In these applications, synchronized data acquisition ensures accurate time stamping of data, enabling the creation of massive and time-aligned data sets. Other topics include Ising machines [\[56\]](#page-11-8), [\[57\]](#page-11-9), [\[58\]](#page-11-10), which are analog computing devices utilizing a network of mutually coupled oscillators to solve optimization problems.

The article is organized as follows: Theoretical considerations on the variations of the frequency response of PLL nodes and their influence on the operating ranges of mutual synchronization are presented in Section [II.](#page-1-0) Section [III](#page-4-0) details the measurement setup and hardware design for the PLL nodes used. Experimental measurements at different free-running open-loop frequencies and in-depth analysis of the effects on synchronized states are presented in Section [IV.](#page-6-0) Finally, a summary and conclusions are at the end of the article.

II. MODEL OF SELF-ORGANIZED SYNCHRONIZATION

Within a network of mutually time-delayed coupled PLL nodes, no reference signal is given unidirectionally to a PLL. Instead, all nodes are equal and democratically organized. A synchronized state emerges from the self-organizing dynamics of the network and the intrinsic dynamics of each PLL nodes. A minimal example consisting of a network with two nodes A and B is shown in Fig. [1.](#page-2-0) The mutual coupling does not provide a unidirectional reference to a PLL. Instead, the frequency-divided feedback signal serves as an output signal v_{out} for coupling to another PLL node input v_{in} . In systems that are spatially distributed, there is a delay between nodes due to finite signal propagation, resulting in a delay

FIGURE 1. Sketch of two PLL nodes A and B, which are mutually delay-coupled. Within this concept, the frequency-divided feedback signal is used similar to a reference signal for coupling with other PLL nodes.

 τ_{delay} of this coupling signal. As a result, the synchronized state of a PLL node depends not only on the incoming signal from another node but also on the phase difference caused by the time delay between the nodes.

A synchronized state emerges through self-organized dynamics, and its emergence can be predicted by a dynamical model, as discussed in previous work [\[38\]](#page-10-32), [\[41\]](#page-10-35), [\[59\]](#page-11-11). In this context, a synchronized state is characterized by equal frequencies at all coupled PLL nodes in the network and a phase difference between them that is constant in time. Unlike previous work, this article assumes that the oscillators of all nodes are slightly different. However, once all dynamics within the network have decayed, these synchronized states are given for each node *k* in the network by the following nonlinear implicit expression

$$
N \Omega_{\text{NET}} = g_k \left(K_{\text{LF}}(0) V_{\text{bias},k} + \frac{K_{\text{LF}}(0) A_{\text{PD}}}{E_k} \times \sum_{i=1}^{M} d_{ki} \triangle \left(-\Omega_{\text{NET}} \tau_{\text{delay},ki} - \varphi_{\text{mode},ki} \right) \right). (1)
$$

N is the frequency division factor of the PLL, Ω_{NET} is the output angular frequency of each node at the coupling plane in a synchronized state, $g_k(\cdot)$ is the nonlinear frequency response of the voltage controlled oscillator (VCO) of node k to its tuning voltage, $K_{LF}(0)$ is the steady state loop filter (LF) $V_{bias,k}$ a constant calibration voltage to set the free-running bias frequency of node k , E_k is the number of external inputs used at node *k*, M the total number of nodes in the network, *dki* the element of the adjacency matrix that indicates whether there is a connection between node *k* and *i*, A_{PD} is the phase detector (PD) amplitude, $\Delta(\cdot)$ the normalized triangular phase error transfer function of an XOR-based PD, $\tau_{delay,ki}$ an effective cross-coupling time delay between nodes k and i , and $\varphi_{\text{mode},ki}$ a constant phase difference between nodes *k* and *i*. This phase difference is called the mode locking phase difference and is a result of the periodicity of the PD and depends on the network topology [\[60\]](#page-11-12). All existing synchronized states, including their characteristic properties Ω_{NET} and $\varphi_{\text{mode},ki}$, can be identified by solving [\(1\)](#page-2-1) for each node *k*. The evaluation of the stability of a synchronized state can be done by analyzing its response to phase perturbations and has been studied in [\[61\]](#page-11-13), [\[62\]](#page-11-14).

On the right side of (1) it can be seen that the synchronized state is given by a nonlinear function $g_k(\cdot)$ of the frequency

FIGURE 2. The operating range of the used VCO is given by [\(](#page-2-1)[1](#page-2-1)**[\).](#page-2-1) This operating range, denoted by the gray shaded area, is affected by the added and averaged phase differences of all other connected nodes. The dashed orange line represent the linearized operating range given by the open-loop free-running frequency. The fitted square root function of the VCO yields** $g_k(V_{\text{tunc}}(t)) = 2\pi/20.7923$ $10^9 + 2.1944 \cdot 10^9 \sqrt{V_{\text{tunc}}(t)}$.

response of the VCO. The argument of this function represents the steady state tuning voltage in a synchronized state. It has two main parts: The filtered constant tuning voltage $V_{bias,k}$, which determines the free-running open-loop frequency $f_{0,k}$, and the frequency range around $f_{0,k}$ that the PLL can operate. This range is given by the summed and averaged phase differences between the operating node and all other connected nodes.

In the presented work the oscillator HMC739 from Analog Devices [\[63\]](#page-11-15) is used. The corresponding frequency response is shown in Fig. [2,](#page-2-2) which is fitted to a square root function $g_k(\cdot)$. To operate in the desired frequency range, $V_{bias,k}$ is used to set $f_{0,k}$ to 24 GHz. Around this value is the operating range of the PLL. Linearizing the nonlinear frequency response $g_k(\cdot)$ at the free-running open-loop frequency $f_{0,k}$, (1) yields the following implicit expression

$$
N \Omega_{NET} = \omega_{0,k} + K_{VCO,k} \frac{K_{LF}(0) ApD}{E_k}
$$

$$
\times \sum_{i=1}^{M} d_{ki} \triangle (-\Omega_{NET} \tau_{delay,ki} - \varphi_{mode,ki}), (2)
$$

where $\omega_{0,k} = 2\pi f_{0,k}$ is the free-running angular frequency of node *k* and $K_{VCO,k}$ is the sensitivity of the VCO at this operating point. Both parameters depend on the nonlinear frequency response $g_k(\cdot)$ of the VCO. It becomes clear that a variation of the response $g_k(\cdot)$ of the oscillator, as the key component within the PLL, not only changes the free-running open-loop frequency $f_{0,k}$, but also $K_{VCO,k}$. The linearized operating range is represented by the dashed line in Fig. [2.](#page-2-2)

This raises the question of how the different sensitivities induced by nonlinearity and free-running frequencies affect mutual synchronization. In previous research, it has been assumed that all nodes are identical, and the open-loop free-running frequencies have been calibrated in the measurements. However, it is critical to reevaluate the validity of this assumption in order to couple more nodes or to use a more nonlinear VCO frequency response. Considering [\(1\)](#page-2-1) and (2) , it becomes apparent that the dynamics of the LF with $K_{LF}(s)$ has not been considered. These expressions only consider the static case $K_{LF}(s = 0)$, which is similar to the hold range in conventional PLL theory [\[42\]](#page-10-36), [\[64\]](#page-11-16), [\[65\]](#page-11-17). However, as known from this theory, dynamics must be taken into account for initial synchronization.

The *hold range* refers to the frequency range $\Delta \omega_H$ of the input signal, in which the PLL can maintain phase synchronization with the input signal and keep the output stable. Within this particular range, the PLL can maintain successful phase synchronization with the input signal. However, it is not necessarily possible for the PLL to achieve initial synchronization within this range. To achieve successful initial synchronization, lock range must be considered. The *lock range*, also known as *capture range*, defines the frequency range $\Delta \omega_L$ of input signals within which the PLL can detect, track, and synchronize with the frequency of an input signal $[64]$, $[66]$, $[67]$, $[68]$. Note that in some literature, the *lock range* refers to the entire range within which a PLL can in principle be locked and pulled by an input signal. In this article, however, the term *hold range* is used to describe this entire range. In contrast, *lock range* is used exclusively used to describe the range within a PLL can achieve initial lock to an input signal.

According to [\[64\]](#page-11-16), the hold range $\Delta \omega_{H,k}$ and lock range $\Delta \omega_{L,k}$ of node *k* are given by the intervals

$$
\Delta \omega_{\mathrm{H},k} = \omega_{0,k} \, \mathrm{N}^{-1} \, \pm \, \mathrm{K}_{\mathrm{VCO},k} \, \mathrm{A}_{\mathrm{PD}} \, \mathrm{K}_{\mathrm{LF}}(0),\tag{3}
$$

$$
\Delta \omega_{\text{L},k} = \omega_{0,k} \, \text{N}^{-1} \, \pm \, \text{K}_{\text{VCO},k} \, \text{ApD} \, \text{K}_{\text{LF}}(\Delta \omega_{\text{L},k}). \quad (4)
$$

Both ranges are centered around the divided free-running closed-loop frequency $\omega_{0,k} N^{-1}$ of the node *k* and are given by the normalized PD phase error transfer function $\Delta(\cdot) \in$ $[-1, 1]$ and factors $K_{VCO,k}$ Ap_D $K_{LF}(\cdot)$.

The complex nonlinear nature of a PLL makes it challenging to find an accurate analytical expression for the lock range. To estimate $\Delta \omega_{L,k}$, the bandwidth and the dynamical response of the PLL can be approximated using the time constant τ_c of the LF $[64]$, $[66]$. For the dynamical response of the PLL node, the open-loop $H_{OL,k}(s)$ and closed-loop $H_{CL,k}(s)$ transfer functions are considered

$$
H_{FF,k}(s) = K_{VCO,k} s^{-1} A_{PD} \triangle' K_{LF}(s),
$$
 (5)

$$
H_{OL,k}(s) = H_{FF}(s) N^{-1},
$$
\n(6)

$$
H_{CL,k}(s) = H_{FF}(s) (1 + H_{OL,k}(s))^{-1}.
$$
 (7)

Here, *s* denotes the Laplace variable, Δ' is the derivative of $\Delta(\Omega_{\text{NET}}, \tau_{\text{delay},ki}, \varphi_{\text{mode},ki})$ at a given steady state, and $K_{LF}(s)$ the impulse response of the LF in Laplace domain. For the case studied, a cascaded second-order RC low-pass filter is used, the impulse response in the Laplace domain is given by

$$
K_{LF}(s) = \left(1 + 3 s \tau_{LF} + (s \tau_{LF})^2\right)^{-1}.
$$
 (8)

The dynamic behavior of the PLL system is shown in Fig. [3.](#page-3-0) Two scenarios have been studied for the dynamic response. In the first case, the cascaded second order RC LF

FIGURE 3. Numerical results of [\(](#page-3-1)[6](#page-3-1)**[\)](#page-3-1) and [\(](#page-3-1)**[7](#page-3-1)**[\)](#page-3-1) in the case of a cascaded second order RC LF characteristic [\(](#page-3-2)**[8](#page-3-2)**[\)](#page-3-2) with** *τ***LF of 149.6ns and with KLF***(***0***)* **of** 1**. The corresponding hold** *f***^H***,^k* **and lock** *f***^L***,^k* **ranges are indicated by markers. The model parameters are KVCO***/***²***^π* **of** 757.46 MHz V−¹**, APD of** 0.8 V**, - of** 1**, and N of** 512**.**

of [\(8\)](#page-3-2) with a time constant τ_{LF} of 149.6 ns was used. In the second case, the steady state gain of the LF was considered with $K_{LF}(0)$ set to 1. The model parameters used for this analysis correspond to the experimental setup used later, the VCO sensitivity K_{VCO} is 757.46 MHz V⁻¹, the PD output amplitude A_{PD} is 0.8 V, and the frequency division factor N is 512. The analysis of the dynamic response focused on the frequency range until the magnitude crosses 0 dB. For the scenario using $K_{LF}(0)$, this range is 1.18 MHz, while including the dynamics of the LF $K_{LF}(s)$ results in a range of 627.6 kHz. The results show a significant dependence of the lock range on the LF characteristics. Neglecting these dynamics leads to an inaccurate representation of the range in which the initial synchronization occurs. For example, in the studied parameter set in Fig. [3,](#page-3-0) the hold range is about twice as large as the lock range. Note that, any type of LF can be used, and this study is not limited to second-order LFs.

A stable synchronized state is defined by the fact that the frequencies of all nodes in the network are identical. From [\(2\)](#page-2-3) or [\(1\)](#page-2-1) it follows that the range of these synchronized states can only be within the hold range. Outside this area no synchronized states can exist, since the PLL can not operate within this range. For the initial synchronization it is of crucial importance to consider the lock range. It defines the frequency range in which a PLL can detect, track and synchronize to an input signal. As shown before, the lock range depends significantly on the characteristics of the LF. Therefore, the following conditions must be met for initial synchronization

$$
\bigcap_{i=1}^{M} \Delta \omega_{L,i} \neq \emptyset,
$$
\n(9)

where M is the number of nodes and $\Delta \omega_{L,i}$ is the lock range of the *i*-th node. Note that the lock range $\Delta \omega_{L,i}$ is a continuous range of frequencies.

The numerical results of (2) for stable synchronized states of two mutually delay-coupled nodes with identical and detuned free-running VCO frequencies $2\pi f_{0,k} = \omega_{0,k}$ are shown in Fig. [4.](#page-4-1) For the numerical calculation, the hybrid

FIGURE 4. Numerical results of [\(](#page-2-3)[2](#page-2-3)[\)](#page-2-3) for the network frequency $2\pi f_{\text{NET}} = \Omega_{\text{NET}}$ of stable **synchronized states for two identical and detuned mutually delay-coupled PLL nodes as a function of the coupling time delay** *τ***delay. The hold** *f***^H***,^k* **and lock ranges** *f***^L***,^k* **for each node** *k* **are shown on the right. The model parameters are listen in Fig. [3.](#page-3-0) In case of detuned nodes, the detuning** $f_{0,A} - f_{0,B}$ **is 582.05MHz.**

FIGURE 5. Numerical results of [\(](#page-2-3)[2](#page-2-3)[\)](#page-2-3) for the network frequency $2\pi f_{\text{NET}} = \Omega_{\text{NET}}$ of stable **synchronized states for two mutually delay-coupled PLL nodes as a function of the frequency detuning** *f***⁰***,***^A −** *f***⁰***,***B. The model parameters are given in Fig. [4.](#page-4-1) The hold range of each node is shown in shaded colors, and the lock range is indicated by dotted lines.**

root solver of SciPy [\[69\]](#page-11-21) is used and the initial guess for the phase difference is varied with 200 points in the interval $(0, 2\pi]$. The hold ranges $2\pi \Delta f_{H,k} = \Delta \omega_{H,k}$ for both nodes *k* are shown in shaded colors and the lock range $2\pi \Delta f_{L,k}$ = $\Delta \omega_{L,k}$ is indicated by dotted lines. The shaded area on the right side of the diagram represents the hold range, while the solid bar represents the lock range of each node. For identical $f_{0,k}$, all operating ranges intersect, resulting in stable synchronized states for almost all analyzed delays up to 65 ns. If the difference between $f_{0,A}$ and $f_{0,B}$ is 582.05 MHz, the two lock ranges still intersect. Stable synchronization can only be achieved for states within the intersecting hold range, denoted by the black markers. In contrast to the identical node, the presence of heterogeneity prevents the observation of a synchronized state for time delays that have a stable synchronized state outside the intersecting domain. This can be seen, for instance, in delay intervals ranging from 20 ns to 22.5 ns or 52 ns to 55 ns.

To answer the question of where a stable synchronized state cannot be achieved, the detuning between the freerunning closed-loop frequencies $f_{0,A} - f_{0,B}$ is increased. Therefore, the numerical results of (2) are given in Fig. [5.](#page-4-2) As the focus is not on the time delay dependence of stable synchronized states, all found states are assigned to the corresponding detuning value $f_{0,A} - f_{0,B}$ for delays up to 65 ns. The previous observation is consistent with the results

FIGURE 6. Block diagram of the PLL node for mutual synchronization. Here only one input and output channels of the PLL are used, all other unused channels are disabled and marked by gray dots.

shown in Fig. [5.](#page-4-2) The intersecting hold ranges of the two PLL nodes define the range in which synchronized states can be found. When the detuning of the free-running frequency becomes large and the hold ranges no longer intersect, no synchronized states can be found. In the analyzed case, this occurs for frequency detuning $f_{0,A} - f_{0,B}$ greater than 1.21 GHz, which is the intersecting hold range $\Delta f_{H,A} \cap \Delta f_{H,B}$. However, [\(2\)](#page-2-3) does not include the previously discussed constraint [\(9\).](#page-3-3) According to this constraint, there should be no stable synchronized state for initial synchronization outside of the intersecting lock range intervals *f*L,A∩*f*L,B. This corresponds to a frequency difference greater than 642.65 MHz.

This theoretical analysis reveals the key finding that understanding mutual synchronization in the presence of frequency heterogeneity depends on recognizing how frequency detuning affects the hold and lock regions differently. These effects depend on the nonlinearity of the frequency response and the dynamics of the loop filter. It is important to note that the intersection of the hold regions defines the range of possible synchronized states, while the intersection of the lock regions indicates where the initial synchronization occurs. These findings underscore the need to consider the dynamic interaction of the loop filter for accurate evaluation of initial synchronization. Note that an intersection of the lock ranges is only necessary for the initial synchronization, once the nodes are synchronized to a particular state, a change of $f_{0,A} - f_{0,B}$ may not affect whether the initial synchronization is successful or not, but only the observed frequencies and phase differences of the synchronized state.

III. PLL DESIGN AND MEASUREMENT SETUP

To validate the theoretical considerations, PLL nodes have been designed that allow control of the free-running closedloop frequency. A comprehensive presentation of these PLL nodes is given in [\[39\]](#page-10-33), [\[40\]](#page-10-34), [\[41\]](#page-10-35), [\[42\]](#page-10-36) and [\[43\]](#page-10-37). The block diagram of the PLL node is depicted in Fig. [6.](#page-4-3) In principle, the PLL node is based on a conventional PLL architecture. However, to enable coupling with multiple nodes, the frequency-divided feedback signal is used as the coupling signal *v*out. In larger networks, multiple XORbased PDs are used in parallel, and their outputs are combined and weighted before being fed into the loop

FIGURE 7. Photograph showing the high-frequency board containing all PLL node functionality. The PCB size is 120mm × 120mm.

filter. In the case studied, only one channel is used. An Analog Devices AD8000 high-speed operational amplifier is used for combination of multiple channels. To change the free-running frequency of the PLL node, an additional timeconstant voltage is applied during the measurement. This voltage V_{bias} is generated by a digital-to-analog converter (DAC) MCP48FEB21 from Microchip Technology with an external precise voltage reference MAX6103 from Analog Devices. A cascaded second-order RC low-pass filter with a time constant τ_{LF} of 149.6 ns is used to filter the control signal. Since this voltage provides insight into the loop dynamics, it can be measured via an additional buffer amplifier MAX4450 from Analog Devices. This buffer has a bandwidth of about 200 MHz to avoid influencing the loop. The VCO HMC739 from Analog Devices operates at frequencies around 24 GHz, and the frequency divider HMC988 from Analog Devices has a factor N of 512 . A photograph depicting the printed circuit board (PCB) with the complete PLL functionality is shown in Fig. [7.](#page-5-0) For the measurements, a second PCB is mounted on top, which is dedicated to provide the power supply.

For the experimental measurement setup, the two PLL nodes are mutually coupled via a programmable time delay board. This board allows the simultaneous enabling and disabling of the coupling paths and the setting of the delay between the PLLs in a range from 11.3 ns to 52.2 ns in increments of 10 ps. The programmable delay board can be configured at run time using a USB interface. Differential low-voltage positive emitter-coupled logic (LVPECL) signals are used to maintain signal integrity, and traces on both the PLL node and the delay board are length-matched. Four cascaded low-jitter delay line SY89295 from Microchip Technology are used per channel. Experiments are conducted in a controlled laboratory environment with temperaturemonitored PCBs to ensure stable conditions. Prior to data collection, a calibration process matches programmable digital delay settings to measured time delays to ensure accuracy.

Two main studies are done to determine the maximum allowable detuning between the nodes. First, the detuning between the nodes is analyzed as a function of the time delay. Second, for a given time delay, the synchronization process

FIGURE 8. The measurement setup with two mutually delay-coupled PLL nodes connected via a programmable delay. The divided cross-coupling frequency, phase difference between the nodes and the tuning voltages are measured with an oscilloscope (Scope 1), while the high-frequency waveforms are captured with a wideband oscilloscope (Scope 2).

FIGURE 9. Photo of the measurement setup in the laboratory where two nodes are mutually coupled using a programmable delay board.

is analyzed as a function of the initial phase difference at the time where the coupling is activated. The first measurement provides information about possible synchronized states, while the second provides information about the probability that a synchronized state will occur in the case of detuning.

A sketch of the measurement setup is presented in Fig. [8.](#page-5-1) To characterize and validate the synchronization process and its synchronized states, the output waveforms v_{out} used for coupling, the tuning voltage v_{tune} and the VCO output frequencies *f*_{VCO} of each node are captured. Using the automated measurement function of the Rohde & Schwarz RTO 1044 Scope 1, the frequency f_{NET} and phase difference $\Delta \varphi_{AB}$ between nodes are extracted. In order to detect whether a synchronized state is unstable, the frequency f_{tune} and peak-to-peak voltage $v_{\text{tune, pp}}$ of the tuning voltage are also measured. In the case of a stable synchronized state, *v*tune,pp and *f*tune are ideally zero. To study the synchronization process, the time dependence of all waveforms is recorded during this process. For this purpose, a trigger signal is used which is generated by the programmable delay board when coupling is activated. These waveforms are subsequently analyzed to determine the instantaneous frequency and phase difference during the transient response. The spectra of the two VCOs are obtained by performing a fast Fourier transform (FFT) on their highfrequency waveforms. These waveforms are recorded using the Keysight UXR0702 wideband oscilloscope (Scope 2). Fig. [9](#page-5-2) shows a photo of the measurement setup in the laboratory.

FIGURE 10. Measurements of the hold and lock ranges for a free-running closed-loop frequency of 24.0GHz. The light shaded area indicates the hold range and the dark shaded area indicates the lock range.

FIGURE 11. Measurements of the hold range (shaded) and the lock range (solid) for different free-running lock frequencies *f***⁰ of a PLL node. The hatched area indicates detuning values up to which [\(](#page-3-3)**[9](#page-3-3)**[\)](#page-3-3) is not valid, assuming that the nominal free-running closed-loop frequency is 24.0GHz.**

IV. MEASUREMENTS

In the following, the detuning of the free-running PLL frequencies and its effect on the mutual synchronization will be experimentally studied. Before starting measurements with mutually coupled nodes, it is necessary to determine the actual hold and lock ranges of the individual PLL nodes. As described in Section [II,](#page-1-0) changes in V_{bias} will change the center frequency f_0 and the sensitivity K_{VCO} of the oscillator. This results in different relative hold and lock ranges of the PLL node. To identify these ranges, a PLL node is unidirectionally entrained by a reference frequency *f*_{REF}, as in conventional PLL operation. In this case, a Keysight 81150A function generator as reference is used. To determine the hold range, the reference frequency is continuously swept between 42 MHz and 50 MHz. While sweeping, the reference frequency f_{REF} the output frequency of the v_{out} waveform of the PLL node is captured.

An example of the hold and lock range measurements for a free-running closed-loop frequency of 24.0 GHz is shown in Fig. [10.](#page-6-1) Depending on the direction of the sweep of f_{REF} , the upper or lower limit of the hold range is determined. If both frequencies are identical, the PLL is locked to this frequency and the hold range can be determined. Changing the direction of the sweep is necessary since the PLL is not synchronized until the reference frequency *f*_{REF} enters the lock range. Since the input signal is continuously sweep and the PLL is synchronized to this input signal, the PLL frequency can be pulled out of the lock range by changing this reference frequency. In the case of the lock range, the reference is switched on and off between each increment of the sweep, so that it can only be detected if the PLL can capture and lock initially to the reference signal. The lock range is smaller than the hold range, and a sharp transition between the two ranges cannot be observed.

The measured operating ranges for various free-running closed-loop frequencies f_0 are plotted in Fig. [11.](#page-6-2) The hold range is a shaded and the lock range is a solid bar. The plot shows that changes in *f*⁰ have a significant effect on the relative width of both the lock and hold ranges, due to the nonlinear VCO sensitivity $K_{VCO,k}$. For instance, if the free-running frequency f_0 is 23.13 GHz, the relative lock

range is 2.04 MHz , and for f_0 at 24.45 GHz it decreases to 1.22 MHz. From these measurements the maximum detuning $f_{0,A} - f_{0,B}$ can be identified. For a nominal free-running closed-loop frequency of 24.0 GHz, the lock ranges intersect if the detuning in frequency is not greater than about \pm 350 MHz or \pm 1.46 %.

The next step is to study the effect of frequency differences on mutual synchronization. Therefore, the first measurement setup described in Section [III](#page-4-0) is used. In this setup, two nodes are calibrated to operate at 24.0 GHz by adjusting a parameter called V_{bias}. To compare and evaluate the effects of detuning, this scenario is used as a reference without detuning. In Fig. [14,](#page-8-0) the measured network frequency f_{NET} of synchronized states is compared with numerical results obtained from [\(2\)](#page-2-3) for different detuning values. During this measurement, the time delay τ_{delay} is increased linearly from 11.3 ns to 52.2 ns. Before each incremental step, the coupling between nodes is temporarily turned off. This ensures that the synchronization process is restarted and that any potentially effects resulting from the transition to a state within the hold range of a previous state are suppressed. To better understand the intersection of the operating ranges of both nodes, the right side of each graph shows the hold range as a shaded bar and the lock range as a solid bar.

Without detuning, as shown in Fig. $12(a)$ $12(a)$, synchronization is observed for all studied time delays. The experimental measurements match the numerical results for stable synchronized states very well. However, synchronization becomes difficult to achieve for certain time delays when detuning is introduced. This can be seen by the fact that the potential synchronized state, which would have fallen within the intersection range without detuning, is now outside this range due to detuning. For example, in Fig. $12(b)$ $12(b)$, with a detuning of $f_{0,A} - f_{0,B}$ of 372.1 MHz, synchronization cannot be achieved in the time delay range of 20 ns to 23 ns. However, as the detuning increases to 416.2 MHz, shown in Fig. [12\(](#page-7-0)e), the range in which no synchronized states are observable expands. Furthermore, in intervals where synchronization was previously possible, there is no apparent evidence of consistently synchronized states.

FIGURE 12. Measurement and numerical results obtained from [\(](#page-2-3)[2](#page-2-3)**[\)](#page-2-3) of the network frequency** *f***NET of synchronized states for different detuning values for increasing cross-coupling time delays** *τ***delay. In case of (a) no detuning, a detuning** *f***⁰***,***^A −** *f***⁰***,***^B of (b) 372.1MHz, (c) 416.2MHz, (d) 528.1MHz, and (e) 636.3MHz. The standard deviation of each measured trace is shown in shaded colors.**

Certain states may appear stable (e.g., between 34 ns and 36 ns), while others may not (e.g., between 36 ns and 41 ns). This phenomenon increases with increasing detuning, as seen in Fig. $12(d)$ $12(d)$ for $f_{0,A} - f_{0,B}$ of 528.1 MHz. In this case, the intersection of the lock range is only 191 kHz. There are no longer any observable unambiguously synchronized states, and the numerical results of (2) only suggest a range in which

FIGURE 13. Measured normalized power spectral densities (PSD) output for both mutually coupled PLL nodes at a time delay *τ***delay of 49.68ns. In case of (a) no detuning** and (b) a detuning $f_{0,A} - f_{0,B}$ of 528.1MHz.

the mutually delay-coupled nodes react in an undefined manner. At the detuning shown in Fig. $12(a)$ $12(a)$, the range is greater than (9) , the range where the lock ranges of both nodes overlap. No synchronized state can be observed in the measurements at this detuning of 636.3 MHz. The measured network frequencies of the two nodes do not overlap for any time delay. The numerical solutions of (2) for stable synchronized states are not visible in the measurement. Comparing the holding ranges of both nodes in Fig. $12(e)$ $12(e)$, it is noticeable that the range of states obtained from numerical result agrees well with the intersecting hold range.

The power spectral densities (PSDs) of the high-frequency VCO output of both nodes are shown in Fig. [13.](#page-7-1) When there is no detuning in Fig. $13(a)$ $13(a)$, the PLL nodes synchronize, and the frequencies of both oscillators are identical. Side peaks in the spectrum are due to signal cross talk from the PD output to the tuning voltage. With a detuning of 528.1 MHz in Fig. $13(b)$ $13(b)$ the lock ranges of the nodes intersect, but no stable synchronization can be achieved. The output spectra of the PLL nodes show an oscillation on v_{tune} .

The previous measurement reveals how the self-organizing synchronization behaves over the time delay τ_{delay} between the nodes. A stable, synchronized state also depends on the initial phase difference $\Delta \varphi_{AB,\text{init}}$ at which the coupling between the nodes is activated $[40]$. In the following, the dependence of this initial phase difference on the detuning *f*_{0,A} −*f*_{0,B} for a fixed time delay of 49.68 ns is analyzed. For this purpose, the basin of attraction of a synchronized state is depicted in a phase portrait. Since the phase difference between two uncoupled oscillators of different types is randomly distributed, the synchronization process for varying initial phase differences can be observed by a series of measurements. The vertical axis of each subplot in Fig. [14](#page-8-0)

FIGURE 14. Phase portrait of the basin of attraction of a synchronized state using the instantaneous frequency difference $\Delta\dot{\varphi}_{AB}$ over the phase difference $\Delta\varphi_{AB}$ between **two mutually coupled nodes for a time delay** *τ***delay of 49.68ns with 200 measurement** samples. In case of (a) no detuning, a detuning $f_{0,A} - f_{0,B}$ of (b) 372.1MHz, **(c) 416.2MHz, (d) 528.1MHz, and (e) 636.3MHz.**

displays the instantaneous frequency difference $\Delta\dot{\varphi}_{AB}$, while the horizontal axis shows the instantaneous phase difference $\Delta\varphi_{AB}$ between nodes during the synchronization process. The trajectories illustrate the progression of the system from an initial point to an attractor, which in this context represents a synchronized state. If the system converges asymptotically to this attractor, its momentum will be zero. However, if this convergence does not occur, the system will oscillate and its momentum will persistently deviate from zero.

The measurement of the synchronization process in Fig. [14](#page-8-0) illustrates how detuning impacts the synchronization for a fixed time delay τ_{delay} of 49.68 ns between nodes. In Fig. [14\(](#page-8-0)a), all initial phase differences result in a synchronized state with a phase difference $\Delta \varphi_{AB}$ of 10°. However, increasing the detuning $f_{0,A} - f_{0,B}$ leads to unstable behavior, which affects the range of initial values that result in synchronized states. For example, in Fig. [14\(](#page-8-0)b), unstable behavior occurs within the 16◦ to 145◦ range, while all other initial values converge to a stable synchronized state with a phase difference $\Delta \varphi_{AB}$ of 39°. The overlapping lock range decreases from 100% at Fig. [14\(](#page-8-0)a) to 53.48% at Fig. [14\(](#page-8-0)b). This behavior continues with increasing detuning, with decreasing intervals leading to stable synchronized states, as shown in Fig. $14(c)$ $14(c)$ and Fig. $14(d)$. In these cases, the overlapping lock range is 41.56 % and 11.17 %, respectively. In Fig. [14\(](#page-8-0)e), the detuning exceeds $\Delta f_{\rm{LA}} \cap$ Δf_{LB} resulting in only unstable states. Moreover, it is notable that the phase difference, which can be associated with in-phase synchronization, drifts to larger values with increasing detuning of $f_{0,A} - f_{0,B}$. The unstable behavior cannot be attributed to a synchronized state since these trajectories do not converge. It is important to note that the instantaneous frequency difference $\Delta \dot{\varphi}_{AB}$ will increase as the detuning of the free-running closed-loop frequencies increase further. During the sweeping of the detuning, the probability of reaching a stable synchronized state decreases from 73.5 % at a detuning of 372.1 MHz to 24.5 % at a detuning of 528.1 MHz and finally to 0% at a detuning greater than 636.3 MHz. Note that this decreasing probability of occurrence of a synchronized state is consistent with the effect of unclear behavior for predicted synchronized states observed in Fig. $12(c)$ $12(c)$ and Fig. $12(d)$.

This study focuses primarily on investigating the influence of frequency detuning between nodes. To validate the maxi-mum allowable detuning as determined by the constraint [\(9\),](#page-3-3) a parameter sweep of the frequency detuning $f_{0,A} - f_{0,B}$ was performed. At each incremental step of this sweep, the time delay between nodes is linearly varied in the range of 11.3 ns to 52.2 ns to capture all possible synchronized states. Each achieved synchronized state is then associated with its corresponding detuning value and visualized in Fig. [15.](#page-9-5) This analysis reflects closely the theoretical investigation previously performed in Fig. [5.](#page-4-2) Determining whether a state is stable or not depends on two criteria: the frequency difference between nodes must be less than 1 kHz, and the tuning voltage of each node must remain constant over time. The results of this investigation clearly indicate that a stable synchronized state is only attained when the frequency detuning $f_{0,A} - f_{0,B}$ satisfies the condition $\Delta f_{L,A} \cap \Delta f_{L,B}$. The maximum theoretical value for the frequency detuning is 642.65 MHz for the case studied. The measured value of about 582.12 MHz falls below the theoretical limit due to the nonlinear characteristics of $K_{VCO,k}$ and its effect on the hold

FIGURE 15. Measured network frequency f_{NET} of synchronized states for time **delays** *τ***delay between 11.3ns to 52.2ns as a function of the frequency detuning** $f_{0A} - f_{0B}$ between nodes.

and lock range as described in Section [II.](#page-1-0) For comparison, the value of the maximum detuning between two PLL nodes obtained from [\(2\)](#page-2-3) is 1.21 GHz, which is significantly larger than the value obtained from the [\(9\)](#page-3-3) constraint or from measurements.

V. CONCLUSION

This work analyzes the effect of different open-loop free-running frequencies on the self-organized mutual synchronization of phase-locked loop (PLL) nodes. Due to the absence of a reference, a synchronized state results from the dynamics of the PLL nodes and the network, including the network topology and the time delay between nodes. Previous research has proposed a theoretical framework for finding steady state synchronized states. This framework includes the nonlinear characteristics of the oscillator frequency response. To estimate the sensitivity of different oscillator characteristics to each other, the nonlinear frequency response is linearized. It can be seen that a variation in the response of the oscillator has a direct effect on the free-running frequency and the sensitivity of the PLL. Moreover, this framework does not consider the dynamic behavior of the PLL nodes during initial synchronization. It only considers the range in which the PLL can maintain synchronization. This corresponds to the hold range in conventional PLL theory. In this work, a constraint is proposed that takes into account the dynamic behavior of the loop filters and thus allows statements to be made about the range in which initial synchronization can occur. To achieve initial synchronization, this constraint requires that the lock ranges of each PLL node in the network intersect. Therefore, this constraint results in limiting the maximum allowable difference in open-loop free-running frequencies between PLL nodes.

To experimentally study the effects of the nonlinear characteristic as well as the effects of different free-running frequencies, two mutually time-delayed coupled 24 GHz PLL nodes were used. The maximum frequency detuning was analyzed over time delays between nodes of up to 52.2 ns. This analysis confirms the theoretical maximum detuning between free-running frequencies found using the constraint.

Furthermore, the basin of attraction of synchronized states were analyzed for different detuning values. It was found that detuning not only affects the delay range in which stable synchronized states emerge, but that detuning also limits the range of the initial phase difference at the beginning of the coupling that lead to a stable synchronized state. In the case investigated, the probability of achieving a stable synchronized state through self-organized synchronization was reduced to 73.5 % when the frequency difference of the free-running closed-loop frequencies of the PLLs was 372.1 MHz or 1.56 %, and no stable synchronization could be achieved at a frequency difference of 642.65 MHz or 2.65 %. Furthermore, it can be seen that detuning does not only affect the initial phase difference leading to a stable synchronized state. It also affects the phase difference between nodes in a stable synchronized state.

The theoretical and experimental validation of this condition showed that it should be considered as a guideline for the implementation of mutual coupling to achieve stable synchronization. In general, the detuning of the freerunning closed-loop frequencies of the PLL nodes must be analyzed with respect to the hold and lock range for the desired application and the time delay between the nodes. An overlapping lock range of less than 50 % leads to unwanted unstable behavior in the case analyzed in this work. In further design considerations, especially for larger networks with integrated PLL nodes, it is recommended to implement compensation methods for process, voltage and temperature (PVT) variations of the oscillator, especially for changes in frequency response and sensitivity. Other possibilities could be a very linear tuning behavior of the oscillator or several tuning inputs for improved control of the oscillator. Nevertheless, the present work provides valuable insights into the complex self-organizing dynamics of coupled oscillators that are useful for future research, e.g., for applications with phase-locked loop used for timing synchronization in localization and multi-sensor systems.

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