Analysis of Discrete-Time Integrating Amplifiers as an Alternative to Continuous-Time Amplifiers in Broadband Receivers

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ABSTRACT Recent advancements in low power and low noise front-end amplifiers have made it possible to support high-speed data transmission within the deep roll-off regions of conventional wireline channels. Despite being primarily limited by inter-symbol-interference (ISI), these legacy channels also require power-consuming front-end amplifiers due to increased insertion-loss at high frequencies. Wireline-like broadband channels, such as proximity communication and human-body-communication (HBC), as well as multi-lane, densely-packed channels, are further constrained by their high loss and unique channel responses which cause the received signal to be noise-limited. To address these challenges, this paper proposes the use of a discrete-time integrating amplifier as a low power ($<$1pJ/b using 65nm CMOS up to 5-6 Gb/s) alternative to traditional continuous-time front-end amplifiers. Integrating amplifiers also reduce the effects of noise due to its inherent current integrating process. The paper provides a detailed mathematical analysis of gain of two conventional and three novel and improved integrating amplifiers, accurate input referred noise estimations, signal-to-noise ratio, and a comparison of the integrating amplifier's performance with that of a low-noise amplifier. The analysis identifies the most optimum integrator architecture and provides comparison with simulated results. This paper also develops theoretical expressions and provides in-depth understanding of input referred noise, while supporting them by simulations using 65nm CMOS technology node. Finally, a comparative analysis between low-noise amplifier and discrete-time integrating amplifier is presented to demonstrate power and noise benefits for both legacy and wireline-like channels, while providing an easier design space as integrator provides two-dimensional controllability for gain.

INDEX TERMS Continuous-time amplifier, discrete-time amplifier, integrating amplifier, legacy channels, low-noise amplifier, noise, transfer function, wireline-like channel.

I. INTRODUCTION

DATA rate of emerging communication devices has shown a consistent upward trend in the last few decades. Energy-efficiency has also emerged as a crucial factor for the feasibility of a design. Recent state-of-the-art transceivers have demonstrated energy efficiency of 1-10 pJ while achieving data rate of up to 256 Gb/s [1], [2], [3], [4].

Supporting higher data rates often places the Nyquist frequency of the data deep in the roll-off region of legacy channel response [1], [2], [3], [4]. As a result, different frequency components of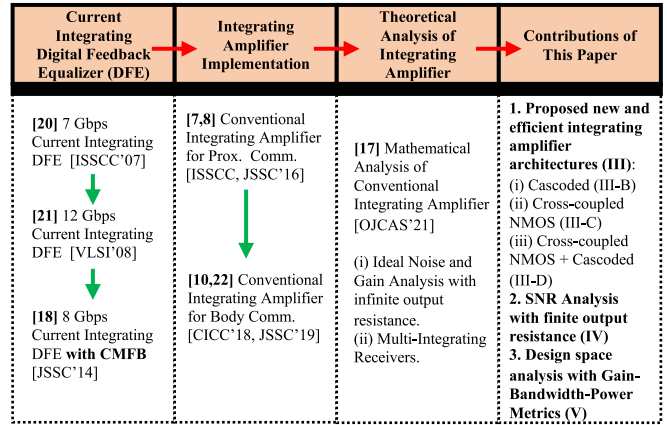 the data experience varying degrees of loss, leading to inter-symbol interference (ISI)-dominated data transmission. In this scenario, the received data eye width begins to narrow primarily due to ISI.

As most high-speed communication modules use legacy channels to transmit data, significant progress has been made in mitigating ISI-dominated received data. Decision feedback equalizer (DFE), feed-forward equalizer (FFE), and continuous time linear equalizer (CTLE) are mainly used to reduce ISI in the received signal before amplification.

It is also possible for the received signal amplitude to be comparable to the noise floor of front-end devices. In such

TABLE 1. Choosing most suitable front-end amplifier for a given channel response and data rate.

Channel Response		Most Suitable Front-End Amplifier		
Data Rate (NRZ, Single Lane)	Insertion Loss	CTLE	LNA	INT
Low(<100M)	Low(<10dB)	✗	✗	✓
Low(<100M)	High (>30dB)	✗	✓	✓
Medium(<10G)	Low(<10dB)	✗	✓	✓
Medium(<10G)	High (>30dB)	✓	✗	✓
High(>10G)	High (>30dB)	✓	✗	✓
High(>10G)	Low(<10dB)	✓	✗	✓
Very High(>30G)	High (>30dB)	✓	✗	✗

Current Integrating Digital Feedback Equalizer (DFE)	Integrating Amplifier Implementation	Theoretical Analysis of Integrating Amplifier	Contributions of This Paper
[20] 7 Gbps Current Integrating DFE [ISSCC'07] [21] 12 Gbps Current Integrating DFE [VLSI'08] [18] 8 Gbps Current Integrating DFE with CMFB [JSSC'14]	[7,8] Conventional Integrating Amplifier for Prox. Comm. [ISSCC, JSSC'16] [10,22] Conventional Integrating Amplifier for Body Comm. [CICC'18, JSSC'19]	[17] Mathematical Analysis of Conventional Integrating Amplifier [OJCAS'21] (i) Ideal Noise and Gain Analysis with infinite output resistance. (ii) Multi-Integrating Receivers.	**1. Proposed new and efficient integrating amplifier architectures (III):** (i) Cascoded (III-B) (ii) Cross-coupled NMOS (III-C) (iii) Cross-coupled NMOS + Cascoded (III-D) **2. SNR Analysis with finite output resistance (IV)** **3. Design space analysis with Gain-Bandwidth-Power Metrics (V)**

FIGURE 1. Progression of integrating amplifiers and contributions of this paper.

cases, channels become noise-limited. When channels are both noise and ISI-limited, significant power is consumed for both data amplification and ISI-correction.

Introduction of new methods of communication diversifies the requirements for a successful receiver front-end operation. Some of these newly proposed channels do not involve a physical wire to transmit data from the transmitter to the receiver. Proximity communication is a prime example of such channels where the transfer function resembles a capacitance divider circuit. A typical proximity communication channel exhibits 20-30 dB insertion loss in flat-band region [5], [6], [7], [8].

Human-Body Communication (HBC) [9], [10], [11], [12], [13], [14], [15], [16] is another emerging technology that uses the human body as a mode for transmitting signals. Although the high-frequency response of such channels is still under study, it has been shown that the channel response stays flat up to 20MHz while showing almost 70dB loss.

For these cases, a broadband signal can be used to transmit data, while taking advantage of wireline communication. This provides an opportunity to communicate data at a much lower power than wireless communication. It can be said that proximity communication, HBC, or similar lossy broadband channels fall between wireline and wireless communication in terms of channel response while showing its own identifiable characteristics.

However, high insertion loss at the flat band makes the received signal noise-limited, as the attenuated signal becomes comparable to the input-referred noise of the amplifier. If the data rate falls within the flat band region, all the significant harmonics undergo the same amount of loss. As a result, the channel does not suffer from ISI limitation.

However, these channels necessitate substantial gain (>50-60 dB) with low input-referred noise to achieve the lowest BER. Integrating amplifiers (INT) offer high gain, low input-referred noise, and consume significantly less power compared to conventional amplifiers [7], [8], [10], [17], [22]. Integrating amplifiers not only address the specific requirements of noise-limited channels

effectively but also find applicability in medium to high-speed transceivers for legacy channels. Additionally, integrating amplifiers rely on the sampler to generate discrete-time (DT) decisions based on the amplified signal. Careful execution of the sampling operation can result in lower error rates compared to conventional continuous-time (CT) amplifiers.

Table 1 demonstrates the suitability of various front-end amplifiers for specific channel responses and data rate requirements. CTLEs offer high gain but consume significant power, making them unsuitable for low-to-medium data rates. Conversely, LNAs have lower gain but are more suitable for medium-to-low data rates or when used in conjunction with other amplifiers for high data rates. Integrators are only limited by extremely low integration times and cannot provide sufficient gain for extremely high data rates. This paper analyzes and compares integrators with continuous-time amplifiers to demonstrate their relevance in all scenarios, as illustrated in Table 1.

Reference [17] demonstrates the advantages of cascading multiple simplistic integrating amplifiers in series to achieve the lowest BER for a given power consumption, based on noise and gain analysis. The study also explores the system-level benefits of combining discrete-time integrating amplifiers with continuous-time amplifiers. This motivates a detailed investigation into circuit-level analysis and enhancement of both new and conventional DT integrators, which is the primary focus of this work. The proposed study delves into the theoretical understanding of these integrating amplifiers for both legacy and noise-limited channels, providing insights into gain estimation, accurate input-referred noise, and signal-to-noise ratio through mathematical analysis.

This study's key contributions are organized into five primary sections (Sections II–VI). Section II provides a brief overview of the background and previous work in the field, including relevant theories used in subsequent subsections.

Section III focuses on the circuit-level analysis of both conventional and newly proposed integrating amplifier architectures. Various approaches to increasing gain while
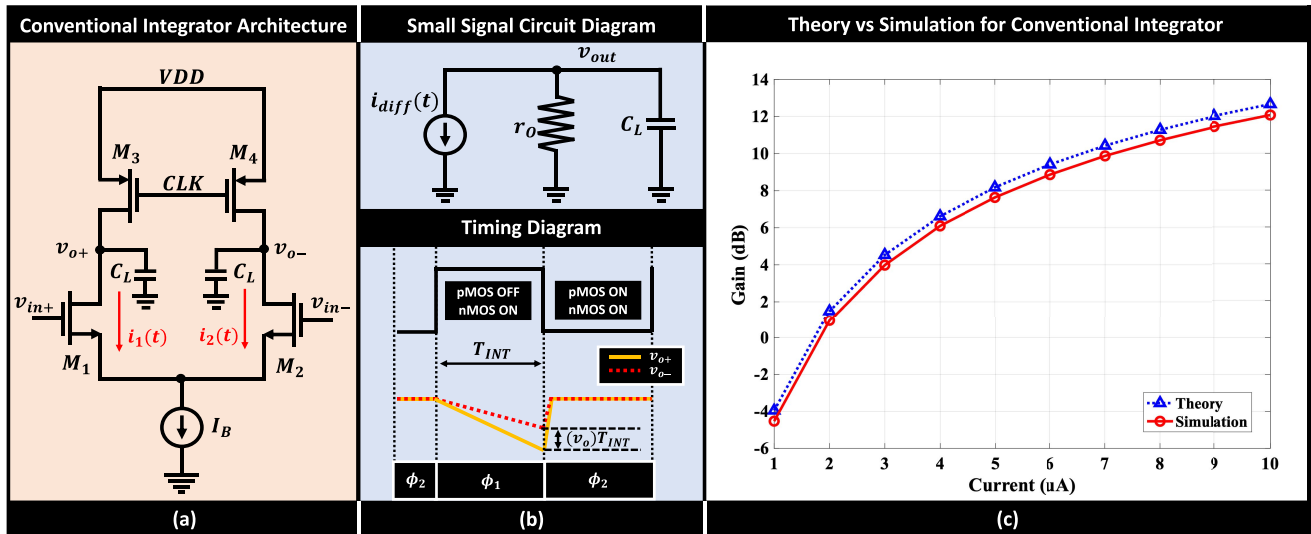
FIGURE 2. (a) Conventional integrator architecture, (b) Small signal circuit diagram of the differential half circuit and timing diagram, (c) Theory vs Simulation for conventional integrator.

maintaining constant current consumption are examined, including theoretical and simulated analysis of current source load with common mode feedback [18].

Section IV derives the input referred noise of the conventional integrating amplifier considering finite output resistance and analyzes the signal-to-noise ratio (SNR).

Section V derives and compares the gain, bandwidth, and power consumption of a conventional low-noise amplifier with self-biasing and a configuration consisting of two stages of conventional integrating amplifiers.

Finally, Section VI provides the conclusion of the paper.

II. BACKGROUND AND RELEVANT WORK

Figure 1 shows the advent of integrating amplifiers from current integrating DFEs, and progression of DT-integrator as a front-end amplifier in proximity and body communication.

Reference [20] shows the first of implementation of current integrating DFE where resistors were replaced with clock gated pMOS devices to accommodate 7Gbps data rate. Later, [21] also uses a similar architecture to design a DFE, which is operating at 12 Gbps. Both show significant power advantage over conventional DFE because of clock gating, which reduces the operation time of the DFE, thereby, reducing the total power consumption. However, having higher number of taps in these DFE architectures would result in extremely low output common mode voltage.

Reference [18] solves this issue by stabilizing the output common-mode voltage using a common-mode feedback (CMFB). The CMFB implementation sacrifices a portion of the differential current to keep the output common-mode voltage at the desired level for subsequent blocks. This architecture is suitable to support high number of taps in exchange of extra power consumption of the CMFB.

It is also shown in [18] that clock gated PMOS based architectures can provide the best energy efficiency with

respect to the number of complex taps when compared to switched-capacitor or resistor based implementations. It is observed primarily due to time-multiplexed operation of the architecture.

References [7], [8] show the first implementations of integrating amplifier as a front-end amplifier in a Proximity Communication transceiver. A conventional integrating amplifier is proposed for 32Gbps communication link at 4pJ/b energy efficiency. References [10], [22] also uses the conventional integrating amplifier architecture for 30Mbps body communication module at 6.3pJ/b energy efficiency. It shows the energy efficient implemention of integrating amplifiers for broadband wireline-like channels.

Reference [17] shows the mathematical analysis of gain for conventional integrating amplifier and proposes multi-integrating receiver (MIR), which uses multiple integrating amplifiers in series to improve the overall gain. In this paper, an idealistic estimation of noise has also been analyzed.

Although conventional integrating amplifiers show energy-efficient implementations as front-end amplifiers, there is still a scope to improve the architecture while understanding them thoroughly. So, in this paper, new and improved integrating amplifiers are proposed. Moreover, more realistic noise analysis has been covered in this paper along with a design space analysis to further showcase the efficacy.

While [17] shows the application of integrating amplifier in front-end receivers based on system-level analysis, this paper focuses on circuit level improvement of the efficiency for integrating receivers by using the proposed designs in the place of conventional integrator as done in [17].

A. SINGLE STAGE CONVENTIONAL INTEGRATOR

A conventional single-stage integrator [7], [8], [10], [22] is shown in Figure 2(a). The architecture involves two differential nMOS input transistors (M_1 and M_2) and two

pMOS transistors (M_3 and M_4), which are used to charge the output nodes to the supply voltage when the *CLK* signal is low.

The operation of the integrating amplifier can be divided into two segments. Figure 2(b) shows the working principle of integrating amplifiers. In the integration phase (ϕ_1), pMOS transistors are switched off as the *CLK* goes high. In this phase, nMOS transistors generate differential currents ($i_1(t)$ and $i_2(t)$) and discharge the output capacitance (C_L) by unequal amounts, as shown in Figure 2(b). The ratio of the output voltage difference ($v_{o+} - v_{o-}$) at the end of the integration period and the input differential voltage serves as the overall gain of the integrating amplifier.

In the charging phase (ϕ_2), the pMOS transistors turn on when the clock goes low. Although both pMOS and nMOS transistors are on in this phase, the size of the pMOS transistors is significantly higher than that of the nMOS transistors. As a result, the output nodes are charged to the supply voltage, serving as a reset phase of the integrator. The charging phase ensures that the discharge of load capacitors always starts from the supply voltage.

Reference [17] shows that the differential output voltage can be empirically determined based on the characteristics of the architecture and transistors. At the start of the integration phase, the output voltages are charged to the supply voltage. The input voltages to M_1 and M_2 are v_{in+} and v_{in-}, respectively. We can estimate the differential currents as:

$$i_1(t) = g_{m_1} v_{in+}(t) \tag{1}$$

$$i_2(t) = g_{m_2} v_{in-}(t) \tag{2}$$

In (1) and (2), g_{m_1} and g_{m_2} are the transconductances of M_1 and M_2 respectively. For a balanced architecture, both of them can be assumed to be same ($g_{m_{1,2}}$).

So, we can write the differential current expression as,

$$i_{diff}(t) = i_1(t) - i_2(t) = g_{m_{1,2}} v_{in}(t) \tag{3}$$

where, $v_{in+} - v_{in-} = v_{in}$ is the input differential voltage.

Fig. 2(b) shows the small signal model of the output node when the differential operation is considered. r_o is the output resistance of the input nMOS transistors. As the pMOS transistors are off during the integration period, they will not have any effect on the output resistance calculations.

The following expression can be written for the output node:

$$i_{diff}(t) = \frac{v_{out}(t)}{r_o} + C_L \frac{dv_{out}(t)}{dt} \tag{4}$$

Comparing (3) and (4), it can be written:

$$g_{m_{1,2}} v_{in}(t) = \frac{v_{out}(t)}{r_o} + C_L \frac{dv_{out}(t)}{dt} \tag{5}$$

Solving the differential equation shown in (5), the output voltage expression can be written as,

$$v_{out}(t) = g_{m_{1,2}} r_o v_{in} \left(1 - e^{-\frac{t}{r_o C_L}} \right) \tag{6}$$

At the end of integration period ($t = T_{INT}$), the final output voltage will be,

$$v_{out}(T_{INT}) = g_{m_{1,2}} r_o v_{in} \left(1 - e^{-\frac{T_{INT}}{r_o C_L}} \right) \tag{7}$$

So, the overall gain at the end of ϕ_1 will be:

$$A_{conv} = \frac{v_{out}(T_{INT})}{v_{in}} = g_{m_{1,2}} r_o \left(1 - e^{-\frac{T_{INT}}{r_o C_L}} \right) \tag{8}$$

This expression can be simplified for slow data rate if $e^{-\frac{T_{INT}}{r_o C_L}}$ is expanded using Taylor series expansion. Simplifying (8) would result in:

$$A_{conv} = \frac{g_{m_{1,2}} T_{INT}}{C_L} \tag{9}$$

However, equation (8) has been used to calculate the theoretical estimation of the gain for the conventional integrator architecture shown in Figure 2(c). The integrator was designed to operate at a 100 MHz clock frequency with an input differential peak-to-peak voltage of 8 mV, and the output capacitance was kept at 100 fF. The simulated gain was compared with the theoretical estimation while the bias current (I_B) was changed from $1\mu A$ to $10\mu A$.

Figure 2(c) shows that the theoretical and simulated results match consistently throughout the current range. The deviation at higher current values arises when the nMOS devices fall into the linear region and are no longer in the saturation region.

However, Figure 2(c) solidifies that equation (8) can be used in the later sections to compare the conventional integrator with other integrating amplifier architectures.

For a conventional integrating amplifier, the final output common-mode voltage is also a crucial parameter to operate the subsequent blocks in the data chain. For example, a Strong-ARM latch would require an input common-mode voltage of $0.7 V_{DD}$ for the most optimum operation [19].

During the integration phase, a common-mode current of $I_B/2$ is flowing through the M_1 and M_2 nMOS transistors at all times, as shown in Figure 2(a), and discharging the load capacitors C_L. The integrating phase (ϕ_1) is active for a duration of T_{INT}. As the output nodes are charged to supply voltage (V_{DD}) during charging phase(ϕ_2), the final common mode output voltage at the end of integration will be:

$$V_{CM} = V_{DD} - \frac{I_B T_{INT}}{2 C_L} \tag{10}$$

When M_1 and M_2 are no longer in the saturation region of operation, the output differential voltage and gain do not significantly change after that. It can be assumed that the nMOS transistors go out of saturation when the drain voltage is $V_{D_{min}}$. Hence, the maximum current for which the common-mode voltage reaches the marginal value can be found using (10), and can be written as:

$$I_{B_{max}} = \frac{2 C_L}{T_{INT}} \left(V_{DD} - V_{D_{min}} \right) \tag{11}$$

Using, (9) and (11), the maximum gain for the marginal case will be given by:

$$A_{max} = \frac{2g_{m_{1,2}}}{I_{B_{max}}}\left(V_{DD} - V_{D_{min}}\right) = \frac{g_{m_{1,2}}}{I_D}\left(V_{DD} - V_{D_{min}}\right) \quad (12)$$

where, I_D is the current flowing through each transistor ($I_D = I_{B_{max}}/2$). Equation (12) shows that the maximum differential gain can be achieved when the input common mode voltage is kept low to achieve the highest g_m/I_D ratio, and $V_{D_{min}}$ of the input transistors is reduced. However, there is scope to improve the architecture of discrete-time integrating amplifiers to improve effective trans-conductance and output resistor of the overall amplifier for maximum current efficiency. Hence, this paper focuses on three improved and novel architectures to increase the overall gain based on the expressions, which are derived in this subsection.

B. INPUT REFERRED NOISE FOR CONVENTIONAL INTEGRATING AMPLIFIERS

In [17], a time domain analysis of conventional integrating amplifiers and Strong-ARM latches is presented, utilizing the ergodicity property of thermal noise. As the primary noise-contributing stage of the Strong-ARM latch is exactly the same as that of an integrating amplifier, both analyses can be performed simultaneously.

Figure 2(a) depicts the circuit diagram of the conventional integrating amplifier, where the nMOS transistors M_1 and M_2 are the only contributors to thermal noise, as the pMOS transistors are off during the integration phase (ϕ_1). The differential output noise voltage can be determined if the integrator stores the entirety of the differential noise current ($i_n(t)$) into the output capacitance. For simplicity, this analysis assumes that the output resistance is infinite. Thus, the output differential noise voltage can be expressed as:

$$v_{o_n} = \frac{1}{C_L}\int_0^{T_{INT}} i_n(t)dt \quad (13)$$

where $i_n(t)$ is the differential noise current, which can be assumed as: $i_n(t) = A\sin(2\pi ft + \phi)$. A is the amplitude of the noise current, f is the frequency, and ϕ is the initial phase of the noise current. It can be said that the probability spectral density of noise can be given as: $PSD = 8kT\gamma g_{m_{1,2}}$. Hence, the integral in (13) would result in,

$$v_{o_n} = \frac{A(\cos(\phi) - \cos(2\pi fT_{INT} + \phi)))}{2\pi fC_L} = \frac{A}{C_L}TF_\phi(f) \quad (14)$$

The multiplication factor $TF_\phi(f)$ in equation (9) depends on the initial phase, integration time, and frequency of the noise. It is crucial to consider all possible frequencies and phases to accurately estimate the output noise voltage. In this analysis, worst-case estimation of $TF_\phi(f)$ is used.

Reference [17] shows the variation of $TF_\phi(f)$ over the frequency range for different initial phases (ϕ) of the thermal noise when the integration phase lasts for $10ps$. Since the noise can have any combination of frequency and phase

during the integration phase, a pessimistic approximation would be to only consider the maximum values of $TF_\phi(f)$. This maximum value is shown in [17]. This has been further shown as a single case in fig. 8(b) where $RC = \infty$. Hence, we can write that $max(TF_\phi(f)) = TF_{env}(f)$.

The rms value of the amplitude can also be found by passing a band-pass filter of bandwidth Δf near frequency f, and it can be given by $\sqrt{8kT\gamma g_{m_{1,2}}\Delta f}$. Now, the final rms output noise voltage can be expressed as:

$$v_{n_o}^2 = \sum_f \left(\frac{\sqrt{8kT\gamma g_{m_{1,2}}\Delta f}}{C_L} \times TF_{env}(f)\right)^2 \quad (15)$$

Equation (15) can be transformed for continuous time, and one can write it as:

$$v_{n_o}^2 = \frac{8kT\gamma g_{m_{1,2}}\Delta f}{C_L^2}\int_0^\infty TF_{env}^2(f) \quad (16)$$

The input referred noise can be found by dividing (16) with the simplified gain found in (9). If the integral is done across the frequency range, it would result in $T_{INT}/2$ [17]. Therefore, the input referred noise can be written as:

$$v_{n_{in}}^2 = \frac{4kT\gamma}{g_{m_{1,2}}T_{INT}} \quad (17)$$

Equation (17) provides an approximation of the input referred noise for conventional integrating amplifier. It is to be noted that this expression shows the worst possible input referred noise estimation. It is also applicable for Strong-ARM latch if T_{INT} is replaced with the amplification time of the latch.

This concept has been used in the latter section, which discusses the effect of finite output resistance on the input referred noise of integrating amplifier, and the dependence of signal-to-noise ratio (SNR) on the output resistance.

III. ANALYSIS OF DIFFERENT INTEGRATOR ARCHITECTURES

Figure 2(a) shows the most simplistic form of an integrating amplifier. Although a single-stage integrating amplifier is capable of providing a gain of 10-14 dB at a significantly lower power cost, it is important to design more efficient integrator architectures to make them suitable for high data rates. If the gain expression of the most simplistic integrating amplifier is considered, the following claim can be made:

$$A = f\left(G_{m_{overall}}, R_{out}, T_{INT}, C_L\right) \quad (18)$$

As the data rate increases to meet state-of-the-art requirements, T_{INT} decreases at the same rate. As a result, the term $(1 - e^{-\frac{T_{INT}}{RC_L}})$ becomes significantly small, reducing the overall gain at the end of the integration period. Therefore, improvements are only possible in terms of the overall transconductance ($G_{m_{overall}}$) of the architecture and output resistance (R_{out}).

In the following subsections, new integrating amplifiers are proposed where the overall transconductance and output
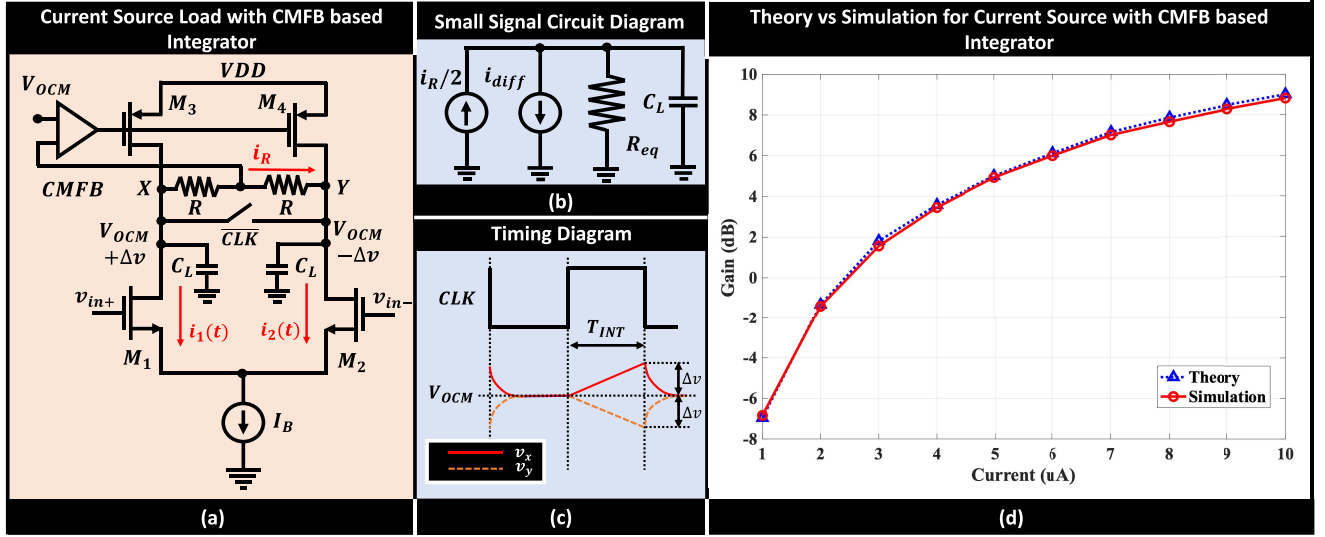
FIGURE 3. (a) Current Source Load with CMFB based integrating amplifier architecture, (b) Small signal circuit diagram of the differential half circuit, (c) Timing diagram of the operation, (d) Theory vs Simulation for current-source load with CMFB based integrating.

resistance have been modified to provide more gain at the same power cost.

A. CURRENT SOURCE LOAD WITH COMMON MODE FEEDBACK BASED INTEGRATOR

Integrating amplifiers suffer from drooping of the common-mode voltage while increasing the overall gain, as briefly explained in Section II-A. A similar issue with current-integrating DFE architectures has been addressed in [18] using a CMFB based architecture to stabilize the common-mode voltage at a fixed, desirable value. Fig. 3(a) shows the 'integrating amplifier' equivalent of the proposed DFE to analyze the applicability of this architecture as an amplifier, which has not been done earlier. The 'integrating amplifier' equivalent of current integrating DFE in [18] is shown in fig. 3(a).

In this architecture, the common-mode voltage is sensed using resistors (R), connected between the output nodes (X & Y). The sensed voltage is fed to the negative input of the operational amplifier, and the positive input is connected to the desired output common-mode voltage reference. The output node of the operational amplifier is connected to the gate terminals of the pMOS transistors $(M_3$ & $M_4)$ to complete the feedback. Using this feedback, the output common-mode voltage is fixed at the desired potential (V_{OCM}).

The operation of this integrating amplifier is shown in Fig. 3(c). During the reset phase, both output nodes are shorted with each other using a pMOS transistor. Thus, output nodes converge to the desired common-mode voltage (V_{OCM}) during the reset phase.

When the *CLK* signal goes high, the differential current pair $(i_1$ & $i_2)$ affects the output capacitance. However, it is to be noted that a portion (i_R) of the differential current goes

through the sensing resistors to ensure that the common-mode voltage stays constant throughout the integration phase. Figure 3(b) shows that i_R actually reduces the differential current that is providing gain. Hence, it is expected that the overall gain of this type of integrating amplifier would be lower than that of a conventional integrator.

Following a similar logic as in Section II-A, the differential current can be written as shown in (1), (2), and (3). As the common-mode voltage is fixed at V_{OCM}, the potential at nodes X and Y can be written as:

$$V_x = V_{OCM} + \Delta v; \; V_y = V_{OCM} - \Delta v \quad (19)$$

Using (19), the current flowing through the sensing resistors can be written as:

$$i_R = \frac{V_x - V_y}{2R} = \frac{\Delta v}{R} \quad (20)$$

Although M_3 and M_4 pMOS transistors are on during the integration procedure, they will not provide any differential ac current as the gate voltage is controlled using the common mode feedback. Hence, there will only be the effects of differential current i_{diff} and i_R on the output capacitance.

To understand the derivation properly, both output nodes are analyzed separately. Using Kirchhoff's current law (KCL) in ac domain at node X, it can be written,

$$i_1 + i_R = \frac{\Delta v}{R_{eq}} + C_L \frac{d\Delta v}{dt} \quad (21)$$

Similarly, the following expression can be written for node Y,

$$i_2 - i_R = \frac{(-\Delta v)}{R_{eq}} + C_L \frac{d(-\Delta v)}{dt} \quad (22)$$

Here R_{eq} is the equivalent resistance at the output nodes, which is the parallel combination of nMOS internal resistance, pMOS internal resistance, and sensing resistance $(R_{eq} = r_{o_n} || r_{o_p} || R)$.

Subtracting (21) from (22), it can be written:

$$i_1 - i_2 + 2i_R = 2\frac{\Delta v}{R_{eq}} + 2C_L\frac{d\Delta v}{dt} \tag{23}$$

Using (3) and (20) in (23), The following expression can be derived:

$$g_{m_{1,2}}v_{in} + 2\frac{\Delta v}{R} = 2\frac{\Delta v}{R_{eq}} + 2C_L\frac{d\Delta v}{dt} \tag{24}$$

Rearranging (24), the differential equation can be written as:

$$\frac{g_{m_{1,2}}v_{in}}{2} = \Delta v\left(\frac{1}{R_{eq}} - \frac{1}{R}\right) + C_L\frac{d\Delta v}{dt} \tag{25}$$

Solving the differential equation (25), the output differential voltage can be written as:

$$\Delta v(t) = \frac{g_{m_{1,2}}v_{in}}{2}R'\left(1 - e^{-t/R'C_L}\right) \tag{26}$$

where $R' = \frac{RR_{eq}}{R-R_{eq}}$. Hence, at the end of integration period, the total differential voltage $(\Delta v - (-\Delta v))$ will be:

$$2\Delta v(T_{INT}) = g_{m_{1,2}}v_{in}R'\left(1 - e^{-T_{INT}/R'C_L}\right) \tag{27}$$

The overall gain of current source load based integrating amplifier can be given as:

$$A_{csl} = \frac{2\Delta v(T_{INT})}{v_{in}} = g_{m_{1,2}}R'\left(1 - e^{-T_{INT}/R'C_L}\right) \tag{28}$$

For infinite sensing resistance, R' approaches the equivalent resistance $(r_{eq} = r_{o_n}||r_{o_p})$ of the output node. In that scenario, the gain expression can be written as:

$$A_{csl}(R' \to r_{eq}) = g_{m_{1,2}}r_{eq}\left(1 - e^{-T_{INT}/r_{eq}C_L}\right) \tag{29}$$

By comparing (8) and (29), it can be concluded that the gain of the current source load based integrating amplifier will always be lower than the conventional integrator even when the sensing resistance is infinite. It occurs because both pMOS and nMOS transistors are on in current source load based integrator unlike conventional integrating amplifier. Moreover, an infinite sensing amplifier also prevents the operational amplifier from maintaining a stable voltage, resulting in a final gain that is always lower than the conventional integrating amplifier for a given current consumption.

Figure 3(d) displays the theoretical estimation of gain plotted using equation (28), with a similar simulation setup arranged for ease of comparison. Although the output capacitance was fixed at 100fF, the actual output capacitance was much higher (120fF) due to additional devices at the output nodes. The bias current (I_B) was varied from $1\mu A$ to $10\mu A$, and amplifier gain was observed in the test setup.

It should be noted that the operational amplifier's current consumption was not considered while plotting fig. 3(d). Therefore, the actual current consumption would be significantly higher than the estimate, as the operational amplifier requires a significant amount of power to maintain stable common-mode feedback. For higher data rate, the CMFB requires loop stability to increase so that the output

common-mode voltage is fixed at V_{OCM}. As a result, the power consumption of the CMFB would need to increase to constitute a stable system at higher data rate. It can be concluded that current source load based integrating amplifier shows the least power efficiency for a given gain requirement in comparison to other integrating amplifiers.

Figure 3(d) shows that (28) provides an appropriate estimate for the gain of the current source load based integrating amplifier. The primary advantage of this amplifier is that the output common-mode voltage remains constant throughout the integration phase, albeit with a lower gain.

Another advantage of the current source load-based integrator is that it can achieve a higher maximum gain, as the transistors do not easily go into saturation. The maximum output voltage swing can range from $V_{D,p_{max}}$ to $V_{D,n_{min}}$. Where, $V_{D,p_{max}}$ and $V_{D,n_{min}}$ are the maximum drain voltage of pMOS and minimum drain voltage of nMOS transistors, respectively. Hence, the maximum possible output differential voltage is given by:

$$v_{out_{max}} = V_{D,p_{max}} - V_{D,n_{min}} \tag{30}$$

To maintain a symmetrical differential output voltage the output common mode voltage should be at the mid-point of the mentioned voltages. Hence, the desired output common mode voltage (V_{OCM}) is:

$$V_{OCM} = \frac{V_{D,p_{max}} + V_{D,n_{min}}}{2} \tag{31}$$

It is apparent from (30) that, current source load based integrating amplifier supports a much higher maximum output swing in comparison to conventional integrator. However, CS-load based integrator achieves it at the cost poor current efficiency.

B. CASCODED INTEGRATING AMPLIFIER

Cascoded DT integrating amplifiers use a pair of cascoded nMOS transistors to increase the overall output resistance of the architecture without affecting the current consumption. Figure 4(a) shows the complete architecture of the cascoded integrating amplifier. The cascoding nMOS transistors, M_3 and M_4, are directly connected to the power supply via the gates. M_1 and M_2 serve as the input differential nMOS transistors, while M_5 and M_6 are used to charge the output voltage nodes to the supply voltage during the charge phase, as shown in Figure 2(b).

The operation of the cascoded integrator is similar to that of the conventional integrating amplifier. The input differential nMOS transistors convert the input voltages into differential current (i_1 and i_2). There is a possibility that a portion of the differential current is lost in discharging the parasitic capacitance of the X and Y nodes in Figure 4(a). However, the parasitic capacitance is significantly less than the output capacitance, and the equivalent resistance of these nodes is extremely small ($1/g_{m_{3,4}}$). As a result, the portion of lost differential current to the parasitic capacitance is negligible (0.05% of i_{diff}). Hence, it can be assumed that
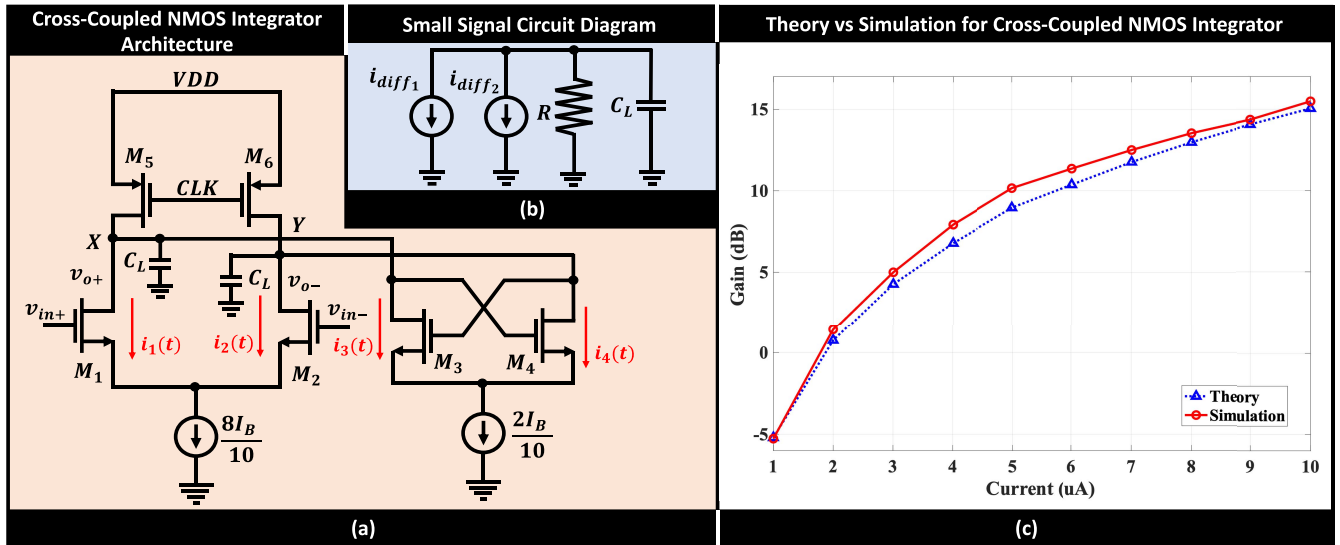
FIGURE 4. (a) Cascoded integrating amplifier architecture, (b) Small signal circuit diagram of the differential half circuit and crucial expressions, (c) Theory vs Simulation for cascoded integrator.

the entirety of the differential current generated by the input nMOS pair goes through the cascoding pair.

Since the differential current almost stays the same following the cascoded stage, it can be written that

$$i_{diff}(t) = i_1(t) - i_2(t) = g_{m_{1,2}}v_{in}(t) \qquad (32)$$

The equivalent output resistance can be written as,

$$R = r_{o_{3,4}} + \left(1 + g_{m_{3,4}}r_{o_{3,4}}\right)r_{o_{1,2}} \qquad (33)$$

Following the small signal circuit as shown in fig. 4(b) for the output node, the following expression can be written,

$$i_{diff}(t) = \frac{v_{out}(t)}{R} + C_L\frac{dv_{out}(t)}{dt} \qquad (34)$$

where R is expressed in (33). Comparing (32) and (34), it can be written:

$$g_{m_{1,2}}v_{in}(t) = \frac{v_{out}(t)}{R} + C_L\frac{dv_{out}(t)}{dt} \qquad (35)$$

Solving the differential equation (35), the output differential voltage can be written as:

$$v_{out}(t) = g_{m_{1,2}}Rv_{in}\left(1 - e^{-\frac{t}{RC_L}}\right) \qquad (36)$$

Hence, the final output voltage at the end of integration phase $(t = T_{INT})$ will be:

$$v_{out}(T_{INT}) = g_{m_{1,2}}Rv_{in}\left(1 - e^{-\frac{T_{INT}}{RC_L}}\right) \qquad (37)$$

So, the overall gain can be written as:

$$A_{cas} = \frac{v_{out}(T_{INT})}{v_{in}} = g_{m_{1,2}}R\left(1 - e^{-\frac{T_{INT}}{RC_L}}\right) \qquad (38)$$

Equation (38) has been used to plot the variation of gain with respect to current as shown in fig. 4(c). For the ease of comparison with other architectures, the test case has been

kept the same. The bias current (I_B) has been varied from $1\mu A$ to $10\mu A$ and the gain has been calculated and plotted.

Fig. 4(c) also shows the simulated result for the given test case. Comparing the simulated and theoretical result shows that (37) can closely predict the simulated gain. However, there is a scope top improve the performance further.

C. CROSS COUPLED NMOS BASED INTEGRATING AMPLIFIER

Cross-coupled nMOS-based DT integrating amplifiers aim to increase the overall gain of the amplifier by boosting the effective transconductance $(G_{m_{overall}})$. Figure 5(a) shows the desired architecture for a cross-coupled nMOS-based integrating amplifier, where M_3 and M_4 provide the extra differential current through cross-coupling.

While the primary nMOS differential pair $(M_1$ and $M_2)$ provides the majority of the differential current, the cross-coupled pair further increases it. Therefore, the overall transconductance $(G_{m_{overall}})$ is much greater than that of conventional integrating amplifiers.

The operation of the cross-coupled nMOS integrator is similar to that of the conventional counterpart, going through similar recharging (ϕ_2) and integrator (ϕ_1) phases. The effect of cross-coupling will be further explained and analyzed during the derivation.

Similar to the conventional integrating amplifier architecture, the primary differential current pair $(i_1$ and $i_2)$ can be calculated using (1) and (2). Hence, it can be concluded:

$$i_{diff_1} = i_1 - i_2 = g_{m_{1,2}}v_{in} \qquad (39)$$

For M_3, the ac current can be expressed as:

$$i_3 = g_{m_3} \times v_{gs_3} = g_{m_3}v_{o-} \qquad (40)$$

Similarly. it can be written that,

$$i_4 = g_{m_4} \times v_{gs_4} = g_{m_4}v_{o+} \qquad (41)$$

FIGURE 5. (a) Cross-coupled nMOS based integrating amplifier architecture, (b) Small signal circuit diagram of the differential half circuit and crucial expressions, (c) Theory vs Simulation for nMOS based integrating amplifiers.

Hence, the extra differential current can be written as:

$$i_{diff_2} = i_3 - i_4 = -g_{m_{3,4}}v_o \qquad (42)$$

It is assumed in (42) that $v_o = v_{o+} - v_{o-}$.

The small signal circuit diagram for the half circuit is shown in fig. 5(b). The resistance (R) in the circuit diagram is the equivalent resistance at the output node. Based on the small signal circuit diagram, the following expression can be written:

$$i_{diff_1} + i_{diff_2} = \frac{v_o}{R} + C_L \frac{dv_o}{dt} \qquad (43)$$

Using (39), (42), and (43), one can modify the differential equation as:

$$g_{m_{1,2}}v_{in} - g_{m_{3,4}}v_o = \frac{v_o}{R} + C_L \frac{dv_o}{dt} \qquad (44)$$

Solving the differential equation (44) would result in:

$$v_o(t) = g_{m_{1,2}}v_{in}\left(\frac{R}{1 + g_{m_{3,4}}R}\right)\left(1 - e^{-t\left(1+g_{m_{3,4}}R\right)/RC_L}\right) \qquad (45)$$

Hence, one can write the gain expression as:

$$A(t) = g_{m_{1,2}}\left(\frac{R}{1 + g_{m_{3,4}}R}\right)\left(1 - e^{-t\left(1+g_{m_{3,4}}R\right)/RC_L}\right) \qquad (46)$$

At the end of integration phase, $(t = T_{INT})$, the final gain expression becomes:

$$A_{ncc} = g_{m_{1,2}}\frac{R}{1 + g_{m_{3,4}}R}\left(1 - e^{-T_{INT}\left(1+g_{m_{3,4}}R\right)/RC_L}\right) \qquad (47)$$

If $g_{m_{3,4}}R \gg 1$, (47) can be written as:

$$A_{ncc} = \frac{g_{m_{1,2}}}{g_{m_{3,4}}}\left(1 - e^{-\frac{T_{INT}g_{m_{3,4}}}{C_L}}\right) \qquad (48)$$

Equation (48) shows that the final gain can be inversely proportional to the transconductance of the differential nMOS transistor pair. By keeping the current consumption low for the cross-coupling transistors and using small devices, the gain can be significantly increased. This is why an 8:2 ratio has been maintained for bias currents between the primary and cross-coupling transistors, as shown in Fig. 5(a).

Figure 5(c) compares the theoretical and simulated results for the nMOS cross-coupled based integrating amplifier. A similar setup was maintained for comparison purposes. The total current consumption was kept the same by dividing it among the primary and cross-coupled transistor pairs. Thus, the x-axis in Fig. 5(c) shows the total current consumption in the circuit, which was varied from $1\mu A$ to $10\mu A$ to observe the gain variation.

Although (48) provides an approximation of the overall gain for cross-coupled nMOS based integrator, (47) was used to derive accurate gain estimations for Fig. 5(c).

D. NMOS CROSS-COUPLING WITH CASCODED INTEGRATING AMPLIFIER

A comparison of different integrating amplifier architectures is shown in Figure 6. In order to ensure a fair comparison between each of these topologies, all test setups have been kept exactly the same. As can be seen, current source-based integrating amplifiers exhibit considerably less gain than conventional integrating amplifiers for a given current consumption. Furthermore, cascoded integrating amplifiers offer benefits over their conventional counterpart.

However, it should be noted that increasing the output resistance has both incremental and detrimental effects on the overall gain. Although the $g_{m_{1,2}}R$ term increases in (37), the $(1 - e^{-T_{INT}/RC_L})$ term decreases with increasing output
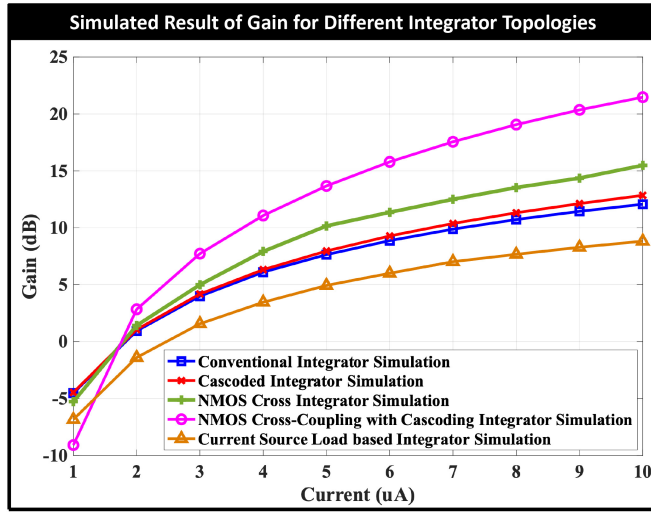
FIGURE 6. Simulation Results for different integrating amplifier architectures.

resistance. Hence, the benefit is not drastic in comparison to conventional integrating amplifiers.

The nMOS cross-coupling based integrator shows further improvement from the conventional integrating amplifier. As the term $1/g_{m_{3,4}}$ is significantly greater than the output resistance, the benefit of the cross-coupled integrating amplifier is more observable.

However, it is possible to combine these effects and improve the gain benefit further. nMOS cross-coupling with cascoded integrating amplifier improves the gain significantly as it can be seen in fig. 6.

Figure 7(a) shows the integrating amplifier architecture where M_3 and M_4 serve as the cross-coupling nMOS pair, and M_5 and M_6 perform the cascoding.

If a similar approach is maintained, the primary and cross-coupling differential currents can be obtained as per (39) and (42). However, in this architecture, the differential currents combine at the nodes P and Q in stead of the output nodes (X and Y). So, the modified value of i_{diff_2} becomes:

$$i_{diff_2} = -g_{m_{3,4}}v_c \tag{49}$$

where v_c is the differential voltage between nodes P and Q.

It is to be noted that nodes P and Q only have parasitic capacitance, and it is assumed to be $C_{P,Q}$. Also, the effective resistance can be given by:

$$R_{P,Q} = r_{o_{1,2}}||r_{o_{3,4}}||\frac{1}{g_{m_{5,6}}} \tag{50}$$

Small signal circuit diagram at nodes P and Q also look similar to fig. 7(b), but with three differential currents. Applying current conservation law at nodes P and Q to find the difference voltage, one can write:

$$i_{diff_1} + i_{diff_2} - i_{diff_3} = \frac{v_c}{R_{P,Q}} + C_{P,Q}\frac{dv_c}{dt} \tag{51}$$

For M_5 and M_6, the differential current i_{diff_3} can be written as:

$$i_{diff_3} = i_5 - i_6 = -g_{m_{5,6}}v_c \tag{52}$$

Using (39), (49), (51), and (52), it can be written:

$$g_{m_{1,2}}v_{in} - g_{m_{3,4}}v_c + g_{m_{5,6}}v_c = \frac{v_c}{R_{P,Q}} + C_{P,Q}\frac{dv_c}{dt} \tag{53}$$

Rearranging (53) would result in:

$$g_{m_{1,2}}v_{in} = v_c\left(\frac{1}{R_{P,Q}} + \left(g_{m_{3,4}} - g_{m_{5,6}}\right)\right) + C_{P,Q}\frac{dv_c}{dt} \tag{54}$$

Solving the differential equation (54) for v_c, one can write,

$$v_c(t) = g_{m_{1,2}}v_{in}R''\left(1 - e^{\frac{t}{R''C_{P,Q}}}\right) \tag{55}$$

where R'' can be given by:

$$R'' = \left(\frac{R_{P,Q}}{1 + R_{P,Q}\left(g_{m_{3,4}} - g_{m_{5,6}}\right)}\right) \tag{56}$$

If $g_{m_{3,4}} \approx g_{m_{5,6}}$, the modified resistance term R'' can be approximated as $R_{P,Q}$. So, (55) can be written as:

$$v_c(t) = g_{m_{1,2}}v_{in}R_{P,Q}\left(1 - e^{\frac{t}{R_{P,Q}C_{P,Q}}}\right) \tag{57}$$

It is to be noted that both $R_{P,Q}$ and $C_{P,Q}$ are small in comparison to the output nodes. As a result, the time constant $R_{P,Q}C_{P,Q}$ is significantly less than the time span of the integration phase. So, one can conclude that the differential voltage for the nodes P and Q would reach $g_{m_{1,2}}R_{P,Q}v_{in}$ almost at the start of integration phase.

As a result, it is assumed that the differential voltage v_c stays constant at $g_{m_{1,2}}R_{P,Q}v_{in}$ for the entirety of integration phase for simplicity. Hence, it can be written:

$$v_c(t) = g_{m_{1,2}}R_{P,Q}v_{in} \tag{58}$$

So, using (52) and (58), it can be written:

$$i_{diff_3} = -g_{m_{5,6}}g_{m_{1,2}}R_{P,Q}v_{in} \tag{59}$$

Finally, KCL at the output node would result in:

$$i_{diff_3} = \frac{v_o}{R_{eq}} + C_L\frac{dv_o}{dt} \tag{60}$$

where R_{eq} is the equivalent resistance at the output node, which is given by:

$$R_{eq} = r_{o_{5,6}} + \left(1 + g_{m_{5,6}}r_{o_{5,6}}\right)\left(r_{o_{1,2}}||r_{o_{3,4}}\right) \tag{61}$$

Putting the expression for i_{diff_3} in (60) and solving the differential equation would result in:

$$v_o(t) = -g_{m_{5,6}}g_{m_{1,2}}R_{P,Q}R_{eq}v_{in}\left(1 - e^{\frac{t}{R_{eq}C_L}}\right) \tag{62}$$

So, the overall gain at the end of integration phase can be given by:

$$|A| = g_{m_{5,6}}g_{m_{1,2}}R_{P,Q}R_{eq}\left(1 - e^{\frac{T_{INT}}{R_{eq}C_L}}\right) \tag{63}$$
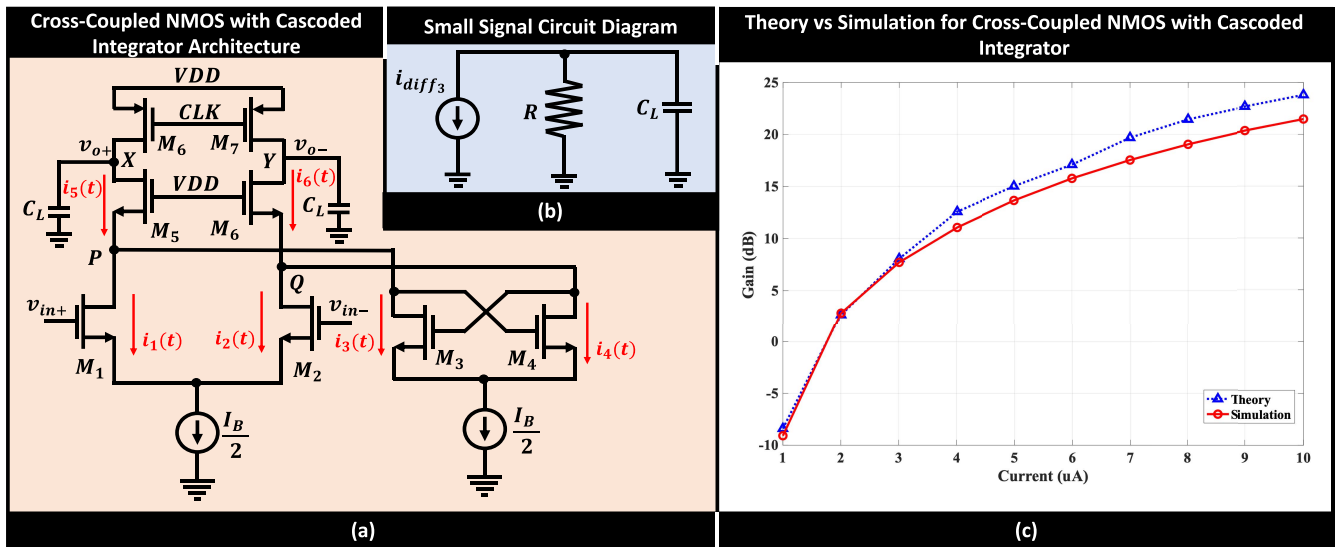
FIGURE 7. (a) nMOS Cross-coupling with Cascoded integrating amplifier architecture, (b) Small signal circuit diagram of the differential half circuit, (c) Theory vs Simulation for Cross-coupled nMOS with cascoded integrating amplifier.

Equation (63) provides an estimation of the gain for nMOS cross-coupled with cascoding-based integrating amplifiers. As shown in (63), the final gain expression is increased due to both the overall $G_{m_{overall}}$ and the improved effective output resistance.

Figure 7(c) compares the simulated and theoretical estimation of the gain for this type of integrating amplifier architecture. The test setup is kept the same to allow for a coherent comparison with the other architectures.

It has been taken into consideration that the assumptions are valid only with careful device sizing. For example, it has been ensured that $g_{m_{5,6}}$ is equivalent to $g_{m_{3,4}}$ to assume R'' to be equal to $R_{P,Q}$. Hence, (63) has been used to estimate the amplifier gain in fig. 7(c). The plot shows that the derived expressions can closely approximate the simulated gain. The deviation in the higher bias current region arises because the transconductances become considerably different. If a non-approximated derivation is followed, a more thorough expression can be derived. However, (63) serves the purpose of estimating the gain in this case.

Finally, examining fig. 6, it is evident that the nMOS cross-coupled integrating amplifier with cascoding provides a significant benefit over other integrator topologies for a given current consumption.

This section proposes various methodologies to increase the overall gain of integrating amplifiers without deteriorating the power consumption, and a comparative analysis was conducted on all of the proposed architectures.

IV. DEPENDENCE OF SIGNAL-TO-NOISE RATIO ON FINITE OUTPUT RESISTANCE

In [17], the derivation of input referred noise for conventional discrete-time integrating amplifier is shown, as presented in Section II-B. However, the derivation assumes an infinite output resistance for simplicity. While these expressions are valid for low data rates, it is crucial to consider the effects of finite output resistance for high data rates. Furthermore, the concept of input referred noise can be extended towards the SNR at the output by associating the effect of gain on the overall output waveform.

For reference, the overall circuit diagram and half circuit small circuit diagram can be found in Figure 2(a) and (b), respectively. Thus, when taking into account the finite output resistance of the integrating amplifier, (13) can be modified to obtain the output differential noise voltage as:

$$\frac{v_{n_o}}{R} + C_L \frac{dv_{n_o}}{dt} = A\sin(2\pi ft + \phi) \quad (64)$$

where $A\sin(2\pi ft+\phi)$ is the differential thermal noise current $(i_n(t))$ through M_1 and M_2. The solution to the differential equation (64) will be of the form:

$$v_{n_o} = C \times \cos(2\pi ft + \phi) + D \times \sin(2\pi ft + \phi) \quad (65)$$

where C and D are two constants, which are dependent on the resistance (R), capacitance (C_L), and frequency (f). Using (64) and (65), one can find the solution of C and D:
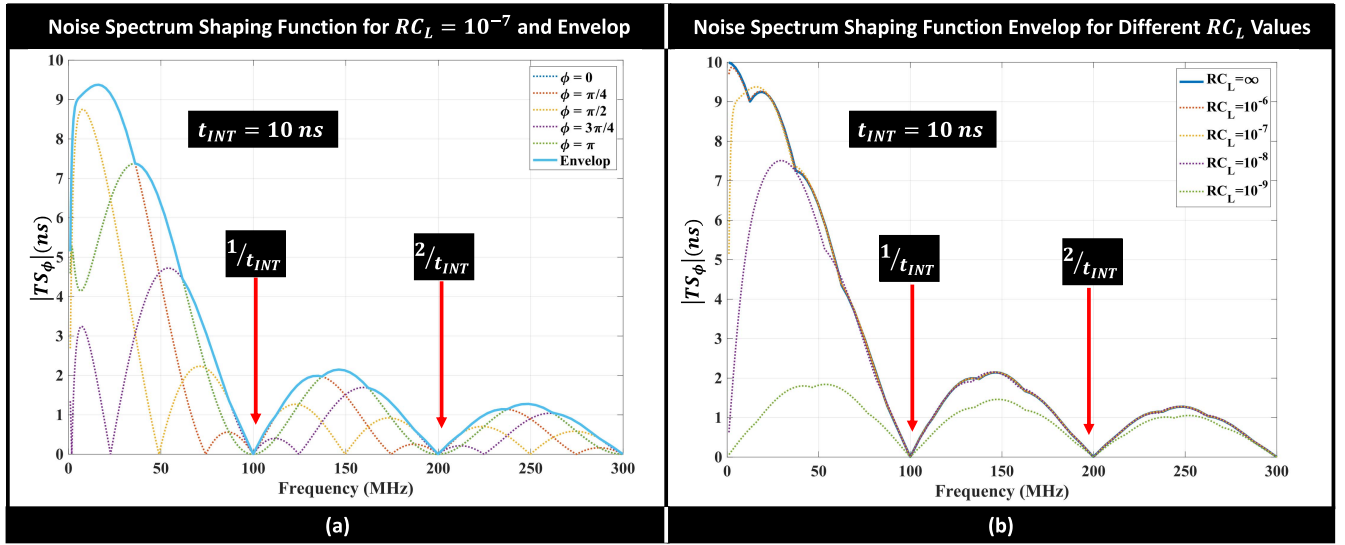
$$C = -\frac{AR^2 C_L(2\pi f)}{1 + 4\pi^2 f^2 R^2 C_L^2}$$

$$D = \frac{AR}{1 + 4\pi^2 f^2 R^2 C_L^2} \quad (66)$$

Substituting the values of C and D in (65) and putting the limits of the integration from $t = 0$ to T_{INT} would result:

$$v_{n_o} = \frac{AR}{1 + 4\pi^2 f^2 R^2 C_L^2}(\sin(2\pi f T_{INT} + \phi) - \sin(\phi))$$

$$- \frac{AR^2 C_L(2\pi f)}{1 + 4\pi^2 f^2 R^2 C_L^2}(\cos(2\pi f T_{INT} + \phi) - \cos(\phi)) \quad (67)$$

FIGURE 8. (a) Noise spectrum shaping function ($TS_\phi(f)$) for finite output resistance using (69) when $RC_L = 10^{-10}$, and the envelop has also been shown, (b) Variation of $TS_\phi(f)$ for different combinations of RC_L when integration time is fixed at 10ps.

Now, the above expression can be rewritten as:

$$v_{n_o} = \frac{A}{C_L}\left[TS_\phi(f)\right] \tag{68}$$

where, the new noise spectrum shaping function $TS_\phi(f)$ is

$$TS_\phi(f) = \frac{RC_L}{1 + 4\pi^2 f^2 R^2 C_L^2}(\sin(2\pi f T_{INT} + \phi) - \sin(\phi))$$
$$- \frac{R^2 C_L^2(2\pi f)}{1 + 4\pi^2 f^2 R^2 C_L^2}(\cos(2\pi f T_{INT} + \phi) - \cos(\phi)) \tag{69}$$

Equation (69) presents the new noise spectrum shaping function for a finite output resistance. Figure 8(a) depicts the variation of the new noise spectrum shaping function concerning phase and frequency. The analysis was performed by keeping the value of RC_L in (69) at 10^{-7}. Furthermore, fig. 8(b) demonstrates the effect of RC_L on the noise spectrum shaping envelope function.

However, it is essential to prove that the expression is also valid for the infinite output resistance case. For this purpose, the $(1 + 4\pi^2 f^2 R^2 C_L^2)$ term can be approximated as $4\pi^2 f^2 R^2 C_L^2$. In that case, (69) can be written as:

$$TS_\phi(f) = \frac{1}{4\pi^2 f^2 RC_L}(\sin(2\pi f T_{INT} + \phi) - \sin(\phi))$$
$$- \frac{1}{2\pi f}(\cos(2\pi f T_{INT} + \phi) - \cos(\phi)) \tag{70}$$

The term $1/4\pi^2 f^2 RC_L \to 0$ for infinite output resistance. So, the noise spectrum shaping function can be written as:

$$TS_\phi(f) = \frac{1}{2\pi f}(\cos(\phi) - \cos(2\pi f T_{INT} + \phi)) \tag{71}$$

Comparing (14) and (71), it can be concluded that $TS_\phi(f) \approx TF_\phi(f)$ for infinite output resistance. It can also be observed

in fig. 8(b), where the variation of the envelop has been shown for different RC_L values.

The analysis in 8(a) has been performed with the value of RC_L in (69) set to 10^{-7}. Figure 8(b) illustrates the effect of RC_L on the noise spectrum shaping envelope function.

It can be seen in fig. 8(b) that the envelope for the $RC_L = 10^{-6}$ case is almost indistinguishable from the infinite output resistance plot. The $RC_L = 10^{-7}$ case also does not show a drastic deviation from the previous two cases. Once the RC_L component becomes comparable or less than the integration time, it shows a significant difference.

Reference [17] has shown that the noise shaping function can be used to determine the output referred noise of the integrating amplifier. Similar to (16), the output referred noise will be:

$$v_{n_o}^2 = \frac{8kT\gamma g_{m_{1,2}}\Delta f}{C_L^2}\int_0^\infty TS_{env}^2(f) \tag{72}$$

As per (72), it can be concluded that the area under the curve, shown in fig. 8(b), provides an estimate of the output referred noise for integrating amplifiers. Hence, the array of curves in fig. 8(b) gives an impression that the output referred noise decreases by lowering the RC time constant, and this can be used to reduce the signal-to-noise ratio (SNR) at the output.

However, the gain of integrating amplifier also starts decreasing while lowering RC time constant, as shown in (8). So, it is crucial to understand the effect of integrating amplifier on the output SNR with the variation of finite output resistance.

Figure 9 shows the dependence of SNR on the RC time constant. The curve has been plotted for a conventional integrating amplifier using the device parameters from TSMC 65nm CMOS technology node. The experiment was
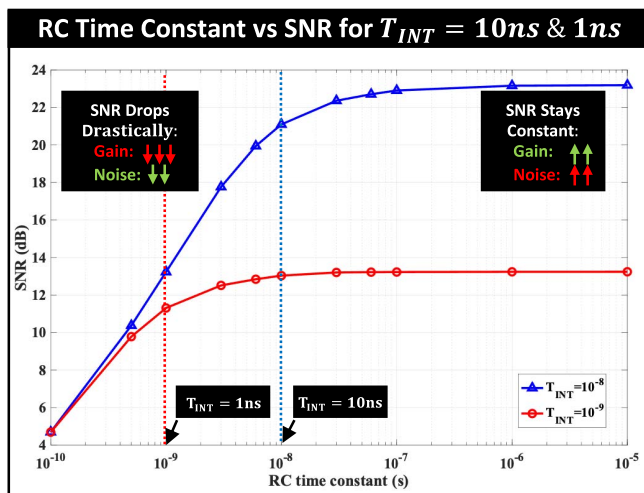
FIGURE 9. Dependence of Signal-to Noise Ratio (SNR) on the RC time constant of an integrating amplifier which is operating with integration time of 10*ns* and 1*ns*.

FIGURE 10. (a) Circuit diagram of conventional low-noise amplifier with self-biased load, (b) Important expression for the shown low-noise amplifier.

conducted with integration time of 1ns and 10ns, and the variation of SNR has been observed.

It can be observed that the degradation of SNR starts at different RC time constants for T_{INT} of 10ns & 1ns. The results have been obtained from the same test setup without changing the intrinsic properties of the transistors and load capacitors. Both gain and output noise of integrating amplifier start saturating as the output resistance become higher, and SNR does not change. However, when the RC time constant is comparable or lower than the integration time (T_{INT}), gain starts to deteriorate faster than the reduction in overall noise. As a result, the overall output SNR starts decreasing rapidly with lower RC time constant. It can be concluded that providing maximum gain should be priority over reducing noise to achieve the maximum SNR for integrating amplifier, unlike conventional continuous-time amplifiers.

This analysis shows that the upper limit of the input referred noise remains the same as shown in (17). However, this new expression can be used to determine the input referred noise for marginal cases. Analyzing the effect on SNR proves that optimization for gain would result in the best SNR due to discrete-time integrator's inherent noise suppression.

V. LOW-NOISE AMPLIFIER VS. INTEGRATING AMPLIFIER
In the previous sections, the gain, input referred noise, and signal-to-noise ratio of discrete-time integrating amplifiers were studied. A comparative study was also conducted among different topologies of discrete-time integrating amplifiers. However, it is important to compare integrating amplifiers with other conventional continuous-time amplifier topologies as well.

Reference [17] demonstrated the performance of a low-noise amplifier (LNA) with integrating amplifier with respect to input referred noise. However, gain analysis of
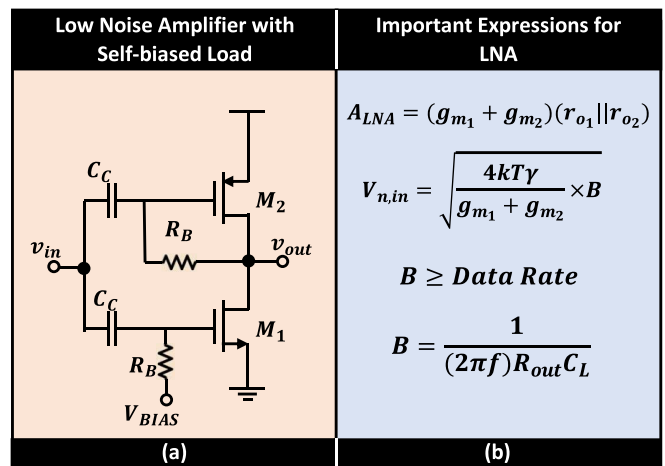
these amplifiers results in a deeper understanding of their applicability. The primary distinction arises from the fact that integrating amplifiers can provide separate gain for different bandwidth requirements and power consumption limits, while the bandwidth and power consumption of LNAs are fixed for a given gain.

The mid-band gain of a conventional LNA with self-biased load as shown in fig. 10 can be expressed as:

$$A_{LNA} = (g_{m_1} + g_{m_2})(r_{o_1}||r_{o_2}) \tag{73}$$

All the parameters g_{m_1}, g_{m_2}, r_{o_1}, and r_{o_2} are completely dependent on the current consumption through M_1 and M_2. Current consumption can be converted to power consumption by multiplying with the supply voltage. The bandwidth of LNA is kept equal to or more than the data rate to avoid inter-symbol interference (ISI) related issues. For a conventional LNA as shown in fig. 10, the bandwidth is given by:

$$B_{LNA} = \frac{1}{(2\pi f)R_{out}C_L} \tag{74}$$

where R_{out} is the output resistance of the low-noise amplifier, given by $R_{out} = r_{o_1}||r_{o_2}$, and C_L is the load capacitance at the output node. These parameters are also dependent on the power consumption of the LNA.

Therefore, for a given power consumption requirement, the bandwidth and gain of the low-noise amplifier are fixed. To determine the dependence of bandwidth and gain on power consumption, a test bench was constructed and simulations were carried out using the 65nm TSMC CMOS technology node. Individual transconductance and intrinsic resistance calculations were performed for both pMOS and nMOS devices under different bias conditions. Equations (73) and (74) were then used to determine the gain and bandwidth for a conventional low-noise amplifier for a given power consumption. Figure 11 shows a three-dimensional plot for the LNA. The x-axis represents power consumption, the y-axis represents bandwidth, and the z-axis represents the
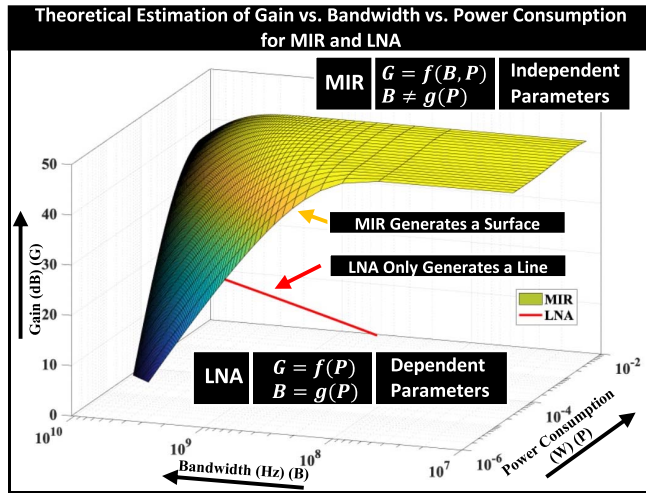
FIGURE 11. A comparative analysis of gain, bandwidth, and power consumption between conventional low-noise amplifier with self-biased load and two stages of integrating amplifier (MIR). Gain decreases at higher bandwidth (low T_{int}) and low power consumption (low I_{Bias}).

gain of the LNA. As bandwidth and gain are correlated, they produce a line in the three-dimensional space.

Fig. 11 shows that only a line plot is possible in the three-dimensional plot for a low-noise amplifier. For a specific current consumption, all the parameters in (73) and (74) become fixed. As a result, it provides only a single point on the plot, and the complete plot generates a line.

Two or more stages of discrete-time integrating amplifiers will have similar or lower power consumption compared to the low-noise amplifier. In this analysis, two conventional integrating amplifiers are cascaded to determine the gain and power conversion of the overall system. Two or more stages of such integrating amplifiers can be referred to as a multi-integrating receiver (MIR).

Reference [17] shows the gain calculation when MIR has two or more stages of integrating amplifiers. Following a similar analysis, the gain of MIR with two stages can be written as:

$$A_{int,2} = (g_{m_{1,2}}R)^2 \left(1 - \left(1 + \frac{T_{int}}{RC_L} \right) e^{-T_{int}/RC_L} \right) \quad (75)$$

Both stages are considered identical. The transconductance of the input nMOS transistor pair for both stages is denoted as $g_{m_{1,2}}$, while the output resistance is represented as R, and the output capacitance is denoted as C_L. These parameters depend on the bias current of the integrating amplifiers.

For both stages, the integration phase duration is denoted as T_{int}. Comparing equations (8) and (75), it is evident that the gain drop-off point for the multi-integrating receiver (MIR) occurs at a lower frequency compared to the single-stage integrating amplifier. However, the MIR exhibits a remarkable gain increment in lower frequency regions.

The 3-dB point of the 2-stage MIR can be found when the T_{int} dependent coefficient decreases by 3dB. Using (75),

it can be said for 3dB point:

$$1 - \left(1 + \frac{T_{int}}{RC_L} \right) e^{-T_{int}/RC_L} = 10^{-\frac{3}{20}} \approx \frac{1}{\sqrt{2}} \quad (76)$$

An approximate of the 3dB bandwidth can be found by solving (76):

$$B_{int} = 1/T_{int} = \frac{1}{RC_L\sqrt{0.3}} \quad (77)$$

It is important to note that T_{int} is still a variable parameter and can be chosen based on the data rate requirement of the receiver. Equation (77) shows where the integration operation is not optimal. For maximum gain, the designer should keep the operating condition in the gain saturated region, which can be obtained by changing the power consumption independently, thereby, ensuring independence of bandwidth and power consumption.

The gain saturation at low bandwidth occurs due to $(1 + x)e^{-x}$ nature of the expression in (75), where $x = \frac{T_{int}}{RC_L}$. When $x \to 0$, the expression reaches 1. It shows that, gain will be tending to 0, which is proved by the decreasing gain for higher bandwidth or lower integrating time. However, when $x \to \infty$, the expression tends to 0. As a result, for infinite integration time, (75) can be modified to

$$lim_{T_{int} \to \infty} A_{int,2} = (g_{m_{1,2}}R)^2 \quad (78)$$

This phenomenon can be explained from circuit analysis as well. The $(1 + \frac{T_{int}}{RC_L})$ term comes due to the integration of differential current on the load capacitors. However, the RC nature of the output nodes provides e^{-T_{int}/RC_L} term, and shows that the entirety of differential current cannot be integrated on the capacitor. Even if the integrator is given infinite time, the effective integrated output voltage is limited and dependent on the output impedance. As a result, output impedance of the integrating amplifier is crucial to determine the gain saturation point as shown in (77).

It is also to be noted that the analysis has been done using small signal ac signal as the input to the integrating amplifier. For such signals, the integrator shows linear behavior due to linear conversion of small input voltage to differential current. However, large input signal does not show a linear conversion to current due to V_{gs} (gate-to-source voltage of input transistors) dependent g_m. So, integrating amplifiers loses linearity for large signals like any other continuous time amplifier.

The gain of the MIR is influenced by both bandwidth and current consumption, resulting in a three-dimensional surface plot (Figure 11). To estimate the gain, a similar approach was employed that involved determining the transconductance and output resistor of nMOS transistors for the 65nm TSMC CMOS technology node, utilizing Equation (75).

Figure 11 illustrates that the gain of the MIR starts to deteriorate as the bandwidth increases due to the shorter integration time. Additionally, it decreases as the power consumption decreases since the small bias current significantly reduces the transconductance of the input nMOS pairs. As

expected from Equation (75), the figure also shows that the gain saturates at higher power consumption and lower bandwidth regions. At this stage, the integrating amplifier reaches the intrinsic gain limit of the input transistors. However, it is possible that the integrating amplifier reaches a saturation limit before the intrinsic gain limit. It is primarily due to input transistor reaching linear region as output common mode voltage reaches too low. However, the overall system still show the plateau for lower bandwidth and higher power consumption limits at a relatively lower gain.

Importantly, both low-noise amplifier (LNA) and discrete-time MIR are optimized for a 2 Gb/s data rate. Comparing the plots in Figure 11, it is evident that the MIR not only offers a more convenient choice for achieving the desired gain requirement but also provides higher gain for a given power consumption. The applicability of integrating amplifiers for wireline-like broadband channels is demonstrated, where the MIR outperforms the LNA in terms of gain with low power requirements. Moreover, it can be further optimized for high-speed operations by utilizing lower technology nodes.

VI. CONCLUSION

This paper aims to develop a theoretical understanding of both conventional and newly proposed discrete-time integrating amplifier architectures. The comparison of these topologies indicates that the newly proposed cross-coupled nMOS with cascoded integrating amplifier provides the maximum gain for a given current consumption. The analysis of input referred noise for finite output resistance shows that, for most practical designs, the worst case analysis presented in [17] remains valid. However, for marginal cases, the derived expressions can be utilized to determine the input referred noise. SNR analysis proves that discrete-time integrating amplifiers provide the best output SNR when it is optimized for maximum gain, unlike conventional continuous-time amplifiers. The derived expressions are verified by comparing the expected estimations with simulated results. Moreover, when compared to a conventional low-noise amplifier, the two-stage multi-integrator provides significantly more gain for a given power consumption while also simplifying the design space for the circuit designer. In conclusion, it can be stated that discrete-time integrating amplifiers offer a low power solution for amplifying highly attenuated signals for legacy and wireline-like channels, while introducing extremely low input referred noise.

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