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Class–CTA: Concept and Theoretical Analysis of a High Linearity and Efficiency Power Stage Architecture

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ABSTRACT This work presents a power stage architecture that combines high–linearity with high–efficiency. The power stage is configured as a push–pull Class–A topology with two buck–converters providing its supply rails. The buck–converters continuously track the stage's output with a small constant margin, creating a minimum, constant voltage drop on the output devices; thus, the stage's efficiency is increased and its linearity is improved. Theoretical analysis of the topology and its feedback control are presented, while a design example is implemented and simulated in Cadence Spectre as proof–of–concept.

INDEX TERMS Buck–converter, push–pull Class–A, Class–CTA, efficiency, linearity, power stage.

I. INTRODUCTION

POWER amplifiers are one of the most commonly used blocks in electronic applications, with their power stage having a major impact on their overall linearity and power consumption [1]; two factors often in conflict. Linearity plays a crucial role in measurement applications and consumer ones, like audio, where power is always a constraint. Various power stage classes try to excel in one or both of these two aspects: Class–A stages offer superior linearity at the expense of efficiency; Class–B stages improve on efficiency but suffer from crossover distortion, while Class–AB topologies stay in between Class–A and Class–B in the efficiency metric. Switching output stages like Class–D and its variants, like Class–E (used mostly for RF applications [2]), feature very high power efficiency [3], [4], but lack in linearity compared to their non–switching counterparts.

An attempt to boost the efficiency of the linear family of output stages comes in the form of Class–G and Class–H power stages. These architectures usually feature an output stage biased in Class–AB (or more rarely, in Class–B), with multiple supply rails or a dynamic one. Class–G employs different supply levels with discrete steps based on the output signal's amplitude through a switching–selection mechanism, and has established itself to both audio [5], [6], [7] and RF applications [8], [9], [10], [11], [12], [13], [14]. One aspect that requires attention is the switching noise introduced during the supply rails' selection [15], since it can severely degrade linearity. Switchless designs have been proposed to deal with the abrupt supply switching [16], [17].

Class–H stages use a dynamic approach. In their most common form, for small signal amplitudes a minimum, fixed supply level is set; when the signal exceeds a threshold value, the supply rail dynamically tracks it with an added offset to keep the output devices in the appropriate operational region. When both positive and negative supply rails are available, they both stay fixed at low absolute voltages for small output level; and one of them tracks the output with an offset, when the output level exceeds certain thresholds [18], [19]. The same approach can be implemented in a fully–differential bridge configuration with a single supply rail [20], [21], [22],

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where a bootstrapping amplifier topology has been proposed to further improve efficiency and linearity [23].

Another flavor of Class–H power stages employs envelope–tracking of the output by the dynamic supply rail. For audio and low–frequency measurement purposes, envelope–tracking has been used in single–rail [24] implementations, and also in a mirrored dual–rail fashion [25], where both rails simultaneously increase or decrease in absolute value. It has also been used in RF applications where more sophisticated tracking schemes can cope with the more demanding signal bandwidths [26].

In this work, a high–linearity and high–efficiency power stage architecture based on the Class–H principles is presented [27]. Instead of being biased in Class–AB or Class–B, the proposed stage's output devices are in a push–pull Class–A scheme (full–cycle conduction) to ensure high linearity. Two buck–converters constantly track the output voltage towards the same direction with an appropriate margin and generate the two supply rails; this way a constant voltage drop on the power transistors is maintained, maximizing the stage's efficiency and further increasing linearity.

The remainder of this paper is organized as follows. Section II presents the concept of the proposed power stage architecture, and Section III outlines its theoretical analysis and a feedback control scheme that can serve as a complete design guide. Finally, a proof–of–concept circuit implementation of the topology is given in Section IV, accompanied by Cadence Spectre simulation results, while conclusions are drawn in Section V.

II. PROPOSED POWER STAGE ARCHITECTURE

The concept of the proposed power stage architecture is depicted in Figure 1. Both positive (u_R^+) and negative (u_R^-) supply rails continuously track the output signal, creating a constant voltage drop (u_M) on the output devices at all times. This scheme offers two advantages. First, power loss on output transistors is minimized; this has a profound effect for a push–pull Class–A topology where both devices conduct during a full cycle and unavoidably decrease the efficiency potential of the stage. Secondly, modulation of the transistors' currents due to the Early effect is ideally eliminated; thus, overall linearity of the stage is improved. The small error in the achieved margin results in a minimal current modulation effect; the smaller this error, the better the stage's achieved linearity.

The system–level architecture of the proposed power stage is given in Figure 2. The two supply rails are generated by two buck–converters that track the output signal plus/minus a margin voltage, u_M. The power stage is biased in Class–A and is a push–pull configuration. The proposed architecture is general; it can employ MOSFET or BJT devices (or a combination of them), and can be implemented in either discrete–component or integrated circuit designs. This paper presents and analyzes a MOSFET version of the topology. For a MOSFET power stage, the selected u_M can be as small as the u_{DS} saturation value of the output devices plus a safety margin to prevent them from entering the triode region throughout the entire output range. The converters' duty cycles are shaped through feedback and pulse–width modulation (PWM).

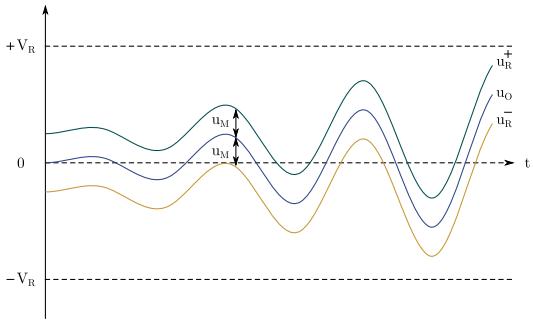

FIGURE 1. Proposed power stage's continuously tracking rails.

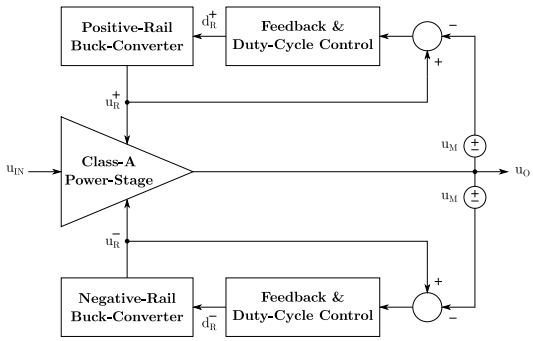

FIGURE 2. Proposed power stage's system–level architecture.

Given the continuous tracking of the output voltage by the power stage rails and the stage's Class–A biasing, the proposed topology is referred to as Class–CTA (*Continuously Tracking A*).

III. CLASS–CTA THEORETICAL ANALYSIS

The proposed power stage can be divided into three blocks: the push–pull Class–A MOSFET power stage, the positive–rail buck–converter, and the negative–rail one. The blocks are modeled as shown in Figure 3. The analysis of Class–CTA starts with the power stage's biasing and its drawn current expressions, and continues on to the buck–converters. All equations required to implement the Class–CTA architecture are provided, so apart from establishing its theoretical background, the foregoing analysis also serves as a complete design guide for sizing the involved components.

A. MOSFET PUSH–PULL CLASS–A POWER STAGE

The push–pull power stage of the proposed design is formed by MOSFETs M_n and M_p in Figure 3. No degeneration resistances are present at their sources, given the smoother current square–law of MOSFETs versus the abrupt exponential–law of BJT devices. This also simplifies the foregoing large–signal, low–frequency analysis.

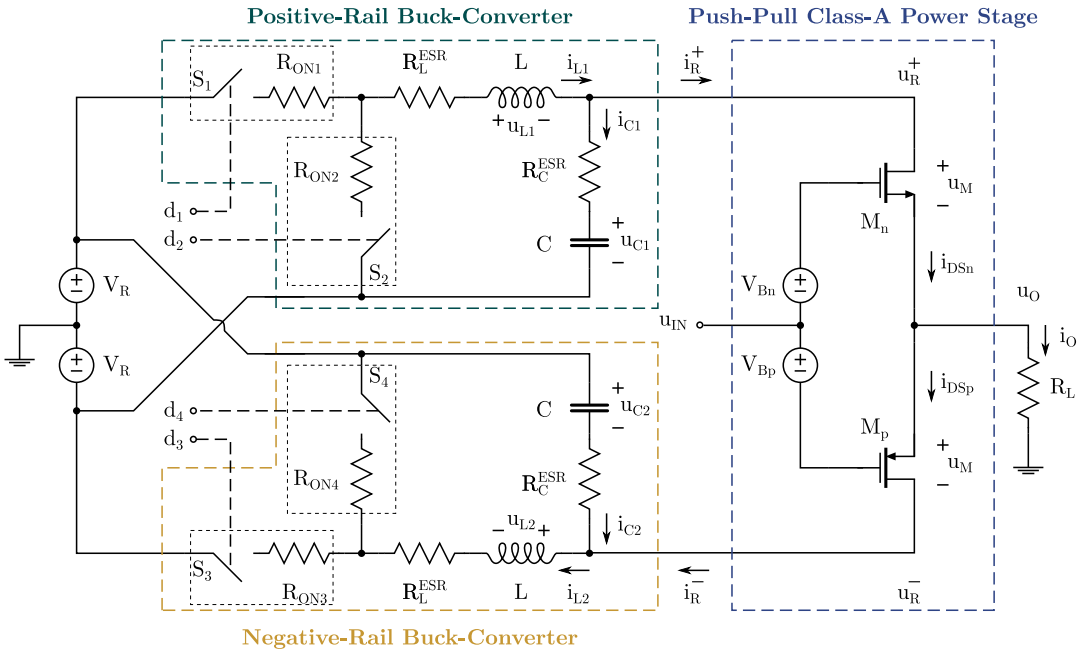

FIGURE 3. Class–CTA model.

Note that the two feedback loops in Figure 2 maintain constant u_{DS} voltage for M_n and M_p, equal to u_M. Moreover, both M_n and M_p are desired to operate in strong–inversion and also to avoid mobility degradation; with these design requirements in mind, their drain currents are expressed as

$$\begin{aligned} i_{DS_n} &= \zeta_n \big(u_{GS_n} - V_{tn}\big)^2 \\ i_{DS_p} &= \zeta_p \big(u_{SG_p} - |V_{tp}|\big)^2, \end{aligned} \tag{1}$$

where it is defined

$$\begin{aligned} \zeta_n &\triangleq \frac{i_{DS_n}}{V_{eff_n}^2} = \frac{1}{2}\mu_n C_{ox}\frac{W_n}{L_n}(1+\lambda_n u_M) \\ \zeta_p &\triangleq \frac{i_{DS_p}}{V_{eff_p}^2} = \frac{1}{2}\mu_p C_{ox}\frac{W_p}{L_p}\big(1+\lambda_p u_M\big). \end{aligned} \tag{2}$$

In the above expressions, V_{tn}, V_{tp} are the transistors' threshold voltages, and V_{eff_n}, V_{eff_p} are their effective voltages, equal to $(u_{GS_n} - V_{tn})$ and $(u_{SG_p} - |V_{tp}|)$, respectively. Finally, W_n, W_p, L_n, L_p represent the transistors' gate width and length values, μ_n, μ_p are their carrier mobilities, λ_n, λ_p depict their output impedance constants, and C_{ox} is the gate capacitance per unit area [28].

1) PURE CLASS–A BIASING CONDITIONS

The biasing of the output stage is set by the sum of voltages V_{B_n} and V_{B_p}, and it holds that

$$V_{B_n} + V_{B_p} = u_{GS_n} + u_{SG_p}. \tag{3}$$

It is convenient to define the positive DC bias voltage

$$V_A \triangleq V_{B_n} - V_{tn} + V_{B_p} - |V_{tp}| = V_{eff_n} + |V_{eff_p}|. \tag{4}$$

Then, using equation (1) that is desired to hold over the entire voltage range of operation, voltage V_A can be expressed as

$$V_A = \sqrt{\frac{i_{DS_n}}{\zeta_n}} + \sqrt{\frac{i_{DS_p}}{\zeta_p}}. \tag{5}$$

In order to have high–linearity Class–A operation, both transistors M_n and M_p must always be in strong–inversion. To achieve this, it is required that their currents are always larger than some minimum values, i.e., $i_{DS_n}^{min} > i_{lim}^{sat_n}$, $i_{DS_p}^{min} > i_{lim}^{sat_p}$, where

$$i_{lim}^{sat_{n,p}} = 16\mu_{n,p} C_{ox}\frac{W_{n,p}}{L_{n,p}} A U_T^2, \tag{6}$$

A is the weak–inversion slope factor, and $U_T = k_b T/q$ is the thermal voltage [29]. From Figure 3 it is

$$i_{DS_n} = i_{DS_p} + i_O, \tag{7}$$

where $i_O = u_O/R_L$ and $i_{DS_n}, i_{DS_p} \geq 0$. Let the minimum and maximum output voltage be $\pm u_O^{max}$, with $u_O^{max} > 0$. Due to i_{DS_n} being strictly increasing with u_{IN} and i_{DS_p} being strictly decreasing with u_{IN}, the minimum and maximum currents of the transistors appear in pairs, $\{i_{DS_n}^{min}, i_{DS_p}^{max}\}$, $\{i_{DS_n}^{max}, i_{DS_p}^{min}\}$; then, from (7)

$$\begin{aligned} i_{DS_n}^{min} &= i_{DS_p}^{max} - \frac{u_O^{max}}{R_L} \\ i_{DS_p}^{min} &= i_{DS_n}^{max} - \frac{u_O^{max}}{R_L}, \end{aligned} \tag{8}$$

where it may very well be $i_{DS_n}^{min} \neq i_{DS_p}^{min}$ and $i_{DS_n}^{max} \neq i_{DS_p}^{max}$.

For the maximum and minimum output voltage, equation (5) implies through (8) that

$$V_A = \sqrt{\frac{i_{DS_n}^{min}}{\zeta_n}} + \sqrt{\frac{i_{DS_n}^{min} + \frac{u_O^{max}}{R_L}}{\zeta_p}}$$
$$V_A = \sqrt{\frac{i_{DS_p}^{min} + \frac{u_O^{max}}{R_L}}{\zeta_n}} + \sqrt{\frac{i_{DS_p}^{min}}{\zeta_p}}. \quad (9)$$

Since it is required that $i_{DS_n}^{min} > i_{lim}^{sat_n}$, $i_{DS_p}^{min} > i_{lim}^{sat_p}$, it must be selected

$$V_A > \max\{V_{A_1}, V_{A_2}\}, \quad (10)$$

where

$$V_{A_1} = \sqrt{\frac{i_{lim}^{sat_n}}{\zeta_n}} + \sqrt{\frac{i_{lim}^{sat_n} + \frac{u_O^{max}}{R_L}}{\zeta_p}}$$
$$V_{A_2} = \sqrt{\frac{i_{lim}^{sat_p} + \frac{u_O^{max}}{R_L}}{\zeta_n}} + \sqrt{\frac{i_{lim}^{sat_p}}{\zeta_p}}. \quad (11)$$

Consider again the drain currents and the output voltage of the power stage in Figure 3,

$$i_{DS_n} = \zeta_n(u_{IN} + V_{B_n} - u_O - V_{tn})^2$$
$$i_{DS_p} = \zeta_p(u_O - u_{IN} + V_{B_p} - |V_{tp}|)^2$$
$$u_O = (i_{DS_n} - i_{DS_p})R_L. \quad (12)$$

For $u_{IN} = 0$ it is desired to be $u_O = 0$, which effectively means that $i_{DS_n} = i_{DS_p}$. This in combination with (12) implies that

$$\zeta_n(V_{B_n} - V_{tn})^2 = \zeta_p(V_{B_p} - |V_{tp}|)^2. \quad (13)$$

As both MOSFETs operate in strong–inversion, it is $V_{B_n} - V_{tn} > 0$ and $V_{B_p} - |V_{tp}| > 0$, leading to

$$V_{B_p} = \sqrt{\frac{\zeta_n}{\zeta_p}}(V_{B_n} - V_{tn}) + |V_{tp}|. \quad (14)$$

From (4) and (14) it is $V_A = (1 + \sqrt{\frac{\zeta_n}{\zeta_p}})(V_{B_n} - V_{tn})$, and so the required bias voltages for the power stage are

$$V_{B_n} = \frac{V_A}{1 + \sqrt{\frac{\zeta_n}{\zeta_p}}} + V_{tn}$$
$$V_{B_p} = \frac{V_A}{1 + \sqrt{\frac{\zeta_p}{\zeta_n}}} + |V_{tp}|. \quad (15)$$

2) POWER STAGE CURRENTS

Assuming that the DC bias voltage V_A has been selected according to equation (10), and that V_{B_n} and V_{B_p} are set following (15), the power stage currents i_{DS_n} and i_{DS_p} are derived. It is important to know their expressions since they are the loads of the buck–converters in Figure 3.

Setting $w_n \triangleq V_{B_n} - V_{tn}$ and $w_p \triangleq -V_{B_p} + |V_{tp}|$ in equation (12) implies that

$$u_O = R_L\Big\{\zeta_n\Big[w_n^2 + u_{IN}^2 + u_O^2 + 2w_n u_{IN} - 2w_n u_O - 2u_{IN}u_O\Big] - \zeta_p\Big[w_p^2 + u_{IN}^2 + u_O^2 + 2w_p u_{IN} - 2w_p u_O - 2u_{IN}u_O\Big]\Big\}. \quad (16)$$

From (13) it is $\zeta_n w_n^2 - \zeta_p w_p^2 = 0$, and from (15) it is derived that $\zeta_n w_n - \zeta_p w_p = V_A\sqrt{\zeta_n\zeta_p}$. Thus, after some algebra, equation (16) gives

$$(\zeta_n - \zeta_p)u_O^2 - \Big[2V_A\sqrt{\zeta_n\zeta_p} + 2(\zeta_n - \zeta_p)u_{IN} + \frac{1}{R_L}\Big]u_O + (\zeta_n - \zeta_p)u_{IN}^2 + (2V_A\sqrt{\zeta_n\zeta_p})u_{IN} = 0. \quad (17)$$

Dividing this equality with $\sqrt{\zeta_n\zeta_p} > 0$ results in

$$\phi u_O^2 - \left(2V_A + 2\phi u_{IN} + \frac{1}{R_L\sqrt{\zeta_n\zeta_p}}\right)u_O + \phi u_{IN}^2 + 2V_A u_{IN} = 0, \quad (18)$$

where

$$\phi \triangleq \frac{\zeta_n - \zeta_p}{\sqrt{\zeta_n\zeta_p}}. \quad (19)$$

Two cases can be distinguished; $\zeta_n = \zeta_p$ and $\zeta_n \neq \zeta_p$. If, in addition to $u_{IN} = 0 \Rightarrow u_O = 0$, it is assumed that $\zeta_n = \zeta_p = \zeta$, then $\phi = 0$ and (18) is transformed to

$$-\left(2V_A + \frac{1}{\zeta R_L}\right)u_O + 2V_A u_{IN} = 0, \quad (20)$$

leading to

$$u_O = k u_{IN}, \text{ with } k \triangleq \frac{2V_A\zeta R_L}{2V_A\zeta R_L + 1}. \quad (21)$$

The current–gain match of M_n and M_p results in a linear input–output relationship. Deviations between ζ_n and ζ_p will result in a nonlinear relationship, as $\phi \neq 0$ and the squared terms of u_{IN} and u_O in (18) will not be eliminated. This will in turn introduce distortion, which makes the sizing of the output devices for very close ζ_n and ζ_p values a desired and targeted design choice. Finally, for $\zeta_n = \zeta_p = \zeta$, equations (12), (15), and (21) result to the expressions of currents i_{DS_n} and i_{DS_p}

$$i_{DS_n} = \Big[\zeta(1-k)^2\Big]u_{IN}^2 + [\zeta(1-k)V_A]u_{IN} + \zeta\frac{V_A^2}{4}$$
$$i_{DS_p} = \Big[\zeta(1-k)^2\Big]u_{IN}^2 - [\zeta(1-k)V_A]u_{IN} + \zeta\frac{V_A^2}{4}. \quad (22)$$

B. POSITIVE– & NEGATIVE–RAIL BUCK–CONVERTERS

Analysis now turns to the converters that generate the tracking supply rails of the Class–CTA power stage. For simplicity, focus will be primarily on the positive–rail buck–converter, as the circuit is symmetrical; only the final results for the negative–rail one will be presented.

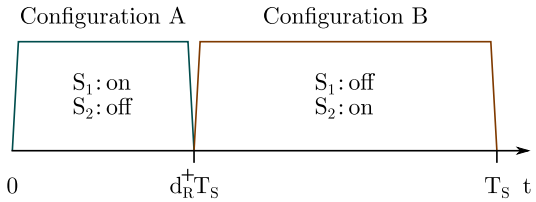

FIGURE 4. Positive–rail buck–converter configurations and timing.

1) STATE–SPACE MODELING

Within a switching period, T_S, the positive–rail buck–converter has two configurations, A and B, as depicted in Figure 4. During configuration A, when $t \in [0, d_R^+ T_S)$, switch S_1 is on and switch S_2 is off, with $d_R^+ \in [0, 1]$ being the converter's duty cycle. For this state, the equations that describe the circuit are

$$\begin{aligned} i_{L_1} &= i_{C_1} + i_R^+ \\ V_R &= i_{L_1}\left(R_{ON_1} + R_L^{ESR}\right) + u_{L_1} + u_R^+ \\ 2V_R &= i_{L_1}\left(R_{ON_1} + R_L^{ESR}\right) + u_{L_1} + i_{C_1} R_C^{ESR} + u_{C_1}. \end{aligned} \tag{23}$$

For configuration B of the converter, during $t \in [d_R^+ T_S, T_S)$, S_1 is off and S_2 is on; then, it is

$$\begin{aligned} i_{L_1} &= i_{C_1} + i_R^+ \\ -V_R &= i_{L_1}\left(R_{ON_2} + R_L^{ESR}\right) + u_{L_1} + u_R^+ \\ 0 &= i_{L_1}\left(R_{ON_2} + R_L^{ESR}\right) + u_{L_1} + i_{C_1} R_C^{ESR} + u_{C_1}. \end{aligned} \tag{24}$$

During both time intervals, the converter's output current is that of the NMOS transistor M_n in the Class–A power stage

$$i_R^+ = i_{DS_n}. \tag{25}$$

Given that the current relationship of i_R^+ and the desired tracking behavior of u_R^+ are known, one could attempt to solve the state–space equations (23) and (24) analytically, and acquire the exact solution over a switching period by means of continuity at the time of the configurations' switching. However, the design philosophy of the proposed architecture allows for a simpler analysis approach; given that the switching frequency, $f_S = 1/T_S$, is much higher than: (a) the maximum input signal frequency, (b) the natural frequencies of the converter, and (c) the frequencies of variations in the converter's inputs, it is concluded that time–averaging of (23) and (24) can be employed [30] instead of the more complicated exact solution. Thus, over a switching period, the time–averaging approach results in

$$\begin{aligned} i_{L_1} &= i_{C_1} + i_R^+ \\ \left(2d_R^+ - 1\right)V_R &= i_{L_1}\left[d_R^+ R_{ON_1} + \left(1 - d_R^+\right)R_{ON_2} + R_L^{ESR}\right] \\ &\quad + u_{L_1} + u_R^+ \\ u_{C_1} + i_{C_1} R_C^{ESR} &= u_R^+ + V_R, \end{aligned} \tag{26}$$

where the third equation results from subtracting the second one from the third in (23) and (24), and time–averaging.

Defining $x^+ = [u_{C_1} \;\; i_{L_1}]^\top$, $y^+ = u_R^+ + V_R$, and replacing i_{C_1} and u_R^+ of the first and third equations in (26) into the second one, it is derived that

$$\begin{aligned} \dot{x}^+ &= \begin{bmatrix} 0 & \frac{1}{C} \\ -\frac{1}{L} & -\frac{\left(R_L^{ESR} + R_C^{ESR} + R_{ON_2}\right)}{L} \end{bmatrix} x^+ + \begin{bmatrix} 0 \\ \frac{2V_R}{L} \end{bmatrix} d_R^+ \\ &\quad + \begin{bmatrix} -\frac{1}{C} \\ \frac{R_C^{ESR}}{L} \end{bmatrix} i_R^+ + \begin{bmatrix} 0 & 0 \\ 0 & \frac{R_{ON_2} - R_{ON_1}}{L} \end{bmatrix} x^+ d_R^+ \\ y^+ &= \begin{bmatrix} 1 & R_C^{ESR} \end{bmatrix} x^+ + \begin{bmatrix} -R_C^{ESR} \end{bmatrix} i_R^+. \end{aligned} \tag{27}$$

Equations in (27) form the (time–averaged) state–space representation of the positive–rail buck–converter when considering the duty cycle d_R^+ as the system's input and y^+ as its output. Similar analysis and reasoning leads to the corresponding state–space equation for the case of the negative–rail buck–converter

$$\begin{aligned} \dot{x}^- &= \begin{bmatrix} 0 & \frac{1}{C} \\ -\frac{1}{L} & -\frac{\left(R_L^{ESR} + R_C^{ESR} + R_{ON_4}\right)}{L} \end{bmatrix} x^- + \begin{bmatrix} 0 \\ \frac{2V_R}{L} \end{bmatrix} d_R^- \\ &\quad + \begin{bmatrix} -\frac{1}{C} \\ \frac{R_C^{ESR}}{L} \end{bmatrix} i_R^- + \begin{bmatrix} 0 & 0 \\ 0 & \frac{R_{ON_4} - R_{ON_3}}{L} \end{bmatrix} x^- d_R^- \\ y^- &= \begin{bmatrix} -1 & -R_C^{ESR} \end{bmatrix} x^- + \begin{bmatrix} R_C^{ESR} \end{bmatrix} i_R^-, \end{aligned} \tag{28}$$

where $x^- = [u_{C_2} \;\; i_{L_2}]^\top$ and $y^- = u_R^- - V_R$.

The term involving multiplication of the state vector and the input signal (duty cycle) makes systems (27) and (28) bilinear [31], and therefore their analysis and feedback design more challenging. However, the bilinear terms $x^+ d_R^+$ and $x^- d_R^-$ can be eliminated by sizing the switches such that $R_{ON_1} = R_{ON_2} = R_{ON_3} = R_{ON_4} = R_{ON}$; this is a convenient design choice. It is desirable to have similar voltage drop on the on–resistance of the converter's switches during its two operation states, and also to opt for similar behavior between the positive– and negative–rail buck–converters, as this favors the use of the same feedback scheme and the same L and C values.

2) SELECTION OF CONVERTERS' L & C VALUES

Based on the assumption of equal R_{ON} values of the switches that led to the elimination of the bilinear term in (27) and (28), one can proceed with the initial selection of the inductor and capacitor values for the two buck–converters.

At equilibrium,[1] $\dot{x}^+ = \dot{x}^- = 0$, and supply rails u_R^+ and u_R^- have reached their targeted values; thus, $u_R^+ = ku_{IN} + u_M$ and $u_R^- = ku_{IN} - u_M$ (recall that $u_O = ku_{IN}$). Replacing the above in the state–space equations (27) and (28), the equilibrium values of the converters' duty

1. According to the assumptions in Section III-B, the two converters must be sufficiently fast so that they always remain close to equilibrium independently of the power stage's input signal.

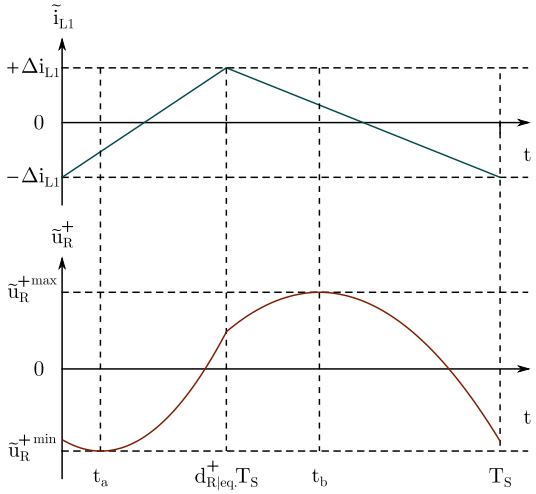

FIGURE 5. Positive–rail buck–converter's inductor current ripple and output voltage ripple waveforms.

cycles are derived

$$d^+_{R|eq.} = \frac{1}{2V_R}\Big[V_R + (ku_{IN} + u_M) + \Big(R_L^{ESR} + R_{ON}\Big)i_R^+\Big]$$
$$d^-_{R|eq.} = \frac{1}{2V_R}\Big[V_R - (ku_{IN} - u_M) + \Big(R_L^{ESR} + R_{ON}\Big)i_R^-\Big]. \quad (29)$$

Assuming small voltage ripple at the outputs of the two buck–converters, over a switching period the inductor current can be approximated by the superposition of a constant current component and a current ripple, $\tilde{i}_L$. The ripple can be approximated by a triangle waveform with zero mean value and maximum–minimum values of $\pm\Delta i_L$ [30], as depicted in Figure 5. In the positive–rail buck–converter, during time interval $[0, d^+_{R|eq.}T_S)$ the derivative of i_{L_1}, $\dot{i}_{L_1}$, can be approximated by

$$\dot{i}_{L_1} = \frac{2\Delta i_{L_1}}{d^+_{R|eq.}T_S}. \quad (30)$$

Within $[0, d^+_{R|eq.}T_S)$, equilibrium condition $\dot{x}^+ = 0$ applied to (27) results in $i_{L_1} = i_R^+ + \tilde{i}_L$, which is simplified to $i_{L_1} \simeq i_R^+$ by assuming the desirable condition that $|\Delta i_{L_1}| \ll i_R^+$. Combining this with (30) and (23) (where $u_{L_1} = L\dot{i}_{L_1}$) gives

$$L\frac{2\Delta i_{L_1}}{d^+_{R|eq.}T_S} = V_R - \Big[ku_{IN} + u_M + \Big(R_L^{ESR} + R_{ON}\Big)i_R^+\Big]. \quad (31)$$

To keep the current ripple below Δi_L^{max}, the inductor must be larger than the following bound

$$L > \frac{T_S}{4V_R\Delta i_L^{max}}\left\{V_R^2 - \Big[ku_{IN} + u_M + \Big(R_L^{ESR} + R_{ON}\Big)i_R^+\Big]^2\right\}. \quad (32)$$

The same result applies to the negative–rail buck–converter.

To keep voltage ripple small, capacitor C should be sufficiently large. A relationship between the voltage ripple and C is obtained by assuming that inductor's current ripple flows only through R_C^{ESR} and C, i.e., $\tilde{i}_{C_1} = \tilde{i}_{L_1}$, which is typically the case for a properly designed converter. For triangle–shaped inductor ripple current, in the case of the positive–rail buck–converter and for $t \in [0, d^+_{R|eq.}T_S)$ it is

$$\tilde{i}_{C_1} = \tilde{i}_{L_1} = \Delta i_{L_1}\left(\frac{2t}{d^+_{R|eq.}T_S} - 1\right)$$
$$\tilde{u}_{R_C^{ESR}} = \tilde{i}_{C_1}R_C^{ESR}$$
$$\tilde{u}_{C_1} = \frac{1}{C}\int_0^t \tilde{i}_{C_1}(\tau)d\tau = \frac{\Delta i_{L_1}}{C}\left(\frac{t^2}{d^+_{R|eq.}T_S} - t\right). \quad (33)$$

Similarly, for $t \in [d^+_{R|eq.}T_S, T_S)$ it is

$$\tilde{i}_{C_1} = \tilde{i}_{L_1} = \Delta i_{L_1}\left[\frac{1 + d^+_{R|eq.}}{1 - d^+_{R|eq.}} - \frac{2t}{\Big(1 - d^+_{R|eq.}\Big)T_S}\right]$$
$$\tilde{u}_{R_C^{ESR}} = \tilde{i}_{C_1}R_C^{ESR}$$
$$\tilde{u}_{C_1} = \frac{1}{C}\int_{d^+_{R|eq.}T_S}^t \tilde{i}_{C_1}(\tau)d\tau$$
$$= \frac{\Delta i_{L_1}}{C}\left[\frac{\Big(1 + d^+_{R|eq.}\Big)t - d^+_{R|eq.}T_S}{1 - d^+_{R|eq.}} - \frac{t^2}{\Big(1 - d^+_{R|eq.}\Big)T_S}\right]. \quad (34)$$

The total output voltage ripple is equal to $\tilde{u}_R^+ = \tilde{u}_{R_C^{ESR}} + \tilde{u}_{C_1}$ (Figure 5), and achieves its minimum and maximum values at $t_a = 0.5d^+_{R|eq.}T_S - CR_C^{ESR}$ and $t_b = 0.5(1+d^+_{R|eq.})T_S - CR_C^{ESR}$, respectively, with

$$\tilde{u}_R^{+min} = -\left(\frac{\Delta i_{L_1}R_C^{ESR^2}}{d^+_{R|eq.}T_S}C + \frac{\Delta i_{L_1}d^+_{R|eq.}T_S}{4}\frac{1}{C}\right)$$
$$\tilde{u}_R^{+max} = \frac{\Delta i_{L_1}R_C^{ESR^2}}{\Big(1 - d^+_{R|eq.}\Big)T_S}C + \frac{\Delta i_{L_1}\Big(1 - d^+_{R|eq.}\Big)T_S}{4}\frac{1}{C}. \quad (35)$$

Note that the expressions of the minimum and the maximum values of the ripple in (35) are valid when $t_a > 0$ and $t_b > d^+_{R|eq.}T_S$, respectively; otherwise $\tilde{u}_R^{+min}$ and $\tilde{u}_R^{+max}$ are only lower and upper bounds of the minimum and the maximum values, respectively.

Thus, for a targeted maximum ripple value of Δu_R^{max}, it is recommended to select the capacitor's value C between the following two bounds derived from (35)

$$C_{a,b} = \frac{\Big(1 - d^+_{R|eq.}\Big)T_S}{2\Delta i_L^{max}R_C^{ESR^2}} \times \left[\Delta u_R^{max} \pm \sqrt{\Delta u_R^{max^2} - \Big(\Delta i_L^{max}R_C^{ESR}\Big)^2}\right]. \quad (36)$$

Equation (36) also implies a lower limit on the desired voltage ripple; it should be $\Delta u_R^{max} \geq \Delta i_L^{max}R_C^{ESR}$, which is of course expected. The same results can be obtained for the negative–rail buck–converter.

Even though one would want both ripples to be very small in value to improve the proposed power stage's linearity, an upper bound of the LC product must also be estimated, since very large values will pose difficulties in tracking input signals with high rise or fall rates (but always within a bandwidth low enough with respect to the converters' switching frequency), and thus, performance degradation. To this end, the following simplified case is considered.

Assume that at $t = 0$ the tracking rail voltage $u_R^+(0)$ is close to its maximum allowed value ($\simeq V_R$) and that its derivative is equal to 0, i.e., $\dot{u}_R^+(0) = 0$. Moreover, to make the problem tractable, lets assume that $R_{ON} = R_L^{ESR} = R_C^{ESR} = 0$. At $t = 0^+$, output voltage u_O starts to rise with its maximum rate, $\rho > 0$, forcing the converter to configuration A (Figure 4). Current i_R^+ is also close to its maximum value, $i_R^+ = I_R^+$, and for simplicity it is assumed almost constant for a brief period of time. Then, it is

$$\begin{aligned} V_R - u_R^+ &= L\dot{i}_{L_1} \\ i_{L_1} &= C\dot{u}_R^+ + I_R^+, \end{aligned} \tag{37}$$

leading to

$$V_R = u_R^+ + LC\ddot{u}_R^+. \tag{38}$$

Differential equation (38) has the solution $u_R^+ = h_s \sin(\psi t) + h_c \cos(\psi t) + V_R$, where $\psi \triangleq 1/\sqrt{LC}$. With the initial conditions of $u_R^+(0)$ and $\dot{u}_R^+(0) = 0$, one derives

$$u_R^+ = V_R - \big[V_R - u_R^+(0)\big]\cos(\psi t). \tag{39}$$

From (39) it is seen that u_R^+ is a convex function of time within a certain time period from $t = 0$ and also $\dot{u}_R^+(0) = 0$. Assuming a large ψ value, and so a fast tracking response due to fast increase of $\dot{u}_R^+$, along with a relatively slow, approximate linear increase of u_O with rate ρ, implies that the voltage margin $u_R^+ - u_O$ attends its minimum value when the slope of u_R^+ equals ρ. Based on the above assumptions, this equation of slopes happens for small t, motivating the approximation $\psi t \ll 1$, giving $\sin(\psi t) \simeq \psi t$. Thus,

$$\dot{u}_R^+ = \psi\big[V_R - u_R^+(0)\big]\sin(\psi t) \simeq \psi^2\big[V_R - u_R^+(0)\big]t. \tag{40}$$

The slope of u_R^+ becomes equal to ρ at approximate time t_ρ

$$\psi^2\big[V_R - u_R^+(0)\big]t_\rho = \rho \Rightarrow t_\rho = \frac{\rho}{\psi^2\big[V_R - u_R^+(0)\big]}. \tag{41}$$

Therefore, the minimum margin voltage is

$$\begin{aligned} u_M^{min} &= u_R^+(t_\rho) - u_O(t_\rho) \\ &= V_R - \big[V_R - u_R^+(0)\big]\cos(\psi t_\rho) - \big[u_O(0) + \rho t_\rho\big] \\ &\simeq V_R - \big[V_R - u_R^+(0)\big]\left[1 - \frac{\psi^2 t_\rho^2}{2}\right] - u_O(0) - \rho t_\rho \\ &\simeq \underbrace{u_R^+(0) - u_O(0)}_{u_M} - \frac{\rho^2}{2\psi^2\big[V_R - u_R^+(0)\big]}. \end{aligned} \tag{42}$$

Thus, for u_M^{min} being larger than a minimum limit, $u_M^{min,lim}$, (42) leads to

$$\psi^2 > \frac{\rho^2}{2\big[V_R - u_R^+(0)\big]\Big(u_M - u_M^{min,lim}\Big)}, \tag{43}$$

which results in the upper bound of the LC product

$$LC < \frac{2\big[V_R - u_R^+(0)\big]\Big(u_M - u_M^{min,lim}\Big)}{\rho^2}. \tag{44}$$

C. OUTPUT–TRACKING RAILS CONTROL

Following the analysis of the buck–converters, one continues with the design of the feedback control scheme for the supply rails to track the output plus/minus the voltage margin, u_M. Given the previous simplifying assumption that all switches have the same on–resistance, both state–space systems of the two converters have the linear, time–invariant (LTI) form of[2]

$$\begin{aligned} \dot{x} &= Ax + Bd_R + Di_R \\ y &= Cx + Ei_R \end{aligned} \tag{45}$$

where the state vector is $x = [u_C \;\; i_L]^\top$, and matrices A, B, C, D, and E are defined in the obvious way according to equations (27) and (28).

1) OUTPUT FEEDBACK CONTROL SCHEME

A common approach is to employ static output feedback with integral action [32], i.e.,

$$\begin{aligned} \dot{\sigma} &= e = y - r \\ d_R &= f_{sat}(k_I\sigma + k_P e) \in [0, 1], \end{aligned} \tag{46}$$

with $k_I, k_P \in \mathbb{R}^{1\times 1}$ and $f_{sat}(\cdot)$ be a saturation function capturing the circuit–level behavior of duty cycle d_R; i.e., $f_{sat}(\eta) = \max[0, \min(\eta, 1)]$ implying that $d_R = k_I\sigma + k_P e$ under normal operating conditions with $k_I\sigma + k_P e \in (0, 1)$, resulting in the classic PI (proportional–integral) controller, and, saturating to 0 or 1 when $k_I\sigma + k_P e$ exceeds normal values.

For the positive– and negative–rail buck–converters it is selected $r^+ = u_O + u_M + V_R$ and $r^- = u_O - u_M - V_R$, respectively. Then, the closed–loop system is described by the following equations

$$\begin{aligned} \begin{bmatrix} \dot{x} \\ \dot{\sigma} \end{bmatrix} &= \begin{bmatrix} A + k_P BC & k_I B \\ C & 0 \end{bmatrix} \cdot \begin{bmatrix} x \\ \sigma \end{bmatrix} + \begin{bmatrix} -k_P B & D + k_P BE \\ -1 & E \end{bmatrix} \cdot \begin{bmatrix} r \\ i_R \end{bmatrix} \\ [y] &= [C \;\; 0] \cdot \begin{bmatrix} x \\ \sigma \end{bmatrix} + [0 \;\; E] \cdot \begin{bmatrix} r \\ i_R \end{bmatrix}. \end{aligned} \tag{47}$$

Scalar gain parameters k_I, k_P need to be selected such that the matrix

$$\begin{bmatrix} A + k_P BC & k_I B \\ C & 0 \end{bmatrix} \in \mathbb{R}^{3\times 3} \tag{48}$$

2. Strictly speaking, (45) should be written as $\dot{x}^\pm = A^\pm x^\pm + B^\pm d_R^\pm + D^\pm i_R^\pm$, $y^\pm = C^\pm x^\pm + E^\pm i_R^\pm$. However, the $''\pm''$ superscript is dropped for simplicity, keeping in mind that the matrix parameters have different values for the positive– and the negative–rail buck–converters.

is Hurwitz, while more elaborate placement of its eigenvalues can be done to optimize the controller's performance with respect to transient response and static error. If tracking proves insufficient, a complete PID (proportional–integral–derivative) controller should be considered. On the other hand, if static error is tolerable, the integral part of the control scheme can be omitted.

2) CONTROL SCHEME ROBUSTNESS

The proposed control scheme (46)–(47) was derived based on the simplifying assumption that $R_{ON_1} = R_{ON_2} = R_{ON_3} = R_{ON_4} = R_{ON}$. A plausible question is whether the controller is acceptable should this condition be violated, where the simplified LTI state–space systems are replaced by the original bilinear ones in (27) and (28). From Figure 3 it is evident that switches S_1 and S_4 will be realized by PMOS devices, with NMOS ones being used for S_2 and S_3; as such, a mismatch in their on–resistor values due to them being realized by different transistor types is to some extent expected.

Here, the bilinear system (27) is investigated in terms of stability; similar analysis holds for system (28). Dropping superscript $''+''$ for simplicity, equation (27) is rewritten as

$$\begin{aligned} \dot{x} &= (A + A_\delta d_R)x + Bd_R + Di_R \\ y &= Cx + Ei_R, \end{aligned} \tag{49}$$

where

$$A_\delta = \begin{bmatrix} 0 & 0 \\ 0 & \frac{R_{ON_2} - R_{ON_1}}{L} \end{bmatrix}. \tag{50}$$

Note that the LTI system (45) results from (49) when the bilinear coefficient A_δ is eliminated.

By adopting the PI controller scheme which was discussed in the previous subsection, the following dynamics for the closed–loop system is obtained

$$\begin{aligned} \begin{bmatrix} \dot{x} \\ \dot{\sigma} \end{bmatrix} &= \begin{bmatrix} (A + A_\delta d_R) + k_P BC & k_I B \\ C & 0 \end{bmatrix} \cdot \begin{bmatrix} x \\ \sigma \end{bmatrix} \\ &\quad + \begin{bmatrix} -k_P B & D + k_P BE \\ -1 & E \end{bmatrix} \cdot \begin{bmatrix} r \\ i_R \end{bmatrix} \\ [y] &= [C \;\; 0] \cdot \begin{bmatrix} x \\ \sigma \end{bmatrix} + [0 \;\; E] \cdot \begin{bmatrix} r \\ i_R \end{bmatrix}. \end{aligned} \tag{51}$$

Equation (51) is rewritten as

$$\begin{aligned} \dot{z} &= \mathcal{A}(d_R)z + \mathcal{B}u \\ y &= \mathcal{C}z + \mathcal{D}u, \end{aligned} \tag{52}$$

with $z = [x \;\; \sigma]^\top$ and $u = [r \;\; i_R]^\top$ being the augmented state and input vectors, respectively. Matrices $\mathcal{A}(d_R)$, $\mathcal{B}$, $\mathcal{C}$, and $\mathcal{D}$ are defined accordingly.

Matrix function $\mathcal{A}(d_R)$ is affine in the control signal d_R, i.e., $\mathcal{A}(d_R) = \mathcal{A}_o + \mathcal{A}_\delta d_R$ with

$$\mathcal{A}_o = \begin{bmatrix} A + k_P BC & k_I B \\ C & 0 \end{bmatrix}, \quad \mathcal{A}_\delta = \begin{bmatrix} A_\delta & 0 \\ 0 & 0 \end{bmatrix}. \tag{53}$$

As imposed by (46), the time–varying duty cycle d_R belongs to the convex set $[0, 1]$.

Proposition 1: If there exists a positive–definite symmetric matrix $P \in \mathbb{R}^{3\times 3}$ such that

$$\mathcal{A}^\top(\delta)P + P\mathcal{A}(\delta) < 0, \tag{54}$$

for $\delta = 0$ and $\delta = 1$, then, (54) is also valid for every value of δ in between, i.e., $\delta \in [0, 1]$. Moreover, due to the continuity of function $\mathcal{A}(\cdot)$ and that of the eigenvalues, as well as the compactness of $[0, 1]$, there exist constant $\gamma > 0$ such that

$$\mathcal{A}^\top(\delta)P + P\mathcal{A}(\delta) \leq -\gamma I \tag{55}$$

for every $\delta \in [0, 1]$, with I being the identity matrix.

Proof: This follows from the fact that $\mathcal{A}(\delta)$ is affine in δ and $[0, 1]$ is convex [33]. ■

Proposition 2: Assuming there exist $P \succ 0$ such that (54) is satisfied, then the system (52) is BIBO (Bounded–Input u, Bounded–Output y) stable.

Proof: Consider the Lyapunov Function V of the form

$$V = z^\top Pz, \tag{56}$$

where z is the augmented state and P is the positive–definite matrix satisfying (54) and (55). Then, it holds that

$$\lambda_{\min}(P)\|z\|^2 \leq V \leq \lambda_{\max}(P)\|z\|^2. \tag{57}$$

Given a control input $d_R = d_R(t) \in [0, 1]$, the time–derivative of V is

$$\begin{aligned} \dot{V} &= (\mathcal{A}(d_R)z + \mathcal{B}u)^\top Pz + z^\top P(\mathcal{A}(d_R)z + \mathcal{B}u) \\ &= z^\top \Big(\mathcal{A}^\top(d_R)P + P\mathcal{A}(d_R)\Big)z + 2z^\top P\mathcal{B}u \\ &\leq -\gamma\|z\|^2 + 2\|z\|\|P\mathcal{B}\|\|u\| \\ &\leq -\gamma\|z\|^2 + 2\|z\|\|P\mathcal{B}\|M, \end{aligned} \tag{58}$$

where M is an upper bound of $\|u\|$ set by the circuit. The $''$quadratic$''$ term $-\gamma\|z\|^2$ will dominate the $''$linear$''$ term $2\|z\|\|P\mathcal{B}\|M$ for large values of $\|z\|$ and so

$$\dot{V} \leq 0 \text{ for } \|z\| \geq \frac{2\|P\mathcal{B}\|M}{\gamma}, \tag{59}$$

which implies that for large values of $\|z\|$, $\dot{V}$ is negative which yields that V stays finite. Following that, it can be seen from (57) that $\|z\|$ has to stay finite and BIBO stability is shown. ■

Due to the affine $\mathcal{A}(\cdot)$, ensuring the stability of the bilinear system (52) requires the verification of only two linear matrix inequalities (LMIs), corresponding to the marginal values of d_R (this is encountered as Common Quadratic Lyapunov Function in the literature [33], [34]).

The set of LMIs described in (54) can be solved using any semi–definite programming suite (e.g., SDPT3 [35]) in standard computational platforms such as Python (e.g., cvxpy [36]), MATLAB (e.g., Yalmip [37]), etc. By checking condition (54), it can be ensured that the bilinear system is BIBO stable even for large mismatches in the on–resistances of the converters' switches that can result from their different transistor type characteristics.

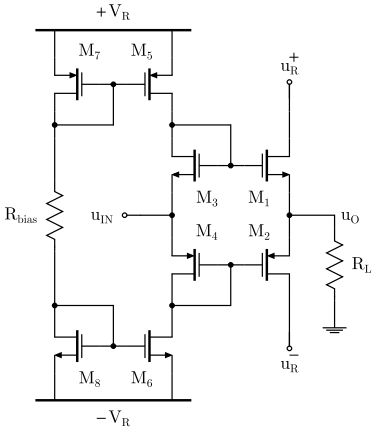

FIGURE 6. Class–CTA power stage.

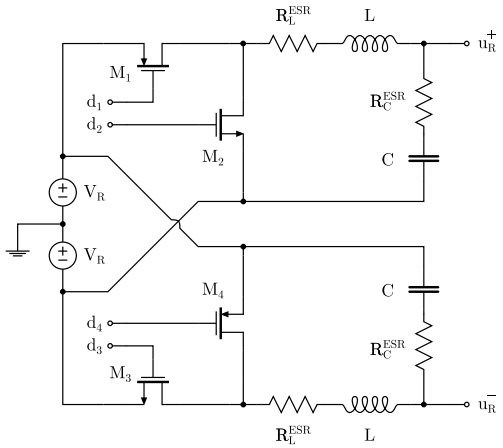

FIGURE 7. Positive– and negative–rail buck–converters of Class–CTA.

IV. PROOF–OF–CONCEPT IMPLEMENTATION

To validate the concept of the proposed architecture and demonstrate its performance potential, a Class–CTA power stage design example is given. For the purposes of this paper, this proof–of–concept design example is implemented and simulated at schematic–level in Cadence Spectre in ON Semi CMOS 0.35 µm technology, while its behavior is compared in terms of output spectrum (linearity) and efficiency versus the classic push–pull Class–A biasing scheme. Sizing of the involved elements was done using the theoretical analysis presented in the previous sections.

A. CIRCUIT IMPLEMENTATION

The push–pull Class–A power stage core of the implemented Class–CTA with its biasing network is given in Figure 6. The output devices are biased with a quiescent current of 385 mA and drive a classic 8 Ω load encountered in audio applications, while supply rails, $\pm V_R$, are set to ±6 V.

The two buck–converters in Figure 7 are equipped with $L = 33\,\mu H$ and $C = 470\,nF$, while $R_L^{ESR} = 50\,m\Omega$ and $R_C^{ESR} = 0.5\,\Omega$. The switching frequency is set to 5 MHz, complying with the assumption of Section III-B that enabled the time–averaging of the state–space model; the maximum

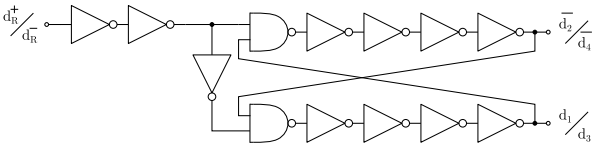

FIGURE 8. Non–overlapping clock generator.

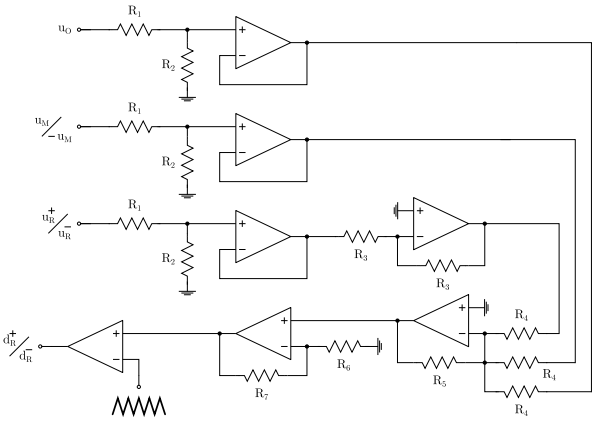

FIGURE 9. PWM control block.

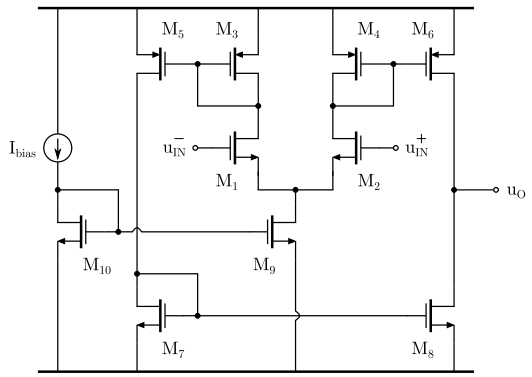

FIGURE 10. Operational amplifier used in the PWM control block.

signal frequency for audio is 20 kHz. The switches feature an average on–resistance of 353 mΩ to minimize voltage drop, and their control signals, d_1 to d_4, are provided by two non–overlapping clock generators like the one in Figure 8.

Tracking margin voltage, u_M, is selected to be 1 V, giving about a few hundred mV of u_{DS} saturation margin for the output devices and ensuring that both of them are always in strong–inversion. A simple proportional–only feedback control scheme is used, implemented by the network in Figure 9. With a selected gain of $k_P = 40$, the maximum observed error in the supply rails' tracking is minimal, without impact on Class–CTA's performance. For the amplifiers and the comparator of the PWM control block, the current–mirror operational amplifier of Figure 10 is used.

B. SIMULATION RESULTS

The proof–of–concept design was simulated at schematic–level over Slow, Typical, and Fast process corners, at

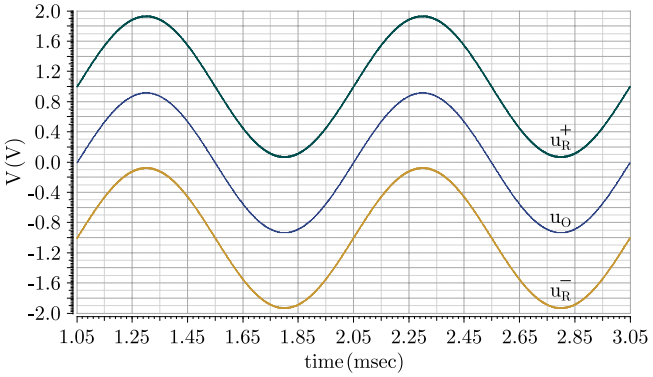

FIGURE 11. Class–CTA rails and output for an 1 kHz, 1 V input.

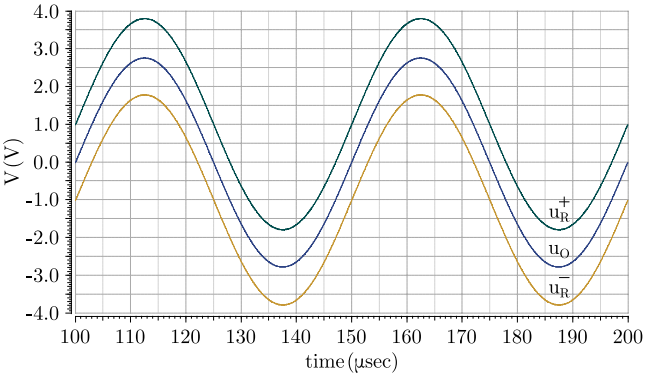

FIGURE 14. Class–CTA rails and output for a 20 kHz, 3 V input.

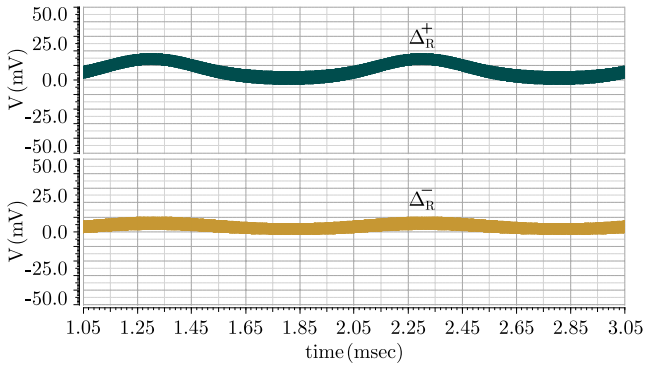

FIGURE 12. Class–CTA rails' error for an 1 kHz, 1 V input.

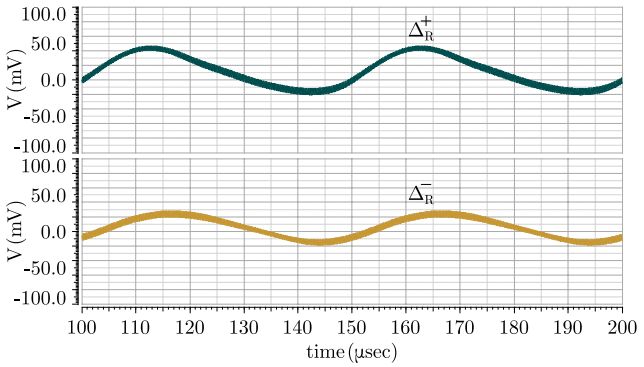

FIGURE 15. Class–CTA Rails' error for a 20 kHz, 3 V input.

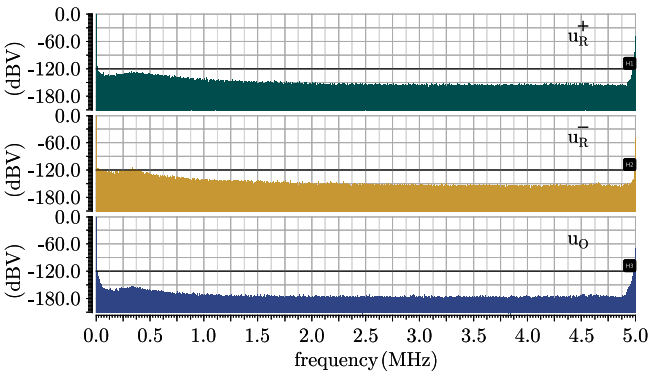

FIGURE 13. Class–CTA rails and output DFTs for an 1 kHz, 1 V input.

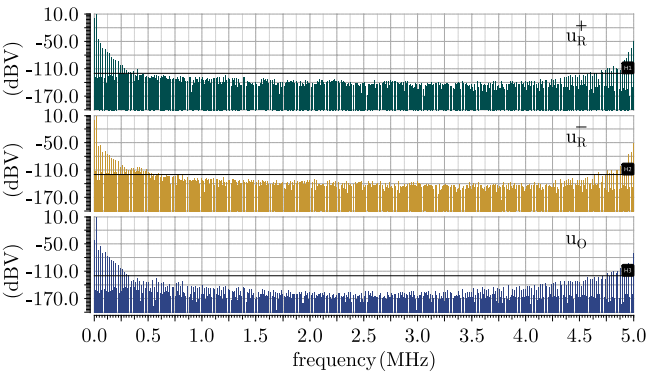

FIGURE 16. Class–CTA rails and output DFTs for a 20 kHz, 3 V input.

temperatures of −25 °C, 27 °C, and 125 °C. The figures in this section capture the behavior in Typical process, 27 °C. Maximum/minimum behavior results over corners are reported in the following paragraphs. Device mismatch does not pose any concern for the proposed architecture, since the topology has no matched pairs and no currents or voltages of critical accuracy.

Figure 11 presents the transient response of the power stage's output, positive–, and negative–rail, with a 1 kHz, 1 V peak input after settling has been achieved. The corresponding tracking errors are given in Figure 12, showing a maximum error value of 18.2 mV and 10.1 mV for the positive– and negative–rail, respectively. The error, $\Delta u_R^{\pm}$, is defined as the actual rail value minus the ideal target of $u_O \pm u_M$; minimum error values are −2.7 mV for the positive–rail and −1.6 mV for the negative–rail. Over corners, maximum and minimum error numbers are 26.1 mV, 24.2 mV, and −5.7 mV, −7.2 mV, respectively. Spectra of the three signals by means of discrete Fourier transform (DFT) are available in Figure 13; the 5 MHz spur is at a −48.8 dBV level for the positive–rail, at −49.5 dBV for the negative–rail, and at −67.9 dBV for the output of the power stage, where no filtering or feedback is applied. The corresponding minimum/maximum power levels over corners

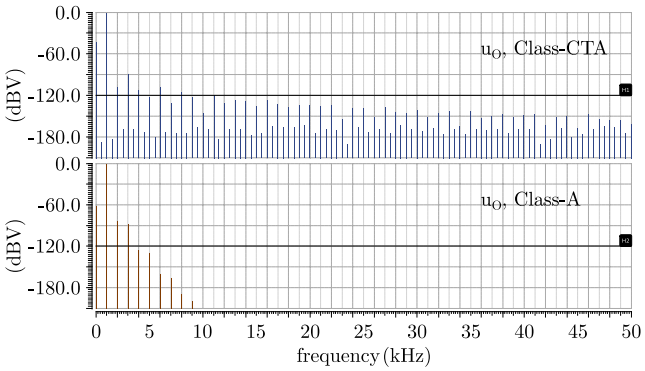

FIGURE 17. Class–CTA vs. Class–A output DFTs for an 1 kHz, 1 V input.

TABLE 1. Output harmonic levels for an 1 kHz, 1 V input over corners.

Harmonic	Class–CTA Worst/Typical/Best (dBV)	Class–A Worst/Typical/Best (dBV)
1st	−0.94/−0.68/−0.54	−0.88/−0.66/−0.53
2nd	−80.0/−107.8/−108.1	−77.0/−84.0/−93.7
3rd	−82.8/−88.8/−94.6	−83.8/−87.9/−90.7

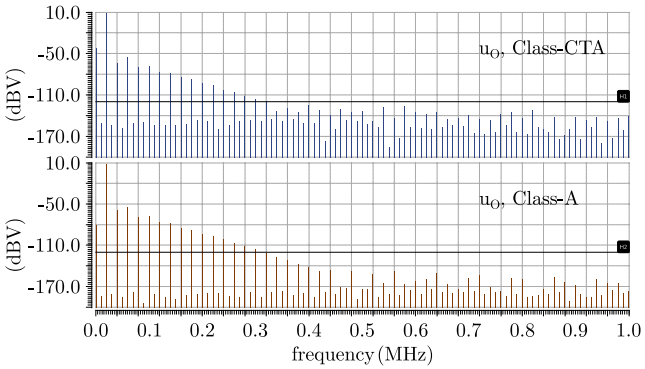

FIGURE 18. Class–CTA vs. Class–A output DFTs for a 20 kHz, 3 V input.

TABLE 2. Output harmonic levels for a 20 kHz, 3 V input over corners.

Harmonic	Class–CTA Worst/Typical/Best (dBV)	Class–A Worst/Typical/Best (dBV)
1st	8.56/8.85/9.00	8.62/8.87/9.00
2nd	−48.3/−64.0/−78.6	−44.1/−58.1/−66.0
3rd	−41.9/−54.7/−61.2	−42.3/−53.7/−59.5

range from −49.8 dBV/−49.1 dBV, −49.5 dBV/−49.1 dBV, and −69.4 dBV/−63.6 dBV, respectively. Due to the switching frequency being two orders of magnitude larger than the maximum input signal frequency, the switching spur can be easily suppressed further by the inclusion of an appropriate load capacitance without affecting performance.

Transient performance for a 20 kHz, 3 V peak input signal is shown next in Figure 14. Tracking of the output signal is again very good, with 46.6 mV of maximum error for the positive–rail, and 28.3 mV for the negative–rail being observed in Figure 15; minimum values are −20.0 mV and −18.5 mV, respectively. Maximum and minimum error values over process and temperature are 60.5 mV, 47.3 mV, and −26.8 mV, −51.2 mV. The strength of 5 MHz spur is similar to that in the previous case; Figure 16 indicates levels of −50.1 dBV, −49.9 dBV, −69.0 dBV for the positive–, negative–rail, and output, respectively. The minimum/maximum values for the corresponding power levels found from corners are −50.3 dBV/−50.0 dBV, −50.0 dBV/−49.8 dBV, and −65.3 dBV/−71.2 dBV.

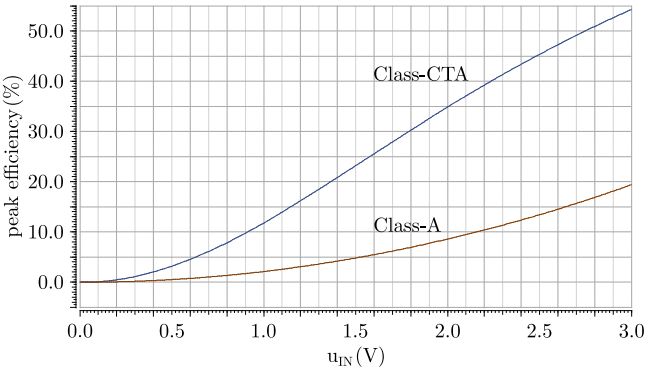

FIGURE 19. Class–CTA vs. Class–A power stage efficiency.

Finally, a comparison on Class–CTA power stage's linearity and efficiency against the competing push–pull Class–A scheme (where the power stage uses the fixed $\pm V_R$ supply), follows. Figures 17 and 18 depict the output DFT for the two schemes; horizontal lines at −120 dBV mark a negligible power level region. Linearity is excellent, with some indicative results on the levels of the fundamental (1st harmonic) and the dominant harmonic tones (2nd and 3rd) at the stage's output being gathered in Tables 1 and 2. For the vast majority of the simulated cases, the 2nd and 3rd harmonic tones of Class–CTA are at lower levels compared to the ones of Class–A operation, due to the almost constant u_{DS} of the output devices in the former case.

The power stage efficiency, evaluated as the ratio of the load power over the load power plus the power dissipated at the output transistors, is also greatly improved. Figure 19 presents the peak efficiency as a function of the input signal amplitude, and indicates that Class–CTA achieves peak numbers of 12.3% and 54.7% at an input signal of 1 V and 3 V peak, respectively; the corresponding numbers for the push–pull Class–A variant are 2.2% and 19.4%. For the same input amplitudes, over corners, the power stage efficiency ranges from 11.3%–13.3%, 53.0%–56.5% for Class–CTA, and from 1.9%–2.3%, 17.8%–20.7% for Class–A. The peak efficiency improvement gets more pronounced at lower input amplitudes, where a Class–A scheme suffers more. Opting for a lower tracking margin voltage in Class–CTA will lead to further improvement in its power stage's efficiency, as u_M is the decisive factor to the peak efficiency that can be achieved by the architecture.

V. CONCLUSION

A power stage architecture was introduced which combines high–linearity with high–efficiency. It uses a push–pull Class–A power stage core, with supply rails driven by two buck–converters. The supply rails continuously track the power stage's output voltage with small constant margins via feedback control. This results in a small and constant voltage drop on the output devices, significantly reducing power loss and improving linearity. The theoretical analysis of the architecture is presented and illustrated by means of a proof–of–concept design example. The simulation results highlight the advantages of the proposed architecture with respect to the classic push–pull Class–A power stage scheme.

REFERENCES

[1] D. Self, *Audio Power Amplifier Design*, 6th ed. New York, NY, USA: Focal Press, 2013.

[2] K. H. Yusof et al., "A systematic approach of generalized reactance compensation technique in wideband class-E power amplifier for lower high frequency (HF) bands," *IEEE Access*, vol. 11, pp. 77254–77266, 2023.

[3] S. Karmakar, M. Berkhout, K. A. A. Makinwa, and Q. Fan, "A –91 dB THD+N, class-D piezoelectric speaker driver using dual voltage/current feedback for resistor-less LC resonance damping," *IEEE J. Solid-State Circuits*, vol. 57, no. 12, pp. 3726–3735, Dec. 2022.

[4] H. Zhang, M. Berkhout, K. A. A. Makinwa, and Q. Fan, "A 121.4-dB DR capacitively coupled chopper class-D audio amplifier," *IEEE J. Solid-State Circuits*, vol. 57, no. 12, pp. 3736–3745, Dec. 2022.

[5] S.-H. Wen et al., "A load-adaptive class-G headphone amplifier with supply-rejection bandwidth enhancement technique," *IEEE J. Solid-State Circuits*, vol. 51, no. 10, pp. 2241–2251, Oct. 2016.

[6] A. Lollio, G. Bollati, and R. Castello, "Class-G headphone driver in 65nm CMOS technology," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC)*, 2010, pp. 84–85.

[7] S.-H. Wen et al., "A 130dB PSRR, 108dB DR and 95dB SNDR, ground-referenced audio decoder with PSRR-enhanced load-adaptive class-G 16Ohm headphone amplifiers," in *Proc. IEEE Asian Solid-State Circuits Conf. (A-SSCC)*, 2015, pp. 1–4.

[8] K. Cho and R. Gharpurey, "An efficient class-G stage for switching RF power amplifier applications," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 66, no. 4, pp. 597–601, Apr. 2019.

[9] N. Wolff, W. Heinrich, and O. Bengtsson, "The efficiency/bandwidth trade-off in class-G supply-modulated power amplifiers," in *Proc. Eur. Microw. Conf. (EuMC)*, 2017, pp. 472–475.

[10] S. Hu, S. Kousai, and H. Wang, "A broadband mixed-signal CMOS power amplifier with a hybrid class-G Doherty efficiency enhancement technique," *IEEE J. Solid-State Circuits*, vol. 51, no. 3, pp. 598–613, Mar. 2016.

[11] S.-W. Yoo, S.-C. Hung, and S.-M. Yoo, "A watt-level quadrature class-G switched-capacitor power amplifier with linearization techniques," *IEEE J. Solid-State Circuits*, vol. 54, no. 5, pp. 1274–1287, May 2019.

[12] M. Ma, F. You, Z. Xiao, T. Qian, Z. Tang, and S. He, "Design of multiphase class-G SCPA with enhanced efficiency," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, 2020, pp. 1–5.

[13] S.-C. Hung, S.-W. Yoo, and S.-M. Yoo, "A quadrature class-G complex-domain Doherty digital power amplifier," *IEEE J. Solid-State Circuits*, vol. 56, no. 7, pp. 2029–2039, Jul. 2021.

[14] K.-S. Choi, J. Ko, K.-M. Kim, J. Kim, and S.-G. Lee, "A 0.3-to-1-GHz IoT transmitter employing pseudo-randomized phase switching modulator and single-supply class-G harmonic rejection PA," *IEEE J. Solid-State Circuits*, vol. 57, no. 3, pp. 892–905, Mar. 2022.

[15] S. Sehajpal, S. S. Taylor, D. J. Allstot, and J. S. Walling, "Impact of switching glitches in class-G power amplifiers," *IEEE Microw. Wireless Compon. Lett.*, vol. 22, no. 6, pp. 282–284, Jun. 2012.

[16] X. Chen, M. Zhao, W. Chen, and Z. Feng, "A 700-2800MHz switchless class-G power amplifier with two-quadrant modulation for back-off efficiency improvement," in *Proc. IEEE/MTT-S Int. Microw. Symp. Tech. Dig.*, 2022, pp. 410–413.

[17] D. Li, W. Chen, and Z. Feng, "An x-band GaN HEMT high-efficiency switchless class-G power amplifier," in *Proc. IEEE MTT-S Int. Wireless Symp. (IWS)*, 2023, pp. 1–3.

[18] K. Higashiyama, "SPICE simulation of variant class-H hybrid power module," in *Proc. IEEE Japan Int. Electron. Manuf. Technol. Sympo.*, 1995, pp. 477–480.

[19] J. Gubelmann, P. D. Fabbro, M. Pastre, and M. Kayal, "High-efficiency dynamic supply CMOS audio power amplifier for low-power applications," *Microelectron. J.*, vol. 40, no. 8, pp. 1175–1183, 2009.

[20] X. Zhang and L. Siek, "A highly efficient, 420mW class-H headphone amplifier with single power supply rail," in *Proc. IEEE Int. Conf. Electr. Devices Solid-State Circuits (EDSSC)*, 2015, pp. 419–422.

[21] X. Zhang and L. Siek, "An 80.4% peak power efficiency adaptive supply class-H power amplifier for audio applications," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 25, no. 6, pp. 1954–1965, Jun. 2017.

[22] N. Utomo, L. Siek, H. G. Yap, D. Disney, L. Selvaraj, and L. Peng, "An 87% peak efficiency, 37W, class H audio amplifier with GaN output stage," in *Proc. IEEE Nordic Circuits Syst. Conf. (NORCAS) (NORCHIP) Int. Symp. Syst.-on-Chip (SoC)*, 2018, pp. 1–6.

[23] N. Utomo et al., "An 85.1% peak efficiency, low power class H audio amplifier with full class H operation," *IEEE Trans. Circuits Syst. I, Reg. Papers*, early access, Aug. 24, 2023, doi: 10.1109/TCSI.2023.3305622.

[24] J. Liu, Y. Allasasmeh, S. Gregori, B. Leesti, and M. Snelgrove, "An envelope tracking H-bridged audio amplifier with improved efficiency and THD less than 0.1%," in *Proc. 25th IEEE Can. Conf. Electr. Comput. Eng. (CCECE)*, 2012, pp. 1–4.

[25] G. Velasco-Quesada, M. Roman-Lumbreras, R. Perez-Delgado, and A. Conesa-Roca, "Class H power amplifier for power saving in fluxgate current transducers," *IEEE Sensors J.*, vol. 16, no. 8, pp. 2322–2330, Apr. 2016.

[26] S. S. Modi, P. T. Balsara, and O. E. Eliezer, "Reduced bandwidth class H supply modulation for wideband RF power amplifiers," in *Proc. IEEE Wireless Microw. Technol. Conf. (WAMICON)*, 2012, pp. 1–7.

[27] D. Baxevanakis, "Distortion estimation methodologies and architectures for high linearity and efficiency power amplifiers in CMOS Technologies," Ph.D. dissertation, School Electr. Comput. Eng., Nat. Tech. Univ., Athens, Greece, 2023.

[28] D. Johns, K. W. Martin, and T. C. Carusone, *Analog Integrated Circuit Design*, 2nd ed. Hoboken, NJ, USA: Wiley, 2011.

[29] R. J. Wiegerink, *Analysis and Synthesis of MOS Translinear Circuits*, 1st ed. New York, NY, USA: Kluwer Acad. Publ., 1993.

[30] R. W. Erickson and D. Marksimović, *Fundamentals of Power Electronics*, 2nd ed. New York, NY, USA: Kluwer Acad. Publ., 2004.

[31] D. L. Elliott, *Bilinear Control Systems—Matrices in Action*, 1st ed. Dordrecht, The Netherlands: Springer, 2009, doi: 10.1007/978-1-4020-9613-6.

[32] H. K. Khalil, *Nonlinear Systems*, 3rd ed. Upper Saddle River, NJ, USA: Prentice Hall, 2002.

[33] C. Briat, *Linear Parameter-Varying and Time-Delay Systems*. Heidelberg, Germany: Springer, 2015, doi: 10.1007/978-3-662-44050-6.

[34] J. Mohammadpour and C. W. Scherer, *Control of Linear Parameter Varying Systems With Applications*. New York, NY, USA: Springer, 2012, doi: 10.1007/978-1-4614-1833-7.

[35] K. C. Toh, M. J. Todd, and R. H. Tütüncü, "SDPT3 a MATLAB software package for semidefinite programming, version 1.3," *Optim. Meth. Softw.*, vol. 11, no. 1, pp. 545–581, 1999. [Online]. Available:https://doi.org/10.1080/10556789908805762

[36] S. Diamond and S. Boyd, "CVXPY: A Python-embedded modeling language for convex optimization," *J. Mach. Learn. Res.*, vol. 17, no. 83, pp. 1–5, 2016.

[37] J. Lofberg, "YALMIP: A toolbox for modeling and optimization in MATLAB," in *Proc. Conf. CACSD*, 2004, pp. 284–289.

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