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An Ultra-Low-Voltage Single-Crystal Oscillator-Timer (XO-Timer) Delivering 16-MHz and 32.258-kHz Clocks for Sub-0.5-V Energy-Harvesting BLE Radios in 28-nm CMOS

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ABSTRACT This paper reports an ultra-low-voltage (ULV) single-crystal oscillator-timer (XO-Timer) for sub-0.5 V Bluetooth low-energy (BLE) radios that aims for self-powering by harvesting the ambient energies. Specifically, we tailor an on-chip micropower manager (μPM) to customize the voltage and current budgets for each sub-function of the XO-Timer. Such μPM shows a high power efficiency by introducing a 3-stage cascaded structure and a single voltage-regulation loop; they together uphold the performance of the XO-Timer amid supply-voltage and temperature variations. The core amplifier of the XO-Timer is ULV-enabled, and is reconfigurable (i.e., 1-stage and 3-stage g_m) to balance between the power budget and performance under the high-performance mode (HPM) and low-power mode (LPM). Fabricated in 28-nm CMOS, the XO-Timer in HPM generates a 16-MHz clock with a power of 24.3 μW, and a phase noise of −133.8 dBc/Hz at 1-kHz offset, resulting in a Figure-of-Merit (FoM_1) of −236 dBc/Hz. In the LPM, the XO-Timer delivers a 32.258-kHz clock while consuming 11.4 μW. The sleep-timer FoM_2 is 14.8 μW and the Allan deviation is 35.1 ppb, achieving the lowest supply voltage (0.25 V) not only for a dual-mode XO-Timer but also for a MHz-range XO.

INDEX TERMS Bluetooth low-energy (BLE), clock, CMOS, crystal oscillator-timer (XO-Timer), energy harvesting, Internet-of-Things (IoT), micropower manager (μPM), ultra-low-power (ULP), ultra-low-voltage (ULV).

I. INTRODUCTION

INTERNET-OF-THINGS (IoT) has the potential to connect the world in a pervasive way and improve different industrial sectors such as logistics, healthcare, and smart cities. Still, the underlying challenges hindering its wide dissemination are the cost, power, and size limitations of the hardware. Batteries dominate the size and operating cost of the IoT networks as their replacement is highly labor-intensive, and their disposal incurs a high environmental cost [1]. An energy harvester (EH) that extracts the ambient energy is promising to prolong the lifetime of the batteries, or even replace them completely. Yet, the EH output voltage is deeply low (∼50 to 300 mV) and inexact [2], being highly difficult to comply with the standard analog and RF circuitries. The micropower manager (μPM) is a viable solution to customize and stabilize the EH output voltage (V_{EH}) [3], [4]. It tailors different voltages and loading currents using separated charge pumps

(CPs) and multiple voltage-regulation loops for the circuitries. Nevertheless, their power and area overheads are still high.

Besides the battery, another factor limiting the footprint of the IoT nodes is the crystal; typically there are two. The first generates a MHz-range reference clock for the RF phase-locked loop (PLL), where the aimed precision is ±50 ppm for the Bluetooth-Low-Energy (BLE) standard. The second is a kHz-range timer for synchronizing the IoT node in sleep mode. In light of the rapid downscaling of the CMOS technologies, the crystal's size (e.g., 3.2×2.5 mm^2) is comparable to the system chip, inevitably increasing the device's footprint and bill of material (BoM) cost. Although the integrated RC timers [5], [6], [7], [8] potentially eliminate the off-chip crystals, a μW-level timer usually has frequency stability >500 ppm. For instance, the frequency variations of the RC timer in [7] against voltage and temperature variation are 2.3% and 2.2%, which are much poorer than that of the crystal oscillators (XOs). Thus, there was ambition to implement a dual-mode XO that offers two clocks with one MHz-range crystal [9], [10], [11], [12]. Yet, their supply voltages are >0.9 V, requiring DC-DC converters to boost the voltages from the EH's output and penalizing the overall efficiency (e.g., 40 to 75% in [13]). In [9], the programmable loading capacitors (C_L) and frequency divider (DIV) enable the generation of a kHz-range timer by frequency division. Due to the fixed Pierce oscillator in both modes, the power is still sub-optimal (37 μW), limiting the effectiveness of duty-cycling the IoT radio. Recently, a single-XO-based clock-management IC was proposed [11]. It utilized a 76.8-MHz XO to provide the MHz-range signal and calibrate the machine-learning-based RC-oscillator to provide the 32.768-kHz clock. Yet, the RC-oscillator's high power consumption (48.2 μW) still renders it ill-suitable as a sleep timer. Hence, this project aims to develop a dual-mode reconfigurable single-crystal oscillator-timer (XO-Timer) directly powered by V_{EH} (0.25 to 0.3 V, 20% variation); it avoids the need for extra regulators that otherwise worsen the power efficiency, and balances the performance and power consumption for different scenarios.

This paper reports an ultra-low-voltage (ULV) XO-Timer suitable for sub-0.5 V BLE radios that target batteryless operation [14]. To supply the modules that require a higher voltage budget but with low current consumption, such as the DIV for the timer, bias circuit for the core amplifier (A_{XT}), and the mode control logic, we utilize a μPM to boost the voltage from the EH (0.25 V), and distribute multiple voltages to the modules accordingly. Unlike the traditional μPM [3], [4] that equip with separated CPs and multiple regulation loops, we co-design the XO-Timer and μPM with a cascaded 3-stage charge pump (CP), where its stage-to-stage voltages ($V_{EH}<V_{O,1}<V_{O,2}<V_{O,3}$) and currents ($I_{EH}>I_{O,1}>I_{O,2}>I_{O,3}$) are customizable for each module. As a result, it is more power-efficient to support different sub-functions according to their desired voltage-current budgets, avoiding excessive voltage headroom. Additionally, with a single voltage-regulation loop, the proposed μPM shields all internal voltages against the supply voltage V_{EH} (0.25 to 0.3 V) and temperature (−20 to 70 °C) variation with a targeted output ripple (5 mV at $V_{O,1}$), while the output ripple is scaled with V_{EH} in [3], [4]. Sharing a single 16-MHz crystal, our XO-Timer is reconfigurable to generate a 16-MHz reference clock for the radio's PLL by using a 1-stage g_m, and a 32.258-kHz clock as the sleep-timer that governs the radio's wake-up accuracy by a power-efficient 3-stage g_m. It attains a lower power consumption (24.3 μW for the 16-MHz clock and 11.4 μW for the timer) than the prior works with a state-of-the-art performance under a 0.25-V supply.

This paper has the following organization. Section II gives a system overview of the XO-Timer. Section III details the μPM, and its advantages over the previous topology. Section IV focuses on the design and analysis of the core amplifier of the XO-Timer. Section V discusses the measurement results, and finally, Section VI concludes the article and presents its key contributions.

II. SYSTEM OVERVIEW

Fig. 1 depicts the block schematic of our ULV XO-Timer. It features a fully on-chip μPM to interface with the EH. The μPM has two key functions: customize the internal voltage and current budgets for each sub-function, and regulate the internal voltages ($V_{O,1}$, $V_{O,2}$, $V_{O,3}$) and bias (V_{bias}) against the inexact V_{EH} and temperature.

The stage voltages ($V_{O,1}$, $V_{O,2}$, $V_{O,3}$) serve different purposes: $V_{O,1}$ powers up the DIV and part of the reconfigurable A_{XT}. The 2nd stage of the CP, $V_{O,2}$, powers the static sub-functions (e.g., reference generator and bias circuit) that demand less current but higher voltage headroom. The final stage, $V_{O,3}$, powers up the error amplifier (A_E) and the mode-control logic. The A_E and the reference generator form a global voltage-regulation loop to regulate the output voltages of the μPM against voltage and temperature variations. The most power-hungry sub-functions are the bootstrapped ring oscillator (BTRO) and reconfigurable core amplifier (A_{XT}). V_{EH} directly powers them to alleviate the power loss and cost of any interim converters or regulators. The 6-phase non-overlap clocks produced by the BTRO benefit the cascaded 3-stage CP to have smaller output ripples and eliminate the short-circuit current loss.

Associated with the μPM, the proposed reconfigurable A_{XT} is ULV-designed to operate with V_{DD} down to 0.25 V. The XO-Timer generates a 16-MHz clock in the high-performance mode (HPM) for the circuits that require better spectral purity, such as the PLL and analog-to-digital converter (ADC). The 1-stage g_m dominates the power in the HPM and allows a clock signal with low phase noise (PN). The always-on timer is available in both HPM and low-power mode (LPM) for timekeeping. The DIV divides the 16-MHz clock by 496 to obtain a 32.258-kHz clock. Further, in the LPM, we adopt a 3-stage g_m, plus C_L reduction to power-efficiently sustain the oscillation on the crystal. Hence, our

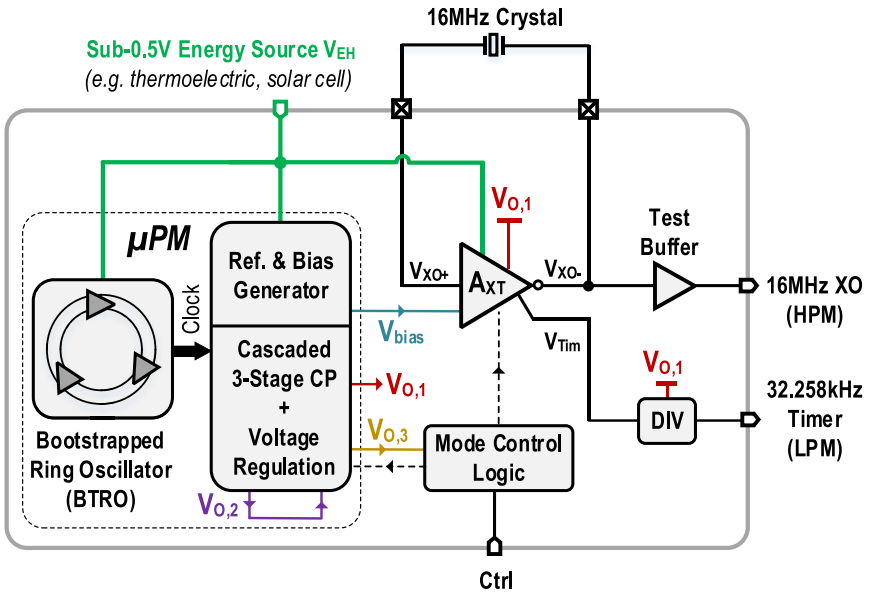


FIGURE 1. Proposed ULV XO-Timer delivering a 16-MHz clock and a 32.258-kHz timer from a single 16-MHz crystal. The on-chip μPM aids in tolerating V_{EH} variation and customizing the internal voltages and currents. An ULV-enabled reconfigurable A_{XT} balances the power and performance in the HPM and LPM.

reconfigurable A_{XT} can provide the clock for the PLL and the always-on timer from a single 16-MHz crystal under an inexact ULV V_{EH} and temperature, while balancing the power budget with the performance.

III. MICROPOWER MANAGER (μPM)

The μPM (Fig. 2) boosts the low-and-unstable V_{EH} to high-and-regulated voltage levels for different sub-functions. It aims to cover V_{EH} of 0.25 to 0.3 V (20% variation) and a temperature range of −20 to 70 °C. The nominal output voltages are $V_{O,1} = 0.37$ V, $V_{O,2} = 0.7$ V, and $V_{O,3} = 1$ V, under $V_{EH} = 0.25$ V.

A. CASCADED 3-STAGE CP

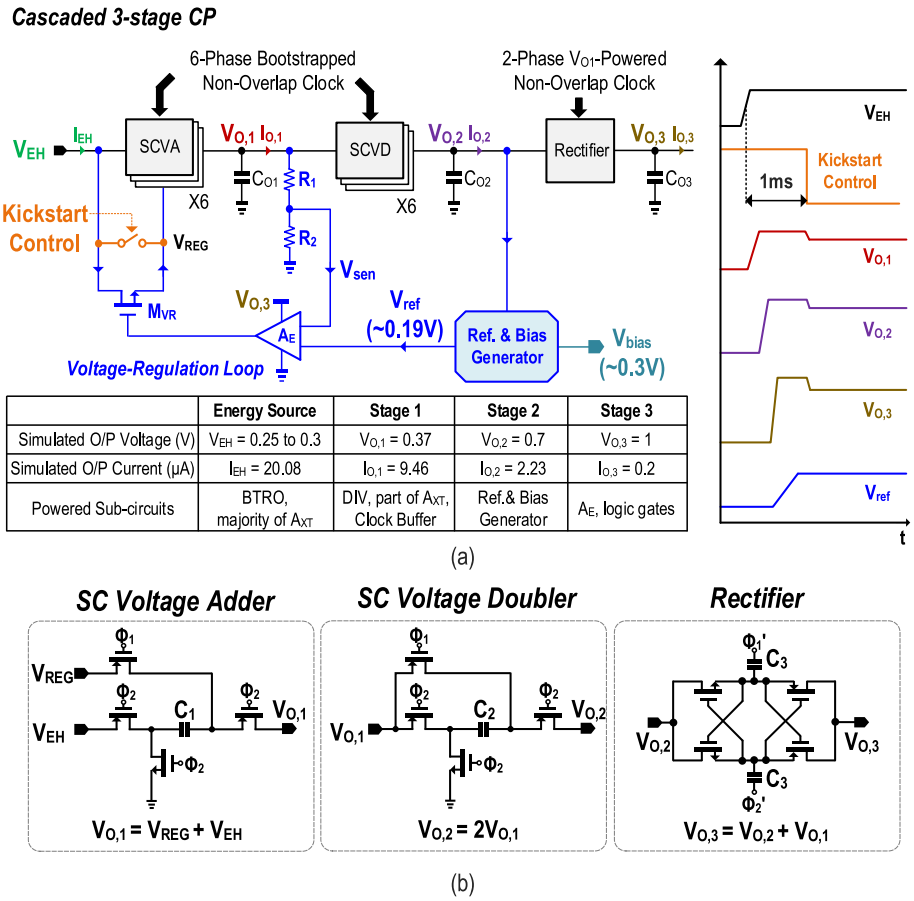
The μPM dominates the total power budget of the XO-Timer. Thus, we contrive a μPM topology that exhibits a high power efficiency. The conventional μPM [3], [4] employs separated CPs and multiple voltage-regulation loops to generate different output voltages, which requires individual switching clocks. Herein, we propose a μPM with a cascaded 3-stage CP and a single voltage-regulation loop to reduce the power and area overheads, described as follows: A switched-capacitor voltage adder (SCVA) heads our cascaded 3-stage CP [Fig. 2(b)]. The complementary non-overlap clocks $\Phi_{1,2}$ control the switches for each unit cell. When Φ_1 is low, V_{REG} (generated by the regulator to stabilize $V_{O,1}$, detailed in Section III-C) charges the flying capacitor C_1 (25 pF). In the next phase, when Φ_2 is low, the bottom plate of C_1 is boosted to V_{EH}. Together with the charges stored in C_1 in the previous phase, the output voltage V_{out} equals the sum of V_{REG} and V_{EH}. The simulated nominal $V_{O,1}$ is pitched to 0.37 V by the regulation loop. This $V_{O,1}$ is offered to the DIV, part of the reconfigurable A_{XT}, and the subsequent stage of the CP. They together draw 9.46 μA from $V_{O,1}$.

The 2nd stage of the CP is a switched-capacitor voltage doubler (SCVD), which is similar to the SCVA with its unit cell shown in Fig. 2 (b) and C_2 is 6.16 pF. Theoretically, its output voltage $V_{O,2}$ is 2× $V_{O,1}$. The simulated $V_{O,2}$ is 0.7 V. This $V_{O,2}$ powers up the reference generator for the regulation loop, the bias circuit for the reconfigurable A_{XT}, and the 3rd stage of CP, which altogether draw 2.23 μA of current.

The final stage of the CP is a single cross-coupled rectifier (C_3: 2.8 pF), as shown in Fig. 2(b). The BTRO generates its switching clocks with $V_{O,1}$ regulating the swing. Hence, the output voltage of this rectifier ($V_{O,3}$) is $V_{O,2} + V_{O,1}$. With a simulated $V_{O,3}$ of 1 V, this stage supplies a differential amplifier A_E with an active current-mirror load to secure the robustness of the regulation loop. Further, it also powers the mode control logic for μPM and A_{XT}. Its current budget is 0.2 μA, which has a negligible impact on the system's overall efficiency.

B. NON-OVERLAP BOOTSTRAPPED RING OSCILLATOR

We can upsize the SCVA and SCVD to raise their output-current capacity and reduce the output ripples by parallelizing 6-unit cells with 6 clock phases [15], [16], [17]. A 3-stage differential BTRO [18], directly powered by V_{EH} for self-startup, generates their 6-phase non-overlap clock (Fig. 3). The swing-boosted clock reduces the loss of the CP and avoids extra clock buffers by using the bootstrapped capacitor C_b. The differential bootstrapped inverter generates complementary clocks $Out_{+/-}$ with swing from $-V_{EH}$ to $2V_{EH}$. Each of these six outputs drives the non-overlap clock generator to deliver non-overlap clocks to reduce the



	Energy Source	Stage 1	Stage 2	Stage 3
Simulated O/P Voltage (V)	V_{EH} = 0.25 to 0.3	$V_{O,1}$ = 0.37	$V_{O,2}$ = 0.7	$V_{O,3}$ = 1
Simulated O/P Current (μA)	I_{EH} = 20.08	$I_{O,1}$ = 9.46	$I_{O,2}$ = 2.23	$I_{O,3}$ = 0.2
Powered Sub-circuits	BTRO, majority of A_{XT}	DIV, part of A_{XT}, Clock Buffer	Ref.& Bias Generator	A_E, logic gates

FIGURE 2. (a) Proposed μPM featuring a cascaded 3-stage CP and a single voltage-regulation loop. Simulated output voltages and currents also shown. Its stage-to-stage voltages ($V_{O,1} < V_{O,2} < V_{O,3}$) and currents ($I_{O,1} > I_{O,2} > I_{O,3}$) are customizable for each sub-function of the XO-Timer. (b) Implementation of the unit cell of SCVA, SCVD, and rectifier.

short-circuit current within the SCVA/SCVD. The NOR and NOT gates within the non-overlap clock generator are also bootstrapped. We also utilize a pair of regular inverters D powered by $V_{O,1}$ to drive the rectifier. From the simulation, the 6-phase operation of the SCVA and SCVD allows a 48.6% reduction of the total smoothing capacitors (C_{O1-2}) under the same output ripple target (i.e., 5 mV at $V_{O,1}$).

C. VOLTAGE REGULATION

Our voltage-regulation loop uses the A_E and a reference generator to globally regulate all internal voltages. During the startup, the voltage reference and error amplifier (A_E) take time to enter steady-state and their output may not be accurate. Hence, a kickstart switch aids in securing a robust startup by forcing $V_{REG} = V_{EH}$ (Fig. 2). After voltage reference and A_E entering the steady-state (1 ms in our design to cope with PVT variations), the kickstart switch is disabled. Then A_E compares V_{SEN} (scaled from $V_{O,1}$ by R_1 and R_2) with the reference voltage V_{REF}. Together with M_{VR}, they can control V_{REG} and thus regulate $V_{O,1}$ as well as $V_{O,2}$ and $V_{O,3}$. Fig. 2(a) shows the timing diagram of the kickstart control, V_{REF}, $V_{O,1}$ $V_{O,2}$ and $V_{O,3}$ during the startup.

Our reference generator operates under a wide supply voltage range of 0.5 to 0.9 V [19]. The transistors work in the subthreshold region with low gate-to-source voltages (~0.2 to 0.3 V). The simulated power consumption of the voltage reference is 181 nW at $V_{O,2} = 0.7$ V. V_{REF} is 0.19 V and its simulated line sensitivity is 0.24%/V.

Fig. 4 (a) shows the simulated $V_{O,1}$, $V_{O,2}$, and $V_{O,3}$ against supply-voltage variation at room temperature with and without the regulation loop. Without the regulation loop, the simulated line regulations ($\Delta V_{OUT}/\Delta V_{IN}$) are 1.9 V/V, 3.1 V/V, and 4.8 V/V, for $V_{O,1}$, $V_{O,2,}$ and $V_{O,3}$, respectively. They improve to 0.2 V/V, 0.97 V/V, and 1.46 V/V with the regulation loop in-place. Similarly, Fig. 4(b) plots the simulated $V_{O,1}$, $V_{O,2}$, and $V_{O,3}$ against temperature variation at $V_{EH} = 0.25$ V with and without the regulation loop. Without the regulation loop, $V_{O,3}$ significantly exceeds the device voltage limit (>1.18 V). In contrast, with the regulation loop, $V_{O,3}$ is limited to <1.06 V. Besides, as shown in Fig. 4(c), the regulation loop also reduces the power of the μPM by 1.72× at $V_{EH} = 0.25$ V. The overall power efficiency of cascaded 3-stage CP is 47.8%. The M_{VR} [Fig. 2(a)] consumes 25.5% of power to safeguard the operation of the μPM against supply-voltage and temperature variation. The

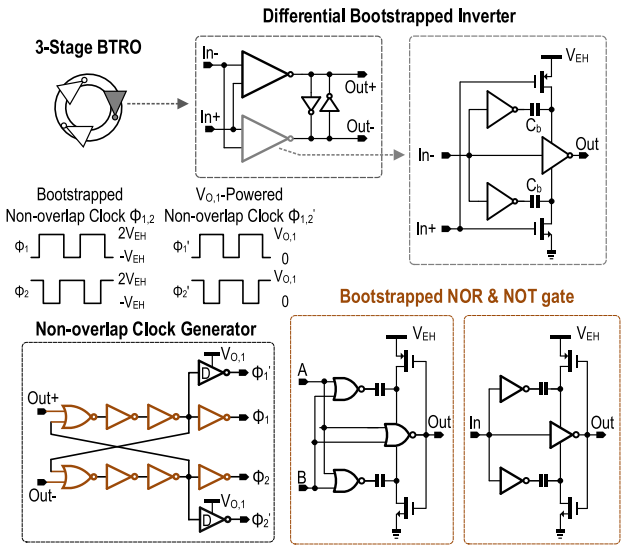


FIGURE 3. The schematics of the BTRO to achieve a swing of 3× V_{EH}. We utilize non-overlap clock generators to obviate the short-circuit current loss within the SCVA and SCVD. The logic elements within the non-overlap clock generators are also bootstrapped logic gates powered by V_{EH}, except D which generate Φ_1' and Φ_2' are regular inverters powered by $V_{O,1}$.

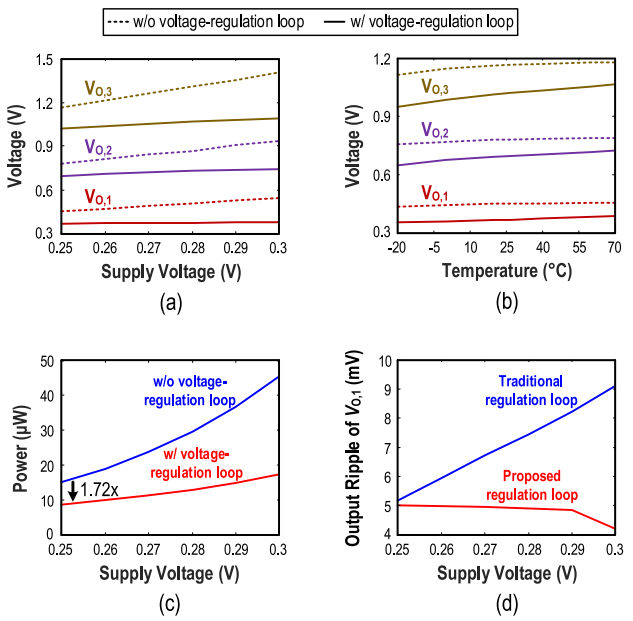


FIGURE 4. Output voltages of each stage with and without the voltage-regulation loop versus (a) V_{EH} and (b) temperature. (c) Simulated power consumption of the μPM with and without the voltage-regulation loop versus V_{EH}. (d) Simulated output ripple at $V_{O,1}$ of traditional regulation loop and proposed regulation loop.

power efficiencies of the 1st, 2nd, and 3rd stages of the CP are 93.3%, 60.3%, and 34.8%, respectively. The power efficiency decreases at the subsequent stages as the shunt loss is proportional to $V_o^2 C_p$, where C_P is the parasitic capacitance [17]. In our design, the parasitic capacitances from the flying capacitors dominate C_P. Thus, we downsize the flying capacitors for the subsequent stages as $C_1 > C_2 > C_3$ to reduce the C_P and the power loss. This reasoning justifies

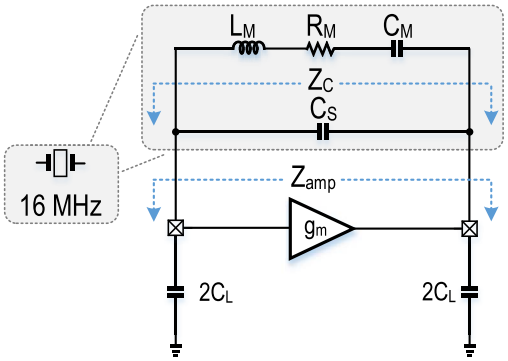


FIGURE 5. One-stage Pierce Oscillator where L_M, R_M and C_M are the motional inductance, motional resistance, and motional capacitance, respectively, and C_S is the parasitic capacitance of the crystal package.

the design viewpoint that $I_{O,1} > I_{O,2} > I_{O,3}$ since the subsequent stage cannot supply heavy load due to the small flying capacitor.

The traditional μPM utilizes separate regulation loops for each output and alters the BTRO's frequency to regulate the output voltages [3], [4]. This architecture leads to two critical drawbacks. First, when V_{EH} increases, the loop reduces the switching frequency of the BTRO to maintain the output voltages. Hence, the output ripple deteriorates, aggravating the reference spur to the XO-Timer. Fig. 4(d) depicts the output ripple of $V_{O,1}$ against V_{EH} for both the traditional and proposed regulation loops. The output ripple of the proposed structure improves as V_{EH} increases, along with the frequency of the BTRO, in contrast to the traditional approach. The output ripple minimization of $V_{O,2}$ and $V_{O,3}$ is consistent with $V_{O,1}$; the output ripples on $V_{O,2}$ and $V_{O,3}$ are 4.6 and 2.4 mV, respectively. Additionally, most blocks powered by $V_{O,2}$ and $V_{O,3}$ are for control logic, which are insensitive to the ripple, except for the biasing circuit of A_{XT}, whose PSRR at 16 MHz is -10 dB. Second, in the traditional μPM, multiple BTROs are compulsory for different CPs to regulate their output voltages, while only one BTRO is necessary for our architecture. From the simulation, with identical output voltages and currents, the power consumption of the proposed μPM is 8.7 μW, while that of the traditional μPM is 12 μW, attributable to the extra two BTROs.

IV. ULV RECONFIGURABLE CORE AMPLIFIER AXT

The Pierce Oscillator (Fig. 5) with an optimum C_L is well-suited as the XO due to its simplicity and low PN profile [20]. The motional inductance L_M, motional resistance R_M, motional capacitance C_M and the parasitic capacitance of the crystal package C_S form the equivalent circuit of the crystal unit. We can determine the characteristics and performance of the XO with the small-signal impedance Z_C sensed from the motional branch. The negative resistance, defined as

$$R_N \equiv -Re(Z_C) \quad (1)$$

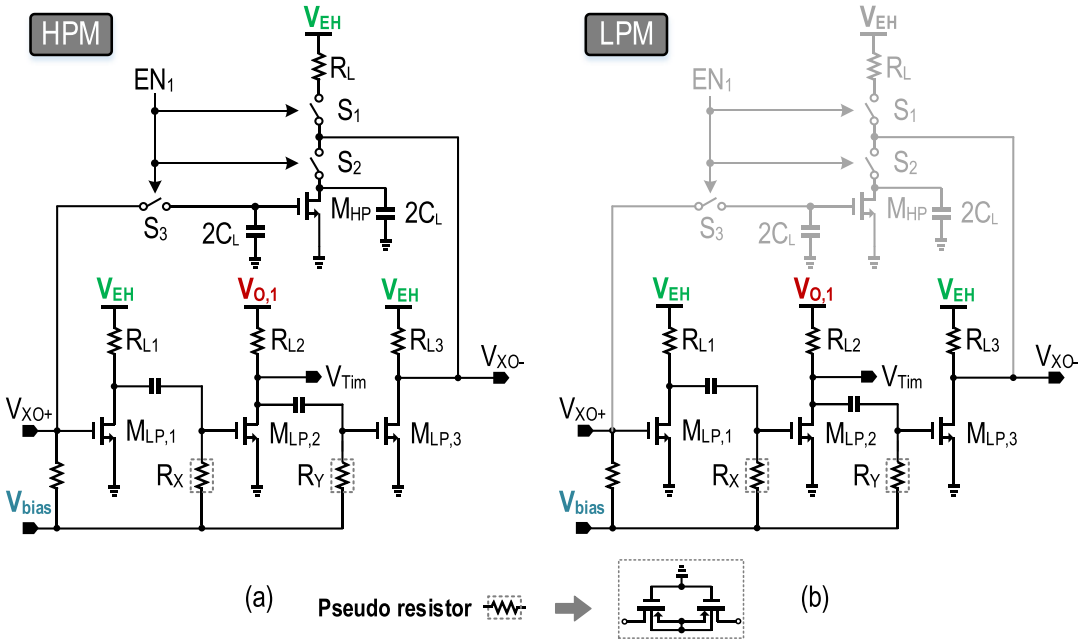


FIGURE 6. Reconfigurable core amplifier (A_{XT}) in the (a) HPM and (b) LPM.

should be larger than R_M to compensate for the loss of the crystal and sustain the oscillation. With a MHz-range 1-stage Pierce Oscillator, the power consumption is at tens of μW, rendering it sub-optimal as the sleep-timer [21], [22].

Compared with the 1-stage g_m, a multi-stage g_m [20], [23] can provide a higher transconductance-over-current ratio with the effective g_m of the amplifier boosted by the gains of the preceding stages. Usually, we choose C_L as specified by the manufacturer to obtain an accurate frequency. For the sleep-timer with the frequency accuracy relaxed, keeping such a specified C_L is not mandatory. Since R_N is inversely proportional to C_L^2, we can set a lower g_m with a reduced C_L while maintaining the R_N, resulting in a lower power budget for A_{XT}. To this end, we propose a reconfigurable A_{XT} featuring different g_m in the HPM and LPM [Fig. 6(a) and (b)]. A 3-stage g_m with C_L reduction secures R_N and sustains the oscillation of the XO with reduced power consumption in the LPM. In the HPM, we juxtapose a conventional 1-stage g_m with the 3-stage g_m to provide an oscillation signal with a premium PN.

Fig. 6(b) presents the reconfigurable A_{XT} in the LPM, which is a 3-stage cascaded common-source (CS) amplifier. The first two stages provide gain to the third stage, thus boosting the effective g_m of the A_{XT} to:

$$g_{m,tot-3} = g_{m1}R_{out1}g_{m2}R_{out2}g_{m3} \tag{2}$$

where R_{out1} (R_{out2}) stands for the parallel resistance of R_{L1} and R_X (R_{L2} and R_Y). Also, we remove C_L from the 3-stage g_m. Still, there are residue capacitances from the I/O pads and the PCB traces (~4 pF on each node). Fig. 7(a) plots the R_N as a function of the total bias current at room temperature, manifesting the improvement brought by the 3-stage g_m plus

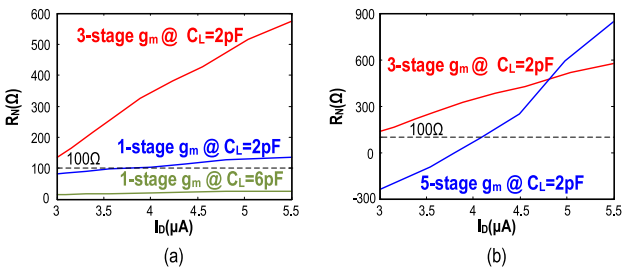


FIGURE 7. (a) R_N of 1-stage g_m with C_L of 6 pF and 2 pF, and 3-stage g_m with C_L of 2 pF versus I_D at room temperature. (b) R_N of the 3-stage g_m and 5-stage g_m versus I_D at room temperature. For (a) and (b), R_N = 100 Ω are depicted with the black dashed line.

C_L reduction. R_N should be >100 Ω to cover the R_M variation of different crystals (measured R_M: 42.5 Ω). Yet, for the 1-stage g_m without C_L reduction, R_N is <30 Ω for I_D < 5.5 μA. If we downsize C_L to 2 pF, R_N of the 1-stage g_m can increase. Then, it is still <100 Ω with I_D < 4 μA. To further R_N, we reconfigure A_{XT} as a 3-stage g_m. With both techniques applied, we obtain R_N > 100 Ω over a wide current range (3 to 5.5 μA). For instance, when I_D = 5.5 μA, R_N of the 3-stage-g_m is >574 Ω, which is ~4.2× larger than that only with C_L reduction.

Theoretically, we can add the number of stages to achieve a higher R_N. Yet, 3-stage g_m is adequate here for two reasons. First, under the same current budget, increasing the number of stages results in a lower current for each stage. Consequently, the preceding stages take up most of the current to secure the bandwidth, leaving a tiny budget for the final stage. Verified from simulation, R_N of 3-stage g_m is larger than that of 5-stage g_m when I_D <4.7 μA [Fig. 7(b)]. Second, the R_N of a 3-stage g_m is less sensitive to PVT

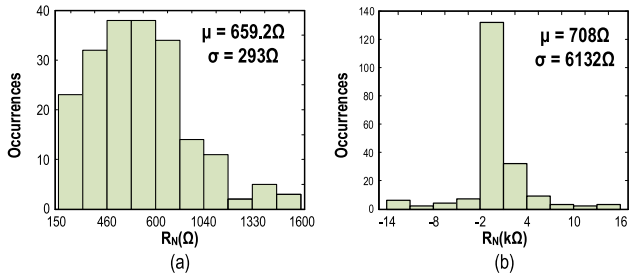


FIGURE 8. 200-run Monte-Carlo R_N simulation: (a) 3-stage g_m and (b) 5-stage g_m.

variations than that of a 5-stage g_m. Considering a 5-stage g_m, we can express the effective g_m as:

$$g_{m,tot-5} = g_{m1}R_{out1}g_{m2}R_{out2} \\ g_{m3}R_{out3}g_{m4}R_{out4}g_{m5} \quad (3)$$

To simplify the discussion, we omit C_S here. Also, we assume an equal distribution of the total current (thus g_m) to each stage for both 3-stage and 5-stage g_m. The impedance Z_{amp} across the amplifier (Fig. 5) is:

$$Z_{amp} = \frac{-g_m}{4\omega_0^2 C_L^2} + \frac{1}{j\omega_0 C_L} \quad (4)$$

Substituting (2) and (3) into (4) with R_{out1}, R_{out2}, R_{out3}, and R_{out4} regarded as R, g_{m1}, g_{m2}, g_{m3}, g_{m4}, and g_{m5} regarded g_m/N where N is the number of the stages, the R_N of the 3-stage and 5-stage-g_m are:

$$R_{N,3} = \frac{-\left(\frac{g_m}{3}\right)^3 R^2}{4\omega_0^2 C_L^2} \quad (5)$$

$$R_{N,5} = \frac{-\left(\frac{g_m}{5}\right)^5 R^4}{4\omega_0^2 C_L^2} \quad (6)$$

We can express the relative sensitivity of R_N to g_m as:

$$S = \frac{\frac{\partial R_N}{R_N}}{\frac{\partial g_m}{g_{m,tot}}} \quad (7)$$

Hence, the relative sensitivity of R_N to g_m for the 3-stage g_m and 5-stage g_m are $S_3 = 3$ and $S_5 = 5$, respectively, signifying that the sensitivity of R_N to g_m is commensurate with N. From the Monte-Carlo simulation, the average R_N of 3-stage g_m is 659 Ω (minimum: 165 Ω) with $I_D = 5.5$ μA (Fig. 8). Under the same current budget, the standard deviation of R_N of 5-stage g_m is 20.9× larger than that of 3-stage g_m, and 20% of R_N is <100 Ω.

Tuning the C_L results in a frequency deviation from the nominal frequency. The frequency deviation between HPM and LPM can be formulated as:

$$\frac{\Delta f_{H-L}}{f_S} = \frac{C_M}{2}\left(\frac{1}{C_L + C_T' + C_S} - \frac{1}{C_T' + C_S}\right). \quad (8)$$

For $C_M = 1.95$ fF, $C_S = 1$ pF, $C_L = 6$ pF, C_T' (dominated by I/O pads and PCB traces) = 2 pF, and f_s (series resonance frequency of the crystal) = 16 MHz, the frequency deviation is 216 ppm, conforming with the BLE standard (≤ ±500 ppm for the sleep-timer [24]).

In the HPM, we use the 16-MHz clock as the frequency reference for the PLL. As the frequency reference requires a superior PN, we employ the Pierce oscillator as the 1-stage g_m [20]. Its PN due to the flicker noise is given as [25]

$$S_{\varphi_n^2} = \frac{\overline{\Gamma_i}^2 K_{fi}}{(2C_L|\ V_{XO+}|)^2 \Delta\omega^3}\left(\frac{C_m}{2C_L}\right)^2 \quad (9)$$

where $\overline{\Gamma_i}$ is the effective impulse sensitivity function, K_{fi} is the flicker noise current source, V_{XO+} is the output swing, and $\Delta\omega$ is the offset frequency. From (9), the PN is proportional to K_{fi} and inversely proportional to C_L^3, which explains the PN degradation in the LPM as we only put the noisy 3-stage g_m in place and remove the 6-pF C_L from A_{XT}. CMOS transistors inserted as switches control the state of A_{XT}. $V_{O,3}$ buffers the control signals to improve the on-resistances of the switches. In LPM, S_{1-3} isolate C_L and R_L from the 3-stage g_m. Also, S_{1-2} cut down the power of the 1-stage g_m in LPM. They should be optimized not only to minimize their on-resistances in the on-state, but also to limit the leakage currents in the off-state. In LPM, the leakage power for the 1-stage g_m is 2.52 nW at room temperature, which is negligible to the sleep-timer's power.

V_{EH} directly powers most of A_{XT} to improve power efficiency. Hence, it is essential to design A_{XT} capable of functioning with V_{DD} down to 0.25 V. Current-source load prevails as the core amplifier of XO [9], [10]. Yet, it demands a higher voltage headroom to bias the active load, rendering it unsuitable for ULV operation. Further, we cannot self-bias the reconfigurable A_{XT} by the feedback resistor with V_{DD} of 0.25 V. Thus, we employ resistive loads for both 1-stage g_m and 3-stage g_m, which offer higher effective g_m (>4×) and are less prone to VT variation than the current-source load. Although the resistive loads are prone to power-supply noise, for energy harvesting applications powered by the solar cell with typical noise spectral density, e.g., < 45 nV/√Hz with 400 μW power at 1-kHz in [26], it degrades the PN by < 0.98 dBc/Hz at 1-kHz offset in the HPM. Herein, a voltage-and-temperature-tracking V_{bias} from μPM secures the robustness of A_{XT} in both HPM and LPM. $V_{O,2}$ powers this bias circuit, which is a typical beta-multiplier. Its power consumption is 1.23 μW. The bias-purposed R_X and R_Y are pseudo-resistors to save the chip area. Their resistances are >15.3 MΩ across –20 to 70 °C, and >18.3 MΩ over a V_{EH} variation of 0.25 to 0.3 V. The simulated PN only degrades by 0.3 dBc/Hz at 1-kHz offset with pseudo-resistors compared with regular polysilicon resistors.

We build the 3-stage g_m (Fig. 6) with cascaded CS amplifiers. V_{EH} drives the first and third branches to maximize the power efficiency, while $V_{O,1}$ drives the second stage to enhance the swing of V_{Tim}, the output to the DIV. After securing the gain and bandwidth of the first two stages, the current is allocated to the third stage to maximize the

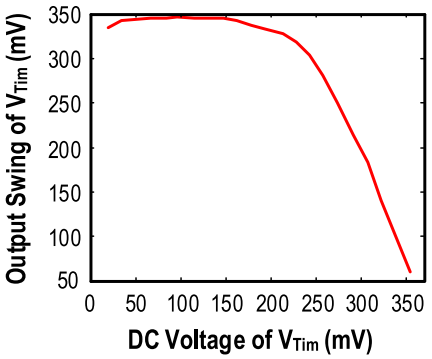


FIGURE 9. The output swing of V_{Tim} as a function of the DC voltage of V_{Tim}.

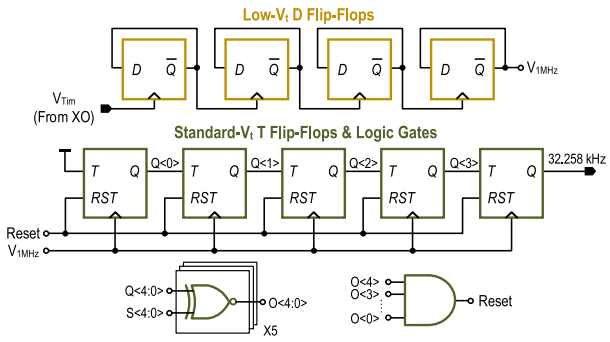


FIGURE 10. DIV implementation, with the signals S<4:0> provided off-chip for design flexibility.

effective g_m. In the conventional amplifier design where linearity is critical, R_{L2} should be designed such that V_{Tim} is $\sim 0.5\times$ $V_{O,1}$ and the swing headroom and linearity are maximized. Yet, for the timer where linearity is relatively unimportant, R_{L2} can be further to enhance the amplifier gain and thus the signal's amplitude and safeguard the operation of the DIV. Fig. 9 shows the signal swing at V_{Tim} as a function of the DC value of V_{Tim} by changing R_{L2} and preserving the current budget. The swing at V_{Tim} reaches a maximum when V_{Tim} is $\sim$100 mV, then decreases when V_{Tim} rises, attributable to the drops in R_{L2} and the gain.

DIV is powered by $V_{O,1}$ to save power (simulated: 139.4 nW). Four asynchronous dividers implemented with low-V_t transistors head the DIV, thus enabling fast switching and dividing the frequency of V_{Tim} by 16$\times$ (Fig. 10). This 1-MHz signal is then delivered to a synchronous divider (div-by-31). The divider is based on T flip-flops and logic gates with standard-V_t transistors to generate the final 32.258-kHz clock. This scheme saves 39.4% (simulation) power due to the inevitable leakage current in the employed 28-nm CMOS process compared with the scheme that has all logic gates implemented with low-V_t transistors while safeguarding the functionality of the DIV.

V. MEASUREMENT RESULTS

We prototyped the ULV XO-Timer with fully on-chip C_L in 28-nm CMOS (Fig. 11). We selected the 28-nm CMOS

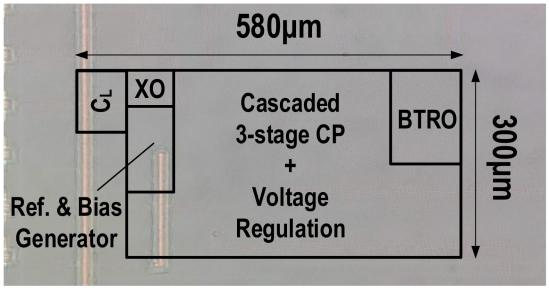


FIGURE 11. Chip micrograph of the fabricated ULV XO-Timer.

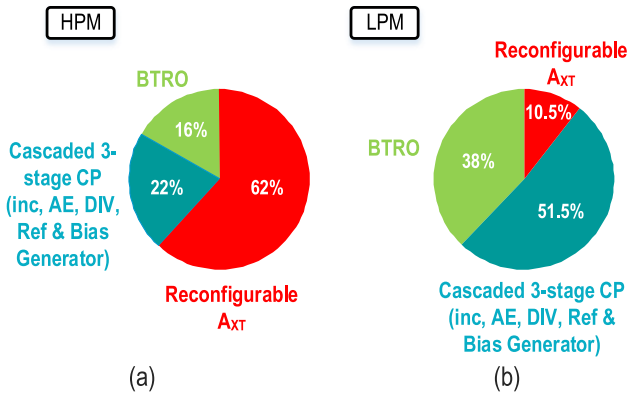


FIGURE 12. Power breakdown of ULV XO-Timer at (a) HPM and (b) LPM.

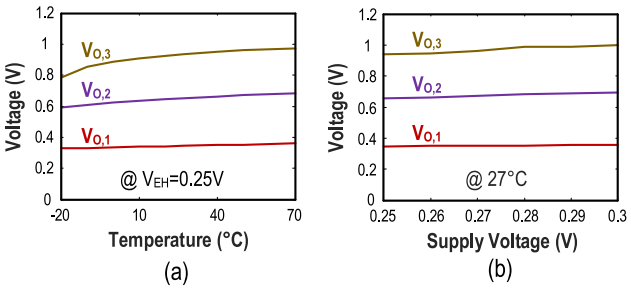


FIGURE 13. Measured $V_{O,1}$, $V_{O,2}$, and $V_{O,3}$ against (a) temperature and (b) V_{EH}.

process to streamline the integration of this XO-timer with the mainstream process for IoT transceivers [3], [4]. The active area is 0.127 mm^2, dominated by the μPM (0.121 mm^2). We employed 16-MHz quartz crystal 7V-16.000MAAE-T from the TXC Corporation. Its inherent frequency stability is ±30 ppm over –20 to 70 °C from the datasheet [27]. Fig. 12 summarizes the simulated power consumption of the XO-Timer in HPM and LPM. The μPM takes up 89.5% of the power at LPM and 92% of the area, which can be partially absorbed at the system level by sharing it with other circuitries [3], [4].

We first characterize the μPM. Fig. 13 plots the $V_{O,1}$, $V_{O,2}$, and $V_{O,3}$ variations against the temperature and supply voltage. Benefitting from the voltage-regulation loop, the variation of $V_{O,1}$, $V_{O,2}$, and $V_{O,3}$ is 9.6%, 14.4%, and 20.6% over -20 to 70 °C, whereas the variation of $V_{O,1}$, $V_{O,2}$ and $V_{O,3}$ is 2.2%, 5.2% and 6.4% over V_{EH} from 0.25 to

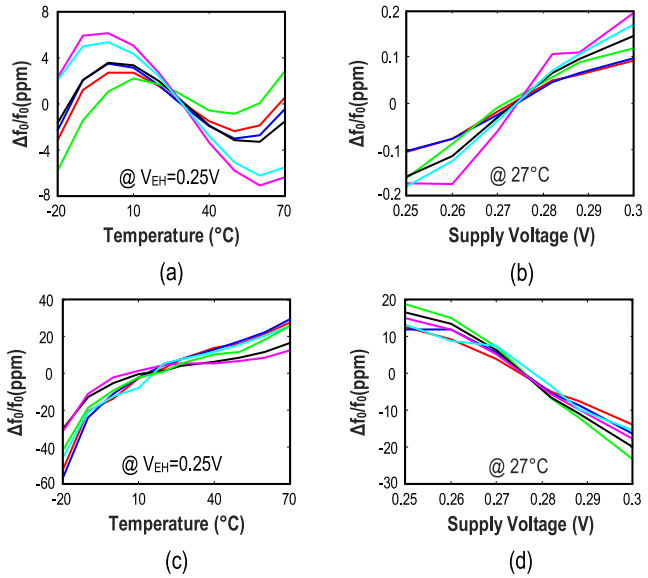


FIGURE 14. Measured frequency deviations of 6 samples against temperature and supply voltage variations at the HPM: (a) and (b), and LPM: (c) and (d).

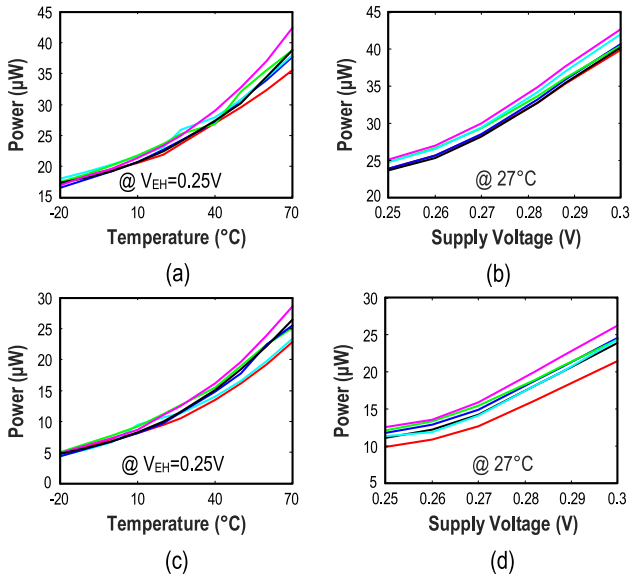


FIGURE 15. Measured power consumption of 6 samples against temperature and supply voltage variations in the HPM (a) and (b), and LPM (c) and (d).

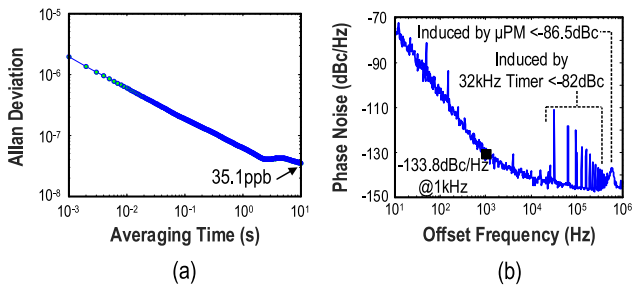


FIGURE 16. (a) Measured Allan deviation of the 32.258-kHz timer in LPM. (b) PN of the 16-MHz XO in HPM.

0.3 V (20% variation), respectively. The BTRO frequency is 2.7 MHz at 0.25 V and at room temperature, which is 1.52× slower than the simulation result in SS corner. This deviation indeed limits our minimum V_{EH} as the low BTRO frequency paralyzes the operation of the μPM. When the frequency is tallied with the simulation result, we could decrease V_{EH} to <0.2 V. On the other hand, the breakdown voltage of the transistor in this process (1 V) limits the maximum V_{EH}.

We characterize the performance of the XO-Timer with 6 available samples (different dies and crystals). Fig. 14 (a)-(d) shows the measured frequency variation of the XO-Timer over the temperature (−20 to 70 °C) and voltage (0.25 to 0.3 V) variations. In the HPM, the worst frequency variation is <13.2 ppm and <0.37 ppm against temperature and voltage variation, respectively. As the intrinsic frequency variation of the crystal is <±30 ppm across −20 to 70 °C, and the measured frequency variation matches with the temperature profile of the AT-cut crystal, the frequency variation in the HPM is attributable to the crystal itself. In the LPM, the worst frequency variation is <86.7 ppm <42 ppm over temperature and voltage variation. Both are considerably larger than the HPM as the 3-stage g_m's equivalent impedance in the LPM is sensitive to temperature and voltage variation. Still, they conform to the BLE standard (< ±500 ppm) with an adequate margin for the timer and aging.

Fig. 15 illustrates the measured power consumption of the XO-Timer across the temperature and voltage in both HPM and LPM. The average power of the XO-Timer in the HPM and LPM is 24.3 and 11.4 μW at room temperature, respectively. Herein, we benchmark the sleep-timer using the figure of merit proposed in [9]:

$$FoM_2 = P_S + P_A V_S, \tag{10}$$

where P_S is the power in the sleep mode, P_A is the transceiver's active power (assume 10 mW), and V_S is the sleep-timer's frequency error across the temperature range and ΔV_{DD} of 0.3 V. The FoM_2 of the proposed timer is 14.8 μW, outperforming the prior art [9], [11], [28], [29].

Next, we measured the Allan deviation of the 32.258-kHz output of the XO-Timer to determine the long-term frequency stability [Fig. 16(a)]. The Allan deviation floor is 35.1 ppb with an average time of 10 s, comparable to other state-of-the-art sleep-timers [9], [30]. Fig. 16(b) shows the PN of the 16-MHz signal in the HPM. It scores a PN of −133.8 dBc/Hz at 1-kHz offset. Its FoM_1, only including the power of XO as in [20] for a fair comparison, is −236 dBc/Hz at 1-kHz offset, comparable with the prior art [20], [31], [32]. There are spurs in Fig. 16(b) due to the crosstalk from the 32.258-kHz output (<−82 dBc) and μPM (<−86.5 dBc). These reference spurs after passing through the PLL are upconverted by $20\log(N)$, where N is 150 for 2.4-GHz PLL output. Hence, these spurs become <−38.5 and <−43 dBc, which meets the BLE standard (i.e., <−30 dBc [33]). There are two spurs at 50 Hz and 150 Hz due to the electromagnetic interference

TABLE 1. Performance summary and comparison with recent art.

	This Work		ISSCC'22 [11]		JSSC'18 [20]	ISSCC'15 [9]	
Key Architecture	**Dual-Mode XO-Timer + On-Chip µPM**		Dual-Mode XO-Timer		XO	Dual-Mode XO-Timer	
Technology [nm]	28		28		65	65	
Area [mm²]	0.127 #		2.51 (inc. LDOs)		0.023	0.13	
Supply Voltage [V]	**0.25 to 0.3**		1.5 to 1.7		0.35	N/A	
Temperature, T_{range} [℃]	-20 to 70		-40 to 90		-40 to 90	-40 to 90	
Frequency	16 MHz	32.258 kHz	76.8 MHz	32.768 kHz	24 MHz	24 MHz	31.25 kHz
Load Capacitance [pF]	6	2 &	N/A		6	N/A	
Power, P [μW]	**24.3**	**11.4**	1080	48.2	31.8	445	37
PN @ 1kHz [dBc/Hz]	-133.8	N/A	-134.03	N/A	-134	--	N/A
FoM_1 @ 1kHz [dBc/Hz]	-236 *	N/A	-231.4	N/A	-236.6*	--	N/A
$\Delta f/f$ versus T_{range} [ppm]	**13.2** †	**86.7** †	--	88.4	14.1	16	26
$\Delta f/f$ versus Supply Voltage [ppm]	**0.37** †	**42** †	--	--	17.9	2.07	2.7
	0.25 to 0.3 V		--		0.3 to 0.5 V	ΔV = 0.3V	
FoM_2 [μW]	N/A	**14.8**	N/A	49.084▲	N/A	37.3	
Allan Deviation [ppb]	35.1 (10s averaging time)		2500 (1s averaging time)		N/A	8 (2s averaging time)	

FoM_1 for XO: PN − 20log(f/f_{offset}) + 10log(P/1mW). FoM_2 for Timer: $P_S + P_A V_S$, where P_A=10mW & V_S is from [9].
µPM is included. & Parasitic capacitance dominated by I/O pads and PCB traces. * Only include the power of the amplifiers.
† Worst values of 6 samples. ▲ Voltage variation data unavailable, excluded from FoM_2.

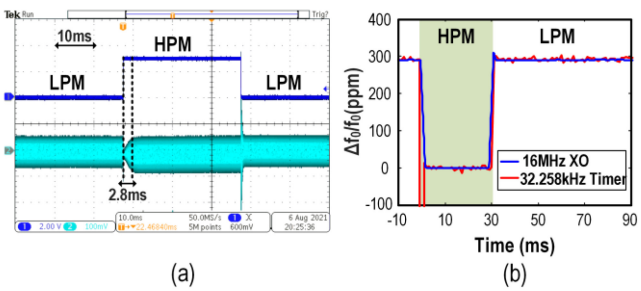


FIGURE 17. Measured (a) transient waveform and (b) frequency variation of the XO-Timer under transition between HPM and LPM.

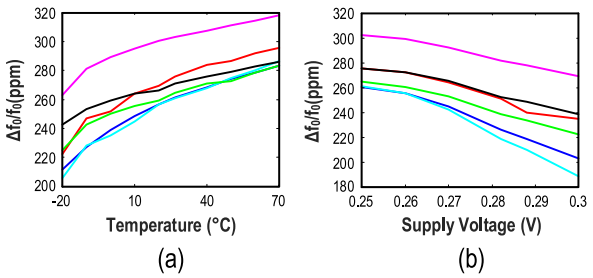


FIGURE 18. Measured frequency variation between HPM and LPM of 6 samples against (a) temperature and (b) supply voltage.

of the power line, which can improve by better PCB layout and shielding.

As there is oscillation on the crystal in the LPM, it can improve the startup time of the XO in HPM from 12 to 2.8 ms without any additional quick-startup technique [Fig. 17 (a)]. The energy consumed in this transition time is 68.0 nJ. As mentioned in Section IV, the C_L-reduction technique results in frequency variation between the LPM and HPM. Fig. 17(b) displays such frequency variation of the 16-MHz clock in the time domain. The frequency deviation $\frac{\Delta f_{H-L}}{f_S}$ between two modes is 290 ppm (room temperature, V_{EH} = 0.25 V). It is larger than the calculated value in Section IV, attributable to the uncertainties in the parasitic capacitances from the I/O pads and PCB traces. Further, Fig. 18 exhibits the frequency variations between HPM and LPM for different voltages and temperatures. As the frequency error induced by C_L reduction is predictable, we can account for it in the digital domain for calibration. Even without calibration, they are all compatible with the BLE standard (<±500 ppm).

There are missing cycles within the DIV when switching from LPM to HPM. This phenomenon derives from the reduction in oscillation amplitude over the crystal after an abrupt increase in C_L (6 pF). Consequently, the DIV may miss some cycles from A_{XT}. Thus, the measured first-cycle period for the sleep-timer is 56 µs. Even so, we can solve this issue by adopting progressive C_L switching as in [9]. From simulation, if we add up a small C_L (0.5 pF) to 6 pF by every 6 µs, which we can achieve with simple digital counters, we can maintain V_{Tim} above 77.4% of its full swing, and no missing cycles will happen.

We also powered the XO-Timer with a solar cell (1.2 × 1.6 cm²) in an indoor irradiance, resulting in an output voltage V_{EH} ranging from 0.25 to 0.3 V [Fig. 19(a)]. To mimic the power profile of a practical IoT node, we assume a BLE advertising packet of 128 µs [34], wherein V_{EH} draws a

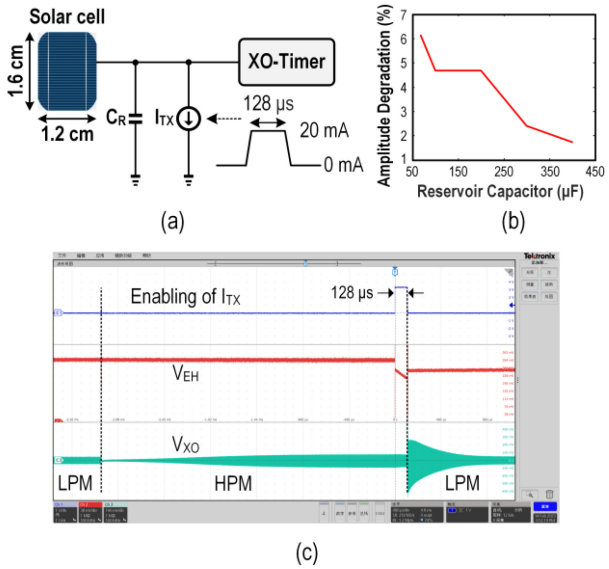


FIGURE 19. (a) Experimental setup for mimicking the operation of the solar-cell-powered XO-Timer together with a duty-cycled TX. The TX drains 20-mA current in a 128-µs interval as BLE advertising packet. (b) Measured amplitude degradation against the reservoir capacitor size. (c) The measured transient plot of XO-Timer when $C_R = 67$ µF.

20-mA current to imitate the operation of the BLE transmitter [4]. Meanwhile, we parallel a reservoir capacitor C_R to the solar cell to buffer the current drain from the high-current load. Fig. 19(b) plots the amplitude degradation of the XO amplitude among various reservoir capacitors during the current drained. The 16 MHz XO can maintain >90% of its amplitude even with a reservoir capacitor of 67 µF. Fig. 19(c) shows the transient of V_{EH} and 16-MHz XO.

Benchmarking with the recent art [9], [11] and [20], this work is the first sub-0.5V single-crystal XO-Timer with an embedded µPM to manage the internal voltages for better power efficiency (Table 1). The MHz-clock's FoM_1 is −236 dBc/Hz, comparable to [20], yet it generates both MHz-clock and sleep timer from one crystal. The sleep timer's FoM_2 is 14.8 µW, outscoring [9] and [11] by 2.5× and 3.3×, respectively. We acknowledge that the power and area overheads of the µPM can be partially absorbed at the system level by sharing its functions with other circuitries.

VI. CONCLUSION

This paper reported an ULV XO-Timer able to generate both a 16-MHz clock reference and a 32.258-kHz timer with a single crystal for ultra-low-power IoT nodes. It features a power-efficient µPM consisting of a cascaded 3-stage CP and a single voltage-regulation loop to tailor the internal voltage and current budgets for each sub-function while regulating them against supply voltage and temperature variations. The core amplifier A_{XT} is ULV-enabled. It is also made reconfigurable to improve the current-to-g_m efficiency in the LPM by using a 3-stage g_m plus C_L-reduction, while safeguarding the PN in HPM by using a 1-stage g_m. The measured power consumption of the XO-Timer in 28-nm CMOS is 24.3 µW in the HPM, and is reduced to 11.4 µW in the LPM. Furthermore, it also has a sleep-timer FoM_2 of 14.8 µW despite a limited voltage headroom, rendering this dual-mode XO-Timer with a single crystal a preeminent solution for the ULV energy-harvesting IoT nodes.

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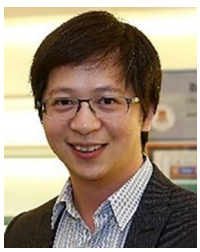

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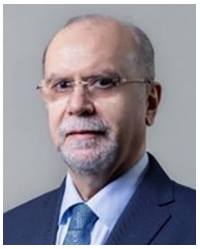

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