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A 672-nW, 670-n*Vrms* ECG Acquisition AFE With Noise-Tolerant Heartbeat Detector

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ABSTRACT This paper presents an electrocardiogram acquisition analog front-end (AFE) with a noise tolerant heartbeat (HB) detector. Source degradation and transconductance bootstrap techniques are incorporated into the AFE to reduce the 1/f noise of the amplifier. Furthermore, the chopper modulation, DC-servo loop (DSL) and pre-charge technology are combined to reduce interference from the environment. A mixed-signal implementation of HB detector with the symmetric-comparison loop is proposed to reduce the power consumption and area, which also suppresses motion artifact interference by adaptive thresholds. Implemented in 0.18 μm CMOS process, the circuit only occupies an area of 0.122 mm^2 and consumes 0.62 μW at a 1.2-V supply, of which AFE and HB detector consume 507 nW and 110 nW, respectively. Simulation results show that the gain and the CMRR of AFE range from 30-45 dB and 65-105 dB, respectively. The input-referred noise is 670 nVrms with a mid-band gain of 42 dB and a bandwidth ranging from 0.5 Hz to 1 kHz.

INDEX TERMS ECG acquisition, low-noise, low-power, AFE, HB detector.

I. INTRODUCTION

HB SERVES as a primary vital sign, which can be used to predict cardiovascular disease and figure out people's physical and mental problems comprehensively by continuously monitoring [1], [2]. Recording Electrocardiogram (ECG) is a common monitoring way but it is complicated and costly outside the clinic. Wearable devices provide solutions to monitor human physiological conditions anytime and anywhere at a lower cost [3], [4]. However, there is still many challenges for the wearable ECG acquisition integrated circuit (IC), including common interferences such as DC offset, thermal noise, and so on. In addition, motion artifacts and baseline voltage drift brought by human body also degrade signal quality, which requires complex signal processing to extract vital information. Besides, long-term monitoring and wearable action require lower power and small chip area.

The classic system architecture used in human vitals acquisition IC is shown in the Fig. 1 [5]. As the bridge between the chip and the environment, AFE usually consists of instrument amplifier (IA) for signals amplifying and interference suppressing, low-pass filter (LPF) for gain and bandwidth (BW) controlling. A moderate resolution 10-12bit SAR ADC or high resolution 16-24bit Sigma Delta ADC [6], [7], [8] are used to quantize and extract key characteristics of the ECG signals for digital processing.

For noise reduction, current-reuse is a traditional method in IA, but it merely improves the transconductance of the input transistors and is not effectively reduce the input referred noise [9]. The chopper circuits are used to modulate

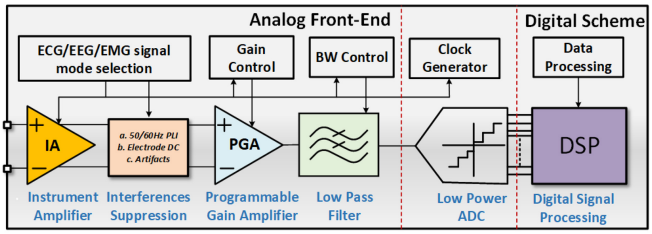

FIGURE 1. Classic system architecture.

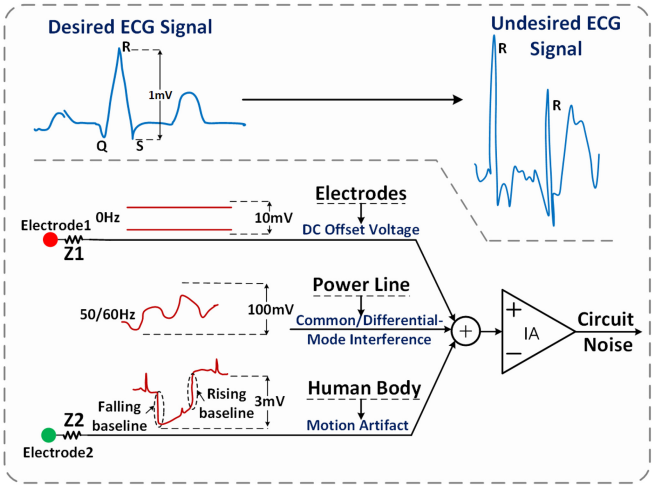

FIGURE 2. ECG signal and interference.

the in-band noise to a higher frequency, which can be removed using LPF with an additional area and power consumption [10]. To minimize the area, [11] integrates the functions of amplification, filtering, and buffering into one block, but limited its performance with a fixed gain setting. In addition, there are ways to reduce noise by adding feedback loops. Reference [12] proposes an eight-channel ECG recording system. The system employs the least-mean-square (LMS) algorithm in the digital domain to extract the noise, and feed it back to compensate the input in different frequency channels. Nevertheless, there is a trade-off between noise performance, circuit area and power consumption.

The typical element adopted in the digital scheme is analog-to-digital converter (ADC), such as successive approximation register (SAR) ADC, Sigma-Delta ADC [6], [7], [8] and so on, which converts the inputs into digital domain. To further flexibly reduce the interference and make the AFE more suitable for variable signals, some algorithms and feedback loops are proposed. But it all means the risk of large capacitance [13], [14]. Others use off-chip devices for programmable functions. Reference [15] adopts integrated digital signal processing (DSP), which has a general advanced RISC machines (ARM) processor optimized for various biomedical signal processing algorithms, but it is not wearable. Moreover, these systems do not mitigate real-world motion artifacts.

In this work, we present a 672 nW, 670 nVrms ECG acquisition AFE with an HB detector. In the AFE, the internal denoise technologies (source degradation and transconductance bootstrap) and chopping modulation techniques are incorporated to reduce the $1/f$ noise of the amplifier. Besides, we propose a mixed-signal implementation of HB detector with the symmetric-comparison loop to reduce the power consumption, which can identify the number of HBs accurately. Compared to other digital circuits, such as ADC, it consumes less power. Furthermore, the HB detector can suppress motion artifact interference by adaptive thresholds. An adaptive reference voltage generator (Adap-V_{REF}) is proposed instead of using reference voltage generator with large capacitors in the previous work [16] to reduce area sharply.

The article is organized as follows. The detailed analysis of variable interference and an overview description of the proposed structure are introduced in Section II. Then Section III describes the noise reduction technologies and detailed circuits of AFE. Section IV describes the principle and implementation of effective HB detection. Simulation results are discussed in Section V. Conclusion is provided in Section VI.

II. INTERFERENCE ANALYSIS AND PROPOSED STRUCTURE

Fig. 2 shows the waveform diagram of the ECG signal. Its amplitude is less than 0.1 mV and the frequency is between 0.5-150 Hz. HB is estimated based on the occurrence of QRS peaks in the ECG signal. As shown in Fig. 2, the various sources of interference come from electrodes, power line, the human body, and the circuit itself.

A. INTERFERENCE ANALYSIS

1) ELECTRODE INTERFERENCE

Since the electrodes connected to AFE have large impedance, when collecting physiological electrical signals, the input impedance R_{in} in the frequency range of interest (0.5–150Hz) needs to be much greater than 10 MΩ to allow proper signal acquisition without affecting its signal's linearity [17]. In addition, a large DC offset is generated due to the electrodes' polarization, usually which can be suppressed by making a high pass (lower than 0.5 Hz) cutoff frequency. The value of this differential offset from electrodes usually can be 10 mV [18].

2) POWER LINE INTERFERENCE

If the equivalent impedances of the two electrodes are equal, a common-mode interference V_{CP} at 50/60Hz occurs. If the impedances are not equal, differential mode interference V_{DP} also occurs. Since this frequency band coincides with that of the physiological electrical signal, the common-mode interference can only be improved by the common mode rejection ratio (CMRR). increasing R_{in} can reduce V_{DP}. According to IEC 60601-2-47, the CMRR of AFE used

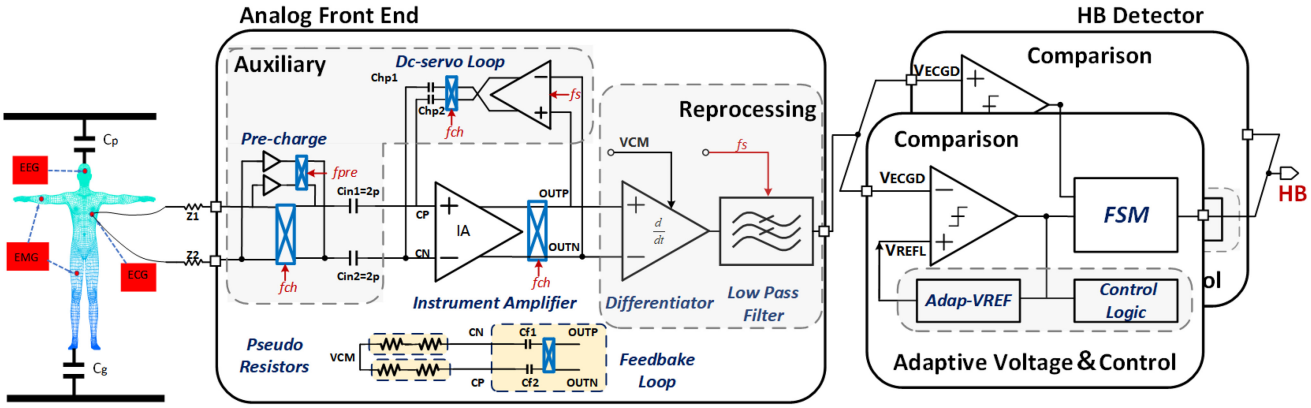

FIGURE 3. The structure of the proposed system.

in ECG signal acquisition should be greater than 60dB at 50-60Hz and greater than 45dB at 100-120Hz [19]. V_{DP} can be reduced by increasing R_{in} [17]. In addition, the human body and the circuit can be grounded together to eliminate the power line interference.

3) HUMAN BODY INTERFERENCE

It mainly refers to the motion artifact interference, which is caused by human breathing and motion. Human activity will cause the baseline to drift for a short time [20]. At the same time, it will also produce voltage at the muscle attached to the electrode, which is mixed in the signal as artifacts.

4) NOISE INTERFERENCE

The thermal noise and $1/f$ noise from MOS transistor would seriously destroy the signal quality. For the ECG signal (typically 2mV), the input-referred noise of the AFE should be less than $20\mu V_{rms}$ [19], the lower the better. Since the gain and noise from the first-stage of IA take the largest proportion in the system noise, the equivalent input noise V_n satisfies $V_n^2 = I_n^2/g_m^2$, thus can be effectively reduced by enhancing the transconductance g_m of circuit and reducing the current I_n.

B. PROPOSED STRUCTURE

Aiming at the above interference, the amplifier and the proposed structure are compared and analyzed.

Within the corresponding bandwidth (0.5-150Hz), the amplifier has enough R_{in} and CMRR to completely collect the ECG signal and suppress the power line interference. However, this frequency band coincides with that of the $1/f$ noise corner, only the input transistors with a large ratio can lower the frequency, which is difficult to eliminate. In the DC frequency band (0-0.5Hz), it cannot resist the influence of slightly higher DC offset and motion artifact without auxiliary support.

Relatively, the block diagram of the proposed system is illustrated in Fig. 3, which consists of an AFE and an HB detector. Coupling with the chopper and integrating the technologies of transconductance bootstrap and source degradation, the IA biased at 100 nA is used to suppress $1/f$ noise. But the modulation of the signal makes R_{in} worse, the pre-charge module in the auxiliary module can improve it by building up a non-overlapping channel to achieve a performance tradeoff. For DC offset and motion artifact, DSL forms negative feedback through the switched capacitor (SC) integrator to sharpen a very low cutoff frequency. And the adaptive threshold function of the HB detector is proposed to mitigate the motion artifacts.

The ECG signal is acquired through the two electrodes and clamped to 0.6 V through pseudo resistors of hundreds GΩ. After amplification, a single-output OTA used in the differentiator increases the stability by shaping amplification and controllable clamping. Besides, to connect with different back-end circuits, the voltage of the passive SC filter is set to follow the differentiator. The HB detector is built up based on two symmetric feedback loops composed of a comparator, a control logic, and an Adap-V_{REF}. After confirmation, the finite state machine (FSM) shared by these two loops outputs the HB signal.

III. ANALOG FRONT-END

A. IA WITH DENOISE TECHNOLOGIES

The schematic of proposed IA is shown in Fig. 4. A folded cascode amplifier with common-mode feedback (CMFB) is used to provide large open-loop gain and output swing, which obtains better stability compared with other structures. The effective gain of the chopper amplifier is given by:

$$A_{eff} = A_0 \times 1 - \frac{4.3}{2\pi f_{-3dB} T_{ch}}, \tag{1}$$

where A_0 is the open-loop gain, f_{-3dB} is the -3dB bandwidth frequency of the amplifier, T_{ch} is the high-level duration of chopper clock. Therefore, f_{-3dB} should be much greater than the chopping frequency to reduce the gain loss of the amplifier. The IA based transconductance bootstrap and source degradation is used to suppress noise and amplify the input signal, provides a closed-loop gain of 45 dB.

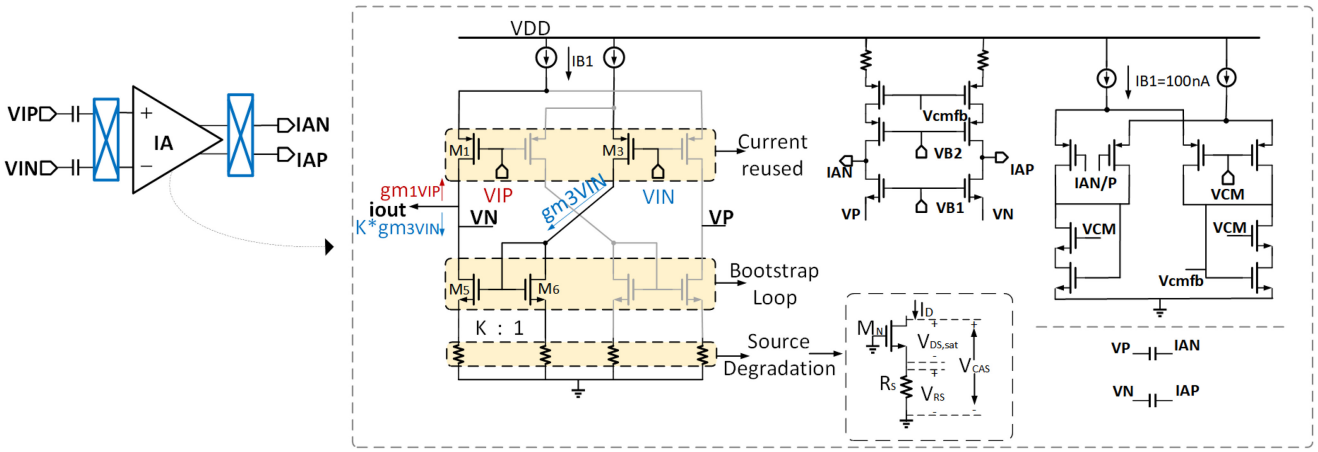

FIGURE 4. The principal and schematic of proposed IA.

B. PROPOSED STRUCTURE

The prototype of IA is a differential pair with current-source loads. The thermal noise formula of the amplifier is:

$$V^2_{(n,in)} = 4kT\gamma\left(\frac{1}{g_{m,eff1}} + \frac{g_{m,eff2}}{g^2_{m,eff1}}\right), \tag{2}$$

where $g_{m,eff1}$ and $g_{m,eff2}$ are the effective transconductance of input and load transistors, respectively.

1) TRANSCONDUCTANCE BOOTSTRAP

The principle of transconductance bootstrap technique is shown in the Fig. 4. The input transconductance with low current bias is improved by a self-biased current-reused topology. In the amplifier, M_1 and M_4 are the differential input transistors, M_2 and M_3 are transconductance bootstrap transistors. Considering the bias current is I_{B1}, the effective transconductance is given by:

$$g_{m,eff} = g_{m,N} + g_{m,P}\,. \tag{3}$$

A positive feedback bootstrap loop is adopted, which amplifies the input signal by M_1 times and $I_{out+} = g_{m1} * VIP$. Meanwhile, I_{out-} goes through the current mirror transistors (M_5 and M_6) and becomes $K * g_{m3} * VIN$. Thus $g_{m,eff1}$ is significantly improved as:

$$g_{m,eff1} = g_{m1} + K * g_{m3}. \tag{4}$$

2) SOURCE DEGRADATION

Source degradation technique attenuates the effective g_m by adding a large resistance to the source of MOS transistor. Fig. 4 illustrates the principle, where $V_{DS,sat}$ is the saturated drain-source voltage, and V_{Rs} is the voltage drop of R_s. The effective transconductance $g_{m,eff}$ is derived as:

$$g_{m,eff2} = \frac{g_m}{1 + g_m * R_s} = \frac{1}{R_s}\frac{2V_{RS}}{2V_{RS} + V_{DS,sat} - 2V_{TH}}, \tag{5}$$

where V_{TH} is the threshold voltage. To maximize the optimization of circuit noise, R_s and g_m must satisfy the condition of $g_m R_s >> 1$, where 1K and 5KΩ are used in the circuit.

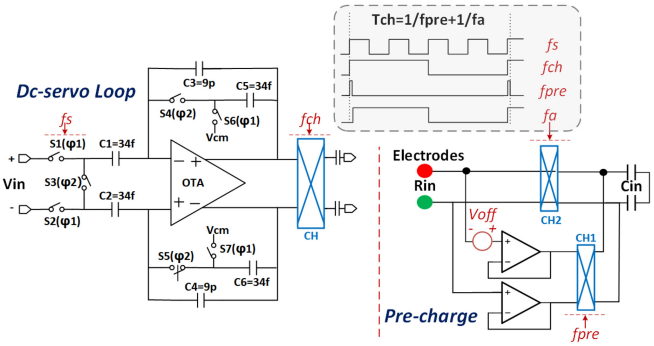

FIGURE 5. The schematic of DSL and pre-charge.

3) CHOPPER MODULATION

The chopper modulation technique is used to reduce $1/f$ noise. Since the low-frequency interference is modulated to high frequency, the mixed signal is finally passed through an LPF to be pure. The equivalent input noise power spectral density (NPSD) is obtained as:

$$S_{in,n}(f) = S_0 + S_{1/f} = S_o\left(1 + \frac{f_{1/f}}{|f_{ch}|}\right), \tag{6}$$

where S_0 is the equivalent input thermal NPSD, $S_{1/f}$ is the equivalent input $1/f$ NPSD, $f_{1/f}$ is the corner frequency equal to $1/f$ noise and thermal noise. f_{ch} is obviously equal to the inverse of T_{ch}.

C. AUXILIARY MODULE WITH PERFORMANCE-BOOSTING

1) DSL TO ELIMINATE OFFSET

The electrode DC offset is modulated to high frequency by the Chopper modulation, which cannot be eliminated by the feedback structure formed of pseudo resistance and capacitance. Therefore, the DSL is proposed. As shown in Fig. 5, DSL consists of a SC integrator and chopper. The frequency of SC integrator is set to $4f_{ch}$ and is consistent with the frequency of the filter (f_s). To suppress DC offset, the dominant pole of IA should be as close to zero as possible, thus

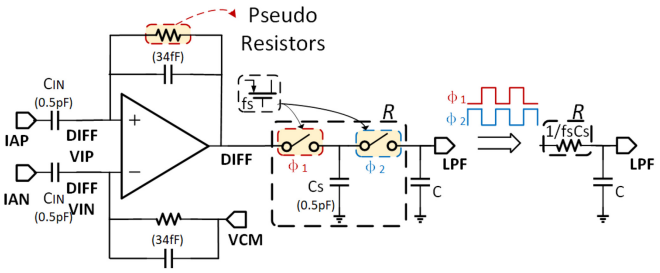

FIGURE 6. The schematics of differentiator and SC LPF.

the integral constant should be large enough. In phase $\phi 1$, C1 transfers charge to C3, and C5 samples the instantaneous output of integrator. In phase $\phi 2$, C3 returns the charge of $C1 * v_{in}$ back to C1, which is shared equally by C5 and C2. C3 is reused in two phases to effectively saves the capacitor area. The low-pass cut-off frequency of the integrator f_0 is calculated by:

$$f_0 = \frac{2f_{ch}C_{1,2}C_{5,7}}{2\pi C_{3,4}^2}. \tag{7}$$

2) PRE-CHARGE TO BOOST INPUT IMPEDANCE

The pre-charge mainly consists of a unity gain amplifier, which transmits ECG signal from the electrode to IA through the non-overlapping channels. The operation is divided into pre-charge phase and chopping phase.

In the pre-charge phase, the chopper CH1, controlled by f_{pre}, receives the ECG signal. At the same time, CH2 is in an inoperative state. The pre-charge module replaces the electrodes to provide charge to Cin and increases R_{in} of IA, which is obtained by:

$$R_{in} = \frac{e^{\frac{T_p}{\tau}}}{2f_{ch}C_{in}}, \tag{8}$$

where τ is the time constant and T_p is the conduction time of CH1. A sufficiently large input impedance can be obtained by adjusting the value of T_p/τ.

The chopping phase is the opposite of pre-charge phase controlled by f_a. The operation is similar to chopper modulation stated earlier.

D. REPROCESSING MODULE WITH CONTROLLABLE CLAMPING

1) DIFFERENTIATOR

The differentiator is used to sharpen the ECG signal so that FSM can accurately identify the number of HBs. As shown in Fig. 6, the active RC differentiator is composed of resistors and a capacitor-AC-coupled amplifier with negative feedback. C_{IN} turns each QRS into double-sided peaks. Then the signal DIFFVIP is amplified by the capacitive-gain amplifier. In addition, the output signal of differentiator is clamped by VCM. The voltage reference varies with VCM so as to connect with different digital circuits.

2) LOW-PASS FILTER

As shown in Fig. 6, in the first-order SC LPF, the resistor is replaced by two switches and a capacitor. C is the load capacitor and f_s is the switching frequency of the MOS transistor. Significantly, the SC LPF can not only reduce the high-frequency clutter of differentiator, but also provide a 20-dB attenuation of the line noise.

IV. HEARTBEAT DETECTOR

Fig. 7 shows the circuit of proposed HB detector, which mainly contains a shared FSM and two symmetric independent loops. Each loop is made up of the comparator, control logic and Adap-V_{REF} generator. With a mixed-signal implementation, the analog part is inactive in the steady state and D-V_{REF} is used to replace the large charging capacitor in [16], thus both the power consumption and the area are significantly reduced.

The control logic is mainly composed of the synchronous pulse generator (Sync Pulse), phase frequency discriminator (PFD) and synchronous delay generator (Sync Delay). V_{ECGD} from AFE is compared with the threshold voltage $V_{REFH/L}$ to determine $P_{H/L}$, which is used to justify HB in FSM. Specifically, $V_{REFH/L}$ is adaptively generated by the feedback loop. The rising edge of $P_{H/L}$ activates Sync Pulse to generate the reference pulse PW_H/L, which is compared with $P_{H/L}$ in PFD to obtain the difference between $P_{WH/L}$ and $P_{H/L}$, named $PW_{EH/L}$. $PW_{EH/L}$ is postponed properly by the Sync Delay to synchronize with HB, then is output to UP/DN in Adap-V_{REF} generator. The digital voltage reference is controlled by UP/DN, derived by the unity-gain buffer, stored in C_{REF} and fed back to the comparator. In this way, the proposed HB detector can automatically adjust $V_{REFH/L}$ to track the baseline. To reduce the power, only when UP/DN activates, the buffer is enabled. The corresponding waveforms are shown in Fig. 7.

Since unilateral pulse signals are generated during the motion period, the proposed AFE adopts the differential signal processing into a bilateral peak to obtain the motion artifact correction. Obviously, only the signal that satisfy the first detected peak is positive and next one is negative, can be considered as a correct HB. If only a single positive or negative peak is detected, such peak will be classified as motion artifacts and FSM will not output HB signal. Meanwhile, PW_E will be cleared and $V_{REFH/L}$ will not change.

A. CONTROL LOGIC

In order to real-time track the positive and negative peak of V_{ECGD}, a pulse generator that can produce a synchronous pulse is designed. In addition, Sync Delay and the FSM are proposed to delay the comparison result $P_{H/L}$ and recognize the real double-peak V_{ECGD} from motion artifacts.

1) SYNC PULSE

The schematic of proposed Sync Pulse is shown in Fig. 8, which is made up of three D flip-flops, a 4-bit counter and

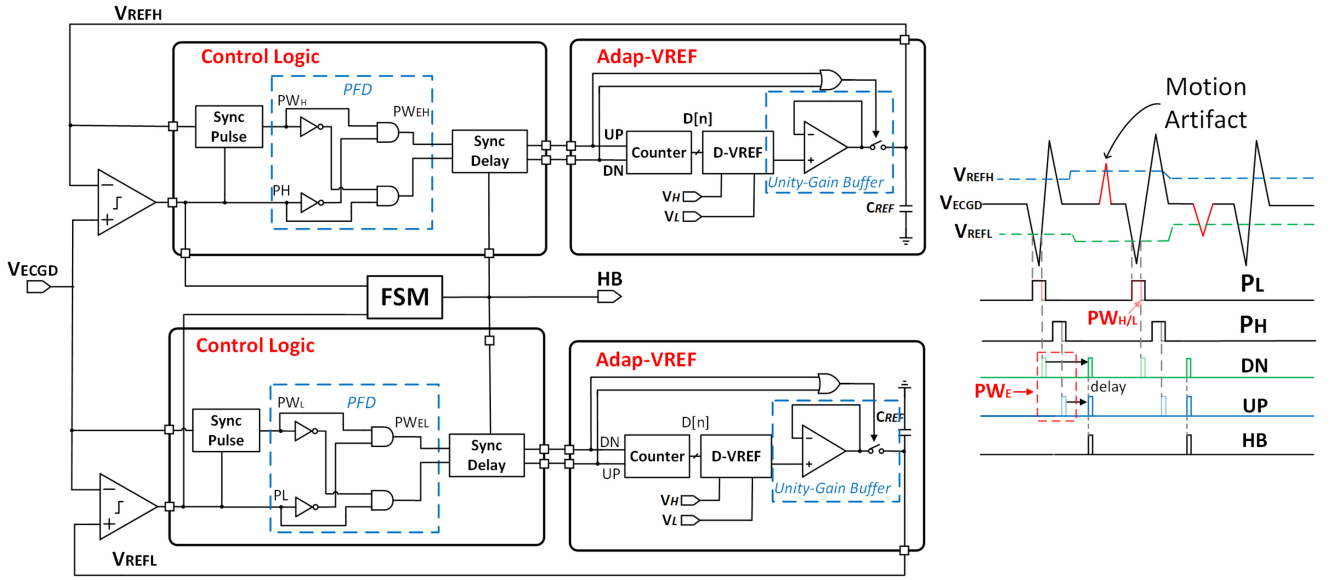

FIGURE 7. The circuit of proposed HB detector.

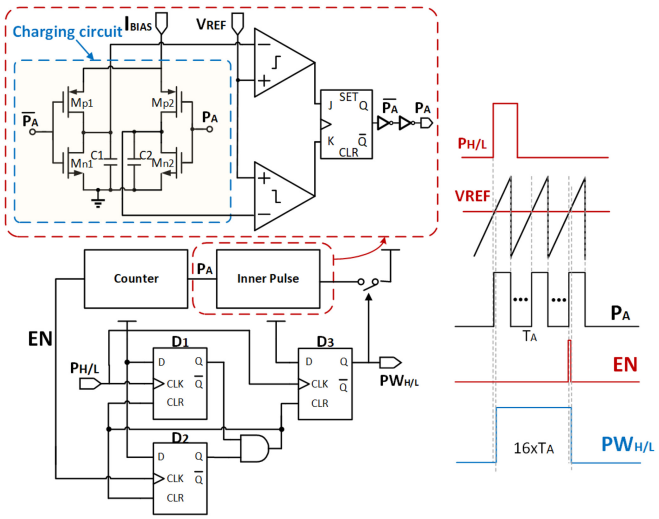

FIGURE 8. The schematic of Sync Pulse.

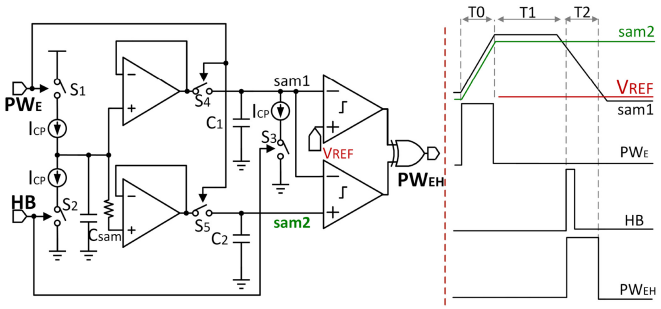

FIGURE 9. The schematic of Sync Delay.

an inner pulse generator. Its operating principle is similar to a frequency divider. The inner pulse generator, composed of a charging circuit, two comparators, and triggers, is used to generate pulse P_A, which can be controlled by the charging current and V_{REF}.

To begin with, $P_{H/L}$ enables D_3 to set $PW_{H/L}$ to be high. Then $PW_{H/L}$ enables the power of inner pulse generator. P_A with a width of 200 μs is generated to enable the counter. Once the counter is full, $PW_{H/L}$ will be clear by D_2, and the inner pulse will also be turned off to reduce the power. Finally, a synchronous pulse $PW_{H/L}$ is produced to real-time track $P_{H/L}$.

2) PFD

As can be seen from both the circuit and waveforms in Fig. 7, once $P_{H/L}$ and $PW_{H/L}$ input to the circuit, a delay namely the error control signal PW_E, which is determined by the difference between $P_{H/L}$ and $PW_{H/L}$, will be obtained and used to control $V_{REFH/L}$.

3) SYNCHRONOUS DELAY GENERATOR

Since the duration of QRS is long, a millisecond level delay module shown in Fig. 9 is proposed to store the result of PFD. The delay module is made up by a sampling circuit, two buffers and two comparators. And the waveforms of synchronous delaying are shown in Fig. 7.

Once PW_E is high, the switch S1 is turned on to charge the sample capacitor C_{sam}, and S4 and S5 are also turned on to sample the voltages stored in C_1 and C_2. Unlike sam1, sam2 has a small amplitude reduction due to the resistor. When PW_E is low, C_1 and C_2 are turned off, thus sam1 and sam2 remain unchanged.

Once the heartbeat signal HB is high, S3 discharges C_1 until sam1 is smaller than V_{REF}. In this way, a pulse, which is not only related to PW_E but also is in sync with HB, is obtained as UP/DN to control the D-V_{REF}.

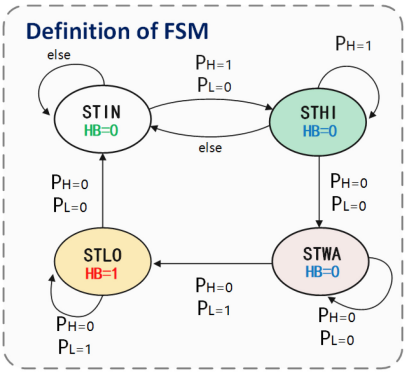

FIGURE 10. The definition of FSM.

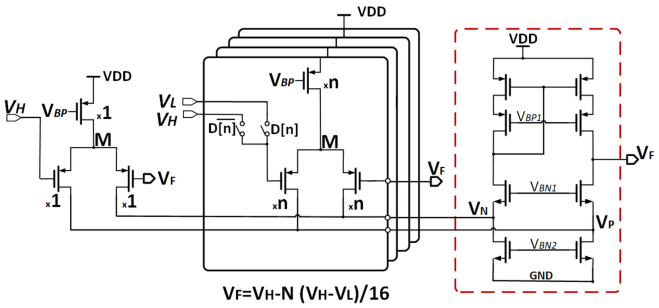

FIGURE 11. The schematic of D-V_{REF}.

B. FSM

Once the comparison and pulse delaying finish, PW_E and $P_{H/L}$ will be input into FSM. As shown in Fig. 10, there are four states, including STIN, STHI, STWA and STLO, which represent initial state, positive peak state, waiting state and negative state, respectively. STLO means that an effective HB is detected and HB will be generated, as shown in Fig. 7. Besides, STWA will return to initial state in several detecting cycles so as to save the power consumption. Only when a positive peak and a negative postponed synchronously are both detected, the HB can be considered as a real one.

C. ADAPTIVE VOLTAGE REFERENCE

The Adap-V_{REF} is mix-signal implemented and mainly composed of a counter, a D-V_{REF} and a unity-gain buffer. The initial reference voltage is generated by the D-V_{REF} and stored in C_{REF}. Once UP/DN comes, the counter will activate and calculate the width of UP/DN. The result D[n] will be input to D-V_{REF} to generate a voltage according the pulse width of UP/DN.

Fig. 11 shows the schematic of the proposed D-V_{REF}, which is a simplified 4-bit DAC-embedded amplifier [21], [22] without offset compensation to reduce the power. To interpolate between V_H and V_L according to the 4-bit digital code (n=3), there are sixteen different arrangements. Then the input differential pairs and tail current sources are divided into five stages in a transistor size ratio of 1:1:2:4:8. When $N = \sum(I[n] * D[n])$, the output voltage V_F can be approximately expressed as $V_H - N(V_H - V_L)/16$.

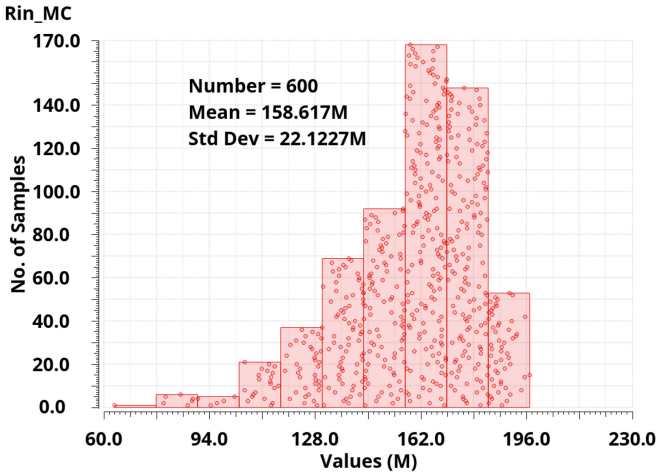

FIGURE 12. The Monte Carlo simulation of Rin with 600 points.

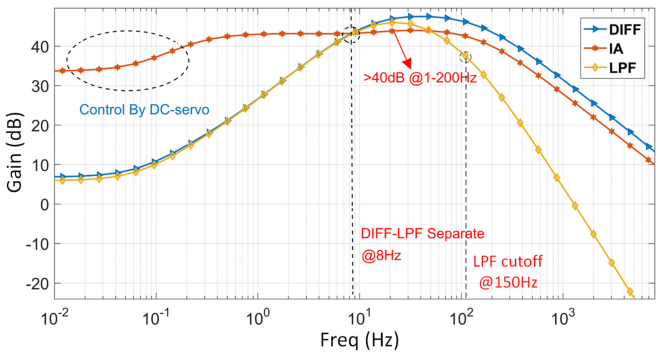

FIGURE 13. Frequency response of each sub-blocks in AFE.

TABLE 1. Corner simulation results.

Corner	R_{in}	CMRR	V_{IRN}
ff	43 MΩ	34-108 80dB@100Hz	1.6 μVrms
ss	187.7 MΩ	42-98 83@100Hz	445 nVrms
tt	150.8 MΩ	65-105 100@100Hz	670 nVrms

V. SIMULATION RESULTS AND DISCUSSION

To verify the features, the proposed ECG acquisition circuit is implemented and simulated in a 180nm CMOS process. Fig. 12 shows the input impedance of AFE R_{in} with a 600-point Monte-Carlo simulation. The mean value and standard deviation are about 158.6 MΩ and 22.1 MΩ. The specific process corner simulation is summarized in the Table 1, which lists the worst-case value of the R_{in}, CMRR, and input reference noise (V_{IRN}) under the extreme process corners. Except the results under the ff process corner, the other are greater than 100 MΩ.

The gain results of several key nodes of AFE are shown in Fig. 13. In middle band (1-200 Hz), the gain of IA is larger than 40 dB. It decreases to about 35 dB in the low frequency

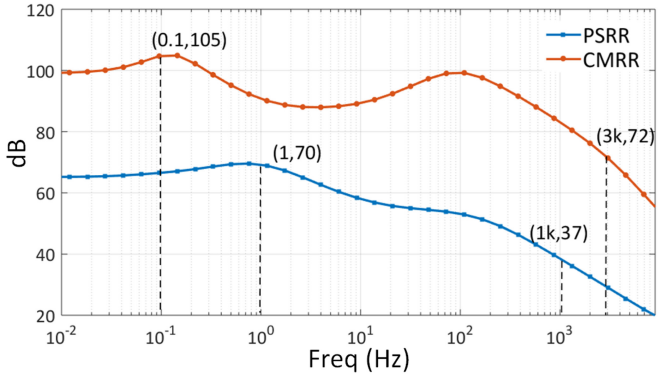

FIGURE 14. The CMRR and PSRR of AFE.

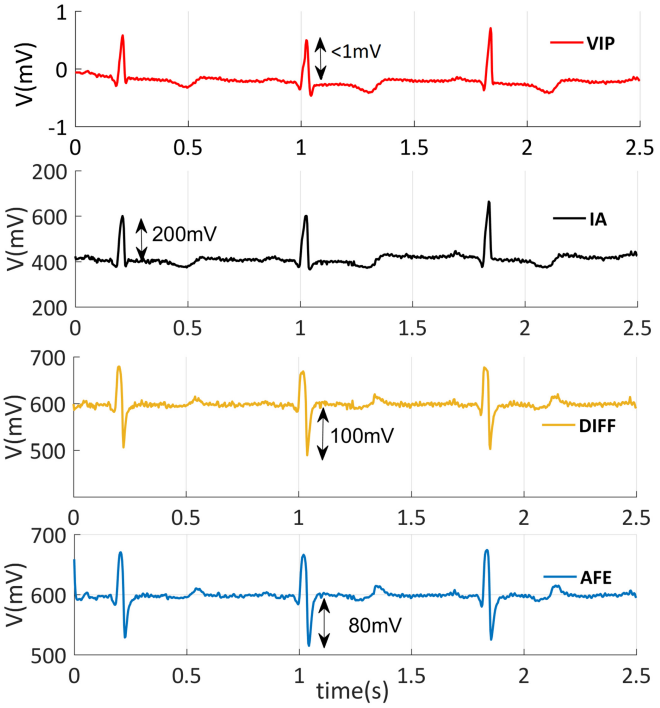

FIGURE 15. The key-node voltages of AFE.

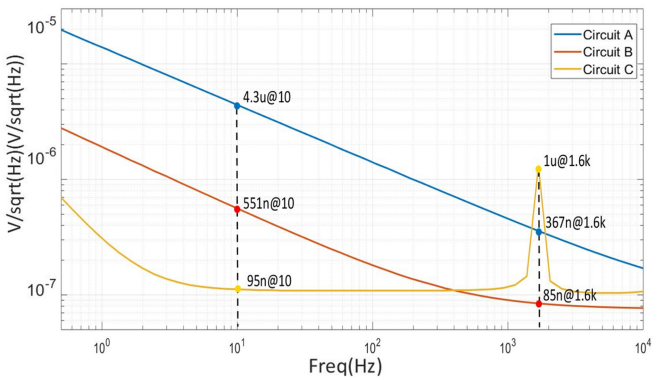

FIGURE 16. The comparison of different technologies on input-referred noise.

domain because of DSL, which is used to suppress the DC offset. The intersection frequency of differentiator and IA, is the frequency at which QRS differentiates into lightning-shape. As for the gain of the LPF, its cutoff frequency is about 150 Hz to retain the intact ECG signal, the band of which is 0.5-150 Hz.

CMRR and power supply rejection ratio (PSRR) represent the ability to suppress common-mode interference signals and noise from power supply, respectively. They are derived from the quotient of differential-mode gain with common-mode one and the gain obtained when the AC voltage of VDD is equal to 1 V.

As shown in Fig. 14, CMRR of proposed AFE ranges from 65 dB to 105 dB during 10m–9k Hz. Also, the value of the measured CMRR at 0.1 Hz and 3kHz are obtained approximately 105 dB and 72 dB, respectively. PSRR ranges from 20 dB to 70 dB during 10m–9k Hz, the value of it at 1 Hz and 1k Hz are about 70 dB and 37 dB. Besides, Table 1 predicts that CMRR of the proposed AFE is stable at about 80 dB at 100 Hz under process corners. The results reach the ANSI/AAMIEC-13 standards from the American National Standards Institute (ANSI) [23], which indicates that the system has a certain ability of resisting common-mode interference and the power supply noise interference.

Fig. 15 shows the key-node voltages of AFE with the ECG data of the MIT-BIH Arrhythmia Database [24]. Benefited from the gain of IA and differentiator, the ECG signal is amplified from around 600 μV to 200 mV, which is loaded on a common voltage of 600 mV and converted into a lightning shape that is easy to identify by HB detector.

As for noise, which depends on many factors, such as the bias current, the size of the input transistors and the frequency of the chopper, etc. Usually, internal denoise techniques includes transconductance bootstrap and source degradation by reducing the noise of op-amp itself instead of chopping, which is external technique. As depicted in Fig. 16, the comparison of original circuit A and circuit B (with internal denoising), whether in the target frequency band (10 Hz) or chopping frequency (1.6 kHz), the noise of circuit B is lower than circuit A. By using external denoise technique, the input noise of circuit C at 10 Hz is 95 $nV/sqrt(Hz)$, which is better than that of circuit B (551 $nV/sqrt(Hz)$) without external denoising. The input-referred-noise between 0.5–150 Hz is 0.67 μV_{rms}.

Fig. 17 shows the noise of AFE with a 600-point Monte-Carlo simulation. The mean value and standard deviation are about 647.5 nV_{rms} and 151.3 nV_{rms}, which indicates that the noise can be stable about 600 nV_{rms} at variable process corner.

As talked before, Table 1 is the comparison results of V_{IRN} under process corners at different temperatures. The table shows that the maximum value of V_{IRN} after simulation is 445 nV_{rms} and 1.6 μV_{rms}, which predicts that V_{IRN} of the proposed AFE can work stably and perform as well as the presented derivations after fabrication.

Eventually, the pure ECG signal is output from the LPF, with a slight drop in amplitude due to switching capacitance.

TABLE 2. Comparison between state-of-the-art designs.

	References	TBCASI'14 [13]	JSSC'14 [15]	JSSC'18 [25]	TBCAS'19 [14]	JSSC'20 [26]	APCCAS'21 [16]	**This work**
SoC	Technology	$180nm$	$180nm$	$180nm$	$180nm$	$180nm$	$180nm$	$180nm$
	Results	Measure	Measure	Measure	Measure	Measure	Simulation	**Simulation**
	V_{DD}/V	1	1.2	0.8	1	1.2	1.2	**1.2**
	Power/μW	8.49	345*	0.289	3.2	4.6	1.2	**▲0.67**
	Area/mm^2	0.49	49	1.92	0.84	6.25	-	**▲0.122**
AFE	Input Signal	ECG	ECG	ECG	EEG	ECG	ECG	**ECG**
	Rin/Ω@Hz	-	>500M	200G@1Hz	102G@1Hz	-	-	**150M@1Hz**
	Noise /μV_{rms}(Hz)	3.77 (60m-950)	0.61 (0.5-150)	8.26 (1-400)	1.5 (0.5-1.2k)	4.6 (1-1k)	1.7 (0.5-150)	**▲0.67 (0.5-150)**
	Gain/dB	34	28-36	34	52-62	66-74	43-57	**30-45**
	Bandwidth/Hz	60m-950	1-1.2k	1-400	1.2k	4-28	1-900	**0.1-1.2k**
	CMRR/dB	>67	>110	>66	108	-	85	**65-105**
	Power/μW	-	15.96	0.228	3.2	0.504	0.8	**0.507**
Digital	Function	Offset Calibration	Artifact Reduction	Self Calibration	EEG Identification	HB Detection	HB Detection	**HB Detection**
	Processor-less	Yes	No	Yes	Yes	Yes	Yes	**Yes**
	Power/μW	-	10/120	0.032	0.5	0.092	0.4	**0.11**

* 3-Channel ECG.

▲ Highlight performance.

As can be seen from Fig. 18, the adaptive reference voltages V_{REFH} and V_{REFL} drift with the double-peak output of AFE. Then the HB can be judged accurately and a pulse HB will be generated once the positive peak flag P_H and the negative one are both high. In addition, the reference voltages will rise when the detecting is over. And in the standby state, the voltage will be reset to a specify value so as to mitigate the current leakage. Obviously, the motion artifact with only a negative peak or a positive one is detected to output a pulse P_L or P_H but isn't recognized as a real HB shown in the above diagram.

Under the supply voltage of 1.2 V and the clock period of 75 μs, the proposed system consumes approximately 670 nW. To achieve low noise, the IA uses 100 nA current and consumes 497 nW. Meanwhile, HB detector consumes only 110.5 nW since the analog part is inactive in the steady state. As depicted in Fig. 19, the chopper coupled AFE, excluding the IA, has 3% power consumption. The IA with CMFB and HB detector consume 73% and 16%, respectively. Due to the generation of the shaped clock f_{pre} and f_{ch}, the bias and clock-generating circuits have a power percentage of 8%.

A prototype of the system was implemented in a 0.18-μm CMOS process, with a total area of 0.122 mm^2 without the pads. The circuit layout photograph is shown in Fig. 20. AFE and HB detector occupy 0.06 mm^2 and 0.062 mm^2, respectively.

In summary, the performances of the proposed system are compared with the prior works in Table 2 [13], [14], [15], [25], [26]. By adopting the above improvements, the proposed circuit performs better in anti-noise, low power, small area and wide bandwidth compared with other designed. Especially, the noise and power consumption are significantly improved by using several noise reduction technologies in AFE and mixed implementation in HB detector. The input-referred noise of 670 nV_{rms} obtained by internal denoise technologies and chopping, which is one-sixth of [26] and 61% improvement from [16]. The total

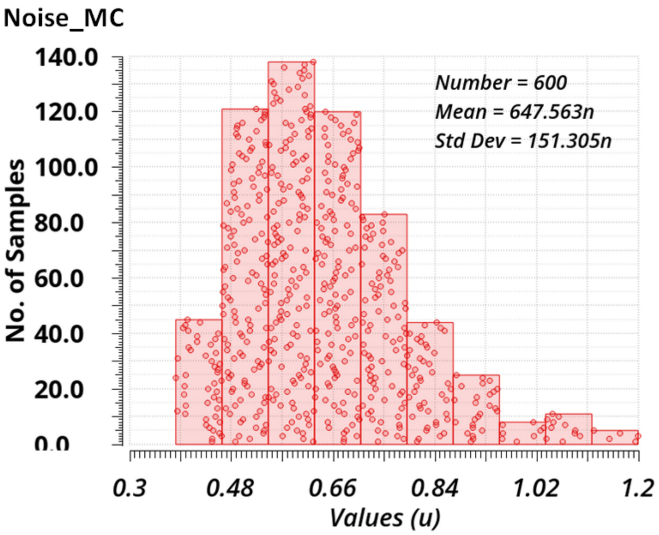

FIGURE 17. The Monte Carlo simulation of noise with 600 points.

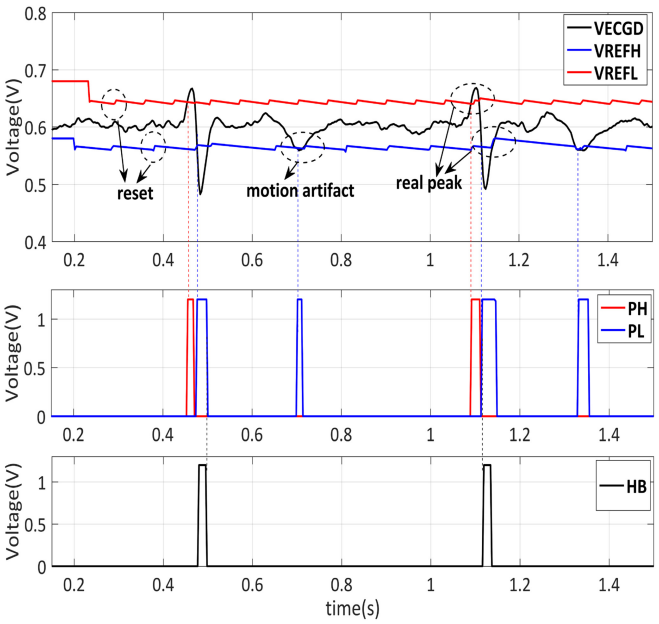

FIGURE 18. The simulation results of HB detector.

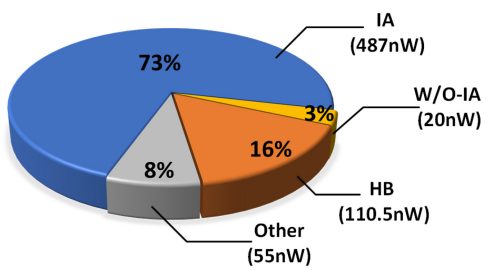

FIGURE 19. The power consumption of the whole system.

power consumption is about 0.67 μW, which is the second lowest in the table and 44% improvement from prior work [16]. In addition, since a Adap-V_{REF} is used to replace the large charging capacitor in [16] and [26], and capacitor of

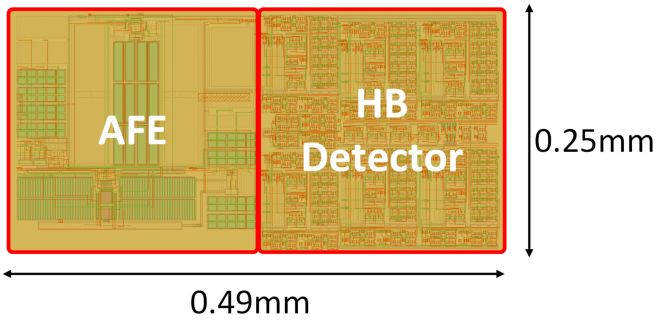

FIGURE 20. The layout of the whole system.

AFE is reduced by using variable compensation technology, the area is reduced to about 0.122 mm^2, which is smaller than other works.

VI. CONCLUSION

This paper presents a 672 nW, 670 nVrms ECG acquisition AFE with a mix-signal implemented HB detector. Particular attention also has been taken to obtain the low noise by chopping, transconductance bootstrap and source degradation. Besides, an adaptive threshold voltage in the HB detector is proposed to resist the baseline drift from motion artifacts. Simulation results verified that the proposed circuit is suitable for ECG acquisition application, owing to the anti-noise, low power, small area and motion artifact correction.

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