Digital Object Identifier 10.1109/OJNANO.2022.3224652

Guest Editorial: Nanopackaging Part II

The first part of the Special Section on Nanopackaging appeared in OJ-NANO Vol. 2, 2021 with five papers [A1], [A2], [A3], [A4], [A5] and an editorial which discussed the field's scope [A6]. This second part with ten papers [A7], [A8], [A9], [A10], [A11], [A12], [A13], [A14], [A15], [A16] has been published in Vol. 3, 2022. It begins with three reviews of diverse nanoscale technologies and then moves on to research papers focused primarily on nanomaterials for on-chip interconnect and noise abatement.

Review papers are a vital component of the scientific and engineering literature, providing both an introduction to the field for newcomers, a roadmap to the literature, and a survey of the status of current understanding and technology for other experts. In the first review, [A7] Sudhindra et al., the Balandin group summarizes the efficacy of graphene, few-layer graphene and graphene composites for thermal transport and thermal interfaces, emphasizing the potential for commercial applications. Thermal conductivities $\sim$12.5 W/m-K are cited. In the second, [A8] Géczy et al., nanocomposite materials for printed circuit substrates are surveyed, with an emphasis on biodegradable properties for environmental protection, and on applications to flexible and wearable circuits. Due to its many advantageous properties, additive manufacturing (AM) is widely considered as one of the key enabling technologies of our times, also expected to address many challenges posed by the increasing miniaturization of electronic devices and the rise of heterogeneous integration strategies. The three main driving forces pushing the technological development in additive manufacturing are 1) miniaturization, i.e., decreasing the feature size, 2) increasing material diversity, and 3) scaling up the throughput of printing technologies. In [A9] Miskovic and Kaufhold, the third review, the authors provide an overview of existing additive manufacturing technologies capable of nanoscale 3D fabrication, addressing resolutions below 500 nm, with particular emphasis on electrohydrodynamic (EHD, or e-jet, printing as a next-generation enabling technology that excels in all three mentioned criteria.

Emerging application areas in health monitoring that require wearable or flexible electronics are a constant driving force for advancing traditional substrate and assembly technologies. The need for higher interconnect density ultimately led to the emergence of embedded-die in flexible substrate (or chip-in-flex) packaging technologies. Besides reviewing the recent developments of flexible electronic packaging and integration techniques, the paper in [A10] Hassan et al., presents a realized embedded-chip planar nanosilver-elastomer interconnect technology for on-skin biophotonic sensor applications, utilizing a fan-out packaging approach as one of the key enabling technologies for embedding chips.

There are two papers on electronic noise minimization issues which primarily focus on signal and power integrity issues in the nano-scale regime. Both problems are related to power supply fluctuations which create critical performance bottlenecks in the designing of integrated circuits at the sub-nano technology nodes where the increase in component count and density exacerbate the problems previously experienced at earlier nodes. These supply fluctuations can cause power supply-induced jitter (PSIJ) that can affect the functionality of the circuits. An accurate and computationally efficient method for the analysis of PSIJ is discussed in the first paper, [A11] by Sharma et al. The method can also estimate PSIJ at intermediate stages of N-stage drivers. Comparing the analytical results with measurements and simulations validates the accuracy of the proposed PSIJ technique. Furthermore, the relevance and impact of small-signal device parameters in the analysis of PSIJ are also discussed. Some critical observations on the behavior of PSIJ with technology scaling and frequency are also discussed in this paper. The second paper, [A12] Tripathi and Junjariya presents an effective method for selecting and placing decoupling capacitors in a power delivery network (PDN). Decoupling capacitors are widely used in PDN to minimize supply fluctuations. The selection and placement of the decoupling capacitors to achieve a lower self-impedance is another issue. This paper proposes a novel and computationally efficient method that is used to tackle the Large-Scale Optimization Problem (LSOP) of decoupling capacitor placement. The proposed method uses an adaptive region search technique to improve the computation time of the large-scale optimization problem of decoupling capacitor placement compared to traditional metaheuristic algorithms. Three case studies are presented that compare the performance of the conventional and proposed methodologies. The method is highly effective when large decoupling capacitors are available for the placement and selection.

A key challenge for achieving high bandwidth at low power is the realization of fast and reliable interconnects. With traditional interconnects, higher data rates degrade the signal integrity and limit the signal speed because of interconnect latency and transmission distances. Interconnect scaling and advanced materials are required to enable higher bandwidths while keeping the frequencies lower so that lower bit error rate and power is achieved. [A13] Krishna and Singh, analyzes copper passivated MgO nano-ribbons (Cu-MgO-Cu

This work is licensed under a Creative Commons Attribution 4.0 License. For more information, see https://creativecommons.org/licenses/by/4.0/

NRs) for possible nano-interconnect applications. The authors utilize first-principles calculations based on density functional theory and the non-equilibrium Green's function. The delay and power delay product, which are important attributes of nano-interconnects, are explored. The findings suggest that Cu-MgO-Cu NRs with low parasitic parameters can potentially be employed for nano-interconnect applications. Copper and CNT interconnects continue to be pursued to achieve such scaling along with high current densities in [A14] Chandrakar et al., which considers the effects of cylindrical, barrel, hourglass and tapered solder bump geometries and tapered CNT-bundle and multilayer graphene nanoribbon (MLGNR) through-silicon vias (TSVs) on crosstalk and power loss. The authors conclude that the tapered bump and MLGNR TSV gives the best results. Cu-CNT composites provide unique electrical and thermal performance advantages along with process integration benefits over Cu or CNT alone and are hence of high interest. In [A15] Kumar and Kaushik, hybrid copper-carbon nanotube (Cu-CNT) interconnect modeling is presented with faster simulation times than by SPICE and with similar results. Finally, the paper in [A16] Singh et al., presents electrical modeling and a comprehensive analysis of Cu-CNT composite interconnects for sub-threshold circuit design. By developing analytical models for frequency-dependent resistivity and inductance, the sub-threshold crosstalk effect, transfer gain, and Nyquist stability of coupled Cu-CNT composite interconnects are analyzed.

ATTILA BONYAR, *Guest Editor*
Budapest University of Technology and Economics
1111, Budapest, Hungary

BRAJESH KUMAR KAUSHIK, *Guest Editor*
Indian Institute of Technology-Roorkee
Roorkee 247 667, India

JAMES E. MORRIS, *Guest Editor*
Portland State University
Portland OR 97201, USA

MARKONDEYARAJ PULUGURTHA, *Guest Editor*
Florida International University
Miami FL 33199, USA

APPENDIX: RELATED ARTICLES

[A1] K. Lahbacha, F. Zayer, H. Belgacem, W. Dghais, and A. Maffucci, "Performance enhancement of large crossbar resistive memories with complementary and 1D1R-1R1D RRAM structures," *IEEE Open J. Nanotechnol.*, vol. 2, pp. 111–119, 2021, doi: 10.1109/OJNANO.2021.3124846.

[A2] P. Zhao, Y. D. Lim, H. Y. Li, L. Guidoni, and C. S. Tan, "Advanced 3D integration technologies in various quantum computing devices," *IEEE Open J. Nanotechnol.*, vol. 2, pp. 101–110, 2021, doi: 10.1109/OJNANO.2021.3124363.

[A3] G. Boschetto, S. Carapezzi, and A. Todri-Sanial, "Graphene and carbon nanotubes for electronic nanopackaging," *IEEE Open J. Nanotechnol.*, vol. 2, pp. 120–128, 2021, doi: 10.1109/OJNANO.2021.3127652.

[A4] J. N. Tripathi, H. Vaghasiya, D. Junjariya, and A. Chordia, "Machine learning techniques for modeling and performance analysis of interconnects," *IEEE Open J. Nanotechnol.*, vol. 2, pp. 178–190, 2021, doi: 10.1109/OJNANO.2021.3133325.

[A5] A. Jain, H. Vaghasiya, and J. N. Tripathi, "Efficient selection and placement of in-package decoupling capacitors using matrix-based evolutionary computation," *IEEE Open J. Nanotechnol.*, vol. 2, pp. 191–200, 2021, doi: 10.1109/OJNANO.2021.3133213.

[A6] A. Bonyar, B. K. Kaushik, and J. E. Morris, "Guest editorial: Nanopackaging part I," *IEEE Open J. Nanotechnol.*, vol. 2, pp. 201–202, 2021, doi: 10.1109/OJNANO.2021.3134382.

[A7] S. Sudhindra, L. Ramesh, and A. A. Balandin, "Graphene thermal interface materials – State-of-the-Art and application prospects," *IEEE Open J. Nanotechnol.*, early access, Nov. 18, 2022, doi: 10.1109/OJNANO.2022.3223016.

[A8] A. Géczy, C. Farkas, R. Kovács, D. Froš, P. Veselý, and A. Bonyár, "Biodegradable and nanocomposite materials as printed circuit substrates: A mini-review," *IEEE Open J. Nanotechnol.*, early access, Nov. 10, 2022, doi: 10.1109/OJNANO.2022.3221273.

[A9] G. Miskovic and R. Kaufhold, "Additive manufacturing for nano-feature applications," *IEEE Open J. Nanotechnol.*, to be published, doi: 10.1109/OJNANO.2022.3224229.

[A10] A. Hassan, S. Soroushiani, A. Abdal, S. Y. B. Sayeed, W. -C. Lin, and M. R. Pulugurtha, "Embedded-component planar fan-out packaging for biophotonic applications," *IEEE Open J. Nanotechnol.*, vol. 3, pp. 52–60, 2022, doi: 10.1109/OJNANO.2022.3163386.

[A11] V. K. Sharma, J. N. Tripathi, and H. Shrimali, "Indefinite admittance matrix based modelling of PSIJ in nano-scale CMOS I/O drivers," *IEEE Open J. Nanotechnol.*, early access, Nov. 14, 2022, doi: 10.1109/OJNANO.2022.3221838.

[A12] J. N. Tripathi and D. Junjariya, "Large-scale optimization of decoupling capacitors using adaptive region based encoding scheme in particle swarm optimization," *IEEE Open J. Nanotechnol.*, to be published, doi: 10.1109/OJNANO.2022.3224061.

[A13] M. S. Krishna and S. Singh, "Copper passivated zigzag MgO nanoribbons for potential nanointerconnect applications," *IEEE Open J. Nanotechnol.*, early access, Nov. 18, 2022, doi: 10.1109/OJNANO.2022.3223151.

[A14] S. Chandrakar, D. Gupta, M. K. Majumder, and B. K. Kaushik, "Performance analysis of bump in tapered TSV: Impact on crosstalk and power loss," *IEEE Open J. Nanotechnol.*, early access, Nov. 14, 2022, doi: 10.1109/OJNANO.2022.3221815.

[A15] A. Kumar and B. K. Kaushik, "Transient analysis of hybrid Cu-CNT on-chip interconnects using MRA technique," *IEEE Open J. Nanotechnol.*, vol. 3, pp. 24–35, 2022, doi: 10.1109/OJNANO.2021.3138344.

[A16] A. Singh, B. K. Kaushik, and R. Dhiman, "Modeling and analysis of cu-carbon nanotube composites for sub-threshold interconnects," *IEEE Open J. Nanotechnol.*, early access, Nov. 10, 2022, doi: 10.1109/OJNANO.2022.3221141.