Performance Analysis of Bump in Tapered TSV: Impact on Crosstalk and Power Loss

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ABSTRACT   This study addresses the first feasible, and comprehensive approach to demonstrate a compact resistance-inductance-capacitance-conductance (*RLCG*) model for a multi-walled carbon nanotube bundle (MWB) and multilayered graphene nanoribbon (MLGNR) based tapered through silicon via (*T*-TSV) along with the different shaped bumps. The physical structures of bumps accurately considered the effect of the high frequency resistive impact and the inter-metal dielectric (IMD) layer. A mathematical framework has been designed for the parasitics of the cylindrical, barrel, hourglass and the tapered bump structures. The bump and via parasitics have been computed by utilizing the current continuity expression, partial inductance method, splitting infinitesimally thin slices of bump and triangular arrangement of tube assemblage. In order to validate the proposed model, the EM simulation is performed and compared against the analytical results. A remarkable consistency of the analytical and EM simulation-based results supports the proposed model accuracy. Furthermore, when compared to the MWB based structures, the MLGNR -based tapered TSV shows a substantial improvement in power loss and crosstalk. Furthermore, regardless of via height, the TSV with tapered bump structure reduces the overall crosstalk induced delay by 33.22%, 28.90%, and 21.61%, respectively, when compared to the barrel, cylindrical and the hourglass structure.

INDEX TERMS   Crosstalk-induced delay, multi-walled carbon nanotube bundle (MWB), insertion and reflection loss (S21, S11), resistance–inductance–conductance–capacitance (*RLGC*) model, through-silicon via (TSV), bump, 3D IC.

I. INTRODUCTION

Solder bumps are a specific type of input/output (I/O) interface between the TSVs in the microelectronics flip chip packaging system. It is a potential interface technique because it possesses superior electrical conductivity and thermal dissipation while maintaining a high connectivity density. This higher density prompted the creation of substantially compact TSV packaging system in the 3D IC [1]. The ever thriving compact system and bump miniaturization significantly lead to high current densities, intense Joule heating, and high temperatures. As a consequence of technology scaling, aggravates the electromigration and stress issues in the bump assemblages. Additionally, it is widely recognized that the electromigration is influenced by the geometry, volume, and structures of the solder bumps. Therefore, this facilitates

further investigated for the appropriateness of various bump structures in the TSV based 3D packages [2]. A state-of-the-art investigation stated in [3] is primarily deliberate about the conventional cylindrical bump in the fabrication attributes. The authors examined an in depth solution-based fabrication method for CNT bump structures at the room-temperature. Herein, the photolithographic process determined the photoresist patterns that are used as stencils during the cylindrical bump fabrication process. However, the cylindrical bump, on the other hand, generates a large current density, heat conduction, and excessive temperature due to the higher volume fraction and CTE, resulting in substantial electromigration. Later in [4], the researchers visualize a novel empirical technique that employs barrel and cylindrical flip chip bumps in the particle image velocimetry (PIV) based underfill flow

methodology. The barrel bump formed under the PIV process can contribute to the attainment of larger I/O, improved performance, and better yield. However, when the pitch of the bumps is excessively small, a large neck diameter and a low pad-to-neck ratio in the barrel structure are eventually realized to be a major consideration for a slower underfill flow, and inevitably lead to a crosstalk effect. In order to mitigate the issues associated with the barrel structure, the researchers in [5] examined hourglass-shaped solder joints. Herein, the hourglass shape has inherent benefits of improved power handling and underfill flow, lower strain and stress during thermal cycling, and longer lifetimes due to its smaller contact angle and neck diameter. However, owing to the larger volumetric topology, filling time increases in case of hourglass bump structure, that might cause delay in the packaging process. In recent, Motoyoshi et al. [6] explored the tapered bump structure for its suitable application at lower temperature, cost, load force and oxidation-free bonding, which is primarily due to the sharp pointed tapering structure resulting in a robust junction. However, the analysis accomplished in [3], [4], [5], [6] explores specific aspects of fabrication, while it pays limited emphasis to electrical modeling of bump and inter-metal dielectric parasitics. Later, Chandrakar et al. [7] considered the parasitic modeling and validation of cylindrical shaped bump by utilizing and comparing the analytical extraction of S parameter and electromagnetic simulation methods. However, the authors focused predominantly on the modeling of cylindrical structure while neglecting the electrical modeling of different shaped bump for the emerging nanomaterials. Therefore, a rigorous investigation is required to apostrophize the electrical modelling of various bump shapes and TSV modeling with the emerging nanomaterial.

In order to address the aforementioned research challenges, this work accurately addresses the electrical modeling based on the physical structures of different bump shapes. A closed form parasitic expression modeling of the bump inductance has been performed by utilizing the partial inductance method. Similarly, in order to obtain an underfill capacitance, the bumps are divided into infinitesimally small segments and integrating the infinite differential capacitance into a parallel segment. In similar manner, the current continuity expression in the cylindrical coordinate method is utilized in order to get the resistive component of the bump shapes. The proposed investigation also emphasizes on the numerical validation of effective parasitic for different bump shapes. Furthermore, scattering parameter in the EM simulation is used to validate the TSV-bump based equivalent circuit model. In the electrical model, a CMOS based DVL setup is utilized to analyze and compare the crosstalk-induced delay and power losses of the MWB and MLGNR based T-TSV model. The analysis was carried out at 22 nm technology, due to its increased device density, lower operating voltage, and power consumption.

The paper is organized as follows: Section I discourses outline of the current state-of-the-art exploration and briefs of the work carried out. Section II demonstrates the physical configuration of the different bump architecture along
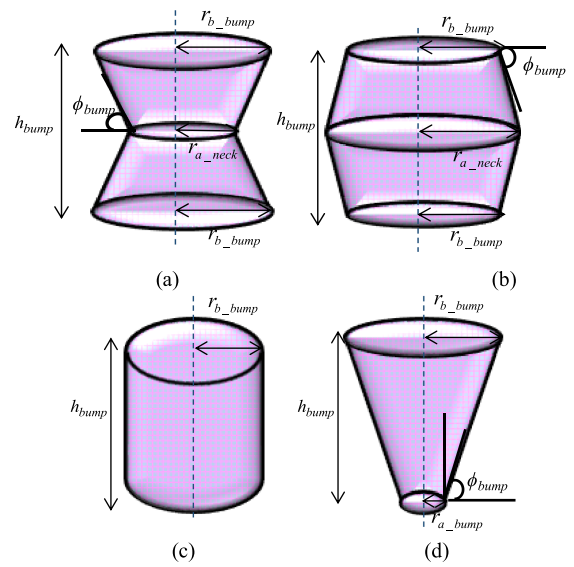

FIGURE 1. Physical configuration of different bump architecture: (a) Hourglass, (b) Barrel, (c) Cylindrical, (d) Tapered.

with the necessary geometrical parameters. Section III confers the *RLGC* model of TSV bump considering accurate physical parameters. Thereafter, Section IV sheds light on the crosstalk, insertion and reflection power losses. Finally, Section V summings-up the proposed work.

II. PHYSICAL CONFIGURATION

This section contains a thorough description of the TSV-bump shapes, physical characteristics and their material properties utilized in signal integrity analysis. The physical structures of different bump shapes, *i.e.*, hourglass, barrel, cylindrical, and tapered are depicted in Fig. 1. In order to fabricate the different bump geometry, a BCB based underfill layer is employed to isolate the bumps, limiting cross-coupling and leakage concerns. In addition, the flip-chip structure with BCB underfill material exhibits good performance with a better return and insertion losses due to its lower dielectric constant ($\varepsilon_r = 2.65$) results in low parasitic capacitive effects that help with the reduction of electrical power loss [8]. Additionally, the Sn-based bump is utilized to connect the CNT/GNR based through silicon via (TSVs) to the different logic systems. In addition, the IMD layer is employed to separate the bumps from the lossy silicon substrate. The physical configuration of the bumps (shown in Table 1) accompanying with the IMD layer is predominantly proposed for 22 nm technology. In the bump-IMD physical configurations, the distinctive physical parameters P_{bump}, h_{bump}, ϕ_{bump}, and h_{IMD} indicate the pitch distance between the bumps, height of the bump, tapering angle, and height of IMD layers, respectively. The r_{a_bump}, r_{b_bump} denotes the lower and upper radii of the bump in case of Tapered structure.

Apart from this, in case of Hourglass and Barrel structures, the r_{b_bump} and r_{a_neck} represents the upper/lower bump raddi
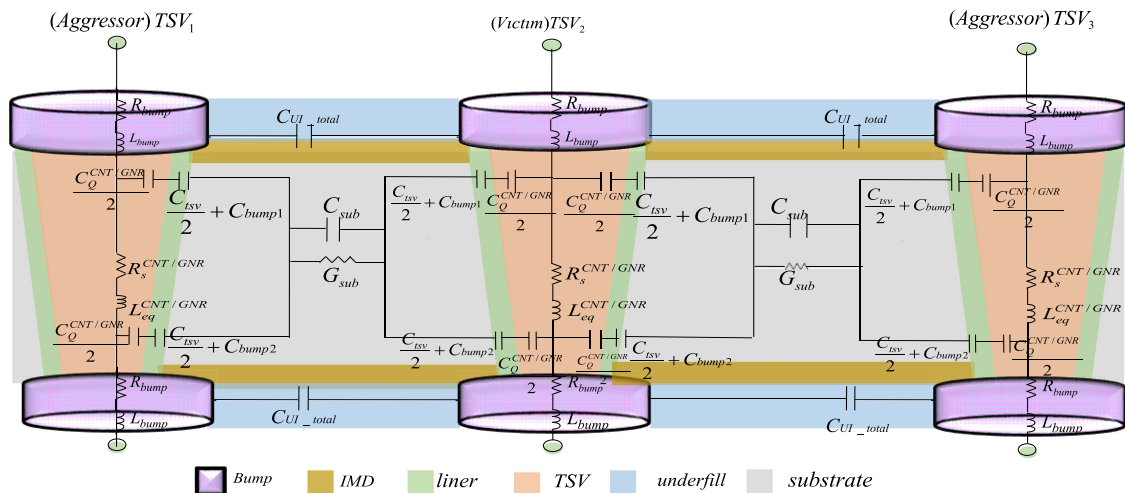
FIGURE 2. *RLGC* model of MWB and MLGNR based *T*-TSV.

Parameter	Symbol	Values
Bump/Via Pitch	P_{via}	3.82 μm
Bump height	h_{bump}	2.76 μm
Tapering angle bump	ϕ_{bump}	89°
IMD height	h_{IMD}	1.18 μm
T-bump upper radius	r_{b_bump}	2.50 μm
T-bump lower radius	r_{a_bump}	2.45 μm
Upper/lower radius of *H,B,C* bump	r_{b_bump}	2.50 μm
Neck radius of *H* bump	r_{neck}	2.48 μm
Neck radius of *B* bump	r_{neck}	2.80 μm
Oxide thickness	t_o^{tsv}	0.105 μm
Depletion layer width	t_d^{tsv}	0.691 μm
T-TSV upper radius	r_{b_tsv}	0.52 μm
T-TSV lower radius	r_{a_tsv}	0.17 μm
T-TSV height	h_{tsv}	20-120 μm
Tapering angle TSV	ϕ_{tsv}	89°

and central neck radius, respectively. In the physical configuration, the metal-insulator-semiconductor (MIS) based *T*-TSV is typically employed as it effectively offers DC isolation and avoids the leakage between the via and substrate. The TSV is surrounded by Metal oxide semiconductor (MOS) like insulating components including a liner (usually SiO_2) and a depletion layer. The performance of a via is mostly governed by the filler material utilized in the TSV bump based 3D packaging systems. In recent years, the necessity for technological scalability has principally drawn emphasis to the utilization of the emerging MWB and MLGNR based TSVs. Considering the scaling effect, an accurate *RLGC* modeling of CNT/GNR based *T*-TSV at 22 nm technology is presented in the subsequent section.

III. *RLGC* MODELING OF TSV-BUMP CONFIGURATION

An equivalent electrical *RLGC* model of a MWB (considering 15 shells in each MWCNT) and a MLGNR (having 208012

layers) based three coupled line via architecture at 22 nm technology is shown in Fig. 2. In the TSV configurations, the skin effect and the IMD layer have been taken into consideration in the extensive analysis of the *RLGC* model. In order to accomplish an analysis of the electrical properties, a lumped *Pi* model is taken into consideration. A TSV can be effectively treated as lumped circuit because an entity of the via can be categorized as relatively small if its physical dimensions are less than one tenth of its wavelength. Therefore, utilizing the lumped-based circuit model shown in Fig. 2, the corresponding parasitic expressions for the MWB and MLGNR-based TSV will be formulated. The parasitics included in the *RLGC* model primarily consists of an equivalent via scattering and bump resistances ($R_s^{CNT/GNR}+R_{bump}$) and inductance ($L_{eq}^{CNT/GNR}+L_{bump}$), equivalent bump and liner capacitance ($C_{tsv}+C_{bump1}+C_{bump2}$), quantum capacitance ($C_Q^{CNT/GNR}$), capacitance between the bump pair and the IMD layer ($C_{UI\_total}=C_{underfill}+C_{IMD}$), substrate conductance (G_{sub}) and capacitance (C_{sub}).

In order to compute the aforementioned bump parasitic, the resistive parameter for the *T*-bump is formulated using the current continuity expression in the cylindrical coordinate system [10] that can be represented as

$$\frac{1}{r}\frac{\partial}{\partial r}\left(rJ_r^{bump}\right)+\frac{\partial}{\partial z}\left(J_z^{bump}\right)=0\Bigg|_{r=0,Jr^{bump}=0} \quad (1)$$

The dc and high frequency resistive components are predominantly utilized the power consumption methodology [11] that can be presented as

$$R_{bump}^{dc}=\frac{1}{\left(I_{total}^{bump}\right)^2}\int_0^{h_{bump}}\left[\int_0^{r_{a\_bump}+\beta z}\left(\frac{\rho_{bump}\times\left(I_{total}^{bump}\right)^2\times 2\pi r dr}{\pi^2(r_{a\_bump}+\beta z)^4}+\frac{\rho_{bump}\times\left(\beta rI_{total}^{bump}\right)^2\times 2\pi r dr}{\pi^2(r_{a\_bump}+\beta z)^6}\right)\right]dz$$

$$=\frac{\rho_{bump}h_{bump}}{\pi r_{a\_bump}\left(r_{a\_bump}+\beta h_{bump}\right)}\times\left\{1+0.5\beta^2\right\} \quad (2)$$

Similarly the high frequency ac resistive component can be obtained as

$$R^{ac}_{bump} = \frac{\rho_{bump}\{2+\beta^2\}}{4\pi\beta\delta_{skin\_depth}} \log\left\{1 + \frac{2\beta h_{bump}}{2r_{a\_bump} - \delta_{skin\_depth}}\right\} \tag{3}$$

Whereas $\beta = \tan\alpha_{bump}$, $\alpha_{bump} = 90 - \varphi_{bump}$ and skin depth $\delta_{skin\_depth} = \sqrt{\rho_{bump}/\pi\mu f}$

Herein, ρ_{bump} represents the resistivity of the bump. The inductance of the T-bump is obtained by integrating the entire magnetic flux passing through the surface contained by the current loop and can be expressed as [12]

$$L_{bump} =$$

$$\frac{-\mu_0 \times \mu_{r,bump}}{4\pi}\left[h_{bump}\times\ln\left(\frac{r_{b\_bump}}{r_{a\_bump}}\right) + F^{bump}_{r_{a\_bump}} + F^{bump}_{r_{b\_bump}}\right] \tag{4}$$

where

$$F^{bump}_{r_{a\_bump}} =$$

$$\sqrt{r^2_{a\_bump}+h^2_{bump}} - h_{bump}\times\ln\left(\frac{h_{bump}+\sqrt{r^2_{a\_bump}+h^2_{bump}}}{r_{a\_bump}}\right) \tag{5}$$

Herein, $\mu_{r,bump} = 1$ denotes the relative permeability of bump, whereas for $F^{bump}_{r_{b\_bump}}$ one can replace r_{a_bump} with r_{b_bump} in the (5) for obtaining the equivalent bump inductance of (4).

Similarly, the underfill layer is utilised to minimize the leakage and cross-coupling between the bumps. The aformentioned underfill capacitance of the T-bump can be obtained by integral of infinitesimally parallel capacitance [13], that is represented by the (6) shown at the bottom of this page.

In similar manner, the bump also possesses capacitance with the Si substrate in the occurrence of IMD as a dielectric layer. The aforementioned T-bump parasitic is predominantly reliant on the thickness of the liner (t_o^{tsv}, t_d^{tsv}) and can be expressed as

$$C_{bump1} = \frac{\varepsilon_0\varepsilon_{r\_IMD}\times\pi\times\left\{(r_{a\_bump})^2 - (r_{b\_via}+t_o+t_d)^2\right\}}{h_{IMD}} \tag{7}$$

$$C_{bump2} = \frac{\varepsilon_0\varepsilon_{r\_IMD}\times\pi\times\left\{(r_{a\_bump})^2 - (r_{a\_via}+t_o+t_d)^2\right\}}{h_{IMD}} \tag{8}$$
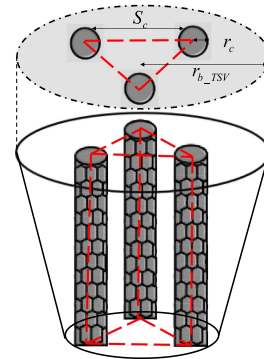

FIGURE 3. Triangular volumerical arrangement of CNT bundle.

In a similar manner, in the case of H and B bumps, one can split the bump into two halves and replace the r_{a_bump} with r_{a_neck} in expression (1) through (6) for obtaining the total bump resistance (R^{dc}_{bump}, R^{ac}_{bump}), inductance (L_{bump}) and underfill capacitance ($C_{underfill}$). Additionally, the bump capacitance (C_{bump1}, C_{bump2}) can be determined by replacing r_{a_bump} with the r_{b_bump}. Similarly, in case of C-bump, the total equivalent resistance, inductance and capacitance can be obtained by substituting $\beta = 0$ and replacing r_{a_bump} with the radius of cylindrical structure i.e., r_{b_bump} in the expression (1) through (8). Furthermore, in order to compute the TSV parasitics comprised of MWB based filler material, the impact of the nanoparticle electromagnetic component is effectively considered by utilizing the triangular intertube arrangement depicted in Fig. 3. In the intertube arrangement, the radius r_C of a MWCNT in MWB is considered as 0.5 nm. In addition, the bundle height placed above the ground plane and inter-shell/ inter-CNT distance are denoted as $H_g = 100$ μm and $S_C = 0.34$ nm, respectively. The overall number of MWCNT (N_{CNT}) in a bundle is proportionate to its volume and inversely related to its triangle configuration. The volume of MWB bundle in triangle configuration is depicted in Fig. 3 can be computed by (9).

$$Vol^{triangular}_{MWB} = \frac{\sqrt{3}}{4}\times(2r_C + S_C)^2 h_{tsv} \tag{9}$$

Thus, by utilizing the triangular volumetric configuration, the N_{CNT} of the T-TSV can be represented as

$$N_{CNT} = \frac{\frac{\pi}{3}\times(r^2_{a\_tsv} + r^2_{b\_tsv} + r_{a\_tsv}\times r_{b\_tsv})}{\frac{\sqrt{3}}{4}\times(2r_C + S_C)^2} \tag{10}$$

$$C_{underfill} = 2\pi\varepsilon_0\varepsilon_{r\_underfill}\left\{\frac{h_{bump}}{cash^{-1}\left[\frac{p^2_{via}}{2(r_{a\_bump})^2}-1\right]} - \frac{h^2_{bump}\tan\alpha_{bump}\times p_{via}\left[\frac{2(r_{a\_bump})^2-p^2_{via}}{\sqrt{p^2_{via}-4r^2_{a\_bump}}}-p_{via}\right]}{4\times r^3_{a\_bump}\left(\cosh^{-1}\left(\frac{p^2_{via}}{2(r_{a\_bump})^2}-1\right)\right)^2\left[\frac{p^2_{via}}{2(r_{a\_bump})^2}-1+\sqrt{\left(\frac{p^2_{via}}{2(r_{a\_bump})^2}-1\right)^2-1}\right]}\right\} \tag{6}$$

At low bias, applicable for TSV-bump application, a weak scattering by acoustic phonons results in a longer mean free path. Beyond the ballistic limit, the resistance of a CNT/GNR based TSV is height dependent. Fundamentally, the resistance of CNT/GNR based TSV has different components. Firstly, an intrinsic resistance that is dependent on the $h/4e^2$ (where h is the Planck's constant and e is the electronic charge) and the electron mean free path as a consequence of scattering [14]. Secondly, an additional contact resistance that is associated with imperfect contact.

In the proposed model, bump and TSV resistances are in the range of 133–1140 mΩ. However, the imperfect contact resistance is highly dependent on the fabrication process and the typical value of contact resistance is $\sim$3.5 kΩ [15]. In the equivalent model, the via ($R_s^{CNT/GNR}$) and bump resistances (R_{bump}) are in series and a higher value of contact resistance neglects the impact of bump and via resistance on the overall performance. Therefore, the adverse effect of contact resistance has been neglected to investigate the impact of TSV bumps on the crosstalk performance. Thus, the scattering resistance of the TSV is predominantly generated by the acoustic phonon scattering and can be represented as

$$R_s^{CNT} = \frac{h \times h_c}{4e^2 \times \lambda \times N_{total}} \quad (11)$$

$$C_{UI\_total} = C_{underfill} + C_{IMD}$$

$$C_{via\_total} = (C_Q^{CNT/GNR}$$
$$\times \left(C_{tsv} + C_{bump}\right))/(C_Q^{CNT/GNR}$$
$$+ C_{tsv} + C_{bump})$$

$$C_{tsv} = \left(C_{ox}C_{dep}\right) / \left(C_{ox} + C_{dep}\right)$$

where h represents the Planck's constant; λ denotes the electron mean free path and the total number of conducting channel $N_{total} = \sum_{i=1}^{N_{CNT}} N_i$ that can be obtained using the sum of each conducting channel (N_i) in a MWCNT [15].

The MWB inductance (L_{eq}^{CNT}) accompanying both kinetic and magnetic effect and the quantum capacitance (C_Q^{CNT}) is characterized using the finite density of states can be obtained from [15].

Additionally, the GNR based T-TSV parasitics (R_s^{GNR}, L_{eq}^{GNR}, C_Q^{GNR}) can be determined by replacing N_{CNT} with the number of graphene sheet (shown in Fig. 4) that can be represented by (12) [16].

$$N_{layer} = 1 + Integer \left(\frac{t_{tsv}}{S_c}\right) \quad (12)$$

where t_{tsv} and S_c denotes the thickness and the interlayer distance of the graphene sheets, respectively. Using expressions (1) through (12), the quantitative values of the via and the bump parasitics are summarized in Tables 2 and 3, respectively.
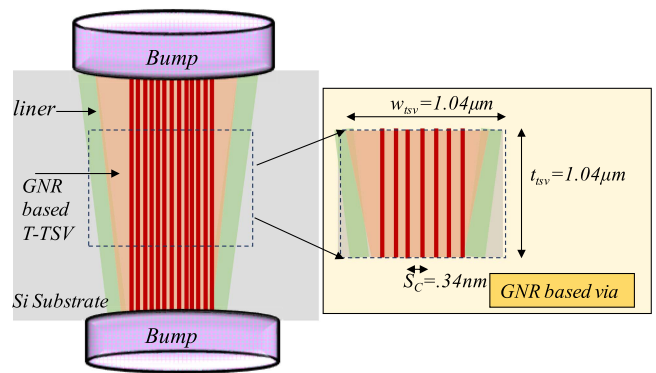

FIGURE 4. Triangular volumerical arrangement of GNR based TSV.

TABLE 2. *RLGC* Parameter of TSV Parasitic

Parasitic	TSV material	Parasitic values of *T*- TSV with *CNT* ,*GNR* filler material for different TSV heights.			
		h_{tsv}= 20 μm	h_{tsv}= 60 μm	h_{tsv}= 100 μm	h_{tsv}= 120 μm
$R_s^{CNT/GNR}$ (mΩ)	*CNT*	820	910	1129	1250
	GNR	770	833	1044	1140
$L_{eq}^{CNT/GNR}$ (pH)	*CNT*	47.21	53.11	61.20	72.33
	GNR	32.99	44.30	51.90	66.98
$C_Q^{CNT/GNR}$(nF)	*CNT*	0.08	0.09	0.10	0.23
	GNR	0.05	0.08	0.09	0.18
C_{via_total}(fF)	*CNT*	3.24	5.44	9.00	10.43
	GNR	3.18	5.22	8.86	9.98
C_{sub} (fF)	-	2.28	3.10	3.91	4.21
C_{tsv} (fF)	-	3.14	5.35	8.91	10.33
G_{sub} (mΩ)$^{-1}$	-	0.21	0.29	0.32	0.38
$N_{CNT/layer}$	*CNT*	11291	11291	11291	11291
	GNR	208012	208012	208012	208012

TABLE 3. *RLGC* Parameter of Bump Parasitic

Parasitic	Bump Shape	Parasitic values of *T*- TSV with *C,T,B,H*-Bump
R_{bump}(mΩ)	*B*	133
	C	186
	H	190
	T	266
L_{bump} (pH)	*B*	5.22
	C	6.91
	H	7.33
	T	9.22
C_{UI_total}(fF)	*B*	1.90
	C	1.77
	H	1.30
	T	1.10
C_{bump1} (fF)	*B*	0.22
	C	0.18
	H	0.10
	T	0.06
C_{bump2} (fF)	*B*	0.22
	C	0.18
	H	0.10
	T	0.08
$C_{underfill}$(fF)	*B*	2.11
	C	1.88
	H	1.50
	T	1.28

$$C_{UI\_total} = C_{underfill} + C_{IMD}$$
$$C_{via\_total} = (C_Q^{CNT/GNR} \times (C_{tsv} + C_{bump}))/ (C_Q^{CNT/GNR} + C_{tsv} + C_{bump})$$
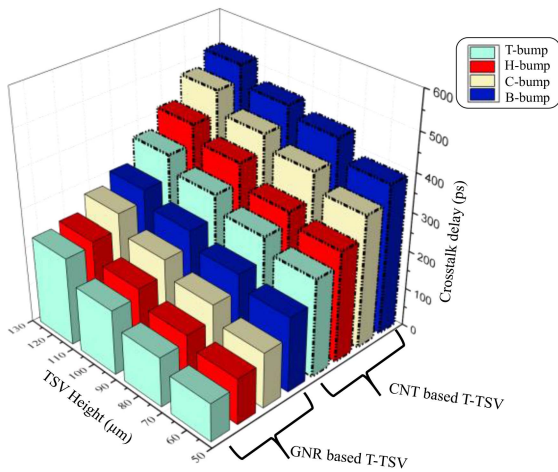$$C_{tsv} = (C_{ox}C_{dep})/ (C_{ox} + C_{dep})$$

FIGURE 5. In phase crosstalk induced delay for different TSV bump configuration.

FIGURE 6. Out phase crosstalk induced delay for different TSV bump configuration.

IV. CROSSTALK AND POWER LOSS ANALYSIS

This section analyzes the signal integrity of the MWB and MLGNR-based T-TSV by utilizing the three coupled line DVL arrangement at 22 nm technology. Using the DVL setup, the barrel, tapered, cylindrical and hourglass shaped bumps are analyzed in terms of crosstalk induced delay and power loss (*i.e.*, insertion and reflection loss). In the three-line coupled TSV, a certain amount of time delay occurs after signal has travelled through a TSV. In this scenario, one of the TSV may behave as an aggressor, while the other as a victim. When all of the signals passing through the aggressor and victim lines are in the same switching state (in-phase) or the opposite (out-phase), the dynamic crosstalk delay phenomenon occurs [17], [18]. A comparative investigation for crosstalk-induced delay is exhibited for MWB and MLGNR based T-TSV by utilizing the different solder bump configurations. The *RLGC* model of the different TSV bumps are driven by a CMOS driver at 22 nm technology. The in-phase and out-phase delays are examined for barrel, cylindrical, tapered and the hourglass bumps with the MWB and MLGNR based T-TSVs for different via heights as shown in Figs. 5 and 6, respectively. It is perceived that the dynamic crosstalk (in-phase and out-phase) are significantly reduced for MLGNR based TSV in comparison with the MWB. It is due to the fact that the conducting channel *i.e.*, N_{total} increases in MLGNR based TSV that can cause the reduction of R_s^{GNR} (shown in Table 2) with a substantial improvement in the C_Q^{GNR}. However, due to the dominating influence of the liner capacitance *i.e.*, C_{tsv}, the equivalent value of total capacitance $C_{via\_total} = (C_Q^{GNR} \times (C_{tsv} + C_{bump}))/(C_Q^{GNR} + C_{tsv} + C_{bump})$ remain relatively constant (Tables 2 and 3). Thus, the cumulative influence of both R_s^{GNR} and C_{via_total} causes the 25.33% lesser crosstalk in case of MLGNR based T-TSV in comparison to the MWB.

In addition, it is also depicted that compared to the other bump shapes, the tapered bump possesses lower crosstalk delay. It is due to the fact that a reduced cross-section area in the tapering structure primarily lowers the cumulative effect
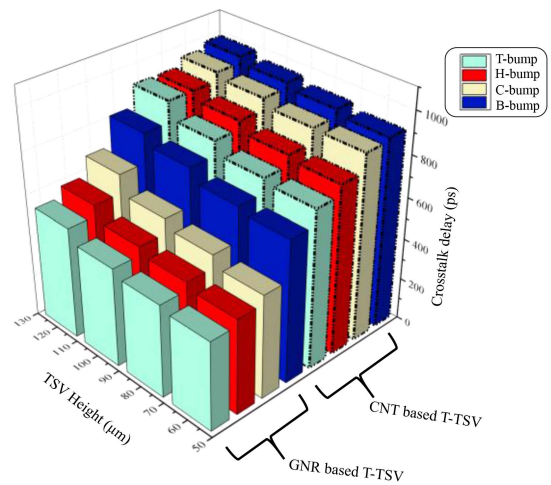
TABLE 4. Percentage Improvement in Crosstalk Induced Delay Using MLGNR Based *T*-TSVs for Different via Heights

TSV height	% improvement in crosstalk induced delay of MLGNR based *T*-TSV in comparison to MWB based *T*-TSV	
	Out-phase	In-phase
50 μm	15.13%	19.12%
70 μm	18.33%	22.31%
90 μm	20.78%	25.18%
110 μm	22.24%	29.22%

of bump parasitics *i.e.*, R_{bump}, L_{bump}, $C_{underfill}$ and hence an improved crosstalk delay.

Furthermore, Table 4 summarizes the percentage improvement in crosstalk induced delay for a MLGNR based T-TSV compared to MWB filler material at different TSV heights. It can be inferred that, the overall out-phase delay improvement is perceived to be less than the in-phase delay. This is due to the fact that the Out-phase produces a larger delay than the in-phase due to the Miller capacitive effect, which causes the coupling capacitance to nearly double by a factor of two. The dominating capacitive coupling parameter in the cross-coupling miller's effect has significant contribution to the Signal integrity (crosstalk) degradation that can be represented in the coupling model (shown in Fig. 7). In the capacitive coupling model, the authors in [19] analyzed the transfer function from V_{in} to V_{out} that can be expressed as

$$V_{out} = V_{in} \cdot \frac{Z_2 Z_3 Z_4}{Z_1(Z_2 Z_3 + Z_2 Z_4 + Z_3 Z_4 + Z_3 Z_5) + Z_2 Z_3 Z_4 + Z_5(Z_1 Z_4 + Z_2 Z_3 + Z_2 Z_4)} \quad (13)$$

where

$$Z_5 = 2Z_{\left[\frac{C_Q^{CNT/GNR} \times (C_{tsv} + C_{bump})}{C_Q^{CNT/GNR} + (C_{tsv} + C_{bump})}\right]} + Z_{C_{sub}}//Z_{R_{sub}} + 2Z_{C_{underfill}} + C_{IMD} \quad (14)$$
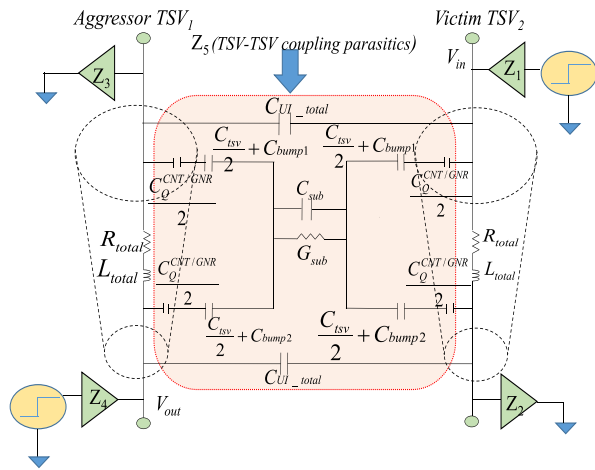
FIGURE 7. TSV-to-TSV capacitive coupling model of the TSV bump architecture.

FIGURE 8. Reflection loss (S11) for different TSV bump configuration in CNT based TSV.

Z_2, Z_3, Z_4 are the termination impedance, Z_1 denotes the driver impedance that is dependent on the technology, and Z_5 represents the coupling-channel impedance. The coupling level between the neighboring TSVs (aggressor and victim) are predominantly influenced by the coupling-channel impedance (*i.e.*, Z_5). Therefore, in order to reduce the cross coupling effect, the channel impedance should be increased in the TSV-bump model that can cause the reduction of in-phase and out-phase crosstalk induced delay. In addition, relative changes on shorter delays obtained in case of in-phase (shown in Table 4), may appear to be more significant because a small absolute change in the number can result in a large percentage improvement.

Furthermore, Table 4 demonstrates that, as the TSV height increases from 50 to 110 μm, the worst case crosstalk delay (*i.e.*, out-phase) worsens by 15.13% in the case of 50 μm and improves by 22.24% in the case of 110 μm. This is primarily due to the fact that, the CNT/GNR concentration increases with higher TSVs, and thus the conductivity becomes a significant physical aspect impacting the crosstalk-induced delay. Furthermore, higher TSVs based on CNTs/GNRs are more beneficial because their conductivity increases as the number of CNTs/GNRs increases, resulting in a substantial improvement in crosstalk-induced delay. In addition, for CNT/GNR-based higher TSVs, the via height profoundly influenced the improved crosstalk-induced delay, that is contributed to less phonon scattering due to a smaller contact interface area [20]. Furthermore, for the better electrical transport, it is critical to reduce the contacts area in order to attain greater electrical conductivity by utilizing the higher MLGNR based *T*-TSVs.

Power loss is one of the most significant factors that can influence the overall performance of a 3D IC. Figs. 8 through 11 depicts the power loss in terms of *S* parameter for different bump structures. The power loss due to reflection (*S11*) and insertion (*S21*) are investigated using the structural EM
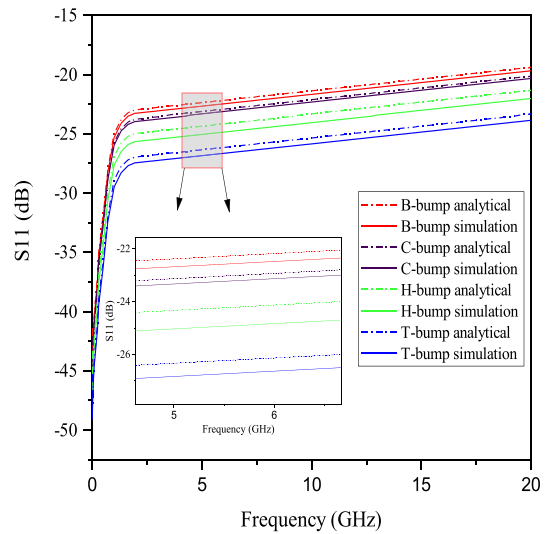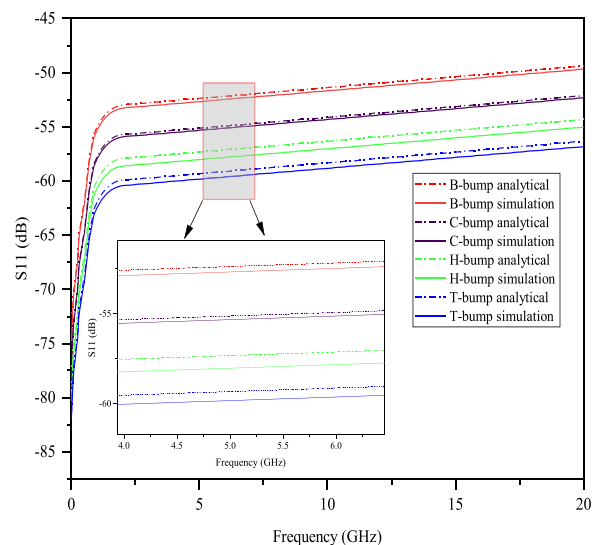

FIGURE 9. Reflection loss (S11) for different TSV bump configuration in GNR based TSV.

simulation. In addition to the EM simulation, the quantitative values of the lossy parameters can be obtained by utilizing the *Pi* based *RLGC* network as shown in Fig. 2.

The network impedance obtained in the power loss electromagnetic model can be expressed as

$$Z_1^{CNT(GNR)} = R_{bump} + R_{tsv} + s(L_{bump} + L_{tsv}) \quad (15)$$

$$Z_2^{CNT(GNR)} = \frac{2 + 2sC_{sub}R_{sub} + 4sR_{sub}C_{via\_total}}{(C_{via\_total} + C_{UI\_total})(2s^2C_{sub}R_{sub} + 2s) + 4s^2R_{sub}C_{UI\_total}C_{via\_total}} \quad (16)$$

The *S* parameter obtained by utilizing the aforementioned expression and the relation obtained from [21], [22], [23].
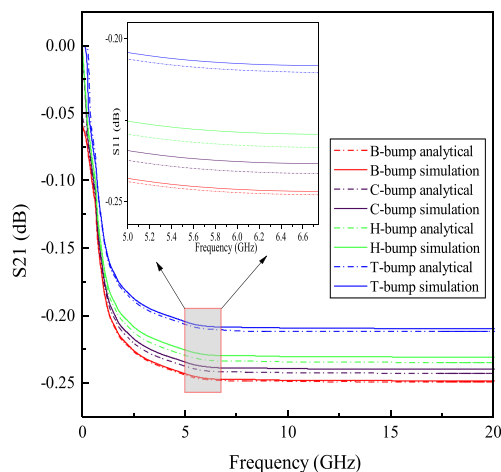
FIGURE 10. Insertion loss (S21) for different TSV bump configuration in CNT based TSV.
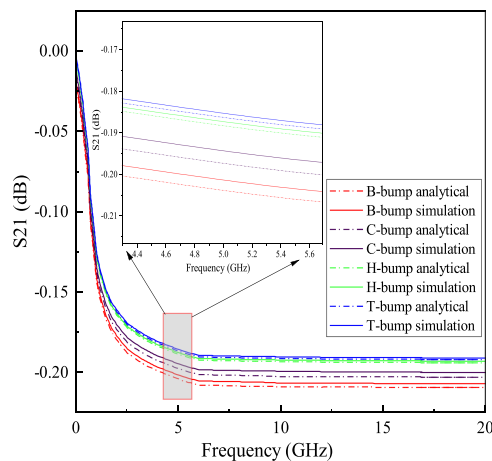

FIGURE 11. Insertion loss (S21) for different TSV bump configuration in GNR based TSV.

A comparative investigation of S parameters for cylindrical, tapered, hourglass and barrel shaped bump structures are represented in Figs. 8, 9, 10 and 11, respectively. The quantitative values of analytical result are found to be in good agreement with the simulated results, with the deviation for insertion and return losses less than 0.003 dB and 0.5 dB, respectively. Furthermore, as illustrated in Figs. 8 through 11, the tapered bump outperforms in comparison with the other shapes in terms of overall power loss ($S11$ and $S21$). This is primarily due to the smaller $C_{underfill}$, implying a larger capacitive reactance, resulting in less signal leakage from the bump to the underfill, and the lower dielectric loss caused by the leakage improves the power loss. Furthermore, when compared to the MWB, an MLGNR-based TSV possesses higher insertion (S21) and lower reflection losses (S11). It is due to the fact that the lower cumulative values of R_s^{GNR} and C_{via_total} prevents the power loss leakage to the substrate. Furthermore, it reveals that irrespective of frequency, the MLGNR based tapered TSV exhibits a reduced insertion and reflection losses of 4.27% and 3.85% respectively. Therefore, it can be concluded that

MLGNR based T-TSV provides an improved signal integrity and power loss.

V. CONCLUSION

An analytic or semi-analytic formulation of the TSV-bump parasitic has been done for the different shaped bump architecture along with the MWB and MLGNR based TSV. In order to validate the proposed bump shapes, the analytical result of the S parameter is compared with the EM simulation. It can be perceived that the analytical results are in good agreement with the simulation methodology. Using an $RLGC$ based Pi model of scattering parameter, an analytical result of S parameter is obtained that reveals an average deviation of only 0.02 dB compared to the EM simulated result. It can be observed that power loss and the crosstalk significantly improved for the T-bump in comparison with the other bump configuration. It is due to the lower parasitic values of T-bump decreases the cross-coupling miller capacitive effect due to its reduced cross-sectional area from top to bottom that can enhance its performance. In order to achieve an improved performance, the 3D chip stacking technology have been utilized the tapered bump structure. It is due to the fact that, the tapered bump is suitable for a thermo-compression bump joint process with low temperature, load force and higher yield. Herein, the collapsed bump height and the electrical parasitics can be controlled by compression force. The lower electrical parasitics in tapered structure provides an improved crosstalk induced delay that can create an improved performance. In addition, the tapered structure provides the better filling that inturn creates a larger capacitive impedance and reduces the underfill capacitances resulting in low loss leakage and improved power handling application. Therefore, it can be inferred that the tapered bump can be utilized in a densely packed next generation 3D IC system.

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