Indefinite Admittance Matrix Based Modelling of PSIJ in Nano-Scale CMOS I/O Drivers

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ABSTRACT The past decade has witnessed a tremendous reduction in the feature size from the deep-submicron to the advanced nano-scale CMOS devices. In nanoscale devices based high-speed systems, the budgeting of jitter due to supply fluctuations is one of the major performance bottlenecks while designing integrated circuits (ICs). In this paper, an accurate and efficient method to analyse power supply induced jitter (PSIJ) in CMOS N-stage inverters is developed using the estimation-by-inspection method. Based on the Indefinite Admittance Matrix, a reduced two-port network is developed for a multiple-input circuit, considering the presence of the supply/bulk/ground sources. The closed-form expressions of the PSIJ have been evaluated for a single and N-stages CMOS inverter chain. The expression is also valid for the PSIJ analysis at any intermediate stage of the N-stage chain. For validation purpose, the circuits are designed in a standard 28 nm CMOS technology with V_{DD} of 1 V. The analytical results are compared with the simulation and the experiments. The maximum mean percentage error for EDA simulation and experimentally measured results are 2.4% and 13%, respectively. The proposed analysis is compared with some of the existing PSIJ modelling techniques and shows a significant improvement in speed-up factor and error percentage.

INDEX TERMS Two-port network, indefinite admittance matrix (IAM), power supply induced jitter (PSIJ), nano-scale devices.

I. INTRODUCTION

Bell Laboratories invented the first working Field Effect Transistor (FET) in 1947. However, at that time, people could not anticipate the broad societal impact of the device. Later, as the research progressed, the invention of the transistor greatly benefited society, and the widely used metal-oxide-semiconductor field-effect transistor (MOSFET) and complementary CMOS were invented by Bell Laboratory in 1959 and 1963, respectively. Due to the scaling ability of MOSFET with technology, it is a popular choice for IC designs. As the continuous research progresses, the feature size scales beyond the nano-scale range (5 nm or beyond), leading to a significant increase in the number of transistors on a die with more functionalities [1]. Additionally, nano-devices (nanotechnology) promise a significant enhancement in electronic devices in terms of faster, smaller and energy-efficient devices to consumers. The development of new nano-devices/materials favours modern science, which continuously satisfies Moore's law [2]. The modern nano-devices will also improve the performance and efficiency of integrated nano-electronics.

Moreover, with the shift towards advanced nanotechnology nodes, the on-die current density increases exponentially along with voltage ripples, with a significant reduction in supply voltages. The voltage ripples (power supply noise) in the present nano-scale regime occur in several hundreds of MHz frequencies with an amplitude variation of $\pm 10\%$ from the nominal supply. These ripples can cause several significant design challenges along with short-channel and higher-order effects that were never before anticipated [3]. The problem is even worse with the increasing prominence of CMOS nano-devices (nanotechnology) in high-performance circuitry with higher operating frequencies and faster transient time. Today, many leading semiconductor industries have already started the mass production of chips in a 3 nm

technology node using Gate-All-Around (GAA) transistor architecture and FinFet [4], [5].

In the smaller technology nodes, power supply noise (PSN) is one of the critical factors that degrade the performance of the overall system [6]. In addition, the highly compact and large number of transistors in a circuit can cause more nonlinear effects by which the amplitude of supply noise harmonics rises, eventually leading to bit failure. Therefore, maintaining signal integrity (SI) and power integrity (PI) is very challenging in high-speed nanodevice-based circuits [7], [8], [9], [10]. The term SI and PI deals with the quality of signal and the quality of power, respectively. The degradation in either term can significantly deteriorate the overall functionality of the system in terms of noise margin, setup/hold time violations, bit error rate (BER), jitter, etc.

The AC fluctuations, commonly known as supply noise, present in the supply voltages are one of the dominant causes that can substantially impact the SI and PI of any high-speed analog and mixed signal (AMS) system [11]. The undesired fluctuations in the nominal supply voltage are known as the PSN, bulk supply noise (BSN), ground supply noise (GSN), and the input data noise (IDN). The sources of these noises are simultaneous switching noise (SSN), IR drop, distortions in the power delivery network, insertion-loss, reflection, etc. [10]. These fluctuations can lead to power supply-induced jitter (PSIJ) at the output of a circuit. It can be defined as dynamic variations in the delay of a circuit due to supply noise. Among the other jitter components, PSIJ significantly impacts the timing budget in present high-speed SoCs [12]. Note that the timing uncertainty and noise increase with technology scaling together with higher integration density [13], [14]. Therefore, accurate analysis of the PSIJ is essential to achieve lower BER in high-speed nanotechnology-based circuits.

Various PSIJ modelling techniques such as frequency-domain analysis, delay-based techniques, statistical methods, recursive method, slope-based methods, piece-wise linear/nonlinear modelling, numerical method, and Input/output Buffer Information Specification (IBIS) model-based approach are discussed in [10]. In the process of determining the closed-form expression for the PSIJ, knowledge of transfer function (TF) is essential in the presence of deterministic supply noise sources. Note that, most of the PSIJ methods are directly or indirectly based on the supply-to-output TF [15], [16], [17], [18], [19], [20], [21], [22], [23], [24], [25], [26], [27], [28], [29], [30], [31], [32]. Among these methods, an efficient method for PSIJ (EMPSIJ) method is a better choice in terms of computational efforts. The EMPSIJ method is based on the one-bit simulation and small-signal TF analysis. The TF analysis in the reported works is based on the conventional nodal analysis which can be further simplified using the Thomas algorithm, symbolic admittance method, etc. in [27], [28]. However, these methods are a bit time consuming as they require a large number of expressions and matrix elements to solve the final expression including the PSN, GSN, and the BSN. Therefore, an efficient, fast, and
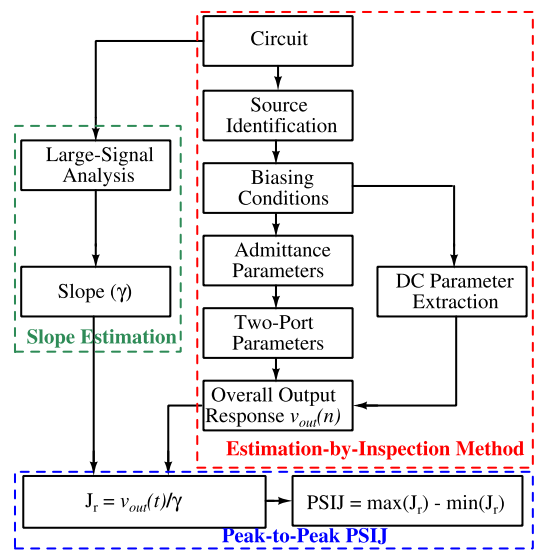

FIGURE 1. Complete flow of proposed PSIJ method.

accurate TF (supply-to-output) method is necessary for the PSIJ analysis for a circuit.

In this paper, a computationally efficient method is developed to determine the closed-form expression for the PSIJ for a chain of CMOS inverters. The method also has the capability to determine the PSIJ at the output of any stage of the chain. The method is based on the generalised two-port network, which is developed using the estimation-by-inspection method [33]. The inverters are considered as I/O circuits for the purpose of analysis. For the validation purpose, five stages of CMOS inverters are modelled and verified by simulation results. Furthermore, the proposed method is compared with some of the existing PSIJ modelling methods in terms of computational time, speed-up factor, and percentage error.

II. PROPOSED ANALYSIS FOR THE ESTIMATION OF PSIJ

Fig. 1 shows the flow chart of the proposed PSIJ methodology. The combination of both the estimation-by-inspection and the slope-based methods develops the closed-form expression of PSIJ. The details of these methods are given in the following sub-sections.

A. ESTIMATION-BY-INSPECTION METHOD

The estimation-by-inspection method, based on the indefinite admittance matrix (IAM), is very efficient in terms of matrix elements and computational complexity [33]. Using estimation-by-inspection method, the SI metrics can be estimated by just using a few node admittance elements. Further, depending on the users' practice, the small-signal model of the circuit is not required.

The algorithm starts by extracting the required IAM elements for the circuit including all the nodes. The required IAM ($Y_{i,i}$, $Y_{o,o}$, $Y_{o,i}$, $Y_{i,o}$) elements refers to the matrix entries those are required for the analysis. The $Y_{i,i}$ and $Y_{o,o}$ refer to the self admittance parameters of input and output nodes,

respectively. $Y_{o,i}$ and $Y_{i,o}$ are the negative signed mutual admittance parameters between output-to-input and input-to-output nodes, respectively. Next, to determine the closed-form expressions of the metrics, the superposition theorem is applied on the circuit by selecting one excited input node at a time. Finally, the individual gain/TF, impedance, overall gain, and phase expressions can be calculated using the following formulae.

$$A_{v_i} = \frac{-|Y_{o,i}|}{|Y_{o,o}|}, \quad \phi = \pi - \angle A_{v_i}(j\omega) \tag{1}$$

$$Z_i = \frac{Y_{o,o}}{\begin{vmatrix} Y_{i,i} & Y_{i,o} \\ Y_{o,i} & Y_{o,o} \end{vmatrix}}, \quad Z_{out} = \frac{|Y_{i_m,i_m}|}{\begin{vmatrix} Y_{i_m,i_m} & Y_{i_m,o} \\ Y_{o,i_m} & Y_{o,o} \end{vmatrix}}, \tag{2}$$

where A_{v_i} is the respective input-to-output voltage gain, and Z_i is the input impedance seen at the input terminal. The subscripts i and o are the notation for input and output terminals, respectively. Next, the term Z_{out} indicates the output impedance, and i_m is the main (primary) input terminal of a circuit.

B. THE SLOPE BASED METHOD

The transition-edge slope deviates due to the presence of small-signal AC ripples riding on the purely DC quantity in the DC-power supply. Hence, the slope can be used to calculate the PSIJ TF. In paper [21], the EMPSIJ has been derived which is based on a one-bit simulation. The EMPSIJ method is a semi-analytical analysis in which both large- and small-signal analyses are required. The large-signal analysis is performed to estimate the slope at a midpoint at the rise/fall output transition edge. To calculate the overall transient response in the presence of supply fluctuations, the small-signal analysis is required. However, the conventional method for the estimation of output transient response is a quite cumbersome and extensive process. Therefore, the proposed estimation-by-inspection method has been used for algebraically simple and computationally fast analysis. The instantaneous jitter (J_r) is calculated as:

$$J_r = \frac{(\Delta v_{out})_{t_m}}{\gamma}, \tag{3}$$

where Δv_{out} is the small-signal TF in presence of all supply noise (PSN, GSN and BSN) sources. γ refers to the slope of output response at the mid-point (t_m) in absence of supply fluctuations.

C. PSIJ ESTIMATION USING INSPECTION METHOD

As discussed in the previous subsection, the PSIJ can be calculated using small-signal transient response and slope of the transition edge. The small-signal transient response in the presence of multiple supply noise sources can be estimated using the proposed inspection-based method.

$$\Delta v_{out} = A_{v_{in}} \frac{1}{Y_{o i_m}} \sum_{i=1}^{p} Y_{oi} v_i \tag{4}$$
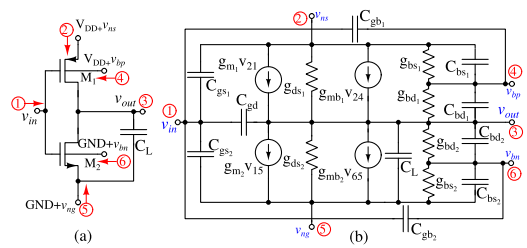

FIGURE 2. Schematic and small-signal diagram of an inverter.

TABLE 1. The Required IAM Parameters for the Inverter

Y_{ij}	Expressions	Y_{ij}	Expressions
Y_{11}	$s(C_{gd}+C_{gs}+C_{gb})$	Y_{13}	$-sC_{gd}$
Y_{22}	$s(C_{gs_1}+C_{bs_1})+\beta_2$	Y_{23}	$-g_{ds_1}$
Y_{31}	$g_{m_1}+g_{m_2}-sC_{gd}$	Y_{32}	$-g_{m_1}-g_{mb_1}-g_{ds_1}$
Y_{33}	$g_{ds}+g_{bd}+sC_1$	Y_{34}	$g_{mb_1}-g_{bd_1}-sC_{bd_1}$
Y_{35}	$-g_{ds_2}-g_{mb_2}-sC_L$	Y_{36}	$g_{mb_2}-g_{bd_2}-sC_{bd_2}$
Y_{43}	$-g_{bd_1}-sC_{bd_1}$	Y_{44}	$g_{bs_1}+g_{bd_1}+s(C_{bd_1}+C_{bs_1}+C_{gb_1})$
Y_{53}	$-g_{ds_2}-sC_L$	Y_{55}	$\beta_3+s(C_L+C_{bs_2}+C_{gs_2})$
Y_{63}	$-g_{bd_2}-sC_{bd_2}$	Y_{66}	$g_{bs_2}+g_{bd_2}+s(C_{bd_2}+C_{bs_2}+C_{gb_2})$

In equation (4), $A_{v_{in}}$ refers to the input-to-output gain of a circuit. Y_{oi} is the admittance between two nodes where subscript o is output terminal, i refer to the input supply noise terminals, and i_m denotes the primary (main) input of the circuit.

The instantaneous jitter can be calculated using the expressions (3) and (4). Finally, the PSIJ can be evaluated as the difference between the maximum and minimum values of J_r.

$$PSIJ = \max\left\{J_r^k\right\}_{k=1}^n - \min\left\{J_r^k\right\}_{k=1}^n \tag{5}$$

III. VALIDATION OF THE PROPOSED METHOD

CMOS inverters have diverse applications in the AMS system such as I/O circuits, drivers, delay-lines, clock-distribution networks, I/O pads, etc. Moreover, the inverters are more sensitive in the presence of a noisy power supply. This leads to jitter at the output, and can further degrade an overall system-performance. For the validation purpose, three different examples viz. a single-stage inverter, an N-stage CMOS inverters, and an intermediate stage of N cascaded inverters have been considered in this paper.

A. A SINGLE STAGE CMOS INVERTER

The schematic, and the small-signal diagram of a CMOS inverter are depicted in Fig. 2. The possible paths of supply noise in the circuit are denoted by red circled arrows (i.e. ①, ②, ④, ⑤ and ⑥) in Fig. 2. The required IAM parameters to estimate the TFs and I/O impedance are mentioned in Table 1.

The voltage gain and the impedance expressions for the inverter can be formulated using (1)-(2) as:

$$A_{v1} = \frac{-g_{m_1}-g_{m_2}+sC_{gd}}{\beta_1+sC_1}, A_{v2} = \frac{g_{m_1}+g_{mb_1}+g_{ds_1}}{\beta_1+sC_1},$$

$$A_{v4} = \frac{-g_{mb_1}+g_{bd_1}+sC_{bd_1}}{\beta_1+sC_1},$$

$$A_{v5} = \frac{g_{m_2} + g_{mb_2} + g_{ds_2} + sC_L}{\beta_1 + sC_1},$$

$$A_{v6} = \frac{-g_{mb_2} + g_{bd_2} + sC_{bd_2}}{\beta_1 + sC_1}, \qquad (6)$$

$$Z_1 = \frac{\gamma_1 + sC_1}{s^2(C_8C_1 - C_{gd}^2) + s(C_8\gamma_1 + g_mC_{gd})},$$

$$Z_2 = \frac{\gamma_1 + sC_1}{\alpha_1 s^2 + \alpha_2 s + \alpha_3}, \qquad Z_4 = \frac{\gamma_1 + sC_1}{\alpha_4 s^2 + \alpha_5 s + \alpha_6},$$

$$Z_{out} = \frac{sC_2}{s^2(C_1C_2 - C_{gd}^2) + s(C_{gd}g_m + C_8\gamma_1)},$$

$$Z_5 = \frac{\gamma_1 + sC_1}{\alpha_7 s^2 + \alpha_8 s + \alpha_9}, \qquad Z_6 = \frac{\gamma_1 + sC_1}{\alpha_{10} s^2 + \alpha_{11} s + \alpha_{12}}. \qquad (7)$$

The subscript in the gain (A) and the impedance (Z) expressions refer to the input terminal. For example, A_{v1} is the input-output voltage gain and Z_1 is impedance at terminal ① of an inverter circuit. The parameters in the above expressions are extracted at the pre- and post-layout stages of the circuit design. The estimations of the above expressions using the estimation-by-inspection method are computationally efficient as compared to the other existing methods [33]. The expressions of unknown parameters in the aforementioned equations are shown in Appendix A. These parameters are useful for the systematic design of a circuit to nullify or minimize the effect of PSIJ.

The overall voltage gain ($\tilde{A}_{v_{inv}}$) of the inverter is:

$$\tilde{A}_{v_{inv}} = G_m Z_{out}, \qquad (8)$$

where,

$$G_m = \frac{A_{v1}(1 + \zeta) \cdot [s^2(C_1C_2 - C_{gd}^2) + s(C_g g_m + C_2\beta_1)]}{s(C_{gd} + C_{gs} + C_{gb})},$$

$$\zeta = \frac{-(g_m + g_{ds} + g_{db} + s(C_{db} + C_L))}{g_m - sC_{gd}}.$$

The G_m depends on the number of input ports (noise sources) and it can be changed by varying the input sources (V_i). The overall output response is the product of $G_m \times Z_{out}$ and used to model the TF of PSIJ for the circuit.

The overall output response ($\tilde{v}_{o_{inv}}$) of CMOS inverter due to deterministic noise fluctuations is as follows:

$$\tilde{v}_{o_{inv}} = A_{v1}\left(v_{in} + \frac{Y_{32}}{Y_{31}}v_{ns} + \frac{Y_{34}}{Y_{31}}v_{bp} + \frac{Y_{35}}{Y_{31}}v_{gn} + \frac{Y_{36}}{Y_{31}}v_{bn}\right). \qquad (9)$$

The above parameters are used to develop a reduced two-port network for a CMOS inverter when the noise signals are applied at the gate, supply, bulk and the ground nodes, shown in [33].

B. A CHAIN OF N-STAGES INVERTERS
Generally, the chain of inverters is used as buffers, I/O drivers, delay lines, etc. Fig. 3 shows such N-stages of chain considering the supply/bulk/common-mode noise (denoted by
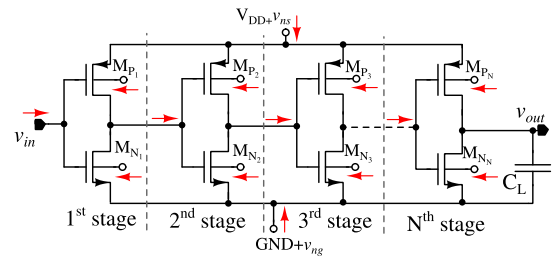

FIGURE 3. Schematic diagram of a chain of CMOS inverters.

red-colored arrows). The required IAM elements for the chain can be written similar fashion, as discussed in the previous example. Generally, the transistors in the chain of CMOS inverter are working in the different operating regions, depending upon the bias conditions. However, the same small-signal equivalent model (refer Fig. 2) is valid for other operating regions by just changing the parameters' value [27]. The impedance and phase expressions for the respective terminals are the same as derived for the inverter. The overall gain ($A'_{v_{ch}}$) with all the supply noise sources for an N-stages of inverter chain is:

$$A'_{v_{ch}} = \sum_{n=2}^{N}\left(\prod_{k=n}^{N}\left(\frac{Y_{o1}}{Y_{oo}}\right)_k \left(\frac{\sum_{i=1}^{p-1}(Y_{oi})}{(Y_{oo})}\right)_{n-1}\right)$$
$$+ \prod_{n=1}^{N}\left(\frac{Y_{o1}}{Y_{oo}}\right)_n + \left(\frac{\sum_{i=1}^{p-1}(Y_{oi})}{(Y_{oo})}\right)_N, \qquad (10)$$

where; N is total number of stages in an inverter chain and p refers to the input noise sources in a single stage. The derivation of the $A'_{v_{ch}}$ and the other details of two-parameters for the inverter chain are omitted due to space constraints.

The output of the N-stages CMOS inverters including the supply noise sources can be written as:

$$\Delta v_{out} = \prod_{n=1}^{N}A_n\sum_{i=1}^{p}\frac{Y_{oi}}{Y_{o1}}v_i + \sum_{j=2}^{N}\sum_{a=2}^{N}\left(\prod_{r=a}^{N}A_r\sum_{i=2}^{p}\frac{Y_{oi_j}}{Y_{o1_j}}\right)v_{i_j}. \qquad (11)$$

Fig. 4 shows the reduced two-port model for N-stage CMOS inverters having multiple supply noise sources. The input impedance at different terminals for one stage are denoted as Z_{in}, Z_{sn}, Z_{bn}, Z_{bp} and Z_{gn}. The closed-form expressions for these impedances for every stage are the same, however, the values of DC model parameters are changed. G_{m_n} and V_{i_n} are the transconductance gain and input voltage, respectively. The subscript n denotes the total number CMOS inverter stages and i refers to the applied input signal where the input signal can be individual or the combination of different input signals. Similar to the input source, the G_m can be changed depending upon the combination of noise source terminals. Using the reduced two-port model, one can estimate the output response in frequency, and time domain for the desired input node. The input node may be an individual node or combination of nodes. In addition to this, the transient and
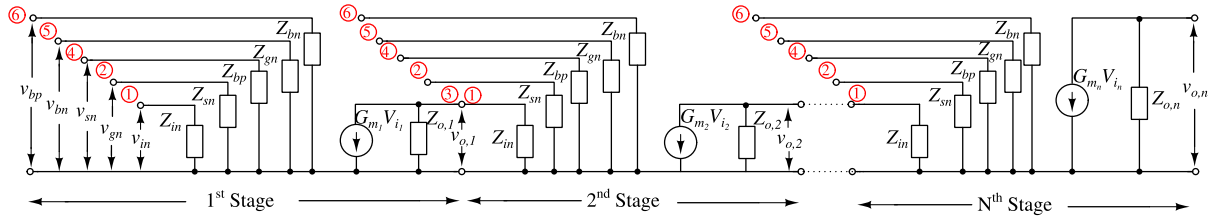
FIGURE 4. Reduced two-port model for multi-input, N-stage CMOS inverters.
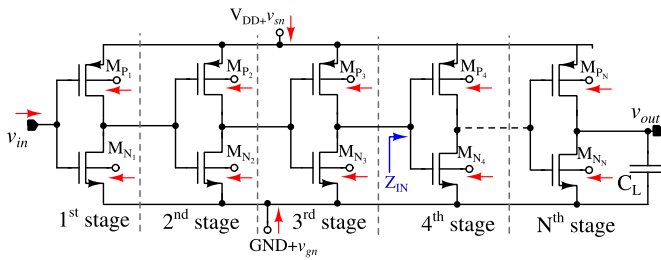

FIGURE 5. PSIJ Estimation at intermediate stage.

phase response at some intermediate stage can also be determined using the proposed two-port model. The procedure to analyse the intermediate TF and PSIJ is discussed in the next sub-section.

C. JITTER ESTIMATION AT INTERMEDIATE STAGE

Based on the proposed method, the PSIJ can also be evaluated, at an intermediate stage or at any point of load, in any circuit/system. Sometimes, jitter at the intermediate stage can be useful to have the insight of a system. The steps to evaluate the PSIJ at the intermediate stage of the cascaded long-chain circuit/system are as follows:

1) Break the cascade-connected stages in two parts from the point at which PSIJ needs to be calculated.
2) Calculate the input impedance (Z_{in}) of the remaining stages using (2), as shown in Fig. 5.
3) Replace the remaining circuit with impedance (Z_{in}) as a load of an intermediate stage.
4) Find the closed-form expression of output transient response including supply noise sources, using (10) and (11).
5) Finally, PSIJ can be calculated using (5).

For the understanding purpose, consider an example of N-stage CMOS inverters as shown in Fig. 5. The PSIJ expression due to all supply noise sources at any point of load can be calculated using the reduced two-port model for multi-input, N-stage inverters, depicted in Fig. 4. As an example, PSIJ at the third stage of the chain can be calculated by dividing the cascade structure into two circuits. The first circuit of the chain has three CMOS inverters and the second circuit contains remaining CMOS inverter stages. After that, the input impedance of the second which is a load of the first circuit has been calculated and replaced as a load (Fig. 5). The small-signal output voltage can be calculated using the N-stage output transient response (refer to (11)). As discussed earlier,

output response can be affected by IDN (①), PSN (②), noise at p-bulk (PBSN) (③), noise at n-bulk (NBSN) (④) and GSN (⑤) sources. Therefore, the small-signal output response (Δv_{out_i}) for three stages ($N = 3$) having five different noise sources ($K = 5$) can be written as (12):

$$\Delta v_{out_3} = A_1 A_2 A_3 \left(\frac{Y_{61}}{Y_{61}} v_1 + \frac{Y_{62}}{Y_{61}} v_2 + \frac{Y_{63}}{Y_{61}} v_3 + \frac{Y_{64}}{Y_{61}} v_4 + \frac{Y_{65}}{Y_{61}} v_5 \right)$$

$$+ A_2 A_3 \left(\left(\frac{Y_{62}}{Y_{62}} \right)_2 v_{2_2} + \left(\frac{Y_{63}}{Y_{61}} \right)_2 v_{3_2} + \left(\frac{Y_{64}}{Y_{61}} \right)_2 \right)$$

$$v_{4_2} + \left(\frac{Y_{65}}{Y_{61}} \right)_2 v_{5_2} \right) + A_3 \left(\left(\frac{Y_{62}}{Y_{62}} \right)_3 v_{2_3} + \left(\frac{Y_{63}}{Y_{61}} \right)_3 \right)$$

$$v_{3_3} + \left(\frac{Y_{64}}{Y_{61}} \right)_3 v_{4_3} + \left(\frac{Y_{65}}{Y_{61}} \right)_3 v_{5_3} \right). \quad (12)$$

In (12), A_1, A_2 and A_3 are the overall gain of first, second and third stages, respectively. v_1, v_2, v_3, v_4, v_5 are the IDN, PSN, PBSN, NBSN and the GSN voltage sources, respectively. The Y_{ii} and Y_{ij} parameters are the same as defined in Table 1. The load capacitance (C_L) in this case is replaced by Z_{in_4}. The different subscript mentioned on each admittance ratios denotes the respective stage number. For example, $(\frac{Y_{65}}{Y_{61}})_2 v_2$ represents the multiplication of admittance ratio with PSN source for stage 2.

Finally, the instantaneous jitter (J_{r_3}) at the end of the third stage in an N-stage inverter chain can be calculated as:

$$J_{r_3} = \frac{\Delta v_{out_3}}{\gamma_3}, \quad (13)$$

where Δv_{out_3} is the small-signal transient response due to supply fluctuations at the third stage of the chain and γ_3 refers to the slope at the output (third-stage) transition edge at nominal supply voltage.

IV. SIMULATION RESULTS AND DISCUSSIONS

In this section, the derived transfer functions (TFs) using the proposed approach have been compared with the results obtained in SPICE-based electronic design automation (EDA) tool. The CMOS inverter circuit has been designed in TSMC 28 nm CMOS technology to validate the derived PSIJ TFs for a single-stage, some intermediate stage, and at the output of five-stage CMOS inverters. For demonstration purposes, different power supply noises such as input data noise, PSN, and BSN are modelled as a sinusoidal signal with amplitude varying from 0 to $\pm 10\%$ V_{DD}. Note that, the DC supply
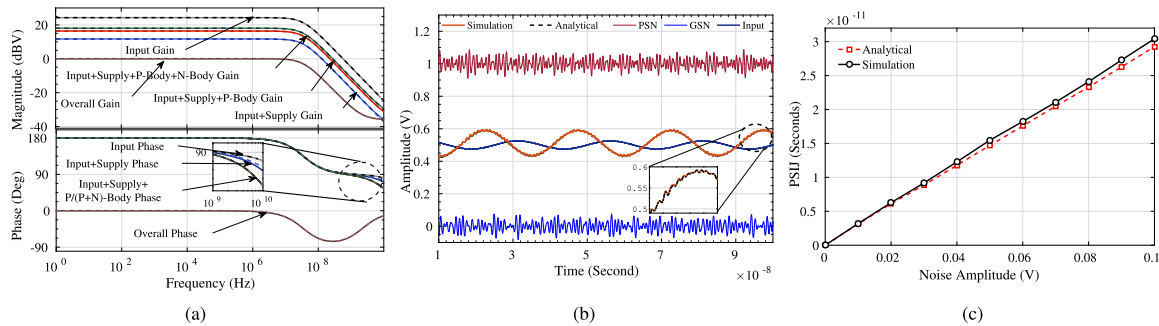
FIGURE 6. Single stage CMOS inverter: (a) magnitude and phase response from the different input terminals, (b) transient response in presence of practical noise sources, and (c) the peak to peak PSIJ with respect to the supply noise including PSN, GSN, IDN and BSN.

voltage (V_{DD}) is 1 V and the input data rate is 1000 Mbps for all the demonstrated examples. The slope is calculated using one-bit simulation in ideal voltage conditions and the DC model parameters have been calculated using the EDA tool based simulations and BSIM model [34]. Usually, PSIJ is measured at the mid-point of the output transition edge of a signal. Therefore, the small-signal model parameters (refer Table 1) are taken into account for the time instant when the output transition edge (rising/falling) reaches the $V_{OH}/2$, where V_{OH} is the maximum output voltage level.

A. EXAMPLE-I: A SINGLE STAGE CMOS INVERTER
Fig. 6(a) compares the analytical and simulation results of magnitude and phase response for a single-stage CMOS inverter. In this plot, different curves show the impact noise sources, which are present at different terminals, on the frequency and phase responses. The analytical results are shown by the dashed line whereas, the solid lines are for the simulation results. The analytical plot matches accurately with the simulation results with a maximum mean percentage error (MPE) of 2%.

Different sinusoidal signals having small amplitudes with different frequencies and phases are combined to mimic the practical effect of the supply noise signals. For PSN, six different sinusoidal signals with amplitude and frequency of {31.5 mV, 1.72 GHz}, {27.5 mV, 1.11 GHz}, {19 mV, 992 MHz}, {17 mV, 893 MHz}, {24 mV, 1.5 GHz} and {12 mV, 1 GHz} are used. In the case of GSN, the amplitude and frequency of six sinusoidal signals are {9 mV, 1.05 GHz}, {19 mV, 693 MHz}, {14 mV, 853 MHz}, {21 mV, 979 MHz}, {25.5 mV, 1.17 GHz} and {29.5 mV, 1.49 GHz}.

The time-domain simulations at DC bias conditions for a single-stage inverter due to these different supply noise sources are shown in Fig. 6(b). Note that the time-interval error (TIE) is measured at the mid-point of the output transition edge. Therefore, the noise-to-output transfer function is also calculated when the transition (rising/falling) edge of the output signal is at the mid-point of V_{OH}. Here, V_{OH} is the rail-to-rail swing of the output signal. For this reason, the inverter in this work is designed in such a way that the output should be at $V_{DD}/2$ when the input bias voltage is also at $V_{DD}/2$.

The plot (in Fig. 6(b)) shows the amplified version of small-signal deterministic noise sources at the output of a single CMOS inverter. The analytical and simulated results are 98% matches with each other which are further useful in the PSIJ estimation. The output transient response can be obtained by multiplying the inverse Laplace of gain with the input signal.

Fig. 6(c) shows the peak-to-peak value of PSIJ (using expressions (3), (5) and (9)) with different noise signal amplitudes. The input data switches between 1 V and 0 V with a bit period of 1 ns. The different supply noise signals are modelled as single-tone sinusoidal signals which are superimposed on the DC supply voltage. The frequency of the v_{sn}, v_{bp}, v_{bn} and v_{dn} are 873 MHz, 413 MHz, 373 MHz and 887 MHz, respectively. The peak-to-peak amplitude of these noise sources are varied from 0 V to 10% V_{DD} and the analytical and simulations values of PSIJ are observed and compared in the Fig. 6(c). The MPE for the PSIJ is 1.4%.

B. EXAMPLE-II: A CHAIN OF CMOS INVERTERS – FIVE STAGES
The circuit has five stages of CMOS inverter with a stage ratio of 2. The input-to-output gain and phase curve in the frequency domain which is obtained using the (10) has been compared with simulation results in Fig. 7(a). Fig. 7(b) shows the magnitude and phase response at the output of the circuit when the AC sources are present at the input, supply and bulk (p-bulk and n-bulk) nodes. As inferred from the plot, the overall gain of the circuit is attenuated due to the presence of supply noise sources. Hence, the performance of any circuit may be degraded due to supply fluctuations. Similar to the single-stage inverter, the impedance seen at the different terminals for the chain can be determined and the plots are skipped in this paper due to the repetition of results. Fig. 7(c) shows the values of PSIJ at the different amplitude levels of supply noise. These PSIJ values are obtained with the help of the proposed TF model (refer (10) and (11)) and one-bit simulation method. The same specifications of noise sources, used in Example I, are considered for this example. The PSIJ due to individual and combination of supply noise sources are analytically calculated and plotted in the same figure. The maximum MPE between the analytical and simulation results is 1.8%.
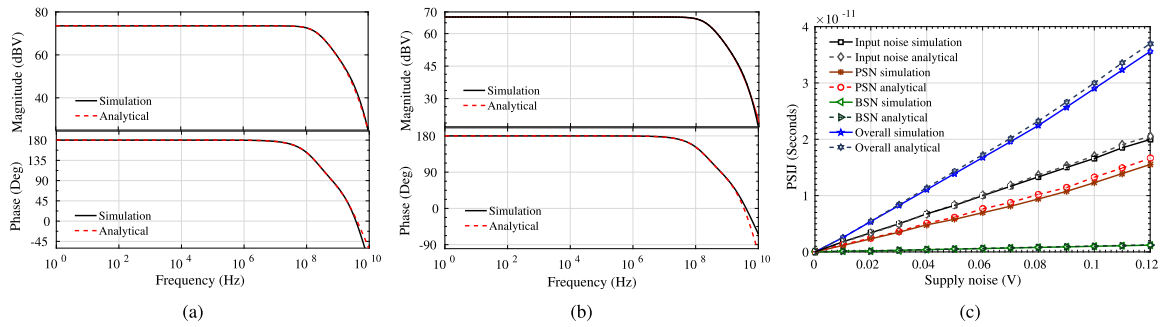
FIGURE 7. Five Stage CMOS inverters: (a) input-to-output frequency, phase response (b) overall frequency and phase response due to IDN, PSN and BSN and (c) the PSIJ with supply noise voltage ranging from 0 to V_{DD}/10.
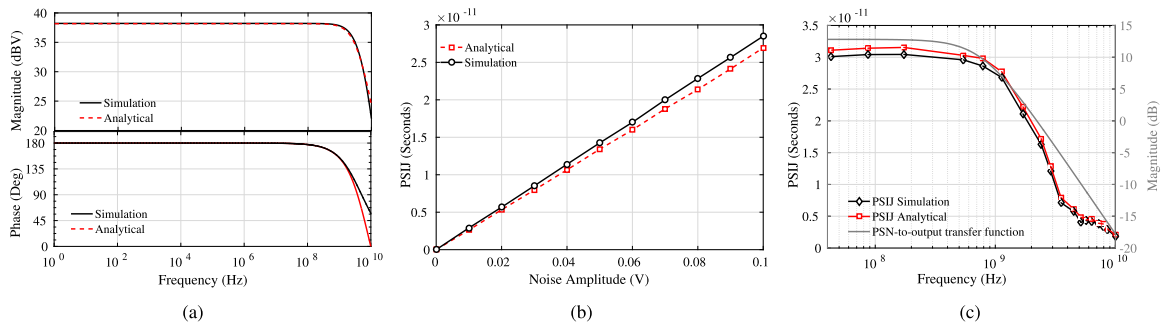

FIGURE 8. (a) Magnitude and phase response at the third stage, when the same in-phase AC sources are applied at the input, power supply and the bulk nodes for the third stage in a five stage inverter chain, (b) PSIJ due to IDN, PSN and BSN at the third stage in a five stage inverter chain, and (c) Magnitude response and the PSIJ with respect to the PSN frequencies.

C. EXAMPLE-III: INTERMEDIATE STAGE CMOS INVERTER CHAIN

The proposed PSIJ methodology at some intermediate stage, discussed in Section III-C, is validated for five-stage CMOS inverters. The third stage is considered as an intermediate stage for the purpose of analysis. Fig. 8(a) shows the frequency and phase responses at the output of the third stage when the same in-phase AC sources are applied at the input, power supply and the bulk nodes. The MPE between analytical and simulation results for voltage gain is 2%. Further, the PSIJ at the same stage is determined due to PSN, BSN, and the IDN and plotted in Fig. 8(b). The specifications of noise sources for this case are same as Example I. The MPE is 2.4% for this case.

Based on the PSIJ analyses in the presence of different supply noise, one important remark has been observed. The unity-gain bandwidth (UGBW), the bandwidth of a circuit at unity gain, is one of the important parameters for circuits. It is used to determine the maximum possible frequency at which the signals can be amplified. Moreover, the value of PSIJ is depended upon the frequency response of a circuit. The PSIJ values have been calculated for different frequencies from a few MHz to GHz. It is observed that the PSIJ curve for different frequencies follows the same pattern as the frequency response. Fig. 8(c) shows the power supply noise-to-output TF in the grey colour plot. The analytical

and simulation results for the PSIJ have been plotted in red and black colour, respectively. Such type of PSIJ pattern is due to the amount of amplified noise present at the output which eventually changes the slope of the transition edge. Note that, the value of PSIJ is nearly zero when the PSN and input data have same harmonics. For simplicity, the PSIJ values at these specific noise frequencies are not shown in this plot.

D. KEY OBSERVATIONS: BASED ON CIRCUIT/DEVICE PARAMETERS

Based on the PSIJ analyses in the presence of different supply noise, a few important remark has been observed which are discussed in this section. The UGBW, the bandwidth of a circuit at unity gain, is one of the important parameters for circuits. It is used to determine the maximum possible frequency at which the signals can be amplified. Moreover, the value of PSIJ is depended upon the frequency response of a circuit. The PSIJ values have been calculated for different frequencies from a few MHz to GHz. It is observed that the PSIJ curve for different frequencies follows the same pattern as the frequency response. Fig. 8(c) shows the power supply noise-to-output TF in the grey colour plot. The analytical and simulation results for the PSIJ have been plotted in red and black colour, respectively. Such type of PSIJ pattern is due to the amount of amplified noise present at the output which
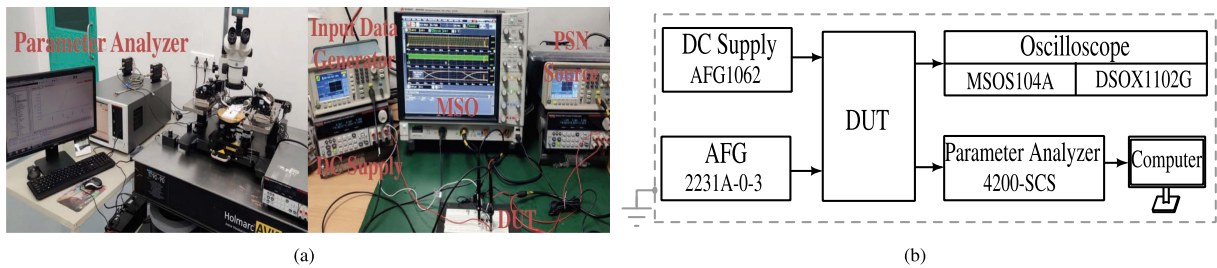
FIGURE 9. Experimental setup: (a) photograph, and (b) block diagram.

eventually changes the slope of the transition edge. Note that, the value of PSIJ is nearly zero when the PSN and input data have same harmonics. For simplicity, the PSIJ values at these specific noise frequencies are not shown in this plot.

As shown in Fig. 6(a), the input-to-output gain of the amplifier depends on the transconductance (g_{m_1} and g_{m_2}) and drain-to-source transconductance (g_{ds_1} and g_{ds_2}) of M_1 and M_2 transistors, respectively. Note that, the inverter behaves as a CG amplifier in case of power supply-to-output node gain calculation. The DC voltage gain for this case is a function of g_{m_1}, g_{ds_1}, and g_{ds_2}. The combined voltage gain of these two signals (input and supply noise) gives reduced gain. This is due to the effect of g_{m_1} and g_{ds_1} of M_1 transistor is nullified and the remaining voltage gain depends on the M_2 (pull-down transistor) parameters. However, the intrinsic parasitic capacitance still shows a significant impact on the location of poles and zeros, hence, the PSIJ value changes with noise frequencies as well. Furthermore, the gain of bulk (both P- and N-type) depends on the bulk-transconductance (g_{mb_1} and g_{mb_2}), and they are 180° out of phase from their respective input signals. Therefore, the effect of fluctuations at these nodes may cancel out each other's effect, depending upon the frequency of noise signals.

Two important observations have been discussed in the above paragraphs. The first one is the behaviour of PSIJ, which relies upon the TF (refer to (6)–(10)). Secondly, the dependence of the TF on the small-signal device parameter (such as transconductance, on-resistance, impedance, parasitic capacitance, load capacitance, etc.) of a circuit. These device parameters are also scaled with the advancement of the feature size [35]. As the technology scales down, the doping concentration increases, due to which the depletion region is wider, resulting in higher drain-source capacitance. Also, the gate oxide thickness (t_{ox}) reduces with the feature size; consequently, the oxide capacitance (C_{ox}) increases. The parameters, viz. parasitic capacitance, contact resistivity and transconductance, increase with the scaling. At the same time, the on-resistance of a device decreases with technology scaling. By virtue of this, the uncertainty in time increases; hence, the adverse impact of PSIJ will increase and puts a greater constraint on the performance of high-speed circuits. Fig. 8(c) also shows that the value of PSIJ mainly depends on the transconductance and on-resistance till the 3-dB bandwidth. After that (at higher frequencies), the parasitic-device parameters dominate the overall dependency.

V. EXPERIMENTAL RESULTS

The proposed closed-form expressions are compared with experimentally measured results. A block diagram and photo of the complete measurement setup is depicted in Fig. 9. The setup requires a parameter analyzer for the estimation of a device under test (DUT) parameters, an oscilloscope for the analysis of gain, phase and the PSIJ, a computer for the mathematical analysis, a power supply for V_{DD}, and an arbitrary function generator (AFG). Two AFG are used in the experimental setup; one for the input waveform and other one for the sinusoidal supply noise generation. For the proof-of-concept, a prototype design of a four-stage CMOS inverter chain is implemented using the discrete MOS within CD4007 chip, with a V_{DD} of 5 V. Four different CD4007 ICs (one pair of nMOS and pMOS from each IC) have been used in this experiment to measure the PSIJ and the interconnect lengths between each of the stages are kept same. In this prototype, the pMOS and nMOS of the first stage are in the saturation region. In the next stages, the operating conditions of transistors are not the same because of the different rise/fall times and delays of the circuit. Therefore, the IAM parameters of the equivalent model change accordingly. For that, a parameter analyzer determines the IAM parameters for the experimental setup. The different parameters such as g_m, g_{ds}, parasitic capacitances, are calculated by incorporating the voltages and currents at each of the nodes with frequency sweeping. In this work, the IAM parameters of the packaged CD4007 IC are extracted; therefore, the effect of capacitance and resistance of packages, bond wire and parasitic diodes are incorporated in the obtained parameters. However, the inductive and other effects have not been included in the analysis. Moreover, the parasitics due to board and interconnects are not considered in this work. Therefore, the error percentage is higher in the case of experimental results (Fig. 10) as compared to the simulation results (Fig. 7). The input data rate and the frequency of the PSN for the experiment are 2 Mbps and 5.213 MHz, respectively. Fig. 10(a)-(b) show the frequency and phase response comparison between analytical and measurement results for a single-stage inverter. The first plot is for the input-to-output response, and the other plot is for the supply-node-to-output response. The in-built function of the oscilloscope is used to calculate the frequency and phase response (measurement results) of the IC, whereas the analytical results are plotted using the transfer functions and by the extracted IAM parameters (using a parameter analyzer). Next,
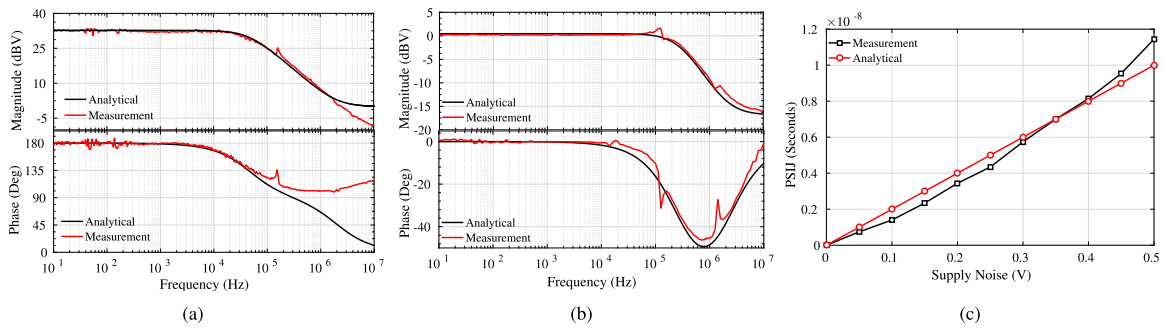
FIGURE 10. Measurement Results: (a) Magnitude and phase response from input-to-output of a single stage inverter, (b) Magnitude and phase response from supply-to-output of a single stage inverter, and (c) PSIJ plot for a four-stage inverter.

TABLE 2. Comparison of the Proposed Method With Some of the Existing Methods

Method	Error (%)	Anal. time (Sec.)	Sim. time (Sec.)	Bits	Tool	Arch.	Noise type (sinusoidal noise)	Supply noise	Data rate (Mbps)	Speed-up Factor	PSIJ estimation node
Piece-wise nonlinear method [21]	9	1.98	618.57	1000	Keysight ADS	VM driver	single-tone	PSN, IDN	120	312	output
EMPSIJ method [21]	7.2	1.78	718.23	1000	Keysight ADS	VM driver	multi-tone	PSN	120	400	output
Admittance-based method [28]	7.4	5	863	1000	Spectre	Comparator	single-tone	PSN, BSN	1	116	output
EMPSIJ+Thomas algo. [27]	2.8	4.18	672	1000	Spectre	Inverters	multi-tone	PSN, GSN	1000	160	output
IBIS based method [36]	6.61	–	–	1000	Spectre	Inverters	multi-tone	PSN, GSN	1000	–	output
Statistical method [37]	4.7	13.7	1260	32767	HSPICE	Buffers	SSO	PSN	4000	91.9	output
Enhance statistical link analysis [38]	8.64	906	–	long PRBS	HSPICE	Buffers	multi-tone	PSN, GSN	2400	–	output
Device Parameter-Based Modeling [39]	3.38	735	186	100	Spectre	Inverters	multi-tone	GSN	120	4	output
This work	**2.4**	1.21	693	1000	Spectre	Inverters	multi-tone	PSN, GSN, BSN, IDN	1000	**572**	output, intermediate

the analytical and measurement PSIJ results for the four-stage inverter chain are shown in Fig. 10(c). The maximum MPE for the input-to-output response, supply-to-output response, and the PSIJ are 12%, 11% and 13%, respectively.

VI. COMPARISON WITH THE EXISTING PSIJ METHODS

Table 2 shows the comparison of the proposed method with some of the existing PSIJ methods. For a valid comparison, all the comparing architectures in the Table 2 have been choosen as inverter based circuits with the TF based listed methods. The comparison has been performed in terms of percentage error, computational time, speed-up factor, supply noise sources, and the PSIJ estimation node. The speed-up factor is the ratio of the EDA simulation time to the time spent in the analytical calculations. Moreover, the other important specifications such as the number of bits, type of noise sources, circuit configuration, etc. are also mentioned in the same table. For the simulation purpose, type of the EDA simulators are also shown. The analytical closed-form expressions are solved using the MATLAB tool. These results are compared with the EDA results, and the difference between these two determines the error. The assumptions for the noise

sources and the affected terminals are also mentioned in the table.

It is worth to mention that, the proposed method is better among the other listed methods in terms of percentage error and speed-up factor. Furthermore, in practice, all of the terminals in a circuit have small-signal AC fluctuations. Therefore, all the possible deterministic noise sources are considered in this work. Such case has not considered for the other reported methods. In addition to this, the PSIJ can be calculated at any intermediate node of the circuits using the proposed method, whereas, in the other methods, the PSIJ had been calculated at the output stage only. Next, the accuracy of the method depends upon the extracted device parameters, which are always available at the time of circuit design. Therefore, the efficiency and accuracy of the proposed method are also correct for the lower technology nodes as well. In the other techniques, the computational time and error percentage are always higher than the proposed method in the scaled supply and feature size.

Note that the accuracy of the proposed method is limited to super-high frequencies (SHF), which is true for the other methods (refer Table 2). The analytical results show a larger MPE when the noise frequency reaches 20 GHz and above.

However, this problem can be resolved by keeping frequency dependence parameters in the analytical expressions. Next, the analysis is valid only for small-amplitude noise signals such that it can not change the operating conditions of a circuit. The limitations mentioned above are valid for the other PSIJ analysis methods.

VII. CONCLUSION

The IAM based estimation-by-inspection method has been used to model the PSIJ in the presence of noisy supplies for the N-stage CMOS inverter chain. Three different example circuits are validated using the proposed method. The derived two-port entities using the proposed method are used to form a reduced two-port network for multi-terminal, N-stage CMOS inverters. Based on the reduced two-port model, the PSIJ can also be calculated at an intermediate stage of the inverter chain. The proposed analysis is algebraically simple, easy to handle, and computationally efficient for the jitter analysis. The same analysis can be extended for the on-chip clock distribution networks, delay lines, phase-locked loop, etc. The analysis has been compared with EDA simulation and CD4007 chip-based prototype design results; it shows a good agreement in both cases.

APPENDIX A UNKNOWN PARAMETERS USED IN THE EXPRESSIONS

The expressions for the unknown parameters mentioned in Section III are as follows. $C_1 = C_{gd} + C_{db} + C_L$, $\beta_1 = g_{ds} + g_{db}$, $g_{ds} = g_{ds_1} + g_{ds_2}$, $g_{db} = g_{db_1} + g_{db_2}$, $C_{gd} = C_{gd_1} + C_{gd_2}$, $C_{db} = C_{db_1} + C_{db_2}$, $C_{gb} = C_{gb_1} + C_{gb_2}$, $C_{gs} = C_{gs_1} + C_{gs_2}$, $C_2 = C_{gd} + C_{gs} + C_{gb}$, $g_m = g_{m_1} + g_{m_2}$, $\beta_2 = g_{ds_1} + g_{bs_1} + g_{m_1} + g_{mb_1}$, $\beta_3 = g_{ds_2} + g_{m2} + g_{mb_2}$, $\alpha_1 = C_1(C_{gs_1} + C_{bs_1})$, $\alpha_2 = C_1\beta_2 + \gamma_1(C_{gs_1} + C_{bs_1})$, $\alpha_3 = \gamma_1\beta_2 - g_{ds_1}(g_{m_1} + g_{mb_1} + g_{ds_1})$, $\alpha_4 = C_1(C_{bd_1} + C_{bs_1}) - C_{bd_1}^2$, $\alpha_5 = C_1(g_{bs_1} + g_{db_1}) + \gamma_1(C_{bd_1} + C_{bs_1}) - C_{bd_1}(2g_{db_1} - g_{mb_1})$, $\alpha_6 = \gamma_1(g_{bs_1} + g_{db_1}) - (g_{db_1} - g_{mb_1})g_{db_1}$, $\alpha_7 = C_1(C_{bs_2} + C_{gs_2} + C_L)C_L^2$, $\alpha_8 = (\beta_3 + g_{bs_2})C_1 + \gamma_1(C_{bs_2} + C_{gs_2} + C_L) - C_L(\beta_3 + g_{ds_2})$, $\alpha_9 = \gamma_1(\beta_3 + g_{bs_2}) - g_{ds_2}\beta_3$, $\alpha_{10} = C_1(C_{bd_2} + C_{bs_2}) - C_{bd_2}^2$, $\alpha_{11} = C_1(g_{bs_2} + g_{db_2}) + \gamma_1(C_{bd_2} + C_{bs_2}) - C_{bd_2}(2g_{db_2} - g_{mb_2})$, $\alpha_{12} = \gamma_1(g_{bs_2} + g_{db_2}) - (g_{db_2} - g_{mb_2})g_{db_2}$.

The above parameters are mainly the device model parameters. These parameters are the combination of parasitics such as; transconductance, resistance and capacitances of the MOSFET. These model parameters can be obtained by the EDA simulations and saved in a result browser. In the proposed method, these parameters are by extracted from the EDA tools for the proposed circuits. For the measurement results, these parameters are estimated for CD4007 (discrete IC with 3 nMOS and 3 pMOS transistors) using the instrument viz. parameter analyzer.

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