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Hybrid Spintronics/CMOS Logic Circuits Using All-Optical-Enabled Magnetic Tunnel Junction

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ABSTRACT Spintronics is one of the emerging fields for next-generation low power, high endurance, non-volatile, and area efficient memory technology. Spin torque transfer (STT), spin orbit torque (SOT), and electric field assisted switching mechanisms have been used to switch magnetization in various spintronic devices. However, their operation speed is fundamentally limited by the spin precession time that typically ranges in 10–400 ps. Such a time constraint severely limits the possible operation of these devices in high-speed systems. Optical switching using ultrashort laser pulses, on the other hand, is able to achieve sub-picosecond switching operation in magnetic tunnel junctions (MTJs). In this paper, all optically switched (AOS) MTJ has been used to design high speed and low power hybrid MTJ/CMOS based logic circuits such as AND/NAND, XOR/XNOR, and full adder. Owing to the ultra-fast switching operation of AOS-MTJ, the circuit level results show that the energy and speed of AOS-MTJ based logic circuits are improved by 85% and 97%, respectively, when compared to STT based circuits. In comparison to SOT based designs, the proposed logic circuits show 10% and 91% improvement in energy efficiency and speed, respectively.

INDEX TERMS All-optical-switching, magnetic tunnel junction, MTJ/CMOS logic circuits, spintronics.

I. INTRODUCTION

The emerging field of artificial intelligence (AI), big data, and the internet of things (IoT) has led to a tremendous increase in the rate of information generation and storage. It is expected that billions of connected IoT devices across the globe will create around 175 zettabytes of data by 2025 [1]. To make such a huge amount of data readily available to the consumers, ultrafast memories are required to process the thread-write cycle in a picosecond time frame. Spintronics has emerged as one of the leading technologies that has the potential to offer a solution for these memory requirements [2]. It demonstrates great potential in the post-Moore era. Owing to its large density, reliability, and low power dissipation, spintronic memory has attracted a great attention in applications such as memory [3], [4], logic [5], in-memory computing [6], [7], data encryption [8], approximate computing [9], [10], and neuromorphic computing [11], [12]. Spin transfer torque magnetic random-access memory (STT-MRAM) and spin orbit torque MRAM (SOT-MRAM) are seen as a promising replacement for the CMOS based on-chip memories [13]. Although STT and SOT MRAMs are considered to be the future memory technologies, there are still several challenges that need to be addressed. These include a low magnetoresistance ratio, high switching currents, and low thermal stability [13]. Moreover, the switching operation of STT and SOT MRAMs are limited by high precessional latencies of 200ps [14] and 400ps, respectively [15], [16]. Over the last few decades, prominent techniques have been investigated and reported in STT and SOT MRAM to eliminate these hurdles. A rectified tunnel magnetoresistance device comprised of PMA-MTJ and Schottky diode has been reported to achieve a high on-off ratio [17]. Wang *et al.* [18] reported that the thermal stability of MTJ can be improved by using the combination of double-barrier and synthetic double-free layers. Kang *et al.* [19] and Barangi *et al.* [20] proposed voltage controlled magnetic anisotropy (VCMA) and strain mediated magnetic anisotropy,

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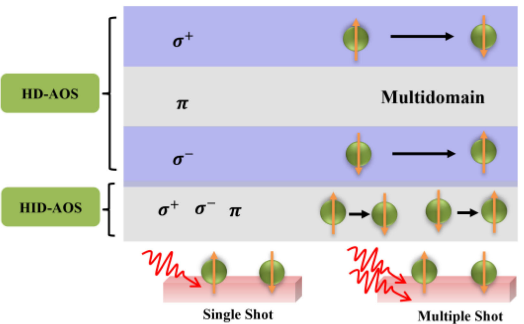


FIGURE 1. Schematic showing different categories of AOS in magnetic layers.

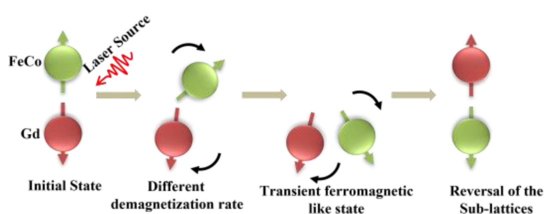


FIGURE 2. Switching mechanism of laser-induced magnetization reversal.

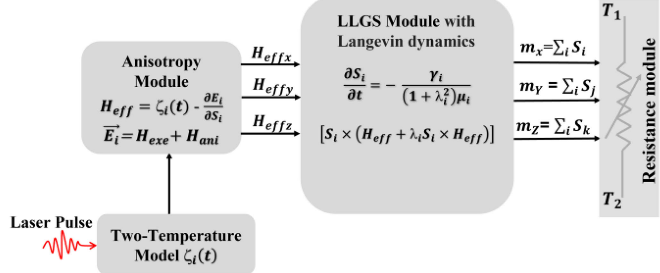


FIGURE 3. Device-Circuit simulation framework.

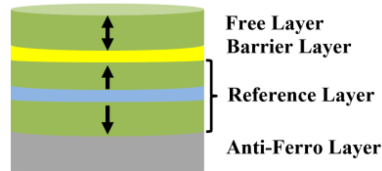


FIGURE 4. MTJ basic structure.

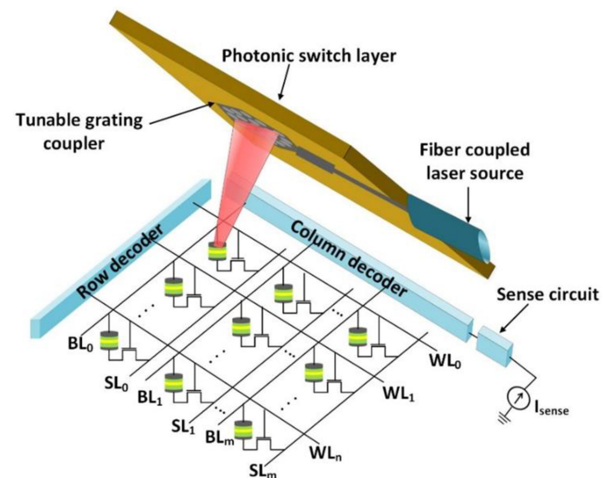


FIGURE 5. Schematic of writing circuit for AOS-MTJ.

respectively to achieve MTJ switching within 1ns duration using a few fJ of energy. Gao *et al.,* further reduced the power consumption of MTJ by employing negative capacitance (NC) effect [21]. NC enhanced MTJ can operate at a working voltage as low as 1 mV and has been used to implement energy efficient memory and logic circuits [22], [23]. Recently, all-optical switching technique has been reported as a potential candidate to achieve ultrafast (in order of a few ps) and low power switching of magnetic devices [24]. It can increase the write speed up to terahertz while eliminating the joule heating and stray field effects. In this paper, AOS-MTJ device has been modelled in Verilog-A and used to implement in-memory computing based hybrid MTJ/CMOS logic circuits such as AND/NAND, XOR/XNOR, and full adder logic. Furthermore, the performance parameters such as energy and delay of these circuits have been evaluated and are compared with the conventional STT and SOT-based designs.

The rest of the paper is organized as follows: Section II discusses the basic principles of AOS of magnetic devices. The read and write operation of the AOS-MTJ is presented in section III. Section IV presents the implementation of hybrid AOS-MTJ/CMOS based logic circuits. The performance evaluation and comparison of the proposed circuits are discussed in section V. The conclusion of this paper is presented in section VI.

II. BACKGROUND

This section presents the basic structure of AOS-MTJ and the physics behind the optical switching of magnetic layers.

A. ALL-OPTICAL SWITCHING OF MAGNETIC LAYERS

An ultrafast demagnetization of Ni crystal in 60 fs using an ultrashort laser pulse has been demonstrated by Beaurepaire *et al.* [25]. This remarkable finding has attracted the attention of various research groups into this emerging field. Stanciu *et al.* [26] demonstrated an ultrafast AOS in magnetic thin films GdFeCo by exploiting the strong Faraday rotation value. It was observed that a single 800 nm laser pulse (40 fs) creates a permanent spin reversal. AOS of the free layer magnetization uses ultrashort laser pulse without any external stimuli. In general, AOS can be classified into two categories based on how helicity impacts the switching process and how many laser pulses are required to flip spins as shown in Fig. 1. In helicity-dependent AOS (HD-AOS) spins are switched by

(a) (b)

FIGURE 6. **(a) Block diagram of writing circuit showing CMOS interfacing, laser diode driver, and laser source (b) CMOS interface circuit to control the laser source.**

employing right-circularly polarized (CP) light (σ^+) or left-CP light (σ^-). The linearly polarized (LP) light (π) is solely responsible for generating multi-domains. On contrary, in helicity-independent AOS (HID-AOS), magnetization switching is achieved by all the three kinds of polarized light i.e., σ^+, σ^-, and π. The second switching category corresponds to the number of laser beams required to flip the magnetization. The magnetization reversal can be achieved either by using single shot or multiple shot laser pulses. Experimental and theoretical studies reveal that the Inverse Faraday effect, transfer of angular momentum, thermal heating, magnetic circular dichroism, creation of transient ferromagnetic state, and laser-induced super-diffusive spin currents are among the underlying principles that are responsible for AOS of magnetic materials. Materials such as ferrimagnets, rare earth/transition metals multilayers, artificial zero moment magnets, and ferromagnets have been extensively explored in AOS experiments [27].

The physics behind the thermal effect of AOS in magnetic layers is governed by the two temperature (2T) model [28]. It relates the transfer of energy between the electron and lattice on the impingement of an ultrashort laser pulse. The mathematical 2T model can be represented by the following coupled differential equations:

$$C_e \frac{dT_e}{dt} = -G_{el}\ (T_e - T_l) + P(t) \tag{1}$$

$$C_l \frac{dT_l}{dt} = -G_{el}\ (T_l - T_e) + C_l \frac{T_l - T_0}{\tau} \tag{2}$$

$$P(t) = \frac{|E(t)|}{\pi r^2 d} \alpha_{opt} \tag{3}$$

where, G_{el} is the coupling constant between electrons and lattice, C_e and C_l represent heat capacity of electron and lattice, and T_e and T_l represent the temperature of the electron and lattice reservoir, respectively. α_{opt} is the optical absorption ratio and τ represents the lattice cooling time constant. Laser-induced heating term is denoted by *P(t)*. *E(t)* is the electric field corresponding to the applied laser beam. *d* and *r* represent the thickness and radius of AOS-MTJ, respectively.

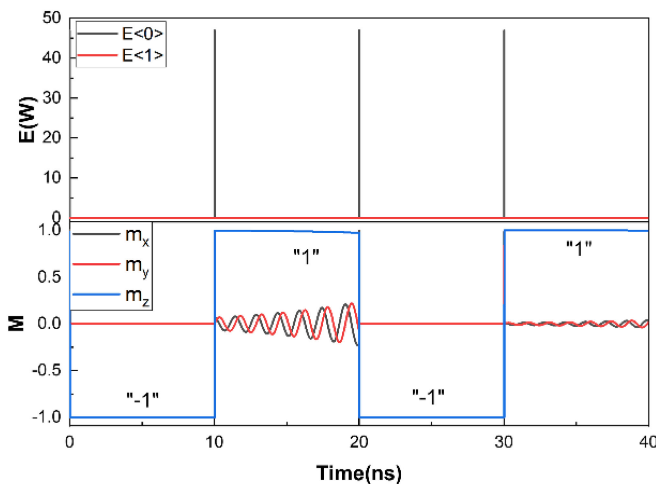


FIGURE 7. **Ultrafast AOS of magnetization using 100 MHz pulse train.**

When a laser pulse strikes on the GdFeCo layer, the thermal energy of electrons increases that results in ultrafast energy transfer into the spin system.

At temperatures greater than Curie point, Gd and Fe sub-lattices are demagnetized at different rates due to their non-equivalence of magnetic moments and exchange relaxation. Therefore, the magnetization of Fe sub-lattice flips at a faster rate as compared to the Gd sub-lattice showing the ferromagnetic behavior as illustrated in Fig. 2 [29]. The exchange-driven relaxation of the system from non-equilibrium state to a partial equilibrium owing to the reversal of the total magnetization. The energy E_i of any spin in the system, is described by the following Hamiltonian:

$$E_i = -\sum_{j=1}^{N} J_{ij} S_i \cdot S_j - d S_{z,i}^2 \tag{4}$$

J_{ij} is the exchange integral between spins i and j (where i and j are lattice sites), S_i and S_j are the normalized spin vectors, d is the uniaxial anisotropy constant, and N is the number of nearest neighbours. The effect of temperature on

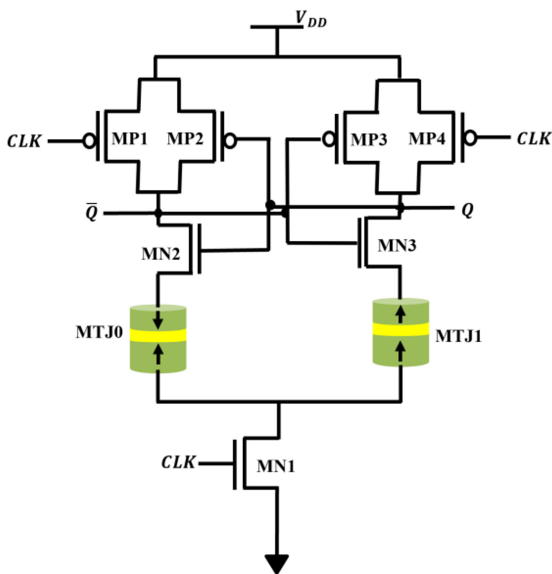


FIGURE 8. Hybrid AOS-MTJ/CMOS pre-charge sense amplifier.

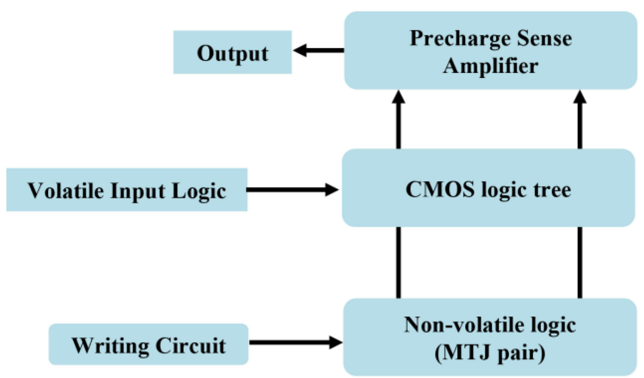


FIGURE 9. Block diagram of hybrid MTJ/CMOS logic.

the magnetization dynamics is modeled by using the Langevin equation, given by [29]:

$$\frac{\partial S_i}{\partial t} = -\frac{\gamma_i}{\left(1+\lambda_i^2\right)\mu_i}\left[S_i \times \left(H_i + \lambda_i S_i \times H_i\right)\right] \quad (5)$$

where, λ_i represents thermal coupling parameter, γ_i is the gyromagnetic ratio, and μ_i is the magnetic moment of the lattice site i . The effective magnetic field H_i is defined as:

$$H_i = \zeta_i(t) - \frac{\partial E_i}{\partial S_i} \quad (6)$$

where, $\zeta_i(t)$ is the stochastic term used to couple the external temperature effect to the spin system. The stochastic process moments are defined by fluctuation-dissipation theory as:

$$\langle \zeta_i^a(t)\,\zeta_i^b(t)\rangle = 2\delta_{ij}\delta_{ab}\left(t-t'\right)\frac{\mu_i\,\lambda_i k_B T}{\gamma_i} \quad (7)$$

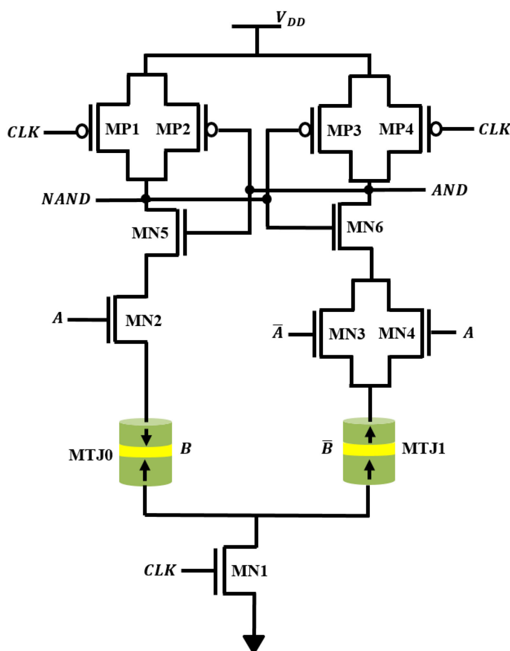


FIGURE 10. Hybrid AOS-MTJ/CMOS based AND/NAND circuit.

where a and b are cartesian components, T is the temperature of the thermal bath to which the spins are coupled. The overall simulation framework showing the incorporation of two temperature model and magnetization switching for circuit applications is shown in Fig. 3.

B. MAGNETIC TUNNEL JUNCTION

MTJ is the most widely used spin-based device that employs the quantum mechanical property for information storage. It is comprised of a thin insulating barrier sandwiched between two ferromagnetic (FM) layers, as shown in Fig. 4. One of the FM layers has fixed magnetization and is named as reference layer (RL), while the second FM layer, called as free layer (FL), has variable magnetization. The FL in AOS MTJ is composed of ferrimagnetic materials such as GdFeCo and Tb/Co multilayers [30]. The magnetization of the RL is pinned with the help of an antiferromagnetic layer such as IrMn or PtMn. The RL is composed of two sub-layers separated by a thin Ruthenium (Ru) spacer to form a synthetic anti-ferromagnetic (SAF) layer to eliminate the magnetostatic field in the FL. The relative orientation of the magnetic moment between RL and FL can be employed to store the digital data in terms of MTJ resistance. The parallel magnetization orientation of FL and RL results in a low resistive state (R_p), representing logic "0". Conversely, the antiparallel magnetization between these layers results in high resistive state (R_{Ap}), representing logic "1". The relative resistance change between the parallel and anti-parallel states of an MTJ is quantitatively represented by tunnel magneto-resistance (TMR). Mathematically, TMR is

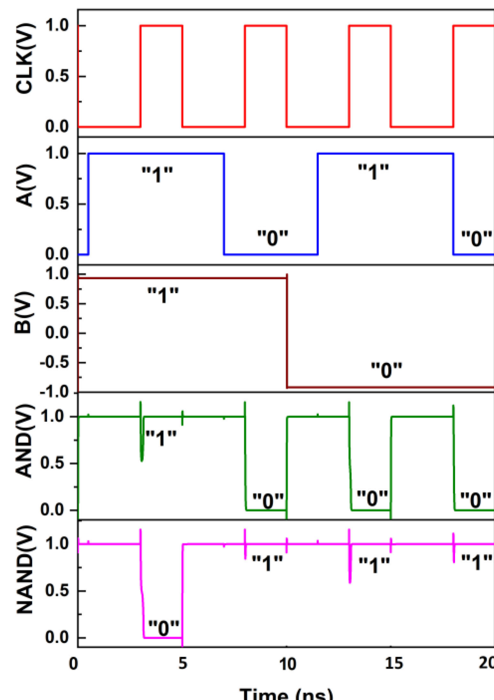


FIGURE 11. Transient waveform of hybrid AOS-MTJ/CMOS AND/NAND gate.

represented as

$$TMR = \frac{R_{AP} - R_p}{R_P} \tag{8}$$

III. WRITE AND READ OPERATION IN AOS-MTJ

This section discusses the write and read operation of the AOS-MTJ. The write operation is achieved using the laser pulse while the read operation is achieved using the conventional sense amplifier circuit.

A. WRITE OPERATION

The AOS-MTJ and laser source models as proposed [31], [32] have been used to integrate photonics, spintronics as well as electronics on a common platform for the implementation of logic circuits. The look up table based AOS-MTJ modeling has been performed by using VAMPIRE software [33], [34]. A total of 44 simulation runs have been performed by varying the input laser fluence from 0.5 mJ/cm^2 to 12 mJ/cm^2 for two different initial magnetization states of the free layer. The circuit simulation of AOS-MTJ has been performed by using Verilog-A in SPICE framework. The device parameters of AOS-MTJ are provided in Table 1. The schematic of the writing circuit is presented in Fig. 5, where an MTJ in an array can be switched by using a narrow laser pulse generated from a vertical cavity surface emitting laser (VCSEL). The selectivity of a particular MTJ is facilitated by a tunable grating. The

TABLE 1. Vampire Simulation Parameters For AOS-MTJ

Device parameter	Description	Default value
x_{Gd}	Alloy fraction of Gd	0.25
α	Damping constant	0.02
J_{Gd-Fe} $(J/link)$	Gd-Fe exchange matrix	-1.09x10^{-21}
J_{Gd-Gd} $(J/link)$	Exchange matrix of Gd	1.26 x10^{-21}
J_{Fe-Fe} $(J/link)$	Exchange matrix of Fe	2.835 x10^{-21}
$D_{Gd} = D_{Fe}$ $(J/spin)$	Uniaxial-anisotropy-constant	8.072 x10^{-24}
μ_{Gd} (J/T)	Gd spin moment	7.63
μ_{Fe} (J/T)	Fe spin moment	1.92

CMOS interface circuit is used to control the operation of VCSEL by adjusting the supply voltage V_{LDD} of the laser diode driver as shown in Fig. 6(a). The CMOS interface circuit as shown in Fig. 6(b) has been designed to generate narrow V_{LDD} pulses to control the time duration of the applied laser pulse. Both the laser source as well as logic circuits are operated using the same clock signal. The switching operation of AOS-MTJ is achieved by applying an ultra-short laser pulse for the duration of 5 ps as shown in Fig. 7. $E\langle 0\rangle$ and $E\langle 1\rangle$ represent the magnitude and phase of the laser pulse, respectively. The optical write energy E_o, required to switch the MTJ device is determined by the following equation [35]:

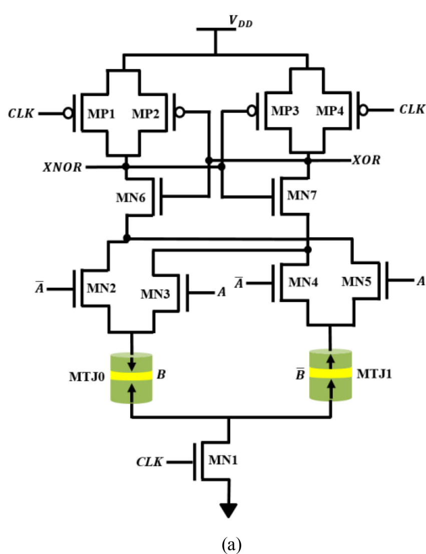
$$E_o = F_l \frac{\alpha_l}{\alpha_{max}} A \tag{9}$$

where, $F_l = 4.7$ mJ/cm^2 is the switching threshold fluence, A is the area of the MTJ structure, $\alpha_l = 1.3$, is the normalized absorption enhancement, $\alpha_{max} = 1.6$ is the maximum absorption enhancement. For MTJ having diameter of 50 nm, the optical write energy is E_o =75.36 fJ.

The electrical energy dissipation of VCSEL is given by $E_{vcsel} = 5.6$ fJ [36]. Moreover, the electrical energy consumption of the CMOS interface circuit for one bit write operation is $E_{circuit} = 1.7$ fJ. Therefore, the total write energy consumption for AOS-MTJ is given by $E_{total} = E_o + E_{vcsel} + E_{circuit} = 82.66$ fJ.

B. READ OPERATION

The read operation has been performed by using a conventional pre-charge sense amplifier (PCSA) circuit [37] as shown in Fig. 8. Due to its dynamic nature, the PCSA operates in two modes: 1. Precharge phase 2. Evaluation phase. In precharge mode, when the clock signal $CLK = 0$, both the output nodes Q and $\bar{Q}$ are set to V_{DD} or logic 1. The evaluation transistor *MN1* turns OFF and there exists no path to discharge the output nodes to ground. In evaluation mode, when $CLK = 1$, the transistor *MN1* turns ON that results in a discharging path between the two output nodes and the ground. However, the discharging speed for the two nodes depends upon the path resistance. If *MTJ0* is in antiparallel state, it provides a high resistance path in comparison to *MTJ1*



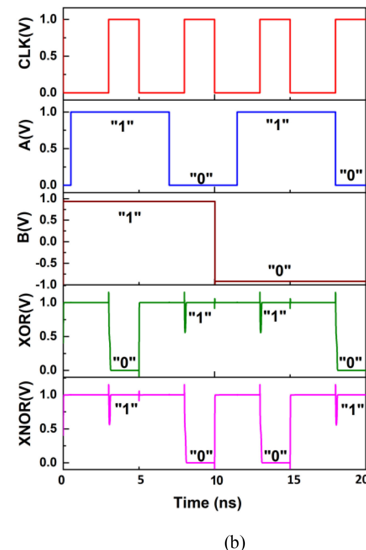


FIGURE 12. **(a) Hybrid AOS-MTJ based XOR/XNOR logic circuit (b) Transient waveform of hybrid AOS- MTJ/CMOS based XOR/XNOR logic operation.**

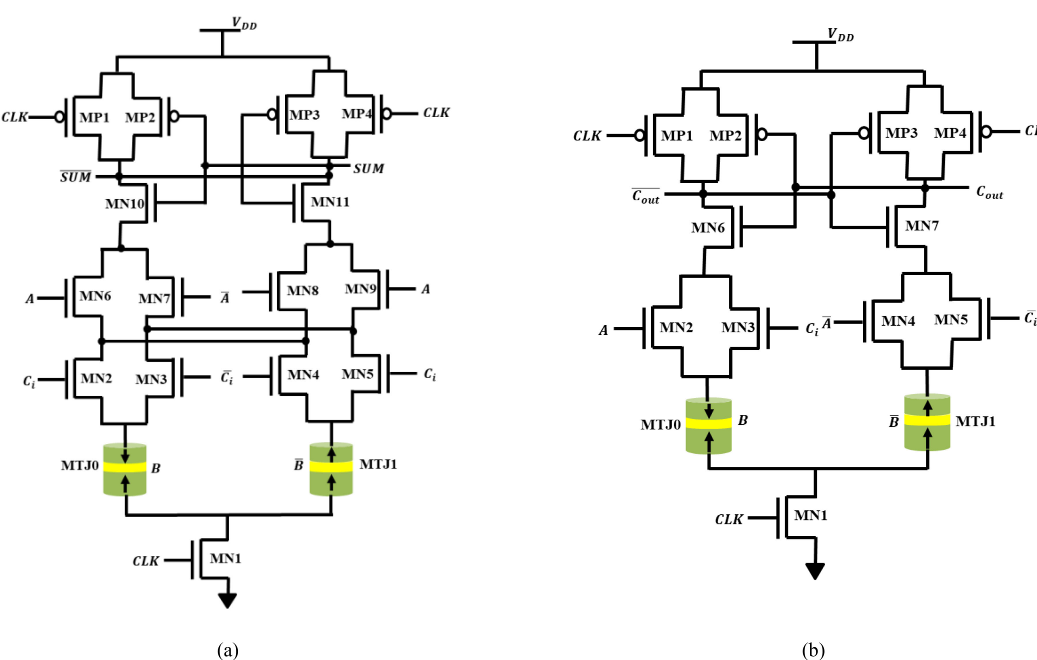


FIGURE 13. **Hybrid AOS-MTJ/CMOS based full adder circuit (a) sum operation (b) carry operation.**

which is in parallel state. As a result, the node Q will discharge faster than the node $\bar{Q}$. The instant Q discharges less than the switching threshold of inverter (*MP2* and *MN2),* node $\bar{Q}$ is pulled up to logic '1'. Q will be discharged to logic '0' through *MN3* and *MN1*.

IV. IMPLEMENTATION OF HYBRID AOS-MTJ/CMOS LOGIC CIRCUITS

The standard hybrid logic circuit as shown in Fig. 9, is comprised of the three major components namely, precharge sense amplifier, CMOS logic tree, and MTJ logic pair. Sense amplifier is employed to sense the state of MTJs. The output is generated based on the differential current flowing through the CMOS logic tree and MTJ pair. The write circuit sets the MTJ either in parallel (R_P) or anti-parallel (R_{AP}) states.

A. AND/NAND LOGIC

The schematic of the hybrid MTJ/CMOS dynamic AND/NAND logic operation is shown in Fig. 10. The transistors *MP1, MP2, MP3, MP4, MN5, MN6*, and *MN1* form the PCSA. The transistors *MN2, MN3*, *MN4,* and *MTJ0*,

TABLE 2. Truth Table For AND/NAND and XOR/XNOR Logic Gates With Corresponding Path Resistances

Logic gate	A	B	LB Resistance	RB Resistance	Resistance Comparison	AND	NAND
AND/NAND	0	0	$R_{OFF} + R_{AP}$	$R_{ON} + R_P$	$R_{LB} > R_{RB}$	0	1
	0	1	$R_{OFF} + R_P$	$R_{ON} + R_{AP}$	$R_{LB} > R_{RB}$	0	1
	1	0	$R_{ON} + R_{AP}$	$R_{ON} + R_P$	$R_{LB} > R_{RB}$	0	1
	1	1	$R_{ON} + R_P$	$R_{ON} + R_{AP}$	$R_{LB} < R_{RB}$	1	0
Logic gate	**A**	**B**	**LB Resistance**	**RB Resistance**	**Resistance Comparison**	**XOR**	**XNOR**
XOR/XNOR	0	0	$R_{ON} + R_{AP}$	$R_{ON} + R_P$	$R_{LB} > R_{RB}$	0	1
	0	1	$R_{ON} + R_P$	$R_{ON} + R_{AP}$	$R_{LB} < R_{RB}$	1	0
	1	0	$R_{ON} + R_P$	$R_{ON} + R_P$	$R_{LB} < R_{RB}$	1	0
	1	1	$R_{ON} + R_{AP}$	$R_{ON} + R_{AP}$	$R_{LB} > R_{RB}$	0	1

R_{ON}: NMOS ON resistance, R_{OFF}: NMOS OFF resistance, LB: Left branch, RB: Right branch, R_P: Parallel state of MTJ, R_{AP} Antiparallel state of MTJ

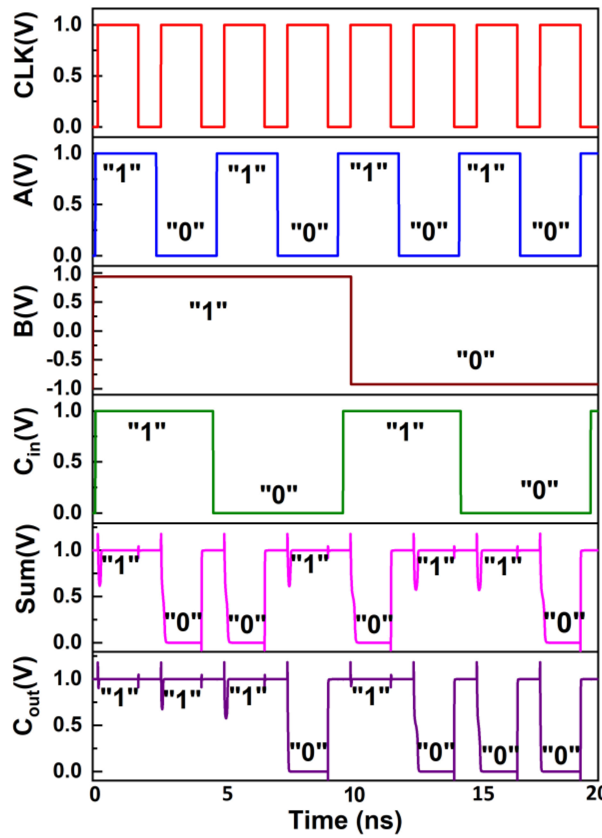


FIGURE 14. Transient waveform of magnetic full adder.

MTJ1 form the logic network. One of the non-volatile inputs B and $\bar{B}$ is stored in MTJ devices. The other inputs A and $\bar{A}$ are applied to *MN2, MN3,* and *MN4* transistors. The working of the hybrid MTJ/CMOS AND/NAND logic circuit is explained in the following two phases:

I) *Precharge phase*: In this phase, the *CLK* is set to low and both the output nodes $AND/NAND$ are charged to V_{DD} or logic "1".

II) *Evaluation phase:* In this phase, the *CLK* is set to high. The transistor *MN1* is ON while *MP1* and *MP4* are *OFF*. Both the output nodes $AND/NAND$ discharge through the evaluation transistor *MN1*. The discharging of the output nodes will depend both on the MTJ state and the input *A*. The voltages at the output nodes depend on the pull-up and pull-down paths that are determined by the MTJ state and the logic transistors *MN2*, *MN3*, and *MN4*. Table 2 shows the *AND/NAND* output and different path resistances corresponding to the different combinations of MTJ and the input. The transient waveform of the hybrid MTJ/CMOS AND gate is presented in Fig. 11.

B. XOR/XNOR LOGIC

The schematic of the 2-input non-volatile $XOR/XNOR$ gate is shown in Fig. 12(a). In precharge phase, both the output nodes XOR and $XNOR$ are charged to V_{DD} or logic '1'.

In evaluation phase, the transistor *MN1* is ON while *MP1* and *MP4* are OFF. Both the output nodes *XOR/XNOR* discharge through the evaluation transistor MN1. The discharging of the output nodes will depend both on the MTJ state and the input *A*. The voltages at the output nodes depend on the state of MTJ and the logic transistors *MN2*, *MN3*, *MN4*, and *MN5*. Table 2 shows the $XOR/XNOR$ output and different path resistances corresponding to the different combinations of MTJ and the input. The transient waveform of the *XOR/XNOR* gate is shown in Fig. 12(b).

C. FULL ADDER

The schematic of the magnetic full adder is shown in Fig. 13 where "*A*," "*B*," and "C_{in}," are the inputs and "*SUM*" and "C_{out}," are the outputs. The non-volatile inputs B and $\bar{B}$ are stored in MTJ0 and MTJ1, respectively. In precharge phase, the output nodes SUM, $\overline{SUM}$, C_{out}, and $\overline{C_{out}}$ precharge to logic '1'. In evaluation phase, the transistor *MN1* of both the sum and carry circuits is ON and output is determined according to the (10) and (11).

$$Sum = ABC_{in} + A\bar{B}\overline{C_{in}} + \bar{A}\bar{B}C_{in} + \bar{A}B\overline{C_{in}} \quad (10)$$

TABLE 3. Truth Table For Full Adder (Fa) With Corresponding Path Resistances

FA operation	A	B	C_{in}	LB Resistance	RB Resistance	Resistance Comparison	SUM	$\overline{SUM}$
SUM	0	0	0	$2R_{ON}+R_{AP}$	$2R_{ON}+R_{P}$	$R_{LB} > R_{RB}$	0	1
	0	0	1	$2R_{ON}+R_{P}$	$2R_{ON}+R_{AP}$	$R_{LB} < R_{RB}$	1	0
	0	1	0	$2R_{ON}+R_{P}$	$2R_{ON}+R_{AP}$	$R_{LB} < R_{RB}$	1	0
	0	1	1	$2R_{ON}+R_{AP}$	$2R_{ON}+R_{P}$	$R_{LB} > R_{RB}$	0	1
	1	0	0	$2R_{ON}+R_{P}$	$2R_{ON}+R_{AP}$	$R_{LB} < R_{RB}$	1	0
	1	0	1	$2R_{ON}+R_{AP}$	$2R_{ON}+R_{P}$	$R_{LB} > R_{RB}$	0	1
	1	1	0	$2R_{ON}+R_{AP}$	$2R_{ON}+R_{P}$	$R_{LB} > R_{RB}$	0	1
	1	1	1	$2R_{ON}+R_{P}$	$2R_{ON}+R_{AP}$	$R_{LB} < R_{RB}$	1	0
FA operation	**A**	**B**	C_{in}	**LB Resistance**	**RB Resistance**	**Resistance Comparison**	C_{out}	$\overline{C_{out}}$
CARRY	0	0	0	$2R_{OFF}+R_{AP}$	$2R_{ON}+R_{P}$	$R_{LB} > R_{RB}$	0	1
	0	0	1	$R_{OFF}+R_{ON}+R_{AP}$	$R_{OFF}+R_{ON}+R_{P}$	$R_{LB} > R_{RB}$	0	1
	0	1	0	$2R_{OFF}+R_{P}$	$2R_{ON}+R_{P}$	$R_{LB} > R_{RB}$	0	1
	0	1	1	$R_{OFF}+R_{ON}+R_{P}$	$R_{OFF}+R_{ON}+R_{AP}$	$R_{LB} < R_{RB}$	1	0
	1	0	0	$R_{OFF}+R_{ON}+R_{AP}$	$R_{OFF}+R_{ON}+R_{P}$	$R_{LB} > R_{RB}$	0	1
	1	0	1	$2R_{ON}+R_{AP}$	$2R_{OFF}+R_{P}$	$R_{LB} < R_{RB}$	1	0
	1	1	0	$R_{OFF}+R_{ON}+R_{P}$	$R_{OFF}+R_{ON}+R_{AP}$	$R_{LB} < R_{RB}$	1	0
	1	1	1	$2R_{ON}+R_{P}$	$2R_{OFF}+R_{AP}$	$R_{LB} < R_{RB}$	1	0

TABLE 4. Device Level Performance Comparison of Energy and Latency

Device	Write energy (fJ/bit)	Write latency (ns)
STT-MTJ	723	6.5
SOT-MTJ	94	2
AOS-MTJ	82.66	0.01

TABLE 5. Performance Comparison Of Hybrid MTJ/CMOS Circuits

Logic circuit	STT-MTJ	SOT-MTJ	AOS-MTJ
NAND gate logic operation energy (fJ)	730.48	98.35	86.56
NAND gate latency (ns)	6.85	2.2	0.192
XOR gate logic operation energy (fJ)	731.33	99.22	86.88
XOR gate latency (ns)	6.87	2.24	0.192
Full adder logic operation energy (fJ)	1082.07	178.15	159.86
Full adder latency (ns)	6.89	2.26	0.195

$$C_{out} = AB + AC_{in} + BC_{in} \quad (11)$$

The "SUM" and "C_{out}" and their dependence on resistance configuration of CMOS logic tree and MTJ pair are shown in Table 3. The transient waveform of the full adder circuit is shown in Fig. 14.

V. PERFORMANCE EVALUATION

The device as well as circuit-level performance parameters of the AOS-MTJ are compared with the existing switching mechanisms such as STT and SOT and are presented in Tables 4 and 5, respectively. It is evident that the write energy of AOS-MTJ is improved by 88.5% and 12% while the switching speed is enhanced by 99.8% and 99.5% when compared with STT and SOT switching techniques, respectively. The circuit level results show that the energy efficiency of AOS-MTJ based NAND and XOR gates is increased by 88% and 12% whereas the logic delay is improved by about 97% and 91% in comparison to STT and SOT based designs, respectively. Moreover, the energy efficiency of AOS-MTJ based full adder is improved by 85% and 10% as compared to STT and SOT based full adder circuits. The logic delay of AOS-MTJ based full adder is improved by 97% and 91% when compared with STT and SOT based circuits.

One of the prominent challenges in the optical MRAM technology is that the on-chip integration of optics increases the footprint. This overhead can be compensated by parallel switching of multiple MTJs. The writing of 10^2–10^6 MTJs can be achieved simultaneously by exposing the MTJs to a spatially tailored excitation of single-shot laser pulse [38]. In such an arrangement, the MTJs are optically selected through tunable gratings [39]. This simultaneous switching of MTJs also allows the implementation of parallel logic operations for applications such as image processing, neuromorphic computing.

VI. CONCLUSION

In this work, hybrid CMOS/MTJ based AND/NAND, XOR/XNOR and full adder logic circuits with all-optical MTJ switching mechanism have been presented. The device as well as circuit-level results show that the energy and speed of AOS-MTJ are improved as compared to STT and SOT based MTJs. Therefore, AOS-MTJ has a great potential for high-speed and low-power computing applications such as in-memory and neuromorphic computing.

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