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Novel Radiation Hardened SOT-MRAM Read Circuit for Multi-Node Upset Tolerance

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ABSTRACT The rapid transistor scaling and threshold voltage reduction pose several challenges such as high leakage current and reliability issues. These challenges also make VLSI circuits more susceptible to soft-errors, particularly when subjected to harsh environmental conditions. Hybrid spintronic/CMOS technology has emerged as one of the promising techniques to achieve low leakage power and non-volatility. Moreover, the spintronic memories are inherently resistant to the radiation effects such as heavy-ion irradiation and total ionizing dose. However, its CMOS peripheral circuitry is more susceptible to radiation-induced single-event upset (SEU) and double-node upset (DNU). In this paper, a new radiation-hardened read circuit for SOT magnetic random access memory (MRAM) on 45nm technology has been presented. The proposed circuit is highly resistant to all the probable SEUs and DNUs when compared to the previously reported designs. The results show that it can tolerate 4.5X, 11X, 9X, and 10.5X more critical charge as compared to the cross-coupled CMOS transistor, 11T, 13T, and 11T radiation hardened circuits, respectively. Moreover, the recovery time of the proposed circuit is improved by 20% when compared to cross-coupled CMOS transistor circuits.

INDEX TERMS Double node upset (DNU), magnetic tunnel junction (MTJ), radiation-hardened, single event upset (SEU), soft error.

I. INTRODUCTION

A single event upset (SEU) is a non-destructive and soft-error type of single event effects (SEEs). SEU is the result of the interaction of a single charge particle with the circuit. As the transistor size of complementary metal oxide semiconductor (CMOS) designs decreased, the problem caused by SEUs became more serious [1]. The circuit integration is increasing and node spacing is reducing due to the advances in CMOS manufacturing technology. Hence, a single particle can also impact two sensitive nodes in a storage element due to charge sharing effects [2], causing both nodes to be disturbed at the same time. This is referred to as a double-node upset (DNU) [3], [4]. Therefore, it is critical for circuit designers to improve the robustness of circuits and systems against the single as well as double-node radiation effects. Spintronics devices have been considered as a viable alternative to achieve resistance against the radiation effects while offering non-volatility, high energy-efficiency, high reliability and endurance, and strong compatibility with the CMOS technology [5]–[7]. Spin-transfer torque (STT) is one of the widely used switching mechanisms in spintronic devices to design memory and logic circuits because of its simple design and high scalability. However, STT-MRAM has several issues owing to the inherent mechanism of STT [8]. The endurance of STT-MRAM is affected due to the same read and write path and a substantial electrical current is also required to perform a high-speed write operation, putting the tunnel junction under a high-stress condition (low thermal stability). Spin orbit torque MRAM (SOT-MRAM) has emerged as a suitable solution to address the issues associated with the STT-MRAM. It has been demonstrated to attain ultrafast and energy efficient switching because of its higher

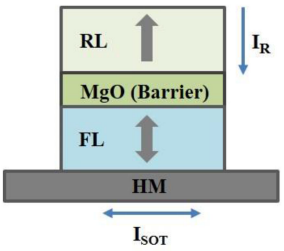

FIGURE 1. The structure of the three terminal SOT-MTJ.

spin-torque efficiency [9]. Furthermore, the decoupled read and write paths result in its improved endurance. SOT-based spintronic memory has provided a unique solution to address the endurance issue while ensuring better performance in power dissipation [10]. Although STT-MRAM and SOT-MRAM are seen as a promising candidate for the radiation hardened memory but their peripheral CMOS write and read circuitry is still susceptible to the radiation effects that pose a significant challenge in aerospace and avionic electronics applications [11]. Many SEU-immune peripherals read circuits such as C-element [12] and XOR logic gate [13] have been reported for STT-MRAM. However, these circuits are not immune to the DNUs. Recently, read and write circuit techniques have been proposed for SOT-MRAM to achieve radiation resistance against both the SEUs and DNUs [14], [15]. However, these circuits can tolerate the radiation particles having the effective charge not more than a few hundreds of fC. Therefore, it is required to improve the radiation tolerance of these circuits for hazardous environments. In this work, a novel radiation-hardened read circuit for SOT-MRAM is presented. The key contributions of the proposed circuit are as following:

1) The proposed read circuit is immune to both the SEUs and DNUs.
2) The circuit exhibits radiation tolerance up to 1000 fC while achieving the recovery time of 0.3 ns.

The rest of the paper is organized as follows: In Section II, the background of SOT-MTJ phenomena has been discussed. Section III explains the basic operation of the radiation-hardening design as well as SEU and DNU recovery analysis of the proposed circuit. Finally, the work is concluded in Section IV.

II. SPIN ORBIT TORQUE-MAGNETIC TUNNEL JUNCTION

SOT magnetic tunnel junction (MTJ) is a three-terminal device composed of two ferromagnetic layers separated by thin MgO tunnel barrier, as shown in Fig. 1. The free layer is in contact with heavy metal (HM) strip. The spin Hall effect (SHE) and the Rashba effect are responsible for generating SOT by passing a charge current (J_e) through the HM layer [16], [17]. The magnetization dynamics of SOT MTJ can be modeled by adding the SOT terms in Landau–Lifshitz–Gilbert (LLG) equation [18]:

$$\frac{\partial m}{\partial t} = -\gamma m \times H_{eff} + \alpha m \times \frac{\partial m}{\partial t} + \gamma \tau_{SOT} \tag{1}$$

$$\tau_{SOT} = \tau_{II}^{0}\,(m \times (\sigma \times m)) + \tau_{\perp}^{0}\,(\sigma \times m) \tag{2}$$

where, γ, α, and $H_{eff,}$ are the gyromagnetic ratio, damping constant, and effective magnetic field, respectively. τ_{SOT} represents the composition of damping-like (τ_{II}^{0}) and the field-like torque ($\tau_{\perp}^{0}$), m is the unit vectors of the magnetization orientation, and σ is the spin polarization.

The resistance of an MTJ depends upon the relative orientation of magnetization of its free and fixed layers: low-resistance (R_P) in parallel state and high-resistance (R_{AP}) in anti-parallel state. The R_P is expressed as [19]:

$$R_P = \frac{t_{ox}}{A_{MTJ} * F * \bar{\varphi}^{1/2}} * exp\left(\frac{2t_{ox}(2em\bar{\varphi})^{\frac{1}{2}}}{\hbar}\right) \tag{3}$$

where m, $\hbar$, and e represent the mass of the electron, reduced Planck constant, an elementary charge respectively, A_{MTJ} is the section area of the magnetic tunnel junction, F is the fitting factor, and t_{ox} and $\bar{\varphi}$ represent the thickness and potential barrier height of the tunnel barrier layer, respectively. The R_{AP} can be evaluated as:

$$R_{AP} = R_P\,(1 + TMR) \tag{4}$$

where the tunnel magnetoresistance (TMR) is measuring the variation between the parallel (R_P) and anti-parallel (R_{AP}) resistance. The TMR of MTJ is set at 150% and the values of R_P and R_{AP} resistances states are 3.47 kΩ and 8.694 kΩ, respectively.

TABLE 1. Critical Parameters of the SOT-MTJ Compact Model

Parameter	Value
Saturation magnetization (A/m)	1×10^{6}
Free layer thickness (nm)	0.6×10^{-9}
Heavy metal dimension (nm)	$200 \times 150 \times 3$
TMR @ zero voltage	150 %
External magnetic field (Oe)	600
Spin Hall angle	0.21

III. PROPOSED RADIATION HARDENED READ CIRCUIT AND ITS OPERATION

Soft errors such as SEU and DNU can be recovered using the radiation-hardened read circuit based on the pre-charge sense amplifier (PCSA) [20]. The unprotected PCSA has two sensitive nodes i.e., Q and Q_b that are disrupted when a particle hits any one of the nodes [21]. The proposed novel 13T-radiation-hardened read circuit comprises of basic PCSA, four PMOS transistors (P_5-P_8), and two NMOS transistors (N_4 and N_5) as shown in Fig. 2. A SPICE-compatible SOT MTJ model [18] and 45nm CMOS technology are used to design the proposed circuit. The critical parameters of the SOT-MTJ compact model are presented in Table 1. The two techniques have been used to improve the radiation tolerance and recovery time: (1) using feedback circuit to discharge

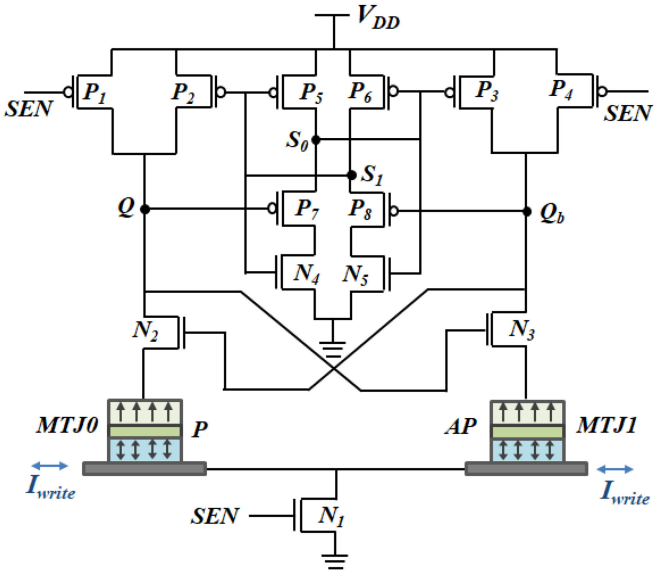

FIGURE 2. The proposed radiation hardened read circuit for the SOT-MRAM cell.

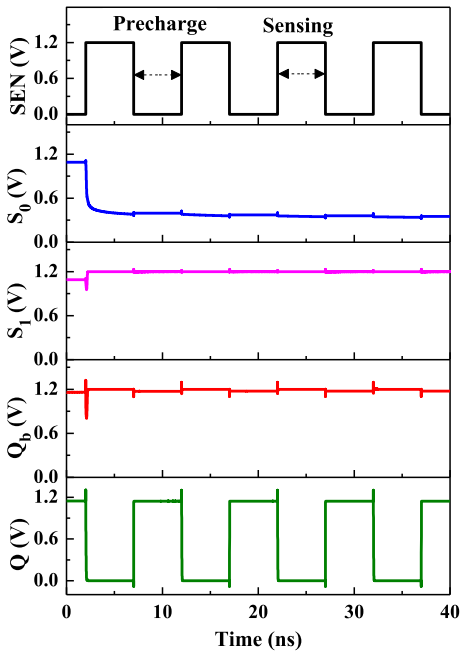

FIGURE 3. Transient analysis of the proposed circuit without radiation effects.

radiation charges induced at the sensitive nodes (2) increasing the equivalent capacitance of the sensitive node to increase its critical charge Q_c. A transient fault is generated if the injected charge (Q_{inj}) exceeds Q_c of the sensitive node, expressed as [22]:

$$Q_c = C_N \, .V_{DD} + I_D \, .T_F \tag{5}$$

where V_{DD}, I_D, and C_N represent the power supply, drain current and equivalent capacitance of the considered node which is proportional to the transistor width, and T_F is the flipping time of the cell. For a fixed value of T_F, increasing the transistor width by x times increases Q_c by almost a factor of x.

The proposed circuit works in the following two phases: (1) Pre-charge phase ($SEN =$ '0'): In this phase, the transistors P_1 and P_4 are turned ON while the discharge transistor N_1 goes into the OFF state. Hence, the output Q and Q_b are charged up to V_{DD}. (2) Evaluation phase ($SEN = '1'$): In this phase, both the PMOS transistors P_1 and P_4 are turned OFF while the discharge transistor N_1 is turned ON. Here, it is assumed that initially the *MTJ0* and *MTJ1* are in parallel and anti-parallel states, respectively. Therefore, the resistance offered by *MTJ0* (R_P) is less than the resistance offered by *MTJ1* (R_{AP}). The current flowing through *MTJ0* is more than the current flowing through *MTJ1*. Hence, when the N_1 transistor is turned ON, both the outputs Q and Q_b begin to discharge at the different speeds. This causes the voltage at Q to drop faster than at Q_b. The transistor N_3 is turned OFF as soon as it is below the threshold voltage of N_2. The node Q_b is then pulled up to V_{DD} or logic '1', while node Q is pulled down to ground or logic '0'. The transient simulations of the radiation-hardened read circuit without considering the radiation effects are shown in Fig. 3.

If a node is located within the range of a reverse-biased drain junction that is in the off state, it is considered as a sensitive node. Hence, for the proposed circuit, there are only three sensitive nodes i.e., Q, Q_b, and S_1 or Q, Q_b, and S_0. Here, the gates of the N_4 and N_5 transistors are controlled by the nodes S_1 and S_0, respectively while the gates of the P_7 and P_8 transistors are controlled by Q and Q_b, respectively. As *MTJ0* and *MTJ1* are in parallel and anti-parallel states, respectively, the states of Q, Q_b, S_0, and S_1 are 0, 1, 0, and 1 respectively.

For the case when $Q = '0'$, the sensitive nodes are Q, Q_b, and S_0. Fig. 4 shows the equivalent MTJ/CMOS read circuit when the state of Q, Q_b, S_0 and S_1 are 0, 1, 0, and 1 respectively. The double exponential current source model [23] as shown in Fig. 6(a) and 6(b) is used to induce SEU/MNU effects in the sensing circuit and is expressed as:

$$I(t) = I_0 \left(e^{\frac{-t}{\tau_\alpha}} - e^{\frac{-t}{\tau_\beta}} \right) \tag{6}$$

$$I_0 = Q_{inj} / (\tau_\alpha - \tau_\beta) \tag{7}$$

where I_0 is the peak current, τ_α is the collection time constant with a typical value of 150 ps. The τ_β is ion track establishment time constant with the typical value of 50 ps. Q_{inj} represents the total amount of charge injected at the sensitive node with values ranging from -2 to 2 pC. Following are the cases for single event upset at all the possible sensitive nodes:

1) SEU at Q: Whenever a particle strikes at the node Q, it becomes "0→1". Due to this, the transistor P_7 is turned OFF while N_3 is turned ON. On the other hand, a significantly stronger PMOS (P_3 is 4 times larger than N_3) keeps Q_b in the logic '1' state. Since P_7 is turned OFF,

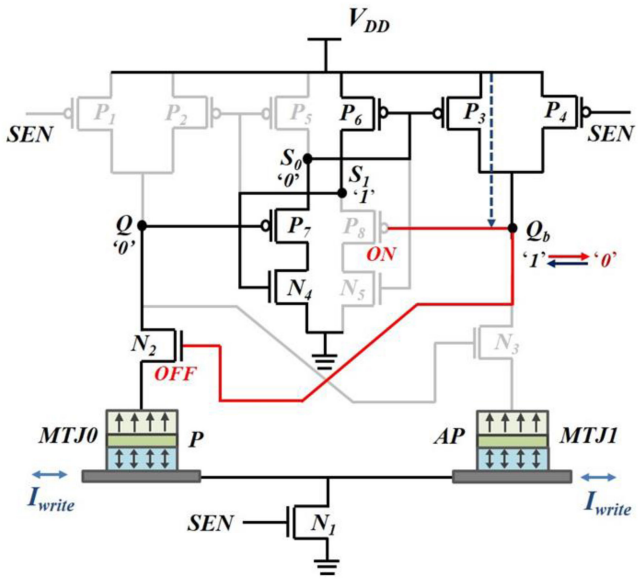

FIGURE 4. MTJ/CMOS read circuit for the SOT-MRAM cell. The light gray color represents the turned-off transistors. The red line shows the impact of the radiation particles, while the blue line represents the charging path to node Q_b.

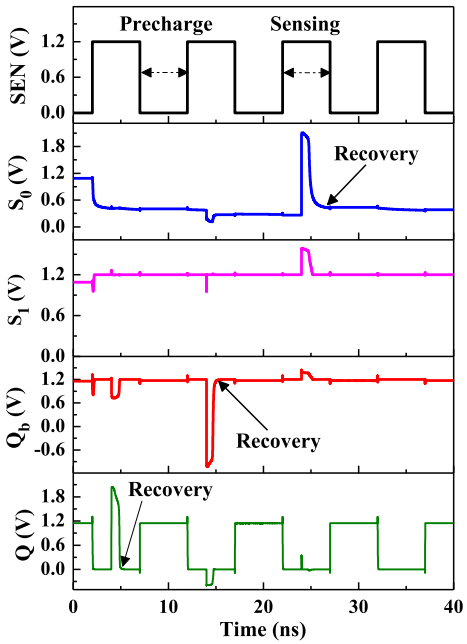

FIGURE 5. Transient simulation results of the proposed radiation-hardened read circuit in the presence of 1000 fC radiation particle striking the sensitive nodes Q, Q_b and S_0. All the states can be fully recovered.

the pull-down path associated with S_0 is disconnected. Here, S_1 is not affected; therefore, the pull-up transistor P_5 remains OFF. As S_0 is isolated from both the pull-up and pull-down resistance paths, a high impedance state occurs, thereby allowing it to maintain its logic value. As soon as, both the sensitive nodes Q_b and S_0 acquire

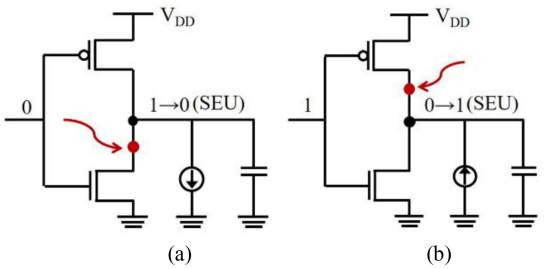

FIGURE 6. The circuit showing the polarity of the current to generate (a) a negative transient pulse at the '1' storing sensitive node (b) a positive transient pulse at the '0' storing sensitive node.

their initial states, the circuit pulls the node Q back to its previous state i.e., logic '0'.

2) SEU at Q_b: The sensitive node Q_b is flipped to '0' when a particle strikes to it. This causes P_8 and N_2 to turn ON and OFF, respectively. The transistors P_6 and N_5 maintained their states i.e., ON and OFF by the unaffected nodes S_0 and S_1. As a result, S_1 keeps P_2 in OFF state, leaving Q in a high impedance state with P_2 and N_2 in OFF state. The transistor N_3 is turned OFF since Q preserves its state. As a result, P_3, which is maintained ON by the sensitive node S_0, pulls the node Q_b back to '1'.
3) SEU at S_0: When node S_0 is affected by a charged particle, it is turned from "0→1". Due to this, N_5 is turned ON while the transistors P_3 and P_6 are turned OFF. It should be noted that the node Q which is unaffected, maintains the OFF state of transistor N_3. Thus, Q_b goes in a high impedance state. As a result, Q_b preserves its state and maintains the OFF state of transistor P_8. Therefore, S_1 enters a high impedance state. The sensitive node S_0 is pushed back to '0' since the transistor P_5 is turned OFF and its pull-down path (P_7 and N_4 is ON) is turned ON.
4) DNU at Q-Q_b: Nodes Q and Q_b are turned to '1' and '0', respectively if they are struck by a DNU. Since the node Q (Q_b) is connected to gates of the transistors P_7 and N_3 (P_8 and N_2), P_7 and N_3 (P_8 and N_2 are turned "ON" and "OFF" respectively) are turned "OFF" and "ON", respectively. However, due to the cross-coupled nature, S_1 and S_0 are unaffected and results in the "ON" and "OFF" states of the transistors P_3 and P_2, respectively. Since P_3 is stronger than N_3, the node Q_b is pulled up to logic '1'. When node Q_b is restored, it switches "ON" N_2 and as P_2 is in "OFF" state already by node S_1, thus the node Q is discharged to the ground through N_2. As a result, Q and Q_b revert to their previous values. Therefore, the proposed circuit is potentially immune to SEUs as well as DNUs. The transient simulation results are depicted in Fig. 5 for all possible SEUs and in Fig. 7(a) for DNU. The proposed read circuit radiation tolerance is validated using a hybrid simulation with values of Q_{inj} ranging from 20 fC to 1000 fC, as shown in Fig. 7(b).

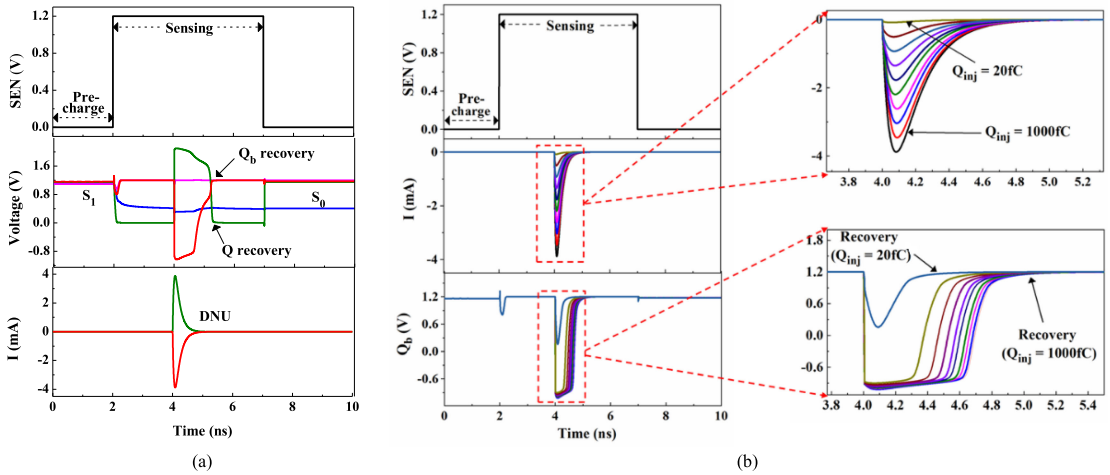

FIGURE 7. **(a) Transient simulation waveform when the sensitive nodes Q and Q_b are struck by DNU with 1000 fC radiation particle. Q and Q_b states are successfully recovered. (b) Hybrid simulation with various values of Q_{inj} from 20 fC to1000 fC at the node Q_b.**

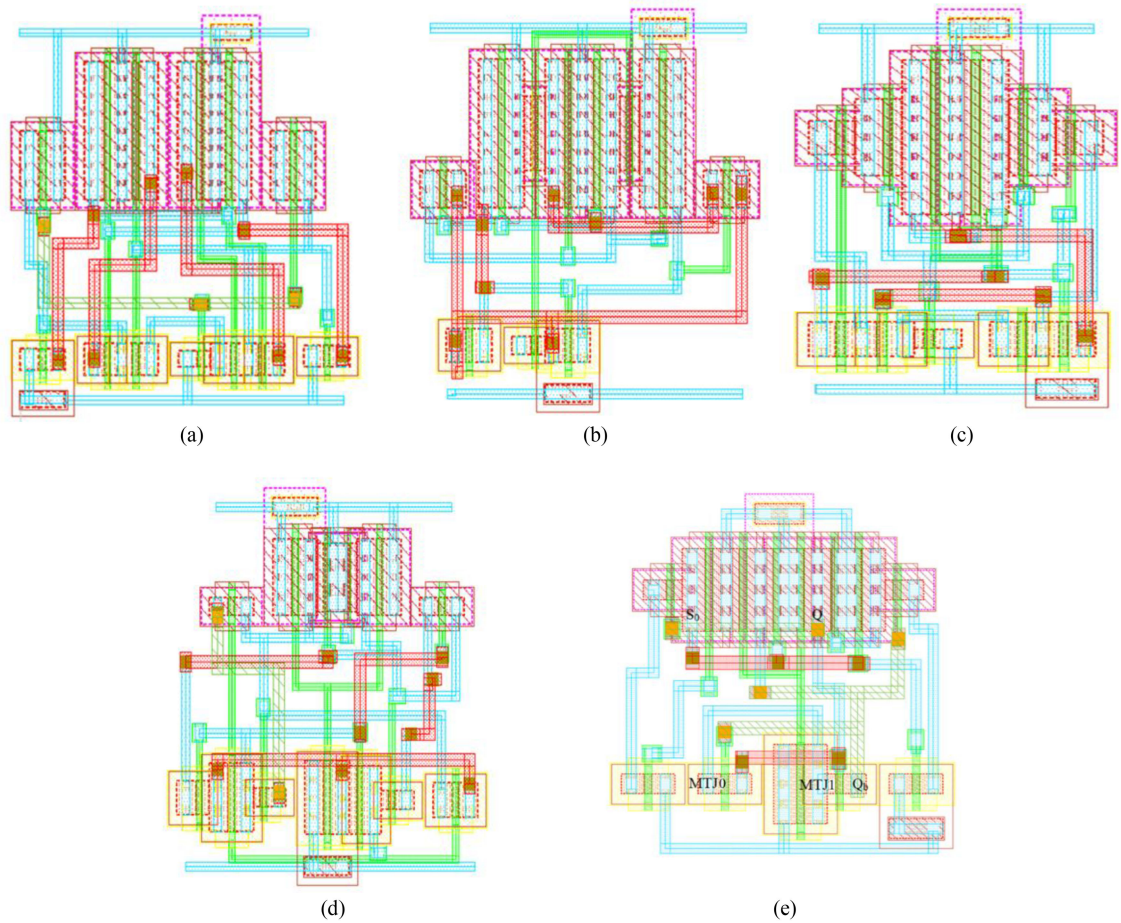

FIGURE 8. **Layout of the previously reported radiation-hardened read circuit (a) 13T [15], (b) 11T [14], (c) 11T [25], (d) Cross coupled [21], and (e) Layout of the proposed radiation-hardened read circuit.**

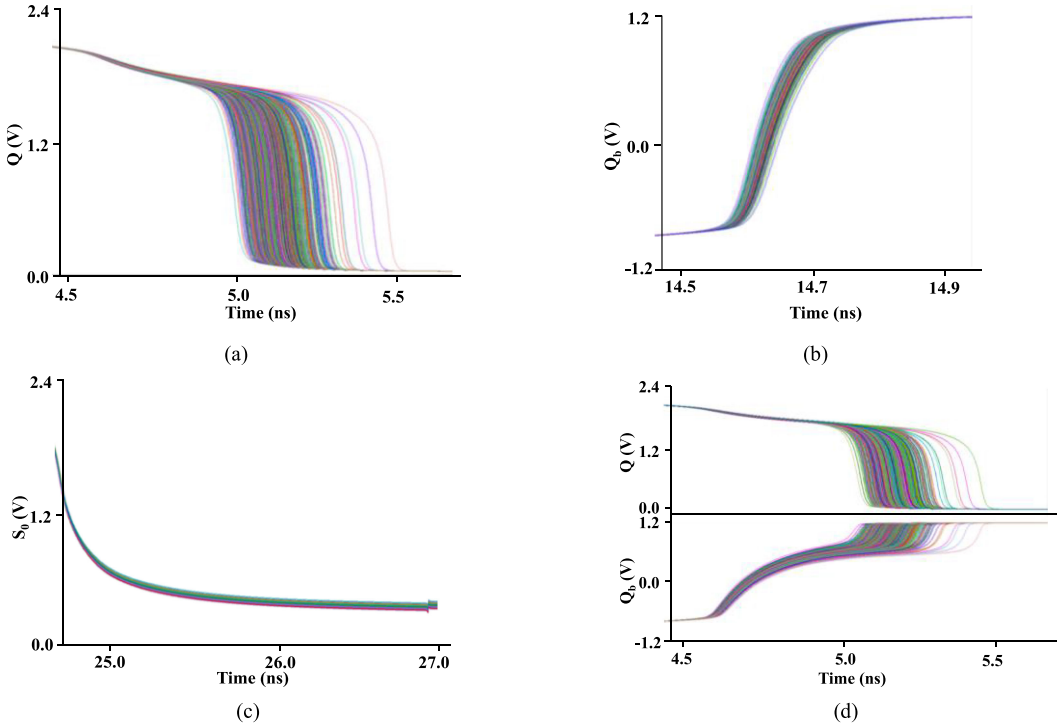

FIGURE 9. Variation in the recovery time due to the MTJ and CMOS transistor parameters for SEU at the sensitive node (a) Q, (b) Q_b, (c) S_0 and DNU at the node pair (d) Q-Q_b.

TABLE 2. Comparison Results Among Various Radiation Hardened Circuits at 45nm CMOS Technology Node

Rad-hard read circuits	No. of transistors	No. of sensitive node pairs @SEU	No. of sensitive node pairs @DNU	Recovery time (ns) @ 20fC	Max. tolerant Q_c (fC)	FOM (fC/μm^2)
Cross coupled [21]	13	3	3	0.35	226	43.72
11T circuits [14]	11	3	3	0.27	95	27.94
13T circuits [15]	13	4	6	0.29	112	17.5
11T circuits [25]	11	4	6	0.27	90	26.50
Proposed rad-hard circuit	13	3	3	0.30	1000	238.09

TABLE 3. Percentage Variation in MTJ and CMOS Parameters [26]

Parameters	Variation
Variation in MTJ device parameters	
Tunnel barrier thickness	2%
TMR	10%
Variation in CMOS transistor parameters	
Threshold voltage	5%
Channel length	10%
Channel width	10%

It is worth noting that the node pairs S_0-Q_b and S_0-Q are not immune to DNU that is caused by charge sharing effect. However, the charge sharing can be avoided by separating the node pairs S_0-Q_b and S_0-Q by at least 1.62 μm and 0.6 μm region, respectively at the layout level design [15], [24]. Fig. 8(a)-(d) shows the layout of all the previously reported radiation hardened read circuits. The layout of the proposed radiation-hardened read circuit with separated node pairs S_0-Q_b and S_0-Q is shown in Fig. 8(e).

The proposed circuit exhibits higher immunity to all possible SEUs and DNUs when the size of the PMOS transistors P_2 and P_3 is greater than two times the size of the NMOS transistors N_2 and N_3. The W/L ratio of the proposed circuit has been optimized as $(W/L)_{P1/P2/P3/P4} = 4(W/L)_{N2/N3} = 10$ and $(W/L)_{P5} = (W/L)_{P6} = 4(W/L)_{P7/P8} = 4(W/L)_{N4/N5} = 10$ to assure the reliability of SEU as well as DNU recovery under the PVT variations as well. In order to access the resilience of the proposed circuit, 1000 Monte Carlo simulations have been carried out with the parameter variation as given in Table 3. It is evident from the transient results, as shown in Fig. 9, that the proposed design is reliable for the given variation of MTJ and CMOS parameters. The figure of merit (FOM) represents the overall efficiency of the proposed circuit and is expressed as:

$$\text{FOM} = Q_c/A \tag{8}$$

where Q_c represents the radiation induced charge and A is the area of RH-MRAM. The FOM of the proposed circuit is improved by 5.44X, 8.52X, 13.6X and 8.98X as compared

to previously reported cross-coupled CMOS transistor [21], 11T [14], 13T [15], and 11T [25] radiation hardened circuits, respectively as shown in Table 2. The proposed radiation-hardened read circuit has the higher Q_c and can withstand 4.5X, 10.5X, 9X, and 11X higher critical charge as compared to cross-coupled CMOS transistors [21], 11T [14], 13T circuits [15], and 11T circuits [25], respectively. Moreover, in comparison to cross-coupled CMOS transistors [21], the proposed cell has a recovery time efficiency of 20% as shown in Table 2.

IV. CONCLUSION

The proposed radiation-hardened read circuit for SOT-MRAM is resistant to both SEUs and DNUs. It can tolerate the charge of 1000 fC and can recover within 0.3 ns. The proposed circuit has a huge potential for applications in aerospace and avionics electronics.

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