Received 7 December 2021; revised 29 January 2022; accepted 8 March 2022. Date of publication 30 March 2022; date of current version 29 April 2022. The review of this paper was arranged by Associate Editor James Morris.

Digital Object Identifier 10.1109/OJNANO.2022.3163386

Embedded-Component Planar Fan-Out Packaging for Biophotonic Applications

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This work was supported in part by Coulter Seed Grants from the Department of Biomedical Engineering at Florida International University, in part by NSquared Technologies, and in part by Advanced Materials Engineering Research Institute (AMERI).

ABSTRACT Embedded-chip planar silver-elastomer interconnect technology is developed with flexible substrates and demonstrated for on-skin biophotonic sensor applications. This approach has several benefits and is also consistent with chip-thinning where the chip thickness is 100 microns and less. The key benefits from this approach arise because both the bottom and top sides are now available as flat surfaces for 3D integration of other components. It also results in the lowest electrical parasitics compared to flipchip with adhesives or printed-ramp interconnections with surface-assembled devices. Embedding of chips in flexible carriers was accomplished with direct screen-printed interconnects onto the chip pads in substrate cavities. Silver nanoflake-loaded polyurethane is utilized in the embedded-chip packages to provide the desired lower interconnect resistance and also reliability in flexible packages under deformed configurations. Viscoelastic models were utilized to model the interconnection stresses. Planar interconnects in flexible substrates are developed with conductive silver-loaded elastomer interconnects. This approach is compared to direct chip-on-flex assembly technology for reliability under bending and high-temperature storage. The embedded-chip technology is demonstrated through biophotonic sensor applications where light sources (LEDs) and photodetectors are embedded inside the package. Functional validation in bent configuration at low curvatures is shown by measuring pulse rate and muscle activity with human subjects. By extending this technology to nanowires in elastomers, further enhancement in electrical and reliability performance can be achieved.

INDEX TERMS Fan-out, die-embedding, deformable, flexible, interconnects, biophotonics.

I. INTRODUCTION

Emerging applications in health monitoring, safety, and security will have the ability to monitor and collect data continuously while maintaining a constant connectivity with data analysis and processing networks [1]. In order to realize this trend, wearable electronics have continuously adapted advances in traditional substrate and assembly technologies that led to high-density electronic components integration for sensor signal processing and communication. The components provide active functions such as photonic light sources, photodetectors, diodes, rectifiers, mixers, voltage-controlled oscillators as RF generators and other passive components. In a typical adaptation, electronic modules with pre-packaged devices on a PCB (printed circuit board) are further assembled onto a flex substrate that interfaces with the skin to receive sensor signals that pertain to biomarkers of interest. Further advances led to the entire electronic system on a flex substrate. This trend is schematically illustrated in Fig. 1. The flex substrate is made of free-standing polymer film carriers of PET (polyethylene terephthalate), LCP (Liquid Crystal Polymer), Polyimide or similar materials. The other emerging trend is to process substrate film layers on a temporary carrier and release them to transfer them onto skin as epidermal electronics for health-monitoring or human-machine interfaces [2]. They could also be thus made so flexible that they can be eventually rolled as mm-scale cylinders and pipes. Both of these shifts require high-density electronics integration in flexible substrates that could be bent or stretched without

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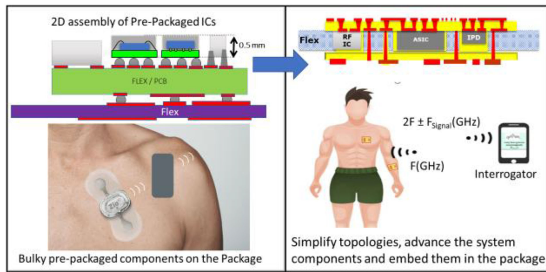

FIGURE 1. Trend towards thin flexible packages for wearable health-monitoring applications.

breaking or permanently losing electrical and structural integrity. Circuit components or devices are assembled onto flex substrates by solders or additively-deposited isotropic conductive adhesives. The off-chip interconnects are also formed through chip-first packaging as described later in this section. Additive manufacturing is typically utilized for forming the conductor traces on polymer flex substrates after suitable surface modifications for improved adhesion. In order to facilitate processing as free-standing carriers, the substrates should also be mechanically stable to make processing easy while being flexible enough for final use, and also enhance the interconnect reliability for high-density integration.

This section reviews the key advances in flexible sensor packaging and integration. In common flex package integration, devices are singulated and discretely-assembled with wirebonds or area-array bump interconnects to result in smaller interconnection lengths and pitch distances. The pitch and footprints of these devices have been continually scaling down to meet the miniaturization and high-density component integration needs [3]. The area-array bumps are formed with solders, isotropic or anisotropic conductive adhesives. Solders are assembled through mass reflow while thermocompression bonding is utilized for conductive adhesives. IC assemblies are often processed under high temperatures of above 200 °C. The substrate material should be stable at the processing temperatures. Assembly using interconnection materials that have high reflow temperatures on substrates and only tolerate low temperatures have been developed using innovative localized heating such as with photonic curing [4]. Higher interconnect density and thinner bumps generate larger stresses on the interconnections. The use of a dielectric gel as a gap-fill can enhance the flexibility by providing stress relief when bending at high curvatures or under thermal stress. Epoxies and silicones are the most common encapsulants. Adhesives such as silicone elastomers (ex., DOWSIL^{TM} 3-4207) protect the electronics and provide stress relief for interconnections under applied displacements. Hydrophobic fluoroelastomers are also utilized to encapsulate the flip-chip packaging structure to resist moisture permeation of embedded electronics under washing cycles. Key innovations in this area, which include printed thin-film multimodal sensors on flexible substrates, compatible process-flow of wiring and electronic component assembly with flexible circuits, and heterogeneous integration have been extensively reported [5]. The electronic interface designs that include communication protocols, power budgets for various wireless link options, power generation and storage are also provided in a recent review [6].

In spite of advances in chip-on-flex packaging with surface-assembled devices, it is imperative that embedded-die packaging in flex (or chip-in-flex) will have a key impact in future electronics. Die-embedding with chip-first assembly is emerging as a major alternative to existing flip-chip assembly technologies with thick solder joints. Embedding reduces the dimensions of the package as the entrenched chip has less of its volume protruding outwards. Embedded-die interconnects feature shorter interconnect length and, thus, superior electrical performance. Another key advantage for on-skin biophotonics arises because the components are flat and in intimate contact with the skin, resulting in better signal quality. Chip-in-flex packaging increases the flexibility of the package, resulting in lower stresses on the interconnects. Furthermore, embedding components into the substrate can allow for packages with simpler 3D architectures, reducing the number of layers required in the circuit design, and therefore result in thinner packages. Fan-out packaging is emerging as the key enabling technology for embedding chips [7]. In fan-out interconnection technologies, interconnections are directly formed from the chip pads to package traces without the need for solder or similar interconnections and assembly. In one such technology, chips are placed first, followed by the formation of the redistribution layers over the reconstituted chips as a molded wafer or a large panel [8]. In this approach towards chip-embedding with wafer-level fan-out packaging, chips are assembled on a temporary carrier while facing down (1st Handler) with a release tape, followed by encapsulation. This stack is now bonded to a second wafer. The release tape can be softened through heating in order to release the layers on the top. The devices on the 2nd Handler or processing wafer are now facing up, which facilitate the formation of redistribution layers that mimic back-end-of-the-line (BEOL). This involves planarization, with redistribution polymers and conductor traces. After, the wiring redistribution, the stack is removed from the 2nd handler and is ready to be integrated with the flex electrode arrays for biosignal recording. The resulting embedded-flex package can be so flexible that it can be rolled into small pipes. It should be noted that the majority of fan-out packaging is done with reconstituted molded wafers. However, chip-embedding in panels is also emerging as an alternative to fan-out wafer-level packaging. These approaches address several limitations of today's packages, such as additional thickness and electrical parasitics.

Interconnect materials in embedded-chip flex packages must meet the required fatigue reliability, and depending on the applications, should be processed at low temperature and cost with high-throughput. There is continued research into materials such as silver composites and metal nanowire elastomer composites which may be able to endure such events

without compromising function [9], [10]. Interconnection resistance is also lowered by mixing micro and nanoparticles in conductive adhesives. Evaluation with commercial inks suggest that the resistances reach <100 milliohms even with the initial formulations [11]. By combining silver nanoparticles with Isotropic Conductive Adhesives (ICAs) composed of 80% wt. silver micro-flakes, Han *et al.* successfully reduced electrical resistivity from 1.14 mΩ.cm to 0.137 mΩ.cm [12]. The silver nanoparticles were sintered at less than 250 °C to connect the silver micro-flakes to die pads, resulting in interconnections with shear strengths greater than 25 MPa which is comparable to assemblies done in traditional flip chip with solder. Nanofiber-based anisotropic conductive films (ACF) developed using conductive filler particles have been utilized to form interconnections with pitches smaller than 20 microns [13]. In-situ synthesis of silver nanowires is another key strategy to obtain inks with low viscosity. Appropriate material modifications are required to create the pseudoplastic shear properties for material flow. The nanowires or nanoparticles are mixed with polyurethane, vinyl polymer and silicone elastomers to encompass a wide range of material properties for the necessary elastomeric properties to achieve the targeted deformable interconnects. In one such approach, the polyurethane phase is created in-situ by the reaction between methylethylketoxime (MEKO) – blocked hexamethylene diisocyanate (HD) and polyethylene glycol (PEG) [14]. These wires are also processed into transparent and stretchable electronics [15].

The mechanical properties of conductive elastomer composites that are processed through additive manufacturing routes are widely studied. Silver-elastomer composites are developed to achieve a conductivity of ∼46000 S/cm with 70% strain [16]. In another study, the deformation of silver nanowire polyurethane composites was shown to be 786% before it ruptures [17]. Conductivity was retained up to 200% of stretching with 17.5 wt% silver nanowire loading. In order to demonstrate the package integration and system reliability, the nanowire composites are processed through subtractive photolithographic etching or additive patterning processes. In subtractive lithographic processing, relatively thinner structures are deposited as the nanowire film is first deposited through spin-coating processes [18]. Nanowire coatings on buckled polydopamine-modified porous polyurethane preform surfaces is known to create negative Poisson's ratio and a combination of high conductivity and high stretchability [19]. Although the conductivities were less than 20 S/cm, with no change in resistance after 1000 cycles to 80% strain. For an ideal stretchable conductor, the increase in the resistance after stretching should be low. The hysteresis in the resistance data during and after relaxing the substrate to its original length is related to its nonlinear strains. The next stage of evolution in fan-out additively-deposited flex package interconnects will rely on self-healing polymers, nanoscale conducting phases such as graphene and PEDOT-PSS. Multiple options are available to initiate crack-healing. These are classified as materials with microcapsules that can release healing agents when a crack propagates, vascular systems where certain hollow fibers or capillary tubes carry the healing agents to the crack opening, or intrinsic crack-healing structures that require an external trigger [20]. Thermal stimulation by heating to close the cracks has also been studied.

With the potential use in wearable and implanted medical devices, interconnection materials and the substrate should be able to withstand many instances of bending while maintaining resistance levels that allow the device to continue operating at max strain from bending without succumbing to large changes to overall resistance as a result. Flexible packages are, therefore, expected to undergo a host of stresses and strains from bending and other forms of mechanical deformations. Chip-on-flex samples experience lower von Mises stresses when bent due to complex mechanical coupling area between the chip and the substrate, as well as having fewer interfacial coupling interactions [21]. Chip-in-flex samples have uniform interfacial coupling interactions resulting in a more rigid core. The silicone gap fill acts akin to a compliant layer; the interaction between the core and the low modulus gap fill induces stress relaxation in the interconnections. The increase in resistance after bending is ascribed to the plastic deformation of the metal composite adhesives that form the interconnections. Conductive adhesives that do not suffer from high increases in resistance after undergoing mechanical stress would be ideal. This paper focuses on demonstrating embedding chips in flex substrates as a viable alternative to current flip-chip on flex technology. By doing so, it advances chip packaging to beyond traditional wafer-level packaging and emerging wafer fan-out packaging approaches, thereby creating the new additive embedded-chip fan-out flex manufacturing. Bending, temperature and humidity tests were conducted on both chip-on-flex and chip-in-flex samples for comparison. Lower or comparable increases in resistance as a result of the tests for the chip-in-flex in comparison to the chip-on-flex samples would suggest that embedding chips in flex is a viable alternative or even replacement for flip chip on flex technology.

II. EMBEDDED-CHIP PACKAGE STRUCTURE AND MECHANICAL MODELING

Modeling helps to perform parametric analysis of interconnection stresses and optimize the assembly stack, material, process and geometric design rules. In our earlier work, silver adhesive interconnects in chip-on-flex packages achieved lower interconnect stresses compared to chip-in-flex interconnects due to the weaker mechanical coupling between the chip and package [21] from thinner substrate and taller interconnections. Chip-on-flex interconnects are realized with a conventional flip-chip process using solder or silver adhesives. In this approach, copper traces that terminate with area-array pads are micropatterned on the surface of thin substrates. Components and devices are assembled onto the area-array terminations. The maximum von Mises stress in the substrate

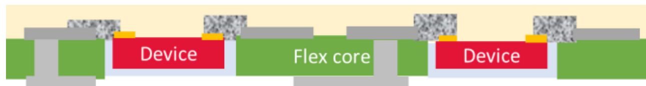

FIGURE 2. Embedded-chip interconnects for thin, flexible and potential 3D packages.

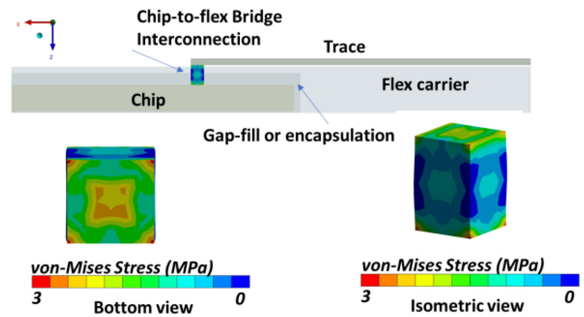

FIGURE 3. Bottom and isometric views of the chip-to-trace interconnect stress distribution with the embedded-chip packages.

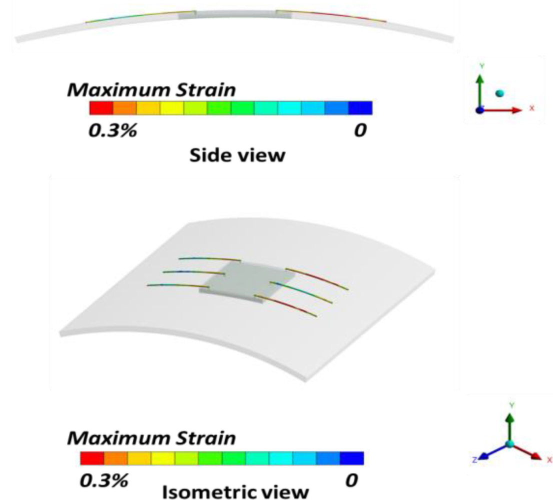

FIGURE 4. von Mises stress distribution in the copper trace interconnect with the embedded-chip packages.

is a strong function of its thickness. For example, when 12 mm bending was applied, these interconnects resulted in a maximum von Mises stress of 2.8 MPa. The effect of interconnect height is also analyzed for these interconnects. With lower interconnection heights, sometimes referred to as stand-off heights, the silver adhesives tend to deform more causing higher von Mises stresses on the substrate and interconnections. Higher standoff height decreases the von Mises stress of the silver adhesive interconnects. Based on initial analysis, von Mises stresses reduced by about 50% when taller interconnect height of 30 μm was used instead of 10 μm to [22]. A higher interconnection height offers lower von Mises stresses that act on the silver adhesives to offer better bending flexibility. An elastomer encapsulation that also acts as an underfill is another design and process modification that can reduce interconnection stresses.

The key approach that is developed in this paper is the embedded-chip fan-out interconnections. In this approach, devices are inserted into cavities inside flexible packages. Fan-out bridge connections are formed between the chip pads and copper traces through silver elastomer adhesive connections. Chip-in-flex package relies on a dielectric gap-fill in the flexible substrate and encapsulation to improve the overall mechanical integrity of the package and its ability to bend with lower thermomechanical stresses under low radius of curvatures. Chip-to-package traces consist of planar bridge connections that are directly printed through screen-printing. If the embedded devices are of different heights, the screen-printing process can readily accommodate the height differences. In this task, 3-D design models are constructed on ANSYS. Fourteen bodies have been constructed with ANSYS to model the assembled module. All the bodies are mechanical bonded at interfaces to avoid any tangential and normal movements of interfacial layers. The geometry of the package is shown in Fig. 2.

The models are designed with a package area of 20 x 20 mm^2. A 5 mm die with 50-micron thick peripheral pads, at 150 micron pitch are assumed to model the stresses in the fan-out interconnects. Viscoelastic silver adhesives provide interconnections between the chip pads and package copper traces. Elastomer PDMS encapsulation of 100 microns was added as encapsulant to reduce interconnection stresses. Elastic material properties for LCP are assumed as 3 GPa and 0.34 respectively. PDMS modulus and Poisson's ratio are assumed as 360 kPa and 0.5, while that of the silver interconnects are taken as 2.7 GPa and 0.37. In our model, silver interconnects and PDMS are further quantified by viscoelastic properties using the Prony method. Relative moduli α_i and relative time τ_i was used as inputs for Prony terms, illustrating the amount of stiffness lost at a given rate [23], [24]. PDMS properties are taken from Table 2 in Ref [24], while silver interconnect properties are assumed from Table A.2 in [23]. The model is setup to cool from the curing temperature of 120°C down to 27°C. The actual curing stresses are not incorporated in this analysis as it mostly aims at bending stresses. A fixed displacement is then imposed onto one side of the substrate, while the opposite end is clamped. The displacement is increased with a ramp-rate of 1mm/s. Large deformations range was enabled to model displacements of 12 mm over a 20 mm package. The mesh span angle center is chosen to be fine to set the goal for curvature. On the boundaries of the model, the mesh will subdivide in curved regions until each element of mesh spans the angle. These conditions allow the geometry to bend in 1-D to analyze flexibility from the subjected displacement.

Discretization was done with hexahedral and tetrahedral quadratic elements. High-density meshing was performed in the interconnect sub-structures to capture high fidelity in the stress distribution. The material details were also added. Fig. 3 and 4 show the von Mises strain distribution in the copper traces along with the stress distribution in the interconnections. The maximum strains are ~0.3% as shown in Fig. 4,

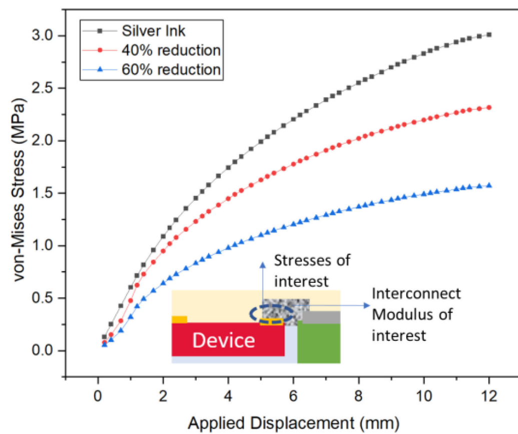

FIGURE 5. Maximum von Mises stress of chip-in-flex assemblies with different interconnection modulus.

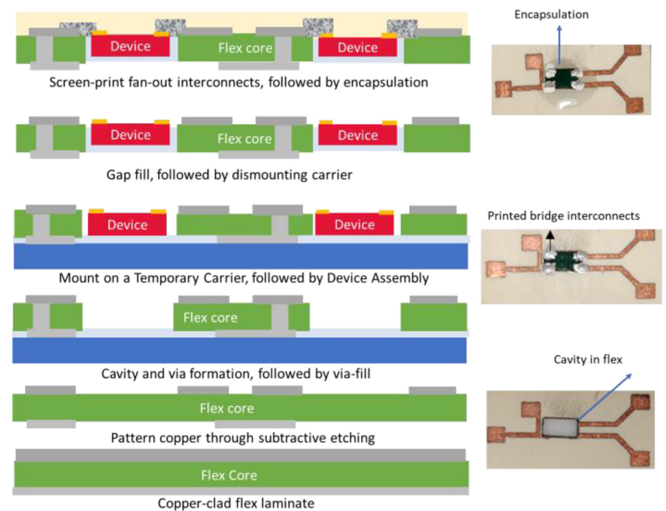

FIGURE 6. Process-flow for fabrication of embedded-chip interconnects.

which is same as the expected yield strain of copper. The von Mises stresses are also found to be less than the yield stress of plated fine-grained copper (~357 MPa) [25], [26]. It should be noted, however, that the yield stress of copper is sensitive to processing and grain structure. The effect of the modulus of silver-elastomer interconnect on the von Mises stresses in silver adhesives is summarized in Fig. 5. With a targeted 10 MPa adhesion strength that are observed with epoxy-based silver adhesives [27], the stresses of 2-3 MPa are low enough to ensure no mechanical failures during bending. When analyzing the stress build-up by the applied displacement from 1 – 15 mm, Fig. 5 indicates that reducing the modulus by 40% and 60% can correspondingly reduce the stresses by similar amounts. With silver nanowire interconnects, lower modulus can be achieved for the same higher conductivity. This can provide key opportunities for lowering the interconnect stresses and enhance the reliability during bending.

III. FABRICATION METHODS

Liquid crystal polymer (LCP) (ULTRALAM 3850HT) is utilized as the substrate material because of its strength, toughness, low moisture absorption, ability to integrate RF functions and several other benefits. The dielectric is manufactured with a thickness of 180 μm, and doublesided copper cladding of 17.5 μm thickness for the two outer layers. The LCP and other polymer films typically have low modulus and good dimensional stability making them flexible; their thin cores allow for smaller form factors for their packages. They also have low dielectric constant and loss, which makes them ideal for RF packaging with low-loss transmission lines, embedded mm wave components and high reliability.

Test-structure patterns were formed through subtractive patterning. Dry-film photolithography is performed on the doublesided copper-clad sheets with LCP core. Prior to chip-on-flex component assembly, the die pads of resistors were silverized using Nagase CI-1036 (Nagase ChemteX America Corporation) and cured twice for 10 minutes at 120 °C. To produce chip-on-flex samples, solder (Chipquik SMDLTLFP) and CI-1036 conductive silver ink were applied onto the copper pads of the substrates. Test resistors with resistances of less than 5 milliohms were then assembled onto the substrates to land their corresponding die pads on the appropriate copper pads using the BGA Rework Station (RW-SV550) by Shuttlestar. A nominal pressure was applied to ensure interconnection between the die and copper pads of the substrate; solder reflow and adhesive curing was performed using the same rework station.

The process flow for fabrication of embedded-chip interconnects is illustrated with test resistors as representative components in Fig. 6. To produce chip-in-flex samples, cavities were cut in the substrate using a CO_2 laser (M-300 Laser Engraving and Cutting System by Universal Laser Systems, Inc) in the dimensions of chips to be embedded. The resistors with die pads facing up were assembled into the cavity using adhesive strips. A silicone gap fill (DOWSIL^{TM} 3-4207 Dielectric Tough Gel Kit) was applied through a nozzle syringe, followed by curing at room temperature for 4 hours; this creates bridges on which interconnections can be formed. Using a screen-printer, bridge connections were made using silver-elastomer composites (CI – 1036), and cured twice at 120 °C for 10 minutes. After the fabrication of the substrates, the assembly was encapsulated (DOWSIL^{TM} 4207 Dielectric Tough Gel Kit), followed by curing at room temperature for 4 hours. The morphology of the silver particles in the fan-out interconnects is shown in Fig. 7. The optical cross-section of the image with embedded chip and fan-out interconnect from the chip termination pad to the package trace is also shown in the figure. Kelvin probe structures were utilized to extract the interconnect resistances. With these structures, current from 0.1 to 1A was applied from a DC source on one side and a Fluke 117 True RMS Multimeter was used to measure the voltages. The resistances were obtained by dividing the voltage drop with the current. To test the reliability of the fabricated samples, bending and temperature tests were conducted. The fabricated samples were bent over a radius of 10.5

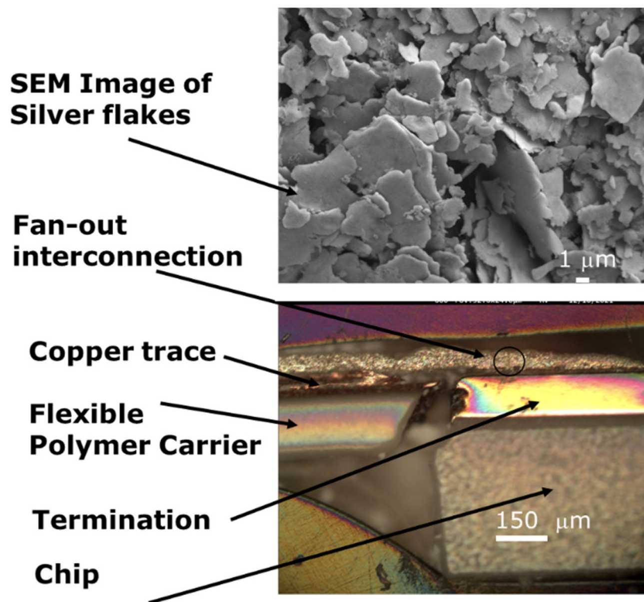

FIGURE 7. Cross-section optical image of chip with fan-out interconnections between the termination and copper trace. The test chip in this case is much thicker than the polymer flexible carrier. SEM image of the flake particles in the silver-polyurethane interconnect is also shown.

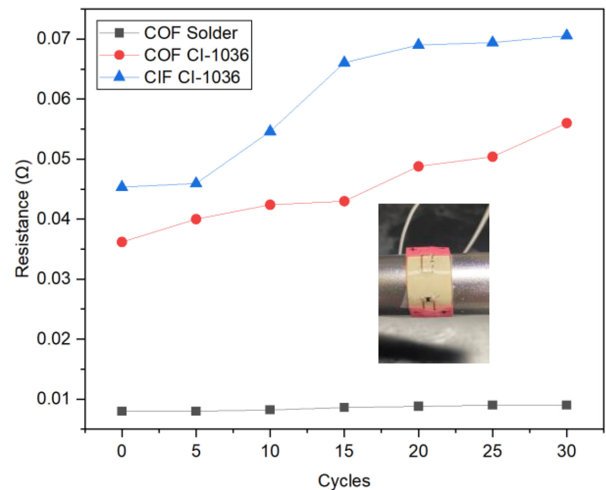

FIGURE 8. Average resistance of interconnects after 30 bending cycles for each type of assembly. Marginal increase in resistance is seen but no interconnect failures are noted.

cm for 3 seconds. The initial reliability test was performed for 30 cycles. To conduct the temperature test, the samples were treated at 90 °C for 24 hours. The resistances were measured before and after the reliability test.

IV. INTERCONNECT STABILITY

Thermal stability tests: The samples were initially stored at 90 °C for 24 hours. to replicate other encapsulation and assembly processes for subsequent layers. After the high-temperature storage, the average resistances for all the samples increased except for the control chip-on-flex (COF) samples with solder. This is expected as solder has more stable metallurgical bonding than conductive adhesives. For chip-in-flex (CIF) packages, the average resistances increased by a mere 3.7% (from 62.9 milliohms to 64.9 milliohms) after subjecting to 90 °C for 24 hours. This is comparable to the 5.2% increase with chip-on-flex samples using the same silver-elastomer interconnect. The stability can be further improved by utilizing devices with gold finish. This could not be performed in the current set of experiments because of the limitations of the off-the-shelf devices. Additionally, coating the die pads of chips with either gold or silver would lead to the formation of chemically stable and stronger bonds with the silver adhesives. This would mitigate the increases in resistance caused by bending. Gold is also more resistant to chemical changes caused by exposure to environmental conditions, which should further improve stability. By performing ENIG (electroless nickel – immersion gold) finish on the traces, the stability towards humidity can be further improved.

Bending tests: As the sample bends or flexes, it is subjected to a complex combination of forces that include tension, compression, and shear. For this reason, bend tests are commonly used to evaluate the response of packages to realistic loading situations. The mechanical bending test is additionally necessary for the flex-package as the target location undergoes constant movement that leads to bending, flexing and stretching. Since the targeted application is for wearable electronics with shorter product life-cycles, reliability for 30 bending cycles is deemed adequate as shown in other studies [28]. The fabricated embedded-chip flexible package prototypes were manually bent over a 10 cm radius cylinder. The resistance changes were measured before during and after the bending. After 10 cycles, chip-on-flex samples assembled using solder showed an increase in resistance of 5%, chip-on-flex samples assembled using CI-1036 silver conductive ink showed an increase in resistance by 20%, embedded samples showed an increase by about 30%. With 30 bending cycles, the resistance increased by about 50% but no failures were noted. The change in resistance with the number of bending cycles for different types of samples is shown in Fig. 8.

As Fig. 8 suggests, the interconnections showed higher increase in resistance for the embedded samples compared to chip-on-flex samples. Chip-in-flex assemblies experience higher von Mises stresses than flip-chip on flex assemblies. The stability in resistance to bending is related to the package flexibility, which results in lower stresses at the interconnects. Bending the samples causes peeling strains to accumulate between silver adhesive and the metal pads [29]. This reduces the interfacial contact with copper traces as found in similar studies. For traces on flexible substrates, the change in resistance is directly related to the strain in the interconnects [30].

In addition to this test, assemblies with components of different sizes and corresponding substrate designs with various geometries were performed. Embedding with larger devices showed more dramatic increase in resistance and

interconnect fractures. Assemblies with smaller chips would provide improved reliability as the decreased volume of rigid structures within the test structure would lower the strain accumulation at the interfaces. The interconnect modulus will have a significant role in the interfacial stresses as described in the modeling section (Fig. 5). Use of silver-elastomer adhesives tends to make interconnections more compliant. Nanowire thermoplastic conductive composites have greater stretchability and resistance to breaking.

Other design, material and process innovations are also effective in addressing the reliability of embedded-chip flexible packages for wearable electronics. Typical metal traces on flexible polymers undergo plastic deformation because the top surface is either under strong tension or compression. By incorporating a stack of materials, the neutral plane can be designed to reside in the sensitive metal circuit pattern. Additionally, the possibility of using conductive adhesives with self-healing mechanisms could secure more long-term use with built-in failure-resistant mechanisms. Conducting fillers with self-healing polymers that can invoke innovative crack-healing mechanisms are expected to further advance this research. Such smart packages will have a key role in future embedded-chip flexible sensor applications.

V. FUNCTIONAL VALIDATION WITH BIOPHOTONIC SYSTEMS

To demonstrate a functional prototype that employs the developed embedded-chip technology, a heartbeat sensor was fabricated with biophotonic components that are embedded inside the substrate. This application specifically benefits from embedding because of several reasons. The primary reason is that embedding provides a flat surface for the photonic components to make intimate contact with the skin. This achieves better signal quality at lower LED and detector power. Embedding also reduces the overall form factor of different systems and allows for the integration of more components into smaller volumes. The flat surfaces on either side allow the integration of other components in 3D multilayered packages. Furthermore, embedding also eliminates the need for vias to communicate signals from the LED and the photodetector on the skin-side to the other side. This has led to further simplification of the circuit. The system consists of a 120-Ohm 4020 packaged resistor, an SFH 2700 photodetector, and an 850nm VSMY5850X01 LED. The components are assembled with their die pads facing backside, allowing for interconnections to be made between pads and the copper traces of the substrate. The LED panel and the receiver of the photodetector face the skin-side of the substrate.

Human tissue allows for the electromagnetic waves in the near infrared (NIR) wavelengths to travel deep into the tissue. As the blood moves through the tissue, it produces sinusoidal-like photonic signals when it interacts with light. By measuring the intervals between peaks of these waves, the rate of heartbeat can be calculated. NIR spectroscopy is thus widely performed to characterize the pulse rate. The LED and the photodetector must be embedded and be able to perform without loss of function during and after many cycles of bending. Validation tests were performed to determine if the LED used was attuned to the correct range of wavelengths after assembly and was functioning as intended. These tests were repeated again after the sample was bent for 20 hours over a rod. Fig. 9 shows the spectroscopy results from the embedded-chip biophotonic package module. The figure also shows the device wrapped around a finger to collect oximeter measurements and further test the functionality of the device. The spectrometer recorded an intensity of 0.74 AU emitted by the LED at a wavelength of 899.7 nm before the sample was subjected to bending. After bending, the spectrometer recorded an intensity of 0.89 AU. The discrepancy in the intensities before and after bending is anticipated as factors such as the location of the LED in relation to the detector affects the intensity of the recorded readings. The structural differences in tissue at different locations reflect light at different intensities to the photodetector. Oximeter measurements demonstrate the functionality of the device. The results are stable with adequate signal-to-noise ratio as shown in Fig. 9.

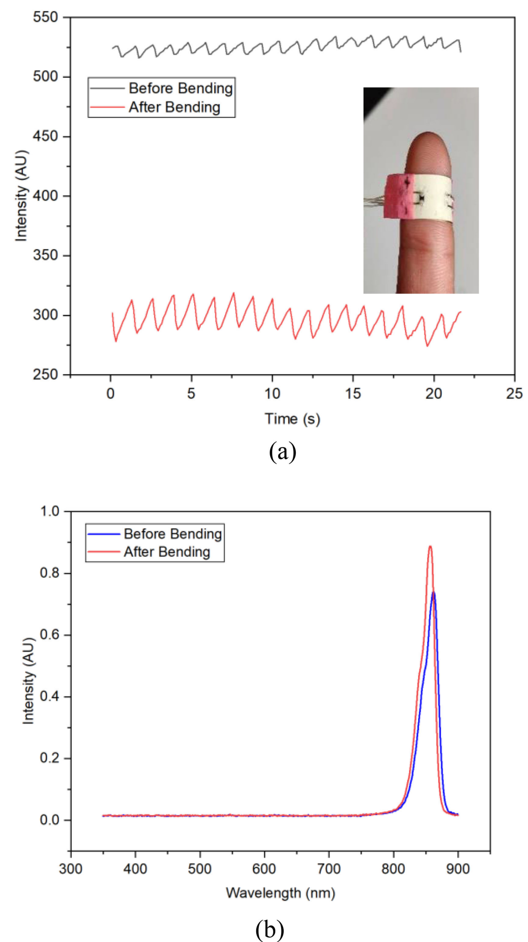

FIGURE 9. a) Intensity versus time measurements to characterize the pulse rate from the circulatory system. Measurements were performed before and after bending the sample. Inset shows a functional sample wrapped around the finger to collect readings of pulse per second before and after bending. b) Spectroscopy results before and after bending.

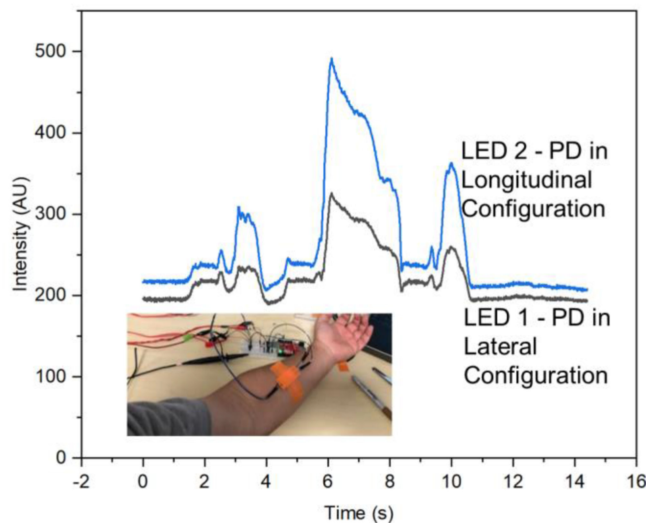

FIGURE 10. Monitoring of muscle-activity with embedded-chip LED and photodetectors (PD) in flex packages. The reduction in blood-flow during fist-closure is monitored to indicate muscle activity.

The flex package was also tested with human subjects during simple muscle activity. The results are compiled in Fig. 10 when the embedded-chip flex prototypes are mounted on the wrist to monitor the hemodynamics during hand-closure and opening. The response to changes in oxygenated hemoglobin and blood volumetric flow during the closure of fist are seen through voltage dip. Three individual LEDs are co-embedded along with a single photodetector and timed such that the performance can be individually monitored at different locations. Maximum change in signal of the backscattered light was observed when the LED and photodetector were longitudinally placed on the wrist (LED 2 in Fig. 10). When the light source and detector were laterally positioned on the wrist, the signal did not dramatically change during the muscle activity as seen in the figure. As shown in our earlier studies, once integrated with the operational amplifiers, the output voltage can drop by about 1000 mV with fist-closure, which is consistent with the hemodynamic models [21]. The outcome of this validation allows for the optimization of the circuit design with amplifier for photodetector and the driver for LED. The final circuit can then be designed to achieve high SNR and sensitivity.

VI. CONCLUSION

Embedded-flex fan-out packages are shown as the next key evolution in wearable medical devices. In this approach, devices and flex substrate are connected through planar printed interconnects with silver nanoflake elastomer adhesives. This new concept of flex packaging can eventually miniaturize future biophotonic systems. By reducing the interconnection length to less than 200 microns, this approach can eventually suppress the electrical parasitics and losses associated with them. Thermomechanical modeling is performed to show the reduction in interconnect stresses with interconnect materials of lower modulus. The flexible substrate, gap-fill material, and the conducting elastomer should eventually be co-designed to minimize the interconnect stresses to less than 1 MPa. By suitable surface finish of pads, the resistance increments during bending and high-temperature storage are managed to achieve high reliability for wearable medical devices

This package innovation is anticipated to bring major advances, leading to further miniaturization of biophotonic systems. The system performance is tested by measuring the output photocurrent pulses at an adjacent photodiode in the same flex package to monitor the heart rate. Initial measurements also confirmed responses to muscle activity as seen through changes in the backscattered light intensity during fist-closure. With planar bridge connections between the embedded photodiodes, no failures were seen with the new design approach. Bending of the flex packages didn't show significant increase in interconnect resistance because of the low stiffness of the flex and conductive elastomer interconnects. Stretchable nanowire or conducting polymer fillers in elastomer polymer matrices would further benefit the reliability of such systems.

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