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Transient Analysis of Hybrid Cu-CNT On-Chip Interconnects Using MRA Technique

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ABSTRACT This paper presents the transient analysis of the equivalent single conductor (ESC) model of hybrid Cu-CNT on-chip interconnects for nanopackaging using matrix rational approximation (MRA) modeling technique. The analysis of propagation delay and peak crosstalk noise is carried out for single and coupled Cu-CNT interconnect lines at 14 nm and 22 nm technology nodes. It has been observed that the proposed MRA model provides a speed-up factor of 131 compared to the HSPICE. An error of less than 1% confirms the accuracy of the proposed model compared to the SPICE simulations. It is observed that Cu-CNT lines are more immune to the crosstalk due to lesser coupling effects compared to Cu and CNT interconnects. The efficacy, accuracy, and comprehensive analysis using the proposed model ensures immense application possibility of the proposed model in the VLSI design automation tools at the nanopackaging level.

INDEX TERMS Carbon nanotubes (CNTs), crosstalk, copper-carbon nanotube (Cu-CNT), electromigration, equivalent single conductor (ESC) model, grain boundary scattering, matrix rational approximation (MRA), nanopackaging, on-chip interconnects, surface roughness scattering, propagation delay.

I. INTRODUCTION

During the past two decades, Copper (Cu) as a conventional on-chip interconnect material has been successfully fabricated with dual damascene metallization process using proper barriers such as Tantalum nitride (TaN) [1]. However, the VLSI integrated circuit (IC) chips' aggressive scaling increased the resistivity of the interconnects in nanopackaging applications [2]. The increase in resistance of aggressively scaled interconnects is due to grain boundary scattering, electromigration, and surface roughness scattering effects [3]. These effects need vigilant consideration during the on-chip nanopackaging interconnect design [4]. The aforementioned effects pose critical challenges and limitations for the conventional on-chip interconnect material beyond the 8 nm technology node [1]. Thus, researchers have to look for alternative solutions to this issue.

Carbon nanotubes (CNTs) gained a lot of interest due to their excellent electrical, thermal, mechanical, and optical properties that can overcome the major bottlenecks faced by Cu [5]–[8]. However, the metal-CNT contact resistance is a major drawback faced by CNTs in the nanopackaged interconnects [9]–[11]. This, in turn, proved to be a barrier for the possible implementation of CNTs in on-chip interconnect applications. The increased current density requirements for state-of-the-art technology nodes must be met by the on-chip interconnects somehow effectively and efficiently. Recent developments in copper-carbon nanotube (Cu-CNT) nanopackaging interconnects, present a credible solution while overcoming the discussed issues [12]–[20].

Efficient modeling of nanopackaged interconnect is vital for high-speed VLSI system [21]. The performance parameters of interconnects, namely, propagation delay and crosstalk, are central for the reliability and overall performance of state-of-the-art circuits and systems [22]. The analysis of these parameters is carried out, preferably in two ways, either by using the simulation techniques or by deriving the closed-form analytical expressions [23]. The simulation tools, such as SPICE, used to simulate interconnects provide accurate results using numerical integration and convolution methods. However, layout optimization is highly computationally expensive if one opts for these techniques [23], [24]. Thus, accurate analytical models of densely populated nanopackaged interconnects are required for their iterative layout designs and delay and crosstalk noise prediction. For this, analytical *RLC*

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models are necessary for the efficient modeling and analysis of contemporary high-speed interconnects. This area of development of fast analytical *RLC* models has been a very active research field presently.

The performance modeling and reliability analysis of CNT interconnects have been done by various researchers [6], [8], [25]–[27]. However, the electrical modeling of Cu lines blended with CNT bundles is an interesting emerging research area of the nanopackaging domain [14], [18]–[20]. It has been observed that Cu-CNT interconnects provide two-order higher ampacity when compared to Cu [12]. Thus, it becomes essential to explore the modeling of the Cu-CNT interconnect lines as well. This paper presents an equivalent single conductor (ESC) model of Cu-CNT interconnect lines, and to the best of authors' knowledge, for the first time employs the matrix rational approximation (MRA) technique to perform transient analysis of the ESC model of hybrid Cu-CNT on-chip interconnects. The modeling is based on approximating the exponential matrix of the Telegrapher's equations (TEs) for hybrid Cu-CNT interconnect lines using Padé approximation. The novelty in using this approach of approximating the exponential matrix component lies in the fact that a considerable reduction in CPU time expense using the proposed model is observed compared to the industry level HSPICE simulator for the nanopackaging technology nodes. Four different structures of these interconnects, namely, single, coupled-two, coupled-three, and coupled-four Cu-CNT lines, have been considered to analyze propagation delay and peak crosstalk noise at 14 nm and 22 nm technology nodes. The remaining paper is organized as follows. Section II explains the ESC model used for hybrid Cu-CNT interconnect structure. Section III presents the proposed MRA technique to model these interconnects. The results and discussion are presented in Section IV. Finally, Section V concludes the paper.

II. ESC MODEL OF HYBRID Cu-CNT INTERCONNECT

The CNTs filled within a Cu interconnect represents a Cu-CNT composite structure as shown in Fig. 1. CNT filling ratio (FR_{CNT}) is a key parameter during the design of a Cu-CNT interconnect line. It is defined as the ratio of total area occupied by CNTs to the total available cross-sectional area, which otherwise would have been entirely occupied by Cu if CNTs were absent. The filling ratio is expressed as,

$$FR_{CNT} = \frac{N_{FR_{CNT}} \pi (r + 0.155)^2}{A_{cross}} \tag{1}$$

where, $N_{FR_{CNT}}$ is the number of CNTs present inside the Cu-CNT cross-sectional area (A_{cross}) and r represents the radius (outermost if MWCNTs are present) of CNT. The value of CNT filling ratio can vary from 0 to 1, where '0' means no CNTs are present, that is, the available cross-sectional area is filled with Cu, and '1' means the entire available cross-sectional area is filled with CNTs. Theoretically, the value one of the CNT filling ratio indicates when the whole cross-sectional area is filled with only CNTs. However, for practical scenarios, the CNT filling ratio can be near one but

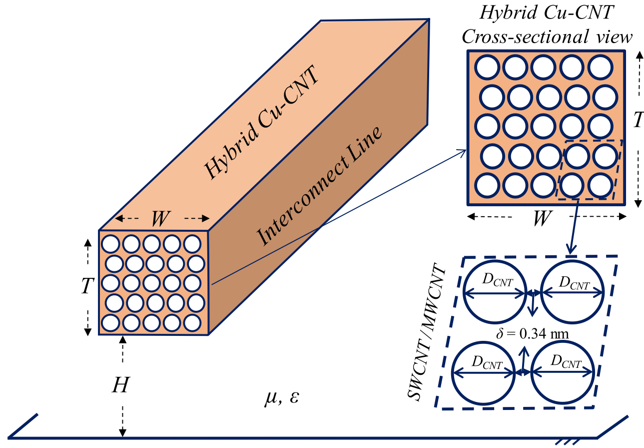

FIGURE 1. Hybrid Cu-CNT composite interconnect structure.

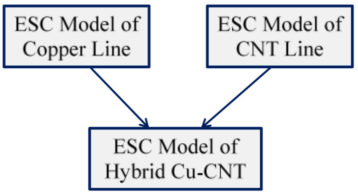

FIGURE 2. Block diagram to obtain the ESC model of Hybrid Cu-CNT line.

cannot be exactly equal to one since there are always certain areas between cylinders that cannot be filled with CNT. Moreover, if MWCNTs are present, then the MWCNT innermost radius is assumed to be half the value of the outermost radius, that is, $r_{inner} = r/2$ [28]. It is also important to note that the distance between Cu and carbon atoms in Cu-CNT composite is 0.155 nm [29].

The block diagram shown in Fig. 2 illustrates that the ESC model of a Cu-CNT line is obtained using the ESC model of Cu line and ESC model of CNT line. The resistance model of a Cu-CNT on-chip interconnect line is obtained by combining the resistance model of a Cu line and resistance model of a CNT line. The resistance model of Cu-line provides the equivalent per unit length (p.u.l.) resistance (R_{Cu}) of the Cu interconnect as

$$R_{Cu} = \frac{\rho_{Cu}}{(1 - FR_{CNT})WT} \tag{2}$$

where, ρ_{Cu} is the resistivity of Cu material [3], [20]; W and T represent width and thickness of the interconnect line, respectively. The resistance model of a CNT interconnect line represents the equivalent p.u.l. scattering resistance (R_{CNT}) of the CNT interconnect line. The resistance of a CNT interconnect is expressed as [27],

$$R_{CNT} = \frac{h}{4e^2 \sum_{i=1}^{N_{FR_{CNT}}} \lambda_i n_i} \tag{3}$$

where, h and e represent Planck's constant and electron charge, respectively; and λ_i, and n_i represent the mean free

path and number of conduction channels of i-th CNT present in the CNT bundle, respectively. The available number of total conducting channels in CNTs can be obtained using [25],

$$n_i = \begin{cases} k_0 & ; \text{for } D_{CNT} < \frac{5600\,[\text{nm.K}]}{T\,[\text{K}]} \\ k_1 D_{CNT} T + k_2 & ; \text{for } D_{CNT} \geq \frac{5600\,[\text{nm.K}]}{T\,[\text{K}]} \end{cases} \tag{4}$$

where k_0 is 2, 0 for metallic and semiconducting CNT, respectively. k_1 and k_2 are 3.26×10^{-4} nm^{-1} K^{-1} and 0.15, respectively, for metallic CNTs; and 3.26×10^{-4} nm^{-1}K^{-1} and -0.20, respectively, for semiconducting CNTs. In the present work, statistically one-third of the CNTs are considered as metallic ones.

The value of mean free path (λ_i) is obtained from [27] as,

$$\lambda_i = \frac{1}{(\lambda_{op,em,i}^{-1} + \lambda_{ap,i}^{-1} + \lambda_{op,ab,i}^{-1})} \tag{5}$$

The RHS of (5) is evaluated using the following steps:

$$\lambda_{op,em,i} = \frac{1}{(\lambda_{op,em,i}^{fld})^{-1} + (\lambda_{op,em,i}^{abs})^{-1}} \tag{6}$$

$$\lambda_{op,em,i} = \frac{1}{(\lambda_{op,em,i}^{fld})^{-1} + (\lambda_{op,em,i}^{abs})^{-1}} \tag{7}$$

where $\lambda_{op,em,i}$ is the mean free path (mfp) due to the emission of an optical phonon. This emission can take place either absorbing the electric field by an accelerated electron or by absorbing an optical phonon. The mfp due to the electric field is denoted by $\lambda_{op,em,i}^{fld}$, and the mfp due to the phonon absorption is denoted by $\lambda_{op,em,i}^{abs}$. Mathematically, $\lambda_{op,em,i}^{fld}$ is expressed as:

$$\lambda_{op,em,i}^{fld} = \frac{\hbar\omega_{op} - k_B T}{eV} l + \lambda_{op,i} \tag{8}$$

where the optical phonon energy is given by $\hbar\omega_{op}$; and k_B ,T, l, V denote the Boltzmann constant, temperature, line length, and voltage respectively. In (8), $\lambda_{op,i}$ denotes the spontaneous scattering length for emitting an optical phonon and it is mathematically expressed as:

$$\lambda_{op,i} = 112 r_i \left\{ \frac{1 + N_{op}(T)}{1 + N_{op}(300)} \right\}^{-1} \tag{9}$$

where r_i is radius of the CNT and $N_{op}(T)$ is number of phonons that obeys Bose-Einstein distribution relation and $N_{op}(T)$ is evaluated as:

$$N_{op}(T) = \left(e^{\frac{\hbar\omega_{op}}{k_B T}} - 1 \right)^{-1} \tag{10}$$

Mathematically, $\lambda_{op,em,i}^{abs}$ is expressed as:

$$\lambda_{op,em,i}^{abs} = \lambda_{op,i} + \lambda_{op,ab,i} \tag{11}$$

where

$$\lambda_{op,ab,i} = e^{\frac{\hbar\omega_{op}}{k_B T}} \lambda_{op,i} \tag{12}$$

TABLE 1. Comparison Among p.u.l. Resistances (Ω/μm)

Technology Node	Cu	CNT	Cu-CNT
14 nm	456.34	406.91	405.56
22 nm	408.16	384.27	321.37

where $\lambda_{op,ab,i}$ is the mfp of the charge carrier due to the absorption of the optical phonon.

$$\lambda_{ap,i} = \frac{2000 r_i}{(T/T_i)} \tag{13}$$

where $\lambda_{ap,i}$ denotes the mfp of the charge carrier due to the acoustic phonon.

As the Cu-CNT composite nanopackaging interconnect line's resistance model represents the parallel combination of resistance models of Cu and CNT interconnect lines, therefore, the p.u.l. resistance of the Cu-CNT composite resistance model (R_H) can be expressed as,

$$R_H = \frac{h\rho_{Cu}}{4e^2 \rho_{Cu} \sum_{i=1}^{N_{FR_{CNT}}} \lambda_i n_i + h(1 - FR_{CNT})WT} \tag{14}$$

The comparison among the p.u.l. resistances of Cu, CNT, and Cu-CNT interconnects at 14 nm and 22 nm are shown in Table 1. It shows that hybrid Cu-CNT lines have lesser resistance than the resistances of CNT and Cu interconnect.

In the ESC model of hybrid Cu-CNT interconnect, the resistance R_{FH} is present at both ends and it behaves as the lumped fixed resistance. It can be expressed as:

$$R_{FH} = \left[\sum_{i=1}^{N_{FR_{CNT}}} \left(\frac{h}{4e^2 n_i} + R_{tec,i} \right)^{-1} \right]^{-1} \tag{15}$$

where, $R_{tec,i}$ is contact resistance at tube-electrode interface, and $N_{FR_{CNT}}$ represents the tube count based on the filling ratio.

The p.u.l. inductance component (L_H) of Cu-CNT interconnect line consists of kinetic inductance (L_{KH}) and magnetic inductance (L_{MH}) parts. The p.u.l. inductance for a Cu-CNT on-chip interconnect is expressed as,

$$L_H = L_{KH} + L_{MH} \tag{16}$$

$$L_{KH} = \frac{h}{4e^2 v_f \sum_{i=1}^{N_{FR_{CNT}}} n_i} \tag{17}$$

$$L_{MH} = \mu\varepsilon [C_{EH}]^{-1} \tag{18}$$

where, v_f, μ, and ε denote the Fermi velocity of the charge carriers, permeability, and permittivity of the medium, respectively. The p.u.l. capacitance component (C_H) of Cu-CNT interconnect line consists of quantum capacitance (C_{QH}) and electrostatic capacitance (C_{EH}) parts. The quantum capacitance of Cu-CNT interconnect line is evaluated using the analytical expression,

$$C_{QH} = \frac{4e^2}{h v_f} \sum_{i=1}^{N_{FR_{CNT}}} n_i \tag{19}$$

FIGURE 3. (a) Coupled-*N* Hybrid Cu-CNT interconnect lines. (b) MTL network of Coupled-*N* Hybrid Cu-CNT conductors driven by *RC* drivers and capacitive loads.

The analytical expression for the evaluation of electrostatic capacitance of Cu-CNT nanopackaging interconnect is [18],

$$C_{EH} = \varepsilon\left[\frac{6}{\pi} + \frac{W}{H} + \frac{4}{\pi}\ln\left(1+\frac{T}{H}\right) + \frac{2}{\pi}\ln\left(1+\frac{0.5\pi W}{(1+\pi)(H+T)}\right)\right] \quad (20)$$

where H is the height of the hybrid Cu-CNT interconnect line above the ground plane. Further, if coupled lines are present as shown in Fig. 3, then the analytical expression for the evaluation of coupling capacitance of Cu-CNT interconnect line is [30],

$$C_{CH} = \varepsilon\left[\frac{3}{\pi} + \frac{T}{S} + \frac{2}{\pi}\ln\left(1+\frac{2W}{S}\right) + \frac{1}{\pi}\ln\left(1+\frac{\pi T}{(1+\pi)(S+2W)}\right)\right] \quad (21)$$

III. PROPOSED MRA TECHNIQUE

After providing a brief review to the Telegrapher's equations (TEs) of transmission lines (TLs), this section will present the proposed MRA technique that will be used to obtain the transfer function and transient response of nanopackaging hybrid Cu-CNT interconnects.

A. TEs FOR COUPLED RLC TLs

The hybrid Cu-CNT on-chip interconnects at nanometer technology nodes behave as TLs in nano regime. These TLs can be described using TEs as [31]:

$$\frac{\partial \boldsymbol{V}(x,s)}{\partial x} + s\boldsymbol{L_H}\boldsymbol{I}(x,s) + \boldsymbol{R_H}\boldsymbol{I}(x,s) = 0 \quad (22)$$

$$\frac{\partial \boldsymbol{I}(x,s)}{\partial x} + s\boldsymbol{C_H}\boldsymbol{V}(x,s) + \boldsymbol{G_H}\boldsymbol{V}(x,s) = 0 \quad (23)$$

where $\boldsymbol{R_H}$ is p.u.l. resistance matrix, $\boldsymbol{L_H}$ is p.u.l. inductance matrix, $\boldsymbol{C_H}$ is p.u.l. capacitance matrix, $\boldsymbol{G_H}$ is p.u.l. conductance matrix of hybrid Cu-CNT interconnect lines that are obtained using the ESC models described in Section II; x and s are position and Laplace-transform variables, respectively; $\boldsymbol{V}$ and $\boldsymbol{I}$ represent voltage and current vectors of TLs. As per the ITRS reports [1], due to the presence of inter-level dielectric (ILD) the conductance matrix becomes zero at all interconnect levels. Therefore, putting the value of $\boldsymbol{G_H}$ equal to zero, the modified form of (23) is given by:

$$\frac{\partial \boldsymbol{I}(x,s)}{\partial x} + s\boldsymbol{C_H}\boldsymbol{V}(x,s) = 0 \quad (24)$$

Equations (22) and (24) represent new set of TEs in frequency domain for coupled hybrid Cu-CNT on-chip *RLC* interconnects.

The solution to this new set of TEs represented by (22) and (24) in exponential form is expressed as:

$$\begin{bmatrix}\boldsymbol{V}(l,s)\\ \boldsymbol{I}(l,s)\end{bmatrix} = e^{\psi l}\begin{bmatrix}\boldsymbol{V}(0,s)\\ \boldsymbol{I}(0,s)\end{bmatrix} \quad (25)$$

with l being length of the TL and

$$\boldsymbol{\psi} = \begin{bmatrix} 0 & (\boldsymbol{R_H}+s\boldsymbol{L_H})\\ s\boldsymbol{C_H} & 0\end{bmatrix} \quad (26)$$

The exponential matrix term in (25) can be expressed in the form of cosine and sine hyperbolic functions as:

$$e^{\psi l} = \begin{bmatrix}\cosh\left(\sqrt{\boldsymbol{ZY}}\right) & Z_0\sinh\left(\sqrt{\boldsymbol{ZY}}\right)\\ Z_0^{-1}\sinh\left(\sqrt{\boldsymbol{YZ}}\right) & \cosh\left(\sqrt{\boldsymbol{YZ}}\right)\end{bmatrix} \quad (27)$$

with $\boldsymbol{Z_0} = \boldsymbol{Z}(\sqrt{\boldsymbol{YZ}})^{-1}$. Since no direct solution to (25) is available in time domain, it becomes difficult to perform the transient analysis of Cu-CNT interconnect lines in terms of propagation delay and crosstalk noise signals analytically. This problem is resolved by using the proposed MRA algorithm for hybrid Cu-CNT interconnects to obtain the transfer function.

B. PROPOSED MRA MODEL FOR HYBRID Cu-CNT INTERCONNECTS

This section presents the MRA algorithm which will be used to obtain the transfer function and analytical transient expression of hybrid Cu-CNT TLs. The basic approach behind MRA technique is to find predetermined coefficients of the approximated rational function that is obtained from the exponential term of (25) [23]. The matrix rational approximation of (25) gives:

$$\begin{bmatrix} \boldsymbol{V}(l,s) \\ \boldsymbol{I}(l,s) \end{bmatrix} \approx \frac{\boldsymbol{P}(\boldsymbol{\psi} l)}{\boldsymbol{P}(-\boldsymbol{\psi} l)} \begin{bmatrix} \boldsymbol{V}(0,s) \\ \boldsymbol{I}(0,s) \end{bmatrix} \tag{28}$$

where $\boldsymbol{P}(\psi l)$ and $\boldsymbol{P}(-\psi l)$ represent the polynomial matrices and are expressed as:

$$\boldsymbol{P}(\boldsymbol{\psi} l) = \sum_{k=0}^{P} \frac{P!(2P-i)!}{(P-1)!(2P)!} (\boldsymbol{\psi} l)^k \tag{29}$$

$$\boldsymbol{P}(-\boldsymbol{\psi} l) = \sum_{k=0}^{P} \frac{P!(2P-i)!}{(P-1)!(2P)!} (-\boldsymbol{\psi} l)^k \tag{30}$$

where P represents the Padé order. The polynomial matrices $\boldsymbol{P}(\psi l)$ and $\boldsymbol{P}(-\psi l)$ are divided into four sub-block matrices in order to obtain the approximated cos hyperbolic and sin hyperbolic functions of (27) and are shown by (31) and (32).

$$\boldsymbol{P}(\boldsymbol{\psi} l) = \begin{bmatrix} \boldsymbol{P}_{11} & \boldsymbol{P}_{12} \\ \boldsymbol{P}_{21} & \boldsymbol{P}_{22} \end{bmatrix} \tag{31}$$

$$\boldsymbol{P}(-\boldsymbol{\psi} l) = \begin{bmatrix} \boldsymbol{P}_{11} & -\boldsymbol{P}_{12} \\ -\boldsymbol{P}_{21} & \boldsymbol{P}_{22} \end{bmatrix} \tag{32}$$

The values of $\boldsymbol{P}_{11}, \boldsymbol{P}_{12}, \boldsymbol{P}_{21}$, and $\boldsymbol{P}_{22}$ are obtained using (33), (34), (35), and (36), respectively.

$$\boldsymbol{P}_{11} = \sum_{k=0}^{P} \frac{P!(2P-i)!}{2!(P-1)!(2P)!} \left(1+(-1)^k\right) l^k (\boldsymbol{ZY})^{0.5k} \tag{33}$$

$$\boldsymbol{P}_{12} = \sum_{k=0}^{P} \frac{P!(2P-i)!}{2!(P-1)!(2P)!} \left(1+(-1)^k\right) l^{2k} (\boldsymbol{ZY})^{0.5k} \boldsymbol{Z} \tag{34}$$

$$\boldsymbol{P}_{21} = \sum_{k=0}^{P} \frac{P!(2P-i)!}{2!(P-1)!(2P)!} \left(1+(-1)^k\right) l^{2k} (\boldsymbol{YZ})^{0.5k} \boldsymbol{Y} \tag{35}$$

$$\boldsymbol{P}_{22} = \sum_{k=0}^{P} \frac{P!(2P-i)!}{2!(P-1)!(2P)!} \left(1+(-1)^k\right) l^k (\boldsymbol{YZ})^{0.5k} \tag{36}$$

The matrix rational approximations are obtained using (28), (29), and (30) for the cos hyperbolic and sin hyperbolic terms present in (27). The obtained rational approximations are given by (37-40).

$$\cosh\left(\sqrt{\boldsymbol{ZY}}\right) = \boldsymbol{A}^{-1}\boldsymbol{B}_{11} = \boldsymbol{B}_{11}\boldsymbol{A}^{-1} \tag{37}$$

$$\boldsymbol{Z}_0 \sinh\left(\sqrt{\boldsymbol{ZY}}\right) = \boldsymbol{A}^{-1}\boldsymbol{B}_{12} = \boldsymbol{B}_{12}\boldsymbol{A}^{-1} \tag{38}$$

$$\boldsymbol{Z}_0^{-1} \sinh\left(\sqrt{\boldsymbol{YZ}}\right) = \boldsymbol{A}^{-1}\boldsymbol{B}_{21} = \boldsymbol{B}_{21}\boldsymbol{A}^{-1} \tag{39}$$

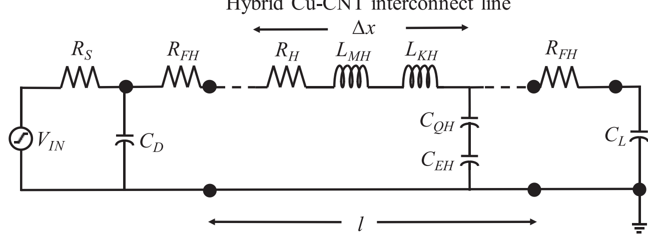

FIGURE 4. DIL structure of hybrid Cu-CNT interconnect.

$$\cosh\left(\sqrt{\boldsymbol{YZ}}\right) = \boldsymbol{A}^{-1}\boldsymbol{B}_{22} = \boldsymbol{B}_{22}\boldsymbol{A}^{-1} \tag{40}$$

where $\boldsymbol{B}_{11}$, $\boldsymbol{B}_{12}$, $\boldsymbol{B}_{21}$, $\boldsymbol{B}_{22}$, and $\boldsymbol{A}$ represent polynomial matrices that are defined as:

$$\boldsymbol{B}_{11} = \boldsymbol{P}_{22}\boldsymbol{P}_{11} + \boldsymbol{P}_{12}\boldsymbol{P}_{21} \tag{41}$$

$$\boldsymbol{B}_{12} = \boldsymbol{P}_{22}\boldsymbol{P}_{12} + \boldsymbol{P}_{12}\boldsymbol{P}_{22} \tag{42}$$

$$\boldsymbol{B}_{21} = \boldsymbol{P}_{11}\boldsymbol{P}_{21} + \boldsymbol{P}_{21}\boldsymbol{P}_{11} \tag{43}$$

$$\boldsymbol{B}_{22} = \boldsymbol{P}_{11}\boldsymbol{P}_{22} + \boldsymbol{P}_{21}\boldsymbol{P}_{12} \tag{44}$$

$$\boldsymbol{A} = \boldsymbol{P}_{11}\boldsymbol{P}_{22} - \boldsymbol{P}_{12}\boldsymbol{P}_{21} \tag{45}$$

It is important to observe that analytical expressions for rational approximations are obtained in (37–40) in the forms of predetermined coefficients present in (29) and (30) and line parasitics. This fact is going to be highly useful in obtaining analytical transient expressions for DIL structures of Cu-CNT interconnects.

Consider next a hybrid Cu-CNT interconnect line of length l driven by a CMOS driver modeled as $R_S C_D$ equivalent and it is terminated with capacitive load (C_L) as shown in Fig. 4. The lumped contact resistance is shown by the symbol R_{FH}, whereas the p.u.l. line parameters are shown by the symbols R_H, L_{MH}, L_{KH}, C_{QH}, and C_{EH}. The output voltage, V_O, at the load end can be expressed in the frequency domain as:

$$\boldsymbol{V_O} = \begin{pmatrix} \boldsymbol{D}\cosh\sqrt{\boldsymbol{ZY}} + \boldsymbol{E}\sinh\sqrt{\boldsymbol{ZY}} \\ +\boldsymbol{F}\sinh\sqrt{\boldsymbol{YZ}} + \boldsymbol{H}\cosh\sqrt{\boldsymbol{YZ}} \end{pmatrix}^{-1} \boldsymbol{V_{IN}} \tag{46}$$

with

$$\boldsymbol{D} = \left(1 + s\boldsymbol{R_S C_D} + s\boldsymbol{R_{FH} C_L} + s^2\boldsymbol{R_S R_{FH} C_D C_L}\right) \tag{47}$$

$$\boldsymbol{E} = \begin{pmatrix} \boldsymbol{R_S} + \boldsymbol{R_{FH}} + s\boldsymbol{R_{FH}^2 C_L} + s\boldsymbol{R_S R_{FH} C_D} + s\boldsymbol{R_S R_{FH} C_L} \\ +s^2\boldsymbol{R_S R_{FH}^2 C_D C_L} \end{pmatrix} \tag{48}$$

$$\boldsymbol{F} = \left(s\boldsymbol{C_L} + s^2\boldsymbol{R_S C_D C_L}\right) \tag{49}$$

$$\boldsymbol{H} = \left(s\boldsymbol{R_S C_L} + s\boldsymbol{R_{FH} C_L} + s^2\boldsymbol{R_S R_{FH} C_D C_L}\right) \tag{50}$$

The MRA-based frequency domain expression of V_O is obtained by substituting (37-40) into (46) and it is given as:

$$\boldsymbol{V_O} = \left(\boldsymbol{D}\boldsymbol{B}_{11}\boldsymbol{A}^{-1} + \boldsymbol{E}\boldsymbol{B}_{12}\boldsymbol{A}^{-1} + \boldsymbol{F}\boldsymbol{B}_{21}\boldsymbol{A}^{-1} + \boldsymbol{H}\boldsymbol{B}_{22}\boldsymbol{A}^{-1}\right)^{-1} \boldsymbol{V_{IN}} \tag{51}$$

Next, the MRA expression of (51) when converted into residues and poles yields,

$$V_O = \left(\sum_{k=1}^{2P+2} \frac{r_k}{s - p_k} \right) V_{IN} \tag{52}$$

Observe that (52) contains (2P+2) number of poles, P being the order of Padé approximation. The 2P poles are due to (37-40), one pole is due to driver capacitance and the other pole is due to load capacitance. The time domain expression is obtained by taking the Laplace inverse of (52) and it is given by (55) and (56) corresponding to saturated rising and falling ramp input signals expressed in (53) and (54) with rising time , falling time, and supply voltage as T_{rise}, T_{fall}, and V_{DD}, respectively.

$$V_{IN_R}(s) = \frac{V_{DD}}{T_{rise}} \left(\frac{1}{s^2} - \frac{e^{-sT_{rise}}}{s^2} \right) \tag{53}$$

$$V_{IN_F}(s) = \frac{V_{DD}}{s} - \frac{V_{DD}}{T_{fall}} \left(\frac{1}{s^2} - \frac{e^{-sT_{fall}}}{s^2} \right) \tag{54}$$

$$\begin{aligned} v_{o_r}(t) = &-\frac{V_{DD}}{T_{rise}} \sum_{k=1}^{2P+2} \left(\frac{r_k}{p_k} t + \frac{r_k}{p_k^2} (1 - e^{p_k t}) \right) u(t) \\ &+ \frac{V_{DD}}{T_{rise}} \sum_{k=1}^{2P+2} \left(\begin{array}{l} \frac{r_k}{p_k}(t - T_{rise}) \\ + \frac{r_k}{p_k^2}(1 - e^{p_k (t - T_{rise})}) \end{array} \right) u(t - T_{rise}) \end{aligned} \tag{55}$$

$$\begin{aligned} v_{o_f}(t) = &V_{DD} \sum_{k=1}^{2P+2} \left(\frac{r_k}{p_k} e^{p_k t} - \frac{r_k}{p_k} \right) u(t) \\ &+ \frac{V_{DD}}{T_{fall}} \sum_{k=1}^{2P+2} \left(\frac{r_k}{p_k} t + \frac{r_k}{p_k^2} (1 - e^{p_k t}) \right) u(t) \\ &- \frac{V_{DD}}{T_{fall}} \sum_{k=1}^{2P+2} \left(\begin{array}{l} \frac{r_k}{p_k}(t - T_{fall}) \\ + \frac{r_k}{p_k^2}(1 - e^{p_k (t - T_{fall})}) \end{array} \right) u(t - T_{fall}) \end{aligned} \tag{56}$$

IV. RESULTS AND DISCUSSION

This section presents the proposed MRA model's implementation to the ESC network of hybrid Cu-SWCNT interconnect lines at 14 nm and 22 nm nanopackaging technology nodes. The filling ratio for the Cu-CNT composite is considered as 0.2 [12]. The implementation is carried out using MATLAB R2020b software. The obtained results are compared using industry-standard HSPICE simulator. Four different structures have been considered to ensure the proposed MRA model's robustness and efficacy in Cu-CNT lines. The first considers a single Cu-CNT interconnect line with width, thickness, and height as 22 nm, 22 nm, and 50 nm, respectively. The values of the evaluated p.u.l. line resistance, inductance, and capacitance using the procedure described in Section II are 65.56 Ω/μm, 0.17 nH/μm. and 0.05 fF/μm, respectively. The value of fixed resistance is 150.42 Ω. The line length is 10 μm.

TABLE 2. Driver and Load Resistance and Capacitance Values (from ITRS Data)

Tech node	Rd (kΩ)	Cd (fF)	Cl (fF)
14nm	18.33	0.03	0.065
22nm	16.67	0.049	0.14

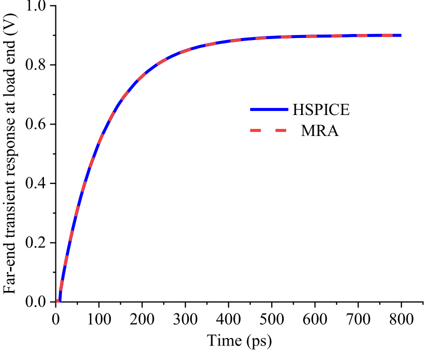

FIGURE 5. Far-end transient response at load end of single (22 nm x 22 nm) hybrid Cu-CNT line for 22 nm technology node.

TABLE 3. Cu-CNT Interconnects - Accuracy and Simulation Time

Number of sections	Delay (ps)			CPU Time (ms)		
	SPICE	MRA	% Error	SPICE	MRA	Speed-up
20	60.34	90.28	33.16	1.06	0.88	1.20
50	70.29	90.28	22.14	3.25	0.88	3.69
80	81.37	90.28	9.87	6.83	0.88	7.76
110	90.29	90.28	0.01	9.10	0.88	10.34
140	90.29	90.28	0.01	19.23	0.88	21.85
170	90.29	90.28	0.01	29.47	0.88	33.49

The driver and load values are in accordance with the 22 nm technology node shown in Table 2. The transient plots obtained using MRA and SPICE for a rising input signal with a rise time ($t_r = 0.1$ ps) are shown in Fig. 5. The Padé order is one. It is observed that the results match precisely with the industry level SPICE simulator. The propagation delay obtained using the SPICE simulator is 90.29 ps, whereas the propagation delay using the proposed MRA model is 90.28 ps, giving rise to an error of less than 0.5%. Furthermore, the CPU time consumed using the proposed model is 0.88 ms, and the CPU time consumed using SPICE is 9.10 ms providing a speed-up by a factor of 10.34 using the proposed MRA model. The line length 10 μm is now distributed into several shorter sections, and corresponding results for the propagation delay for each distribution are obtained using the industry level SPICE simulator. The number of sections, accuracy, and simulation time are presented in Table 3. The SPICE results values are compared with the results values of the MRA model. It has been observed that the lesser are the number of sections for the interconnect line, the faster is the computational speed of the SPICE simulator at the cost of reduced accuracy.

The second structure considers coupled-two Cu-CNT interconnect lines with width, thickness, height, and spacing as 22 nm, 22 nm, 50 nm, and 22 nm, respectively. The values of

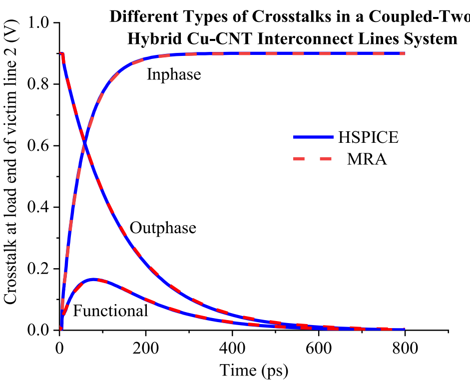

FIGURE 6. Different types of crosstalks in coupled-two (22 nm × 22 nm) hybrid Cu-CNT lines at 22 nm technology node.

TABLE 4. Comparing the Accuracy of Proposed MRA Model with SPICE W-Element Model for Coupled-Two Cu-CNT Lines

Type of Crosstalk	50% delay (ps) (Victim Line2)		Type of Crosstalk	Peak crosstalk (mV) (Victim Line2)	
	MRA	SPICE		MRA	SPICE
Inphase	42.14	42.15	Functional	165.18	165.19
Outphase	84.97	84.98			

the p.u.l. line parasitics and the fixed resistance are evaluated using the procedure described in Section II. The obtained values are:

$$R_H = \begin{bmatrix} 65.56 & 0 \\ 0 & 65.56 \end{bmatrix} \Omega/\mu m;$$

$$L_H = \begin{bmatrix} 0.1707 & 0.0001 \\ 0.0001 & 0.1707 \end{bmatrix} nH/\mu m;$$

$$C_H = \begin{bmatrix} 0.1004 & -0.0484 \\ -0.0484 & 0.1004 \end{bmatrix} fF/\mu m;$$

$$R_{FH} = \begin{bmatrix} 150.42 & 0 \\ 0 & 150.42 \end{bmatrix} \Omega$$

The line length is 50 μm in this case. The driver and load values are in accordance with the 22 nm technology node, as shown in Table 2. The rise time of the input signal is 1 ps. The transient plots obtained using the proposed MRA model and HSPICE simulations are shown in Fig. 6. These plots include the results corresponding to dynamic in-phase crosstalk, dynamic outphase crosstalk, and functional crosstalk. The results are tabulated in Table 4. It is observed that the results obtained match closely with the industry level SPICE simulator and lie within 1% error. Further, the CPU time consumed using proposed model for coupled-two hybrid Cu-CNT interconnect lines is 3.10 ms and the CPU time consumed using SPICE for coupled-two hybrid Cu-CNT interconnect lines is 10.20 ms. It can be seen that a speed-up of a factor of 3.3 is obtained using the proposed MRA model. The Padé order is two in this second example. The proposed MRA model can be tuned by increasing or decreasing the Padé order depending on the inputs based on the line length and rise time.

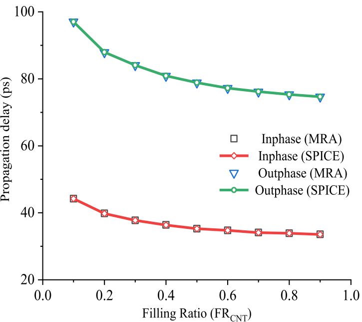

FIGURE 7. Dynamic crosstalks vs. Filling Ratio (FR_{CNT}) in coupled-two (14 nm x 14 nm) hybrid Cu-CNT lines at 14 nm technology node.

The effect of the filling ratio (FR_{CNT}) variation on the dynamic crosstalk is also illustrated with the help of Fig. 7. Next, the range of kinetic inductance and temperature are considered from 8–120 nH/μm and 300–500 K, respectively [17], [20]. The impact of these variations is analyzed on the inphase and outphase switching in coupled-two Cu-CNT interconnect lines, and the results are compared with the SWCNT lines network. It is observed that an increase in kinetic inductance and temperature values increases the delay in both the networks, as shown in Figs. 12 and 13. However, the Cu-CNT lines offer lesser delay in comparison to the SWCNT line.

The results for the inphase and outphase switching at the far-end of victim line 2 are shown in Table 5 and Table 6, respectively, using the proposed model and the industry-level SPICE simulator. An excellent accuracy between the proposed model results and industry-level SPICE simulator has been obtained with less than 1% error.

The third structure considers a coupled-four hybrid Cu-CNT interconnect lines with dimensions in accordance with 14 nm technology node. The spacing between each interconnect 14 nm. The values of the p.u.l. line parasitics are evaluated using the procedure described in Section II. The obtained values are,

$$R_H = \begin{bmatrix} 189.87 & 0 & 0 & 0 \\ 0 & 189.87 & 0 & 0 \\ 0 & 0 & 189.87 & 0 \\ 0 & 0 & 0 & 189.87 \end{bmatrix} \Omega/\mu m;$$

$$L_H = \begin{bmatrix} 0.41758 & 0.00014 & 0.00005 & 0.00003 \\ 0.00014 & 0.41758 & 0.00011 & 0.00005 \\ 0.00005 & 0.00011 & 0.41758 & 0.00014 \\ 0.00003 & 0.00005 & 0.00014 & 0.41758 \end{bmatrix} nH/\mu m;$$

$$C_H = \begin{bmatrix} 0.07963 & -0.04002 & -0.00043 & -0.00000 \\ -0.04002 & 0.11922 & -0.03958 & -0.00043 \\ -0.00043 & -0.03958 & 0.11922 & -0.04002 \\ -0.00000 & -0.00043 & -0.04002 & 0.07963 \end{bmatrix} fF/\mu m;$$

$$R_{FH} = \begin{bmatrix} 368.27 & 0 & 0 & 0 \\ 0 & 368.27 & 0 & 0 \\ 0 & 0 & 368.27 & 0 \\ 0 & 0 & 0 & 368.27 \end{bmatrix} \Omega$$

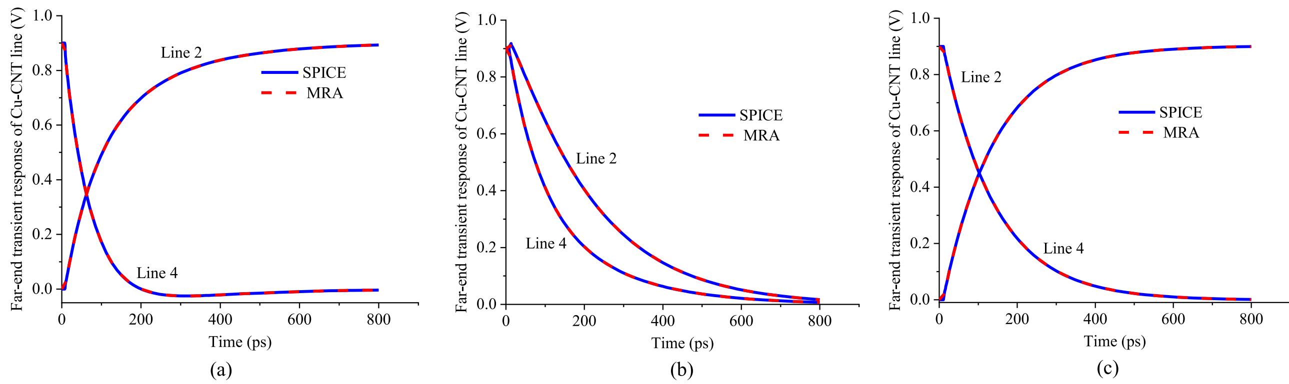

FIGURE 8. Transient responses corresponding to coupled-four hybrid Cu-CNT interconnect lines at 14 nm technology node. Far-end transient response at Line 2 and Line 4 of Hybrid Cu-CNT network for (a) ↑ ↑ ↓ ↓ input switching (b) ↑ ↓ ↑ ↓ input switching (c) ↑ ↓ ↓ ↑ input switching.

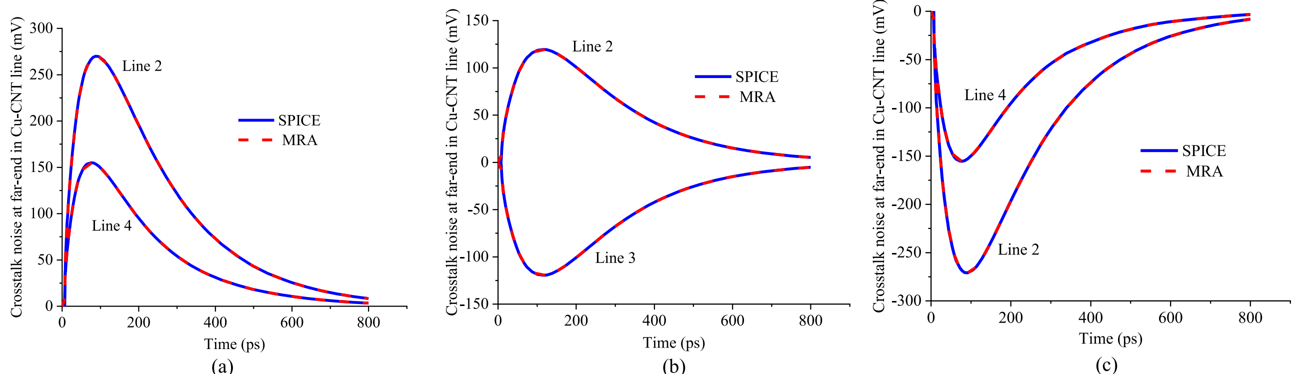

FIGURE 9. Far-end crosstalk noise transient response of coupled-four Hybrid Cu-CNT network at (a) Line 2 and Line 4 for ↑ 0 ↑ 0 input switching (b) Line 2 and Line 3 for ↑ 00 ↓ input switching (c) Line 2 and Line 4 for ↑ 0 ↓ 0 input switching at 14 nm technology node.

TABLE 5. Inphase Switching Delay (ps) Comparison Between Cu-CNT and SWCNT Interconnects

Interconnect line	Kinetic Inductance (L_K) (nH/μm)	T_1 = 300K		T_2 = 400K		T_3 = 500K	
		Proposed	SPICE	Proposed	SPICE	Proposed	SPICE
Cu-CNT	L_{K1} = 8	489.51	489.50	512.20	512.21	541.26	541.26
	L_{K2} = 64	492.67	492.67	515.18	515.19	544.10	544.09
	L_{K3} = 120	496.83	496.84	518.21	518.20	546.42	546.42
SWCNT	L_{K1} = 8	520.85	520.86	536.42	536.42	562.48	562.49
	L_{K2} = 64	523.49	523.48	539.67	539.68	566.32	566.33
	L_{K3} = 120	527.67	527.66	542.89	542.90	569.51	569.52

The line length is 100 μm. The driver and load values are following ITRS reports, as shown in Table 2. The rise time of the input signal is 1 ps. The transient plots obtained for different input switching scenarios using the proposed MRA model and HSPICE simulations are shown in Fig. 8 and Fig. 9. Table 7 includes the results for propagation delay that corresponds to different input switching scenarios. Table 8 contains the results for functional crosstalk that corresponds to different input switching scenarios. It can be seen from Table 7 and Table 8 that the results of the proposed MRA model match very closely with the HSPICE simulations. The Padé order is three. The CPU time consumed using the proposed model for coupled-four hybrid Cu-CNT interconnect lines is 28 ms while the CPU time consumed using SPICE for coupled-four hybrid Cu-CNT interconnect lines is 47 ms, ensuring that the proposed MRA model always remains faster than the industry level SPICE simulator.

This paper presents the transient analysis of hybrid Cu-CNT interconnects using the proposed MRA model. Further, it shows the advantages that the MRA technique offers in the modeling of these lines. Besides, the simulation results have also been carried out for other interconnect structures, namely, coupled-two Cu lines and coupled-two SWCNT bundle lines at the 22 nm technology node, as shown in Fig. 10. The line length considered for each interconnect line is 50 μm. Line 1 is active line with saturated rising ramp input signal and line

TABLE 6. Outphase Switching Delay (ps) Comparison Between Cu-CNT and SWCNT Interconnects

Interconnect line	Kinetic Inductance (L_K) (nH/µm)	T_1= 300K		T_2 = 400K		T_3 = 500K	
		Proposed	SPICE	Proposed	SPICE	Proposed	SPICE
Cu-CNT	L_{K1} = 8	1403.03	1403.02	1473.18	1473.19	1560.24	1560.23
	L_{K2} = 64	1407.12	1407.13	1476.59	1476.60	1563.05	1563.05
	L_{K3} = 120	1411.36	1411.36	1479.65	1479.64	1566.10	1566.11
SWCNT	L_{K1} = 8	1723.71	1723.72	1790.24	1790.24	1882.03	1882.03
	L_{K2} = 64	1726.86	1726.85	1793.13	1793.14	1884.91	1884.92
	L_{K3} = 120	1729.66	1729.65	1797.28	1797.29	1887.79	1887.80

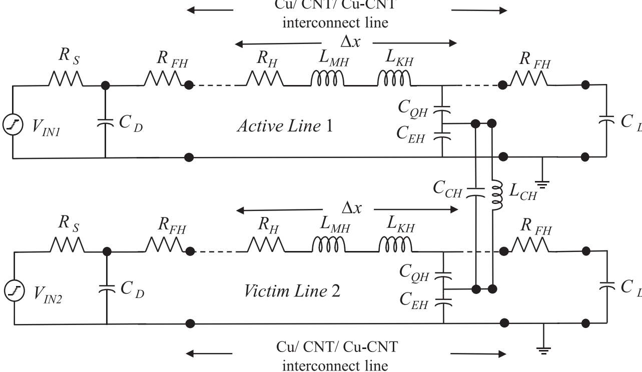

FIGURE 10. Coupled-two Cu/SWCNT bundle/hybrid Cu-CNT interconnect lines.

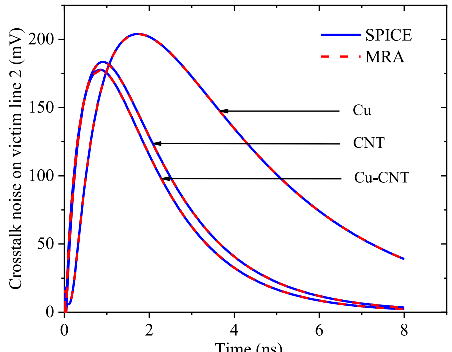

FIGURE 11. Peak crosstalk noise on far-end of Victim line2 at 22 nm technology node for coupled-two Cu, SWCNT bundle, and hybrid Cu-CNT interconnect lines.

TABLE 7. Comparing the Accuracy of Proposed MRA Model with SPICE W-Element Model in Coupled-Four Cu-CNT Lines

Input Switching Scenarios	50% delay (ps)							
	(Line1)		(Line2)		(Line3)		(Line4)	
	MRA	SPICE	MRA	SPICE	MRA	SPICE	MRA	SPICE
↑↑↑↑	40.58	40.58	40.58	40.58	40.58	40.58	40.58	40.58
↑↓↑↓	103.29	103.30	155.71	155.72	201.96	201.97	75.24	75.25
↑↑↓↓	54.05	54.06	102.83	102.83	74.41	74.42	40.98	41.00
↑↓↓↑	118.63	118.64	88.39	88.40	88.39	88.40	118.63	118.64

2 is quiet victim line. The results for the peak crosstalk noise at the far-end of victim line 2 in Fig. 10 are compared with coupled-two hybrid Cu-CNT interconnects with 0.2 filling ratio [12], [17] and are shown in Fig. 11. The proposed MRA

TABLE 8. Accuracy of Proposed MRA Model With SPICE W-Element Model For Victim Lines in Coupled-Four Cu-CNT Interconnects

Input Switching Scenarios	Maximum crosstalk (mV)			
	(Line2)		(Line4)	
	MRA	SPICE	MRA	SPICE
↑0↑0	269.96	269.98	154.89	154.90
↑0↓0	25.85	25.86	-142.62	-142.63
↓0↑0	-26.05	-26.06	143.74	143.75
↓0↓0	-271.00	-271.02	-155.37	-155.38

TABLE 9. CPU Time Expense (min) of Proposed Model and SPICE

Line-length (cm)	Proposed (minutes)	Conventional [23] (minutes)	SPICE (minutes)	Speed-up
0.5	3.6	395	432	120
1	5.4	605	648	120
1.5	6.6	815	864	131
2	8.4	953	1080	128

model results and SPICE simulations match very-well. The peak crosstalk noise at the far end of the victim line 2 for Cu, CNT, and Cu-CNT networks are 203.98 mV, 183.48 mV, and 177.75 mV, respectively. These results show that hybrid Cu-CNT interconnects lines are more immune to crosstalk noise than the CNT and Cu interconnect lines networks due to the lesser capacitive coupling effects in Cu-CNT lines. These results regarding crosstalk analysis further strengthen the candidacy of Cu-CNT interconnect lines over CNT and Cu interconnects in the nano regime.

The fourth example considers coupled-three Cu-CNT lines. The proposed model is implemented at larger interconnect lengths and is parameterized to incorporate the effects due to the surface roughness variations of the dielectric in which the hybrid Cu-CNT interconnect is placed. The dielectric surface roughness range is considered from 10–180 pm [32]. The entire 1-D grid for dielectric surface roughness variation is divided into 180 grid points. A 1-D Legendre polynomial function is used for the parameterization of the proposed model. The comparison of the computational CPU time expense between the proposed model, conventional MRA [23], and SPICE at varying line lengths are shown in Table 9.

Further, the results using the proposed model and SPICE at an interconnect line length of 0.5 cm at three distinct points at the far-end of line 1 and line 2 for input switching (↑ 0 ↑) are shown in Figs. 14 and 15, respectively, at 14 nm technology node. The propagation delay (line 1 and line 3) and peak crosstalk (line 2) at surface roughness values 10 pm, 90 pm, and 180 pm using the proposed model and SPICE are

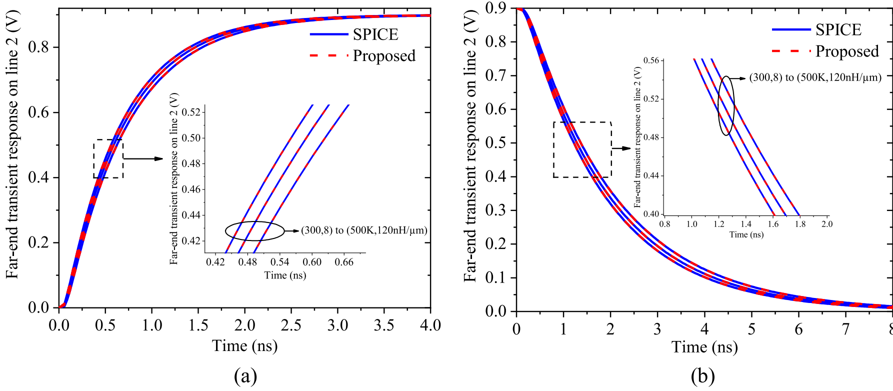

FIGURE 12. Far-end transient responses on line 2 corresponding to Cu-CNT at 22 nm technology node for (a) Inphase switching (b) Outphase switching.

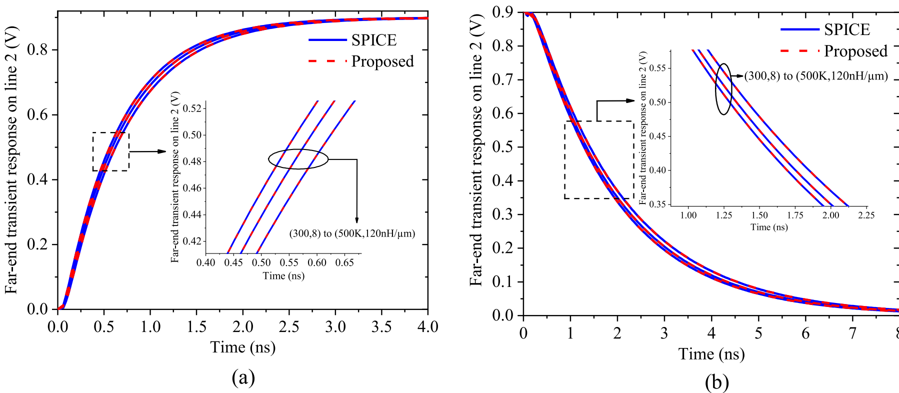

FIGURE 13. Far-end transient responses on line 2 corresponding to SWCNT at 22 nm technology node for (a) Inphase switching (b) Outphase switching.

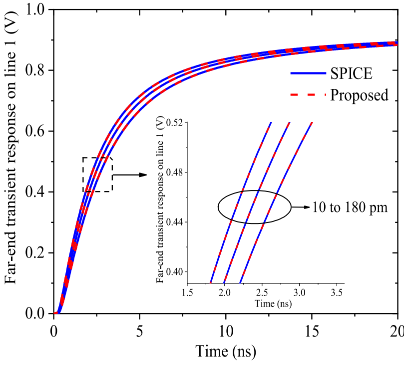

FIGURE 14. Far-end transient responses on line 1 corresponding to Cu-CNT at 14 nm technology node for input switching (↑ 0 ↑) for dielectric surface variations from 10–180 pm.

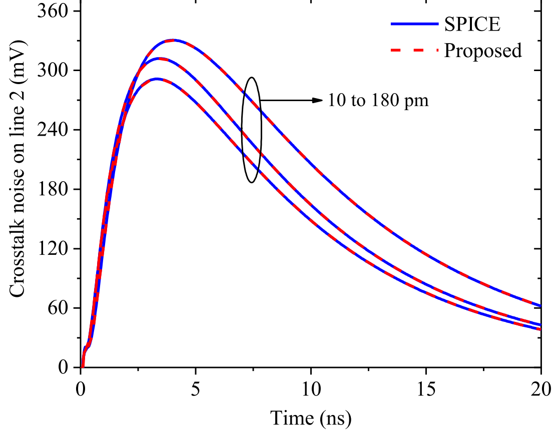

FIGURE 15. Crosstalk on line 2 corresponding to Cu-CNT at 14 nm technology node for input switching (↑ 0 ↑) for dielectric surface variations from 10–180 pm.

tabulated in Table 10. An error less than 1% is seen from the proposed model results and SPICE simulations, ensuring the proposed model's excellent accuracy. It has been observed that the propagation delay and peak crosstalk increases with the increase in dielectric surface roughness (DSR) value.

V. CONCLUSION

This paper presented a robust and efficient MRA model used in the transient analysis of the ESC model of hybrid Cu-CNT nanopackaged interconnects. It is observed that the MRA model provides the key performance parameters fastly than the industry-level SPICE simulator. A maximum speed-up

TABLE 10. Coupled-Three Cu-CNT Interconnects – Signal Integrity Parameter Analysis For Different Dielectric Surface Roughness

Signal integrity parameter	Δ_{SR} = 10 pm		Δ_{SR} = 90 pm		Δ_{SR} = 180 pm	
	Proposed	SPICE	Proposed	SPICE	Proposed	SPICE
Propagation Delay on Line 1 (ns)	2.1433	2.1432	2.3521	2.3521	2.6029	2.6028
Peak crosstalk on Line 2 (mV)	291.36	291.36	312.06	312.05	330.54	330.53
Propagation Delay on Line 3 (ns)	2.1432	2.1432	2.3521	2.3520	2.6030	2.6030

factor of 131 has been obtained using the proposed model compared to SPICE. The MRA results and SPICE simulations match very well with an error of less than 1% , thereby, ensuring the proposed MRA model's excellent accuracy. Its efficacy and accuracy ensure its immense possibility in the VLSI design automation tools to analyze hybrid Cu-CNT nanopackaging interconnects. The crosstalk noise in coupled hybrid Cu-CNT interconnects network is compared with the Cu and CNT-based networks using the proposed model and SPICE simulations. The results obtained show that coupled hybrid interconnects structures are more immune to the crosstalk due to lesser coupling effects than other interconnects, and therefore strengthening their candidacy for future nanopackaged interconnects. The impact of the DSR variations in Cu-CNT interconnects are analyzed by parameterizing the proposed model using Legendre polynomial function resulting in an excellent accuracy.

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REFERENCES

[1] International technology roadmap for semiconductors (ITRS-2015) reports. [Online]. Available: http://www.itrs2.net/itrs-reports.html

[2] A. Pyzyna *et al.*, "Resistivity of copper interconnects at 28 nm pitch and copper cross-sectional area below 100 nm2," in *Proc. IEEE Int. Interconnect Technol. Conf.*, 2017, pp. 1–3.

[3] J. M. Roberts, A. P. Kaushik, and J. S. Clarke, "Resistivity of sub-30 nm copper lines," in *Proc. IEEE Int. Interconnect Technol. Conf. IEEE Mater. Adv. Metallization Conf.*, 2015, pp. 341–344.

[4] "IEEE international roadmap for devices and systems report," 2017. [Online]. Available: https://irds.ieee.org/roadmap-2017

[5] Q. Lu, Z. Zhu, Y. Yang, and R. Ding, "Analysis of propagation delay and repeater insertion in single-walled carbon nanotube bundle interconnects," *Microelectron. J.*, vol. 54, pp. 85–92, Aug. 2016.

[6] S. Subash, J. Kolar, and M. H. Chowdhury, "A new spatially rearranged bundle of mixed carbon nanotubes as VLSI interconnection," *IEEE Trans. Nanotechnol.*, vol. 12, no. 1, pp. 3–12, Jan. 2013.

[7] A. Naeemi and J. D. Meindl, "Compact physical models for multiwall carbon-nanotube interconnects," *IEEE Electron Device Lett.*, vol. 27, no. 5, pp. 338–340, May 2006.

[8] A. Kumar, V. R. Kumar, and B. K. Kaushik, "Transient analysis of crosstalk induced effects in mixed CNT bundle interconnects using FDTD technique," *IEEE Trans. Electromagn. Compat.*, vol. 61, no. 5, pp. 1621–1629, Oct. 2019.

[9] A. Mishra, H. Gossner, and M. Shrivastava, "ESD behavior of MWCNT interconnects—Part I: Observations and insights," *IEEE Trans. Device Mater. Reliab.*, vol. 17, no. 4, pp. 600–607, Dec. 2017.

[10] A. Mishra and M. Shrivastava, "ESD behavior of MWCNT interconnects—Part II: Unique current conduction mechanism," *IEEE Trans. Device Mater. Reliab.*, vol. 17, no. 4, pp. 608–615, Dec. 2017.

[11] A. A. Vyas, C. Zhou, and C. Y. Yang, "On-chip interconnect conductor materials for end-of-roadmap technology nodes," *IEEE Trans. Nanotechnol.*, vol. 17, no. 1, pp. 4–10, Jan. 2018.

[12] C. Subramaniam *et al.*, "One hundred fold increase in current carrying capacity in a carbon nanotube-copper composite," *Nature Commun.*, vol. 4, Jul. 2013, Art. no. 2202.

[13] Y. Feng and S. L. Burkett, "Modeling a copper/carbon nanotube composite for applications in electronic packaging," *Comput. Mater. Sci.*, vol. 97, pp. 1–5, Feb. 2015.

[14] L. Ladani, "The potential for metal–carbon nanotubes composites as interconnects," *J. Electron. Mater.*, vol. 48, no. 1, pp. 92–98, Jan. 2019.

[15] L. Ladani , "Copper-CNT hybrid TSVs: Thermo-mechanical stresses and reliability analysis," *Int. J. High Speed Electron. Syst.*, vol. 24, no. 03n04, 2015, Art. no. 1550006.

[16] I. Awad and L. Ladani, "Mechanical integrity of a carbon nanotube/copper-based through-silicon via for 3D integrated circuits: A multi-scale modeling approach," *Nanotechnology*, vol. 26, no. 48, Nov. 2015, Art. no. 485705.

[17] W. Zhao *et al.*, "High-frequency analysis of Cu-carbon nanotube composite through-silicon vias," *IEEE Trans. Nanotech.*, vol. 15, no. 3, pp. 506–511, May 2016.

[18] Z. Cheng *et al.*, "Investigation of copper–carbon nanotube composites as global VLSI interconnects," *IEEE Trans. Nanotechnol.*, vol. 16, no. 6, pp. 891–900, Nov. 2017.

[19] Q. Lu, Z. Zhu, Y. Yang, R. Ding, and Y. Li, "Electrical modeling and analysis of Cu-CNT heterogeneous coaxial through-silicon vias," *IEEE Trans. Nanotechnol.*, vol. 16, no. 4, pp. 695–702, Jul. 2017.

[20] K. Fu, J. Zheng, W.-S. Zhao, Y. Hu, and G. Wang, "Analysis of transmission characteristics of copper/carbon nanotube composite through-silicon via interconnects," *Chin. J. Electron.*, vol. 28, no. 5, pp. 920–924, Sep. 2019.

[21] J. M. Rabaey, A. Chandrakasan, and B. Nikolic, *Digital Integrated Circuits – A Design Perspective*, 2nd ed. Pearson, 2016.

[22] X. C. Li, J. F. Mao, and M. Swaminathan, "Transient analysis of CMOS-gate-driven RLGC interconnects based on FDTD," *IEEE Trans. Comput. Des. Integr. Circuits Syst.*, vol. 30, no. 4, pp. 574–583, Apr. 2011.

[23] A. Dounavis, R. Achar, and M. Nakhla, "Passive macromodels for distributed high-speed networks," *IEEE Trans. Microw. Theory Tech.*, vol. 11, pp. 1686–1696, Oct. 2001.

[24] R. Achar and M. S. Nakhla, "Simulation of high-speed interconnects," *Proc. IEEE*, vol. 89, no. 5, pp. 693–728, May 2001.

[25] A. Maffucci, F. Micciulla, A. E. Cataldo, G. Miano, and S. Bellucci, "Modeling, fabrication, and characterization of large carbon nanotube interconnects with negative temperature coefficient of the resistance," *IEEE Trans. Compon., Packag. Manuf. Technol.*, vol. 7, no. 4, pp. 485–493, Apr. 2017.

[26] M. D'Amore, M. S. Sarto, and A. Tamburrano, "Fast transient analysis of next-generation interconnects based on carbon nanotubes," *IEEE Trans. Electromagn. Compat.*, vol. 52, no. 2, pp. 496–503, May 2010.

[27] M. Sahoo, P. Ghosal, and H. Rahaman, "Modeling and analysis of crosstalk induced effects in multiwalled carbon nanotube bundle interconnects: An ABCD parameter-based approach," *IEEE Trans. Nanotechnol.*, vol. 14, no. 2, pp. 259–274, Mar. 2015.

[28] H. J. Li, W. G. Lu, J. J. Li, X. D. Bai, and C. Z. Gu, "Multichannel ballistic transport in multiwall carbon nanotubes," *Phys. Rev. Lett.*, vol. 95, no. 8, Aug. 2005, Art. no. 86601.

[29] Y. Matsuda, W.-Q. Deng, and W. A. Goddard, "Contact resistance for 'end-contacted' metal−graphene and metal−nanotube interfaces from quantum mechanics," *J. Phys. Chem. C*, vol. 114, no. 41, pp. 17845–17850, Oct. 2010.

[30] W. Zhao, X. Li, S. Gu, S. H. Kang, M. M. Nowak, and Y. Cao, "Field-based capacitance modeling for sub-65-nm on-chip interconnect," *IEEE Trans. Electron Devices*, vol. 56, no. 9, pp. 1862–1872, Sep. 2009.

[31] C. R. Paul, *Analysis of Multiconductor Transmission Lines*, 2nd ed. Wiley-IEEE Press, 2007.

[32] M. Sanaeepur, "Dielectric surface roughness scattering limited performance of MLGNR interconnects," *IEEE Trans. Electromagn. Compat.*, vol. 61, no. 2, pp. 532–537, Apr. 2019.

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