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Guest Editorial: Nanopackaging Part I

This is the first of two Special Sections on Nanopackaging. This first one has appeared in OJ-NANO Vol. 2, 2021 and the second will appear in Vol. 3, 2022. Electronics packaging is a very multidisciplinary activity requiring an understanding of Electrical, Mechanical, Materials, Thermal (and Thermomechanical) Engineering, and of the underlying Physics and Chemistry. The papers in these two Special sections will reflect this diversity, and the application of modern mathematical algorithms and computational techniques to advance the engineering design techniques. Nanopackaging could refer to the packaging of possibly disruptive nanoelectronics technologies, and this would undoubtedly be a challenging and useful field, but so far, the term has been applied more to the application of nanotechnologies to microelectronics packaging. Although this is the case with some of the papers in this collection, two are particularly driven by the packaging needs of the continuation of Moore's Law into advanced nanoscales.

The first paper "Performance Enhancement of Large Crossbar Resistive Memories with Complementary and 1D1R-1R1D RRAM Structures," K. Lahbacha *et al.* [A1], deals with electrothermal issues in nanoscale resistive RAM (RRAM) arrays and demonstrates an innovative solution based an architectural and materials modifications. The simulations demonstrate that significantly lower temperatures are achieved in individual cells, which then improve the performance and reliability of crossbar arrays. Although the specific study is at the device level, it is essentially an interconnect problem with implications for the crossbar array interconnections.

In the review paper, "Advanced 3D Integration Technologies in Various Quantum Computing Devices," P. Zhao *et al.* [A2], classical electronics packaging concepts are indeed applied to nanoelectronic devices, in this case the quantum computer. As in many electronic systems, the obvious problem is thermal dissipation, and since quantum computers must be maintained at cryogenic temperatures to function, these quantum systems are subject to similar constraints as nanoscale 3D microelectronics. The paper reviews the application of electronics packaging techniques to four distinct quantum computing technologies: trapped ion qubits, (the authors' own field,) superconducting circuit qubits, silicon spin qubits, and photon qubits.

Driven by the ever-increasing miniaturization and integration density of electronic devices, there is an unquenchable need for new materials to solve the increasingly severe thermal management issues. The rise of new packaging technologies and novel heterogeneous system-in-package integration strategies also rely on new, advanced packaging, support, and interconnect materials. Since their discovery a couple of decades ago, the allotropes of carbon, such as graphene and carbon nanotubes (CNTs), are considered wonder materials with high expectations for their many favourable properties. Owing to our growing understanding of their physical properties and the recent development in more reliable fabrication technologies, their application in nanopackaging areas is steadily increasing. In their timely review, the Todri-Sanial group gives an excellent overview of their utilization for interconnects, flexible electronics, and thermal management in "Graphene and Carbon Nanotubes for Electronic Nanopackaging," G. Boschetto *et al.* [A3].

In this special section on nanopackaging, a couple of papers are included that focus on interconnect related issues. Both papers deal with signal and power integrity issues that primarily occur due to the transistor dimensions in the nanometer range. The paper titled "Machine Learning Techniques for Modeling and Performance Analysis of Interconnects" J. N. Tripathis *et al.* [A4], presents an overview of applications of ML techniques to various aspects of interconnects such as design, optimization, modeling and variability analysis. The paper also discusses the need for reducing computational efforts for design and analysis of interconnects in the nanometer regime. The second paper titled "Efficient Selection and Placement of In-Package Decoupling Capacitors using Matrix-Based Evolutionary Computation" A. Jain *et al.* [A5], discusses a problem of in-package decoupling capacitor optimization. The decoupling capacitors in a high-speed system are used to suppress noise generated due to faster switching devices designed in nanometer ranges. The paper presents a faster computational approach for efficient selection and placement of decoupling capacitors by a recently introduced matrix based evolutionary optimization technique.

ATTILA BONYAR, *Guest Editor*
Budapest University of Technology and Economics
1111, Budapest, Hungary

BRAJESH KUMAR KAUSHIK, *Guest Editor*
Indian Institute of Technology-Roorkee
Roorkee 247 667, India

JAMES E. MORRIS, *Guest Editor*
Portland State University
Portland OR 97201, USA

APPENDIX
RELATED WORKS

[A1] K. Lahbacha, F. Zayer, H. Belgacem, W. Dghais, and A. Maffucci, "Performance enhancement of large crossbar resistive memories with complementary and 1D1R-1R1D RRAM structures," *IEEE Open J. Nanotechnol.*, vol. 2, pp. 111–119, 2021, doi: 10.1109/OJNANO.2021.3124846.

[1] James E. Morris (editor) "Nanopackaging: Nanotechnologies in Electronics Packaging" (Springer) 2nd Edition (2018) ISBN: 978-3-319-90361-3

[A2] P. Zhao, Y. D. Lim, H. Y. Li, L. Guidoni, and C. S. Tan, "Advanced 3D integration technologies in various quantum computing devices," *IEEE Open J. Nanotechnol.*, vol. 2, pp. 101–110, 2021, doi: 10.1109/OJNANO.2021.3124363.

[A3] G. Boschetto, S. Carapezzi, and A. Todri-Sanial, "Graphene and carbon nanotubes for electronic nanopackaging," *IEEE Open J. Nanotechnol.*, vol. 2, pp. 120–128, 2021, doi: 10.1109/OJNANO.2021.3127652.

[A4] J. N. Tripathi, H. Vaghasiya, D. Junjariya, and A. Chordia, "Machine learning techniques for modeling and performance analysis of interconnects," *IEEE Open J. Nanotechnol.*, vol. 2, pp. 178–190, 2021, doi: 10.1109/OJNANO.2021.3133325.

[A5] A. Jain, H. Vaghasiya, and J. N. Tripathi, "Efficient selection and placement of in-package decoupling capacitors using matrix-based evolutionary computation," *IEEE Open J. Nanotechnol.*, vol. 2, pp. 191–200, 2021, doi: 10.1109/OJNANO.2021.3133213.