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Advanced 3D Integration Technologies in Various Quantum Computing Devices

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ABSTRACT As a key approach to augment Moore's Law scaling, 3D integration technologies have enabled small form factor, low cost, diverse, modular and flexible assembly of integrated circuits in the semiconductor industry. It is therefore essential to adopt these technologies to the quantum computing devices which are at the nascent stage and generally require large scale integration to be practical. In this review, we focus on four popular quantum bit (qubit) candidates (trapped ion, superconducting circuit, silicon spin and photon) which are encoded by distinct physical systems but all intrinsically compatible with advanced CMOS fabrication process. We introduce the specific scalability bottlenecks of each qubit type and present the current solutions using 3D integration technologies. We evaluate and classify these technologies into three main categories based on the hierarchy. A brief discussion regarding the thermal management is also provided. We believe this review serves to provide some useful insights on the contributions of interconnect, integration and packaging to the field of quantum computing where rapid development is ongoing.

INDEX TERMS 3D integration, 3D packaging, TSV, flip-chip, ion trap, superconducting circuit, silicon spin, silicon photonics, quantum computing.

I. INTRODUCTION

With the slowdown of transistor node scaling in the past decade, advanced three-dimensional (3D) integration technologies have been developed as an alternative approach for the continuity of Moore's law, specifically in reducing form factor, cost, power and increasing performance [1]–[3]. By extending the conventionally two-dimensional layout, assembling, or interconnections into the third dimension, 3D integration has progressively become the primary building block of advanced electronic devices. For example, in the hybrid memory cube (HMC) reported by Micron, four stacked memory dies were integrated on the top of a logic die and interconnected using through silicon via (TSV) [4]. In general, depending on the interconnect hierarchy, 3D integration technologies can be classified into three categories: 3D System-in-Package (SiP, package or system level), 3D System-on-Chip (SoC, device level) and 3D monolithic integration (transistor level) [5].

On the other hand, quantum computing based on quantum mechanisms (i.e., superposition and entanglement) has been intensively investigated in the past two decades, in view of the superior potential in handling certain problems that are intractable for most advanced classical supercomputers [6], [7]. To realize quantum computing, various platforms with distinct physical implementations of quantum bit (qubit) are being developed simultaneously, including trapped ion, superconducting circuit, silicon spin, NV (nitrogen-vacancy) centers, photon, topological qubits, etc. To date, the number of qubits that are fully connected are ∼10 in most quantum computing devices. However, in the fault-tolerant quantum computing scheme, it is estimated that millions of physical qubits are required to build sufficient logical qubits (∼1000) to run the useful quantum algorithms and demonstrate the quantum supremacy [8]. This yields significant challenges in scaling up the state-of-the-art devices to that broad blueprint. The frequently required individual control with multiple signals

on every single qubit will further aggravate the situation. One of the possible solutions is to leverage the well-established CMOS (complementary metal–oxide–semiconductor) fabrication process in semiconductor industry which builds billions of transistors in a fingernail-size chip. At the same time, 3D integration technologies can also be adopted to boost the scalability of qubits by extending to the third dimension either in a hybrid or monolithic manner. Similar to the classical electronics, the 3D integration in quantum devices can be also classified according to its hierarchy. We summarize the hierarchy into three levels: the system or package level, the classical-quantum interface level and the qubit level. The detailed discussion on this classification is given in Session VI.

This review covers the state-of-the-art 3D integration technologies that were employed in various quantum computing devices based on their respective qubit types, namely trapped ion qubit, superconducting circuit qubit, silicon spin qubit as well as the photon qubit in silicon photonics. These devices are currently the most popular candidates due to their favorable manufacturability by leveraging the advanced semiconductor fabrication process. For each device, first, we will give a brief introduction in terms of two-level system implementation, universal gate operation, initiation, readout, etc. Following that, the specific scalability bottlenecks for different qubits are presented. Finally, the current solutions particularly those using 3D integration technologies are summarized and classified. In the last session of this review, a brief discussion on the thermal management in 3D integrated quantum computing devices is provided.

II. TRAPPED ION QUBIT

Trapped ions are dynamically confined and isolated from the environment by the RF electric field generated by the electrodes in an ion trap, where the trapping height in radial plane is determined by the RF electrodes width and pitch [9]. Lasers with specific wavelengths are focused onto the ions for cooling, manipulation, and detection. An ultra-high vacuum chamber (10^{-10} to 10^{-11} mbar) is required to minimize the collisions between trapped ions and surroundings. Ion trapping system does not require cryogenic environment, whereas the ion itself is cooled to sub-millikelvin temperature with Doppler cooling and sideband cooling techniques. The internal electronic states of the electron at the ion outermost orbit are encoded as qubit, which can be further categorized into optical qubit, Zeeman qubit and hyperfine qubit depending on the energy splitting between the two states [10]. In the context of quantum computing, we use optical qubit to illustrate the basic quantum operations related with trapped ion qubits. The rotation between states $|0\rangle$ and $|1\rangle$ can be simply performed by focusing a laser beam that resonant at the transition frequency. The shared motional mode in a string of ions can be used as a quantum bus to transfer information. Along with certain single qubit gate rotations, the entangled two qubit gate can thus be performed [11]. For readout, only the ions at state $|1\rangle$ can be excited into a transition cycle by lasers and emit the detectable photons during this cycle, whereas the ions at the state $|0\rangle$ will remain dark.

In 2005, the first ion trap with coplanar surface electrodes was developed in place of the mechanically assembled ion trap, paving a way for its incorporation with microfabrication techniques [12], [13]. Different materials (e.g., sapphire, glass, silicon, etc.) have been extensively explored to be used as the trap substrate [14]–[17]. The key requirements are low RF loss and high manufacturability. At the same time, over the past 15 years, the geometry of surface electrode ion traps has been progressively evolved from ∼10 electrodes to hundreds of electrodes with complex layout, in order to trap more ions and facilitate operations like ion shuttling [18], [19]. However, to scale up to the next stage, a modularity hierarchy is required, in which a large ion trapping system is built from medium-scale individual traps, where the communication between modules can be achieved via ion shuttling or photonic link [20], [21]. To realize this promising blueprint in terms of large-scale ion trapping implementation, numerous challenges remain to be overcome. From the integration point of view, two particular challenges are respectively the overcrowding interconnection and the on-chip integration of conventionally bulk components (e.g., voltage sources, mirrors, etc.).

With the development of ion trap geometry, certain electrodes located at the geometry center are inevitably surrounded by the peripheral electrodes, which cannot be accessed by bonding wires. Meanwhile, since wire bondings are laterally situated at the edges of a chip in a finite area, the increase of electrodes number will result in the interconnections overcrowding, and the incorporation of other functional components that necessitate independent signal wires will worsen the case. To mitigate these issues, one needs to explore the third dimension of interconnections. Multilayer metallization was first adopted in place of wire bonding to introduce additional degree of freedom for signal routing. Up to 10 metal layers were accommodated underneath surface electrodes (Fig. 1(a)), where neighboring layers were insulated with dielectric layers (e.g., SiO_2) and interconnected with small vias as needed [22]–[25]. However, a notable challenge along with this approach is the thick dielectric layer fabrication ($>10\ \mu$ m) which necessities processes not compatible with CMOS foundry [26]. Also, though multiple steps of chemical mechanical polishing (CMP) are used, the accumulated wafer thickness variations may hinder the on-chip integration of optical components. Meanwhile, in 2015, TSVs encircled with trench capacitors were integrated in ion trap [27]. The vias featured a ring shape and were filled with conductive polysilicon, yet the growth of platinum silicide on top of vias were required to form Ohmic contacts. To avoid the RF loss induced from the relatively large resistance of TSV, only DC electrodes were connected with vias. Recently, our group employed the 'zero-change' CMOS back-end-of-line process to develop the first Cu-filled TSV integrated ion trap, where all electrodes (including RF) were connected with vias (Fig. 1(b))

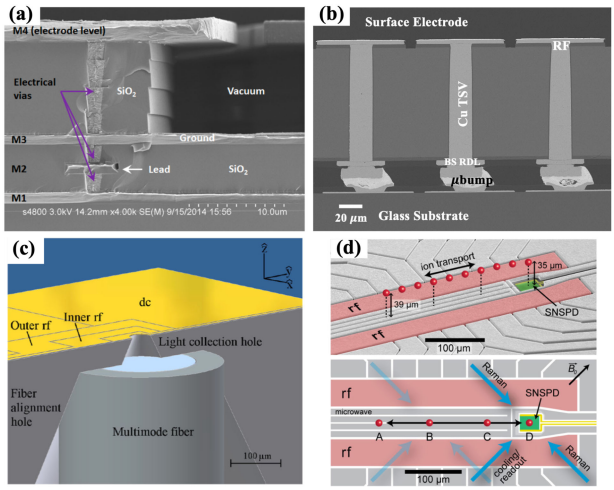

FIGURE 1. **(a) Ion trap with multilayer metallization underneath surface electrode for signal routing. (b) Ion trap using Cu-filled TSV to transmit signal from interposer to the surface electrode. (c) Schematic of fiber embedded into the ion trap for fluorescence collection. (d) Integrated superconducting nanowire single photon detector into ion trap for on-chip fluorescence collection. Panels used with respective permission from [23], [28], [34], [42].**

[28]. It was found that the incorporation of TSVs were able to reduce the parasitic capacitance of ion trap by ∼90%, with regards to the counterparts using wire bondings. However, the relatively large diameter and pitch of TSV make it less suitable for electrodes with extremely small dimensions (e.g., those at junction area). A combination of TSV and multilayer metallization is foreseen in the future ion trapping devices.

Free-space optics (e.g., mirrors and lenses) are heavily used in ion trapping setup, from which laser beams are routed through the vacuum chamber window and delivered onto the ions. Similarly, fluorescence from the ions is collected by photomultiplier tube located outside the chamber. However, with increasing number of trapped ions, the optical input and output interface for control and measurement of individual ions is significantly compressed. At the same time, the increased dimensions of ion trap itself may lead to undesired beam scattering. In 2011, optical fibers for light delivery were embedded underneath ion trap through drilled holes on the substrate [29], [30]. Nevertheless, the large diameter of fibers, complex hole drilling process and exposed dielectric surface make direct fiber integration less compatible for large-scale application. Until year 2016, a waveguide and grating coupler integrated ion trap was demonstrated [31]. A 120 nm SiN layer was introduced underneath surface electrode as the core material for the photonics components, of which similar micro/nano fabrication process was adopted. Light with wavelength of 674 nm was routed by the waveguides and focused to the ions by the grating couplers at multiple locations. Recently, with similar techniques, waveguides and grating couplers were designed for all wavelengths of light (from 422 to 1092 nm) required for the quantum operations of Sr^+ ion, and were fully integrated into a single trap. This undoubtedly demonstrates a milestone for complete photonics integration of single ions [32]. However, the precise alignment of multiple beams at same location remained a challenge [32]. Meanwhile, in another work, the integrated photonics were used to implement the two-ion quantum logic gate with a fidelity as high as 0.993(2) [33]. Simultaneously, the integration of optical components that facilitate efficient fluorescence collection was also advancing in the past decade, with a similar roadmap as light input integration. At the beginning, bulk optics (e.g., fibers) were mounted into the traps in relatively brute-force approaches (Fig. 1(c)) [34]. Following that, localized components like micromirrors and lenses were integrated and fabricated together with ion trap to improve the coupling efficiency [35]–[37]. In addition, traps directly fabricated onto high-reflectivity or transparent substrates were also demonstrated [38]–[40]. In recent years, the ion trapping communities were also exploring the monolithic integration of high-efficiency photodetectors into the ion trap [41], [42]. In a work reported in 2020, an average readout fidelity of 0.9991(1) was achieved for a trap-integrated superconducting nanowire single photon detector (Fig. 1(d)) [42]. At the same time, passive electronic components like trench capacitors were integrated in ion trap to filter the RF pick up on the control electrodes [27], yet the full integration of RF resonators commonly used for voltage step-up is still not demonstrated, partially due to the power dissipation issue. In terms of active electronics integration, in 2019, voltages sources together with DACs (digital-to-analog converters) were integrated into trap to generate low-noise control potentials on the electrodes [43]. Besides, it is necessary to mention that the 3D integration of magnetic components (e.g., microwave conductors) for qubits driven by microwave fields is also undergoing [44], [45].

III. SUPERCONDUCTING CIRCUIT QUBIT

At sufficiently low temperature ($kT \ll \hbar\omega$), the potential of a resonant circuit consists of a capacitor and inductor becomes quantized with a constant energy difference ($\hbar\omega$) between neighboring levels (harmonic oscillator). By introducing a Josephson Junction (a thin insulated layer sandwiched by two superconducting thin films) into the circuit, the energy difference turns into anharmonic, enabling specific state addressing and thus the encoding of qubit.

Depending on the types of encoded qubit (e.g., flux, charge, etc.) [46], [47], different layouts are implemented for the fundamental circuits built from capacitors, inductors and Josephson Junctions (Fig. 2(a)). In this review, we use the most popular transmon qubit (charge qubit) as an example to demonstrate the quantum operations for superconducting qubit [48], [49]. The single qubit gate (x or y axis rotation) is predominately driven by coupling a microwave signal (5-10 GHz) via a coplanar waveguide line, whereas the z axis rotation is driven through a flux tunning line if needed. For

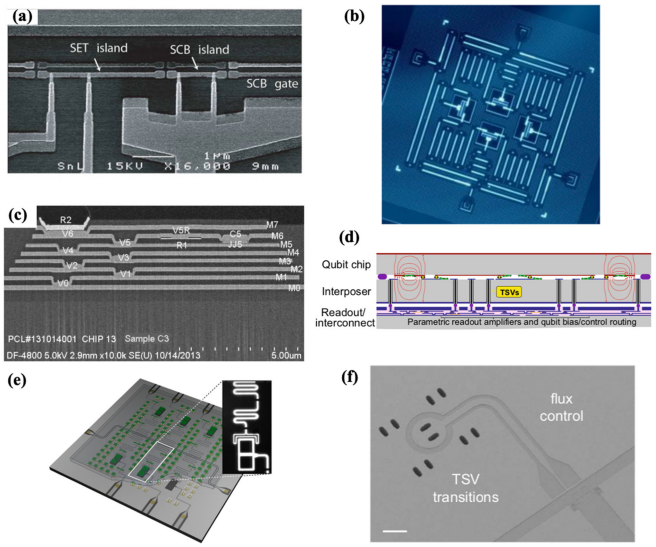

FIGURE 2. (a) SEM (scanning electron microscope) image of a charge qubit consists of Copper-pair box and single electron transistor. (b) Image of a device with 4 qubits, 4 quantum bus and 4 readout circuits. (c) Cross-sectional SEM image of 8 Nb layers, with Josephson junction (JJ), resistor (R) and vias (V). (d) The 3D integrated superconducting qubits scheme. Readout circuit and qubit circuit were separated and interconnected with interposer that contains TSVs. (e) Schematic of a qubit chip that was flip-chip bonded to the chip specifically designed for readout and control. (f) Superconducting circuit built directly on the TSV integrated substrate. Panels used with respective permission from [47] for (a), [49] for (b), [60] for (c), [62] for (d) and (e), [63] for (f).

two qubit gate, two neighboring transmon qubits are normally coupled through a capacitor in between (capacitive coupling). In addition, the qubit transition frequency can be dynamically tuned by incorporating a dc superconducting quantum interference device (dc SQUID, a superconducting loop interrupted by two Josephson Junctions), which is essential for both single and two qubit gates implementation [50]–[53]. For superconducting circuit readout, dispersive readout is typically used by coupling the qubit to a transmission line resonator [54]. In summary, all components that are required to define, manipulate and readout superconducting qubits are macroscopic circuits, which can be patterned on the superconducting films with lithography-based techniques (Fig. 2(b)). This makes it inherently compatible with advanced CMOS process and thus promising for large-scale realization. However, some challenges are remained. As differed from large array of classical bits in memory that can be parallel addressed using Word or Bit lines, every single superconducting qubit requires independent circuits designed for control, readout, and qubit-qubit coupling, resulting in huge footprint and interconnection overhead. Meanwhile, most of the circuit layouts are still in a 2D scheme, where interconnections for various signals can only access the qubits via chip perimeters. In the Sycamore processor demonstrated by Google in 2019, a rectangular array of 54 qubits took a surface area of $\sim$10 $\times$ 10 mm [55]. Therefore, to scale up the 2D scheme and maintain the qubit addressability, 3D integration technologies are essential.

The incorporation of superconducting multilayers to increase wiring density was started in 2005 [56]. In 2010, D-WAVE employed four superconducting Nb layers to supply 64 flux biases to flux qubits, where Josephson Junctions were located between the bottom two layers [57]. HYPRES also developed a technique to extend eight superconducting layers underneath conventional four-layer chip [58]. Similarly, MIT Lincoln Laboratory released a roadmap, envisaging the fabrication development for 4, 8 and 10 superconducting layers with minimized Josephson Junction diameter (from 1000 to 500nm) [59], [60] (Fig. 2(c)). Though superconducting multilayers is able to ease the interconnections crowding issue, the obtained coherence time is generally shorter as compared to the qubits with single layer structure, which is limited by the fabrication complexity (CMP process is heavily used) and undesired interlayer coupling. Furthermore, the natural defeats exist in the interlayer amorphous dielectric materials (SiO_2 and Si_3N_4) can disturb the electric field and thus decrease the qubit lifetime [61].

To mitigate this challenge, a 3D integrated superconducting qubit scheme was proposed in 2017 [62]. This scheme consists of three bonded chips that are individually fabricated. The top chip is the qubit chip which contains qubit circuits, and the bottom chip is for readout and interconnection. To bridge these two chips, an interposer chip that incorporates superconducting TSV is bump-bonded in between as shown in Fig. 2(d). With this scheme, the capability for complex interconnection routing is maintained in the bottom chip, while the qubit performance in the top chip will not be degraded. The first step of this scheme was demonstrated in 2017, where the qubit chip was flip chip bonded to a chip underneath containing circuits specifically for qubit readout and control (Fig. 2(e)) [62]. As the second step, superconducting TSVs that transmit signals from chip backside to the front side were integrated into the interposer chip, controlling the qubits chip bonded on the top [63]. In addition, to demonstrate the full potential of this 3D scheme, qubit circuits were also directly fabricated onto superconducting TSVs integrated interposer (Fig. 2(f)). The resulting mean lifetime is $\sim$10 μ s, in favorable comparison with state-of-the-art planar devices.

Indeed, as an important component in the abovementioned 3D scheme, superconducting TSVs have been independently investigated over past 5 years [64]–[67]. However, most of the work focused on the via fabrication process (e.g., via etching, sputtering or atomic layer deposition for via metallization), and did not move forward to the cointegration of superconducting TSVs with real qubits. Meanwhile, other structures like airbridges and sapphire balls with diameter of 200 μ m were also explored to extend the control and measurement circuits into the third dimension [68], [69]. In addition to those using microfabrication techniques, mechanically assembled 3D packaging architectures were also proposed using either spring-mounted 3D microwires or multilayer PCB clamping [70], [71]. However, the alignment process and large form factor hinder them from large scale implementation.

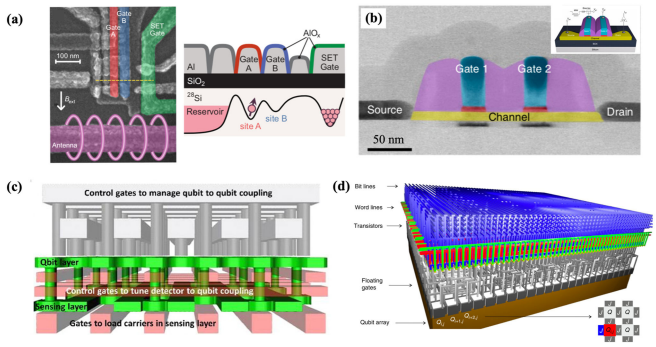

FIGURE 3. **(a) False-colored SEM image of silicon spin qubit device consists of gate electrodes, microwave transmission line and SET. A corresponding schematic is shown on the right. (b) Colorized TEM (transmission electron microscopy) image of the CMOS qubit device, where two quantum dots were defined in series. (c) The 3D architecture of silicon spin qubit. Two layers of quantum dots that respectively used as qubit and for sensing were coupled through a vertical tunnel barrier. (d) The 3D architecture of classical-quantum interface of silicon spin qubits. Transistors on the top were used to control the qubits array underneath. Panels used with respective permission from [79], [88], [89], [91].**

IV. SILICON SPIN QUBIT

Different from qubits based on trapped ion or superconducting circuit that have a relatively long research history, the first single qubit gate and two qubit gate of silicon spin qubits were respectively demonstrated in 2012 and 2015 [72], [73]. To date, the number of entangled qubits reaches three in silicon and four in germanium [74], [75]. Silicon spin qubits are encoded on the spin of electrons, that either bound to the embedded dopants or quantum dots (MOS and SiGe material systems are commonly used to define quantum dots) [76], [77]. Unlike charge-based qubits that generally suffer from electric noise, spin qubits can only be interacted magnetically and therefore feature long coherence time. An in-plane large static magnetic field is required to create the Zeeman splitting. The single qubit gate is achieved using electron spin resonance (ESR) technique, in which an AC current is sent into a transmission line close to the qubit and thus generate a localized AC magnetic field resonant with spin transition frequency. The two qubit gate is implemented via the exchange interaction [78]. To facilitate the entanglement beyond immediate neighbors, coherent transport of spin qubits across the chip can be used [79]. For the qubit readout (spin encoded by single electron), a process known as spin-to-charge conversion is used, where the qubit electron is coupled to a single electron transistor (SET), and under specific conditions spin-up electron will tunnel to the electron reservoir and produce a detectable current pulse [80], [81]. We note that all these basic operations are controlled and enabled by appropriate voltages tunning on the corresponding gate electrodes located on top of qubits (Fig. 3(a)) [82]. In addition to the abovementioned simplest spin qubit defined by single electron, singlet-triplet qubit and three-electron spin qubit (e.g., hybrid qubit) are also being investigated which can be controlled partially or fully electrically [83], [84].

The counted, deterministic implantation of single donors, as well as the novel methods for precise placement and alignment are key challenges that significantly limited the large-scale application of the spin qubit bound in donor system [85], [86]. On the other hand, taking advantage of the lithography-based fabrication, quantum dot-based silicon spin qubit has exhibited the favorable scalability. In terms of fabrication compatibility, quantum dot in MOS (metal-oxide-semiconductor) system is naturally more appealing than its counterparts in SiGe system, though the interface disorder between Si and amorphous SiO_2 may introduce undesired noise and degrade the fidelity [87]. In 2016, silicon spin qubit with a geometry derived from the field effect transistor (compact two gate FET) was developed as shown in Fig. 3(b), where two top gates were respectively used to control two quantum dots (in series) that defined in the silicon channel [88]. This work started from the standard CMOS process in transistor fabrication and adapted it to achieve the quantum functionality. Though auxiliary quantum dot was required for readout and two qubit gate was yet performed, this work indeed demonstrated the often-argued compatibility of silicon spin qubits with CMOS fabrication process.

Similar to the superconducting circuit qubits, even in a huge array of millions of qubits, the independent control from multiple gate electrodes is anticipated to be indispensable for every single silicon spin qubit. As a result, the gate electrodes number and corresponding classical circuit that control electrodes will boost with the increase of qubits number, posing significant challenges to the qubit architecture itself as well as the quantum-classical interface. To mitigate the first challenge, a 3D architecture was proposed in the qubit level [89], [90]. As shown earlier, two quantum dots in series were fabricated, of which one was encoded as a spin qubit whereas the other one was for qubit readout (sensing dot) [88]. In the new 3D architecture, the sensing dot was repositioned to the layer underneath the qubit dot layer (Fig. 3(c)). A controllable and addressable tunnel barrier was introduced to transmit electron in between the two layers. In addition, separate control layers that contain gate electrodes were required for both sensing and qubit dot layers. In this scheme, the footprint overhead due to the additional sensing dot can be minimized and therefore the scalability is enhanced. In terms of the interface overcrowding, 3D integration scheme was also proposed for future quantum computer processor where the bottom layer and top layer of a silicon-on-insulator wafer were respectively used to accommodate qubits array and classical transistors for control (Fig. 3(d)) [91]. Vias through the insolation layer were required to connect the bottom and top layers, enabling a scalable quantum-classical interface. Although current CMOS manufacturing capabilities may not fulfill the stringent requirement in terms of qubits uniformity and reproducibility, this conceptual architecture makes an important step towards large-scale silicon spin qubits scenario. Recently, a 3D dielectric resonator was stacked on top of the qubits circuit with a sapphire spacer in between [92]. In place of conventional transmission lines that placed close to every single qubit, the

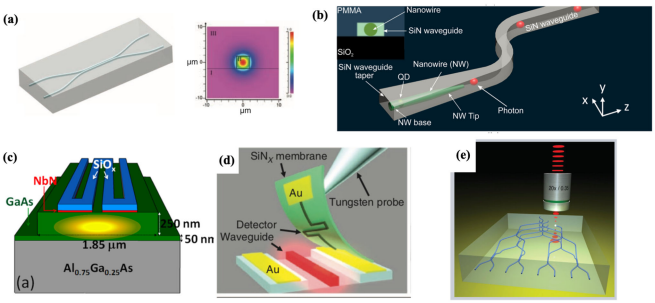

FIGURE 4. **(a) Schematic of a waveguide circuit used to entangle photons, together with a modeled transverse intensity profile. (b) Schematic of a III-V quantum dot in a nanowire that was transferred into a SiN waveguide. (c) Schematic of a waveguide integrated superconducting nanowire single photon detector. Four NbN wires were directly patterned on top of the GaAs waveguide. (d) Schematic showing the process of transferring individually fabricated SNSPD onto a waveguide circuit. (e) Schematic of a laser writing process to build 3D waveguide circuits. Panels used with respective permission from [93], [101], [104], [109], [113].**

dielectric resonator was used to generate a global magnetic field across the entire quantum circuits underneath and the ESR of single qubit with this field was successfully demonstrated. Again, this global field eases the concern of large AC current running into the quantum circuits and the control of millions of qubits appears to be practical.

V. PHOTON QUBIT IN SILICON PHOTONICS

Photons are appealing to be used as qubits since they are almost free of decoherence. With that, the stringent environmental conditions (e.g., millikelvin temperature and ultra-high vacuum) as required by other qubit candidates can be eliminated, enabling photon qubits with high scalability. The previous concern was the heavily used bulk optics (beam splitters and mirrors) that located on the large vibration-free table. However, with the incorporation of silicon photonics, photons can now be guided and routed by waveguides with high phase stability (Fig. 4(a)) [93], [94]. Meanwhile, photons generation, state manipulation, and photons detection can also be performed on-chip using corresponding photonics components together with delicate photonic circuit design [95], [96]. Though the photon qubit can be encoded in various degrees of freedom (polarization, path, etc.) and the single qubit rotation can be straightforwardly performed by using waveplates and beam splitters, the extremely strong nonlinearity required for a two-qubit gate (i.e., Controlled NOT gate) implementation has not been demonstrated [97]. In 2001, a landmark scheme was proposed to implement the universal quantum computing with linear optics only, in which the CNOT gate on control and target qubits is conditional on the single photon detection of two auxiliary photons [98]. Nevertheless, the unfavorable consequence is that the gate is non-deterministic and only a small fraction of the outputs is used. To achieve a near-deterministic gate, the overhead of auxiliary photons will become exceptionally huge. Different from the abovementioned qubit candidates that have demonstrated single and two qubit gates but lack scalability, photon in waveguide circuits is naturally scalable thanks to the silicon photonics advancement. However, the challenge is to make it quantum, or more particularly, to achieve the entangled logic gate efficiently, which requires further theoretical and experimental innovations. Currently, one of the key requirements is to develop high efficiency single photon sources and single photon detectors, which are integratable to the sophisticated photonics circuit [96].

Two types of single photon sources are commonly used which are respectively quantum dots single-photon source and parametric photon-pair source. The superior advantage of quantum dots is that the resonance fluorescence photons from them are deterministic. Nevertheless, it is challenging to fabricate quantum dots array with high uniformity and repeatability. Also, the alignment between quantum dots and waveguides-based quantum circuit is troublesome [99], [100]. In 2016, a pick-and-place technique was developed as shown in Fig. 4(b), in which preselected III-V quantum dots in nanowires were transferred and integrated into SiN waveguides on silicon substrate using a micromanipulator [101]. This technique allows for the precise alignment and high coupling efficiency between quantum dots and waveguide circuits. On the other hand, parametric photon-pair source is normally generated by pumping nonlinear waveguides, which makes it inherently integratable. Using similar fabrication techniques as quantum circuits, identical but individually controllable single photon source array was achieved [102]. However, parametric photon-pair source is non-deterministic with a probability of 5-10%. Though time or spatial multiplexing techniques can be applied to increase the probability, the resultant source overhead will degrade the overall performance (computation speed and chip footprint).

Single photon avalanche diode (SPAD) and superconducting nanowire single photon detector (SNSPD) are particularly popular in the quantum photonics circuit for single photons detection. As compared to SNSPD, SPAD eliminates the stringent requirement of low operation temperature (several Kelvins). However, the poor performance (detection efficiency of $<10\%$) and relatively complex fabrication process make it less applicable in the integrated system [103]. On the contrary, waveguide integrated SNSPDs have been demonstrated with $>90\%$ detection efficiency and extremely low dark counts [104]–[107]. The trade-off is that the required cryogenic apparatus (for SNSPDs only) introduces resources overhead. In a typical integrated SNSPD, patterned superconducting nanowires are used to absorb the photons incident from the waveguide underneath (Fig. 4(c)). To enhance the absorption process, as reported in [108], waveguide was etched with holes to define a microcavity for superconducting nanowire and thus achieving the near-unity quantum efficiency. However, due to the incorporation of various superconducting materials and additional tens of fabrication steps, the resultant yield of large-scale quantum circuit may be significantly degraded as the number of integrated SNSPDs grows. In 2015, a micrometer-scale flip chip method was demonstrated to transfer ten SNSPDs onto the same photonic

TABLE I Comparison of Various Quantum Computing Devices

Qubit type	Temperature and vacuum	Control signal	Feature size	Pitch between qubits	Challenges to scale up	Commercialization
Ion Trap	Ambient and ultra-high vacuum^	Lasers, RF and DC voltage	~5 μm (gap width between electrodes)	~10 μm	a. flexible interconnection b. electrode and photonics fabrication node difference c. off-chip light alignment with ions	IonQ, Honeywell
Superconducting circuit	~10mK and high vacuum*	Microwave current, DC current, RF control[#]	~50 nm (Josephson Junction)	~1 mm	a. complex circuit layout b. cryo-electronics c. noise shielding and filtering d. entangle with neighboring qubits only	IBM, Google
Silicon spin	1K and high vacuum*	DC magnetic field, AC magnetic field, DC voltages, RF control[#]	~50 nm (gate electrode)	10-100 nm	a. multiple quantum dots placement and alignment b. complex electrodes layout c. cryo-electronics d. noise shielding and filtering	Intel
Photons	Ambient and atmosphere	Lasers, DC voltage, RF control[#]	200 nm (waveguide)	~200 μm	a. high efficiency single photon source and detector b. the integration and alignment with waveguide circuit	PsiQuantum, Xanadu

^Cryogenic apparatus in ion trapping test also benefits for anomalous heating reduction; $*$ The high vacuum (down to 0.1 mbar) is required by the dilution refrigerator; [#]RF control is required for the pulsed operations within qubit lifetime.

circuits as shown in Fig. 4(d) [109]. Based on separate fabrication and individual pre-selection of SNSPDs and photonic circuits, a 100% device yield was achieved.

Though single photon sources and detectors can be integrated into the photonic circuits in an out-of-plane approach, the waveguide circuits themselves generally feature a 2D geometry. This is limited by the lithography and etching based fabrication process. However, the femtosecond laser direct-write (FLDW) technique is able to build a novel 3D integrated waveguide circuits by focusing the laser beams at different depth in the substrate (Fig. 4(e)) [110]–[113]. In terms of device level integration, single photon sources, detectors as well as multiple waveguide circuits can be stacked vertically in a 3D fashion. Optical vias may be required to interconnect modules at different heights [114], [115].

VI. DISCUSSION

A. CLASSIFICATION FOR 3D INTEGRATION TECHNOLOGIES

Table I gives a comparison of the abovementioned four qubit candidates, in terms of the environment requirement, various control signal, qubit feature size and pitch, challenges to scale up as well as the current status of the investment from industry. Fig. 5 summarizes the 3D integration technologies adopted in various quantum computing devices according to the integration hierarchy. We use the well-known concepts in electronics 3D integration as reference. The first hierarchy (3D SiP) is to integrate the bulk components into the quantum chip, such as the fibers in ion trap. The next hierarchy (3D SoC) is at the classical-quantum interface. The goal is to maintain the I/O accessibility of individual qubits with the boost of qubits number, such as the TSV integration in ion trap in place of wire bonding. The final hierarchy (3D monolithic integration) is at the device itself, aiming to transfer the 2D qubit architecture into a 3D fashion. Laser written 3D waveguide circuits is a good example in this hierarchy. Meanwhile, quantum dots that aligned vertically was proposed but has not been demonstrated.

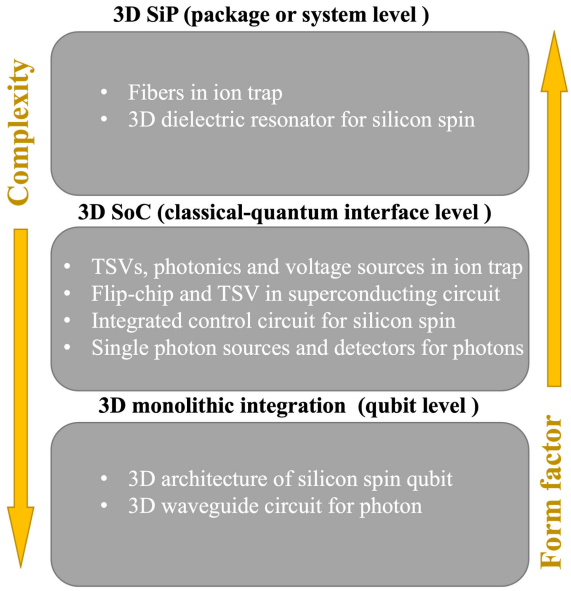

FIGURE 5. The hierarchy of 3D integration technologies used in various quantum computing devices. .

B. THERMAL MANAGEMENT FOR 3D INTEGRATED QUANTUM COMPUTING DEVICES

The heating issue of 3D integrated chips is one of the major constraints for its broad applications. In general, as more components and interconnections are incorporated, higher loss/heating will be generated. The compact architecture will

aggravate the situation due to the lack of efficient heating dissipation path. Moreover, the commonly used organic substrates (e.g., printed circuit board) that located 3D integrated chips are not a good heat sink.

In the field of quantum computing, heating issue becomes more daunting as additional decoherence source is introduced. As a result, the qubit lifetime and gate operation fidelity may be reduced. In the Cu-filled TSV integrated ion trap, a slight vacuum level increase (of the order of 10^{-11} mbar) was observed due to the high trap temperature during operation [28]. Similarly, in the voltage source integrated ion trap, the temperature of trap increased from 4 K (cryogenic apparatus) to 50 K due to the high power dissipation (500 mW) from integrated DACs, leading to a high heating rate of the trap [43]. The situation is more complex for qubit candidates working at ~10 mK. Conventionally, for superconducting circuit and silicon spin qubits, most of the classical control electronics are located outside the dilution refrigerator and connected to the qubits layer with long coaxial cables. However, the induced signal latency is even comparable with the two-qubit gate speed. Also, the arrangement of free-space cables for millions of qubits will become unmanageable. To mitigate these issues, the idea of placing the classical electronics closer to the qubit layer was proposed, triggering the recent developments of cryo-electronics working at 4 K [116]–[118]. Though a 3D architecture is required to integrate the cryo-electronics with qubits layer as envisioned in [119], a major concern is that the limited cooling power (thermal budget) at 4 K. Further systematic investigations are required to evaluate the possible impact of temperature increase both on the integrated classical electronics and the qubits performance.

Although this article mainly focuses on the applications of 3D integration technologies in individual quantum computing device, 3D integration is foreseen to be essential in the future hybrid quantum system. By integrating two or more quantum systems, it is believed the strength of different systems can be amplified while the shortages can be avoided [120]. For example, the design to simultaneously leverage the high gate speed of superconducting circuit and the long lifetime of trapped ion has been proposed [121]. However, as mentioned earlier, quantum systems are generally fabricated with different nodes and processes, hindering the direct combination. This is exactly where proper integration technologies can contribute, in particular at the system and interface level.

VII. CONCLUSION

In this review, the scalability issues of quantum computing devices have been discussed for four popular qubit candidates (trapped ion, superconducting circuit, silicon spin and photon) that are compatible with CMOS fabrication process. Specifically, the role of 3D packaging in large-scale integration is highlighted. From the prior studies covered in this review, it can be concluded that 3D integration technologies exhibit promising potential in architecture scaling-up and device miniaturization to achieve the future fault tolerant quantum computer.

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