IEEE Open Journal of Nanotechnology

Received 4 June 2021; revised 13 August 2021; accepted 30 August 2021. Date of publication 3 September 2021; date of current version 16 September 2021. The review of this article was arranged by Associate Editor Kazuhiko Endo.

Digital Object Identifier 10.1109/OJNANO.2021.3109897

Modifying Threshold Voltages to n- and p-Type FinFETs by Work Function Metal Stacks

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This work was supported by the Ministry of Science and Technology, Taiwan, under Grant MOST 109-2221-E-390-001.

ABSTRACT High-k metal gate technology improves the performance and reduces the gate leakage current of metal–oxide–semiconductor field-effect transistors (MOSFETs). This study investigated four different work function metal (WFM) stacks in the gate of fin field-effect transistors (FinFETs) on the same substrate. These devices not only successfully produced distinct levels of threshold voltages ($|V_t|$) but also converted n- to p-type features merely by adding p-type WFM in the gate of the MOSFETs. All of the devices satisfied short-channel effects with shrinking channel length. The gate-to-body electric field induced drain leakage due to the nature of bulk FinFETs. However, the n- and p-type gate stacks presented different gate current leakage. For reliability, hot carrier injection (HCI) could have a higher reliability impact than the negative-bias temperature instability (NBTI) for p-MOSFET, although the stress voltage of HCI was roughly half that of the NBTI test. This multi-threshold voltage tuning allows designers to design CMOS and choose the trade-off between low power consumption and high performance on the same platform.

INDEX TERMS Work function metal, threshold voltage tuning, energy-dispersive X-ray spectroscopy, FinFETs, reliability.

I. INTRODUCTION

High-k metal gate (HK/MG) technology has replaced the conventional polysilicon gate to avoid high-k dielectric crystallization during the thermal process. The technology also reduces the depletion effect, increases the gate dielectric equivalent thickness, and lowers driving force. The advancement satisfies the requirement of high performance and low power consumption [1]. Selecting the work function metal (WFM) can modulate the threshold voltages (V_t) of a metal–oxide–semiconductor field-effect transistor (MOSFET). The modulated V_t depends on the dipole formation of WFM atoms from the interface to dielectrics. Multi-V_t tuning allows designers to choose the trade-off between low power consumption and high performance [2], [3]. Although post-fabrication via back biasing can modulate V_t [4], [5], only a limited V_t range is possible.

With regard to conventional planar MOSFETs, the fabrication process commonly uses ion implantation to tune the V_t value. However, ion implantation is difficult for the narrow fins of fin field-effect transistors (FinFETs), although a specific range for changing V_t is possible [6]. Moreover, ion implantation can cause random dopant fluctuation, which is unsuitable for advanced integrated circuit fabrication. An undoped or low-doped channel is commonly adopted for advanced devices to avoid this uncertainty. Therefore the WFM gate was introduced as a solution to modulate V_t in FinFET devices [7]–[16].

The WFM gate can be an n-type WFM (nWFM) or a p-type WFM (pWFM), thus making MOSFETs become n- or p-type MOSFETs by modulating V_t. Titanium nitride (TiN) is a typical pWFM. The work function of TiN depends on the ratio of Ti to N and metal thickness [7]–[9], [16]. An increase in TiN thickness changes WFM and V_t [11], [17]. In addition to metal thickness, metal gate granularity is another determinant that varies V_t [18], [19]. Oxide charge has a secondary factor for V_t variation due to dipole formation at the interface. The roughness edge and the dopant exert a minor impact on V_t variation [14], [15].

The fundamental objective of the WFM gate is to determine the valence (E_V) and conduction (E_C) band curve (up or down) near the interface from the band diagram of a MOSFET. Fig. 1 presents an unbiased MOSFET energy diagram representing

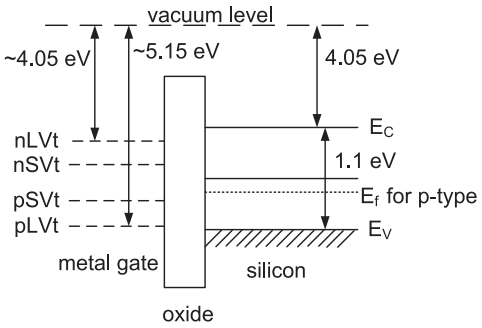

FIGURE 1. Energy diagram of unbiased MOSFETs that use a WFM gate to modulate threshold voltages. The n-type low threshold voltage (nLVT) FinFET has the lowest work function (~4.05 eV) in all devices, followed by the n-type standard threshold voltage (nSVT) FinFETs. On the contrary, the p-type low threshold voltage (pLVT) FinFETs have the highest work function (~5.15 eV), followed by the p-type standard threshold voltage (pSVT) FinFETs.

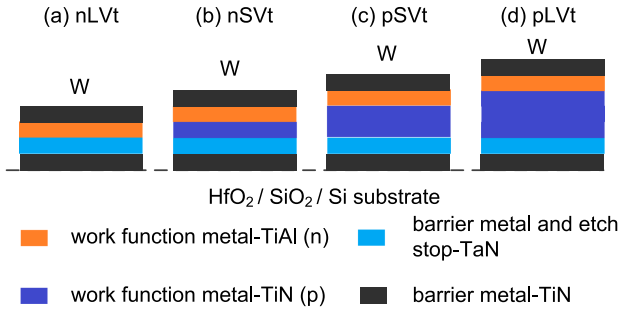

FIGURE 2. Schematic of metal gate stacks on FinFETs. The metal stacks include metal barriers and etch stop (TiN and TaN), nWFM (TiAl), and different thicknesses of pWFM (TiN) to generate (a) n-type low threshold voltage (nLVT), (b) n-type standard threshold voltage (nSVT), (c) p-type standard threshold voltage (pSVT), and (d) p-type low threshold voltage (pLVT) FinFETs. Low-resistivity tungsten (W) fill serves for contact, and interfacial dielectric (SiO_2) deposition is applied before the high-k dielectric (HfO_2).

multi-V_t due to a work function difference in the gate. The WFM in n- and p-channel MOSFETs should possess a low work function near 4.05 and 5.15 eV, respectively [20]. N- and p-channel MOSFETs with a low $|V_t|$ are denoted as nLVT and pLVT, respectively. The typical WFM is 4.1–4.3 eV in nMOSFET and 5.0–5.2 eV in pMOSFET [21]. N- and p-MOSFETs with a standard $|V_t|$ (higher than those of nLVT and pLVT) are denoted as nSVT and pSVT, respectively. Although a few studies have reported on WFM for n- and p-MOSFETs and the determinants of V_t, metal WFM stacks to control V_t have not been investigated. The present study examines WFM stacks to generate multiple V_t and alter n- and p-MOSFETs on the same substrate. The results allow for CMOS and multi-V_t design on the same platform, resulting in low power consumption and high performance.

HK/MG technology can effectively suppress the short channel effect (SCE) and the fluctuations induced by random interface traps [22]. The aging degradation of FinFETs may involve several reliability mechanisms; for example, gate bias stress (or bias temperature instability) on p-channel MOSFET causes hole trapping and interface state generation [23], [24]. The failure mechanism of negative-bias temperature instability (NBTI) is to break the silicon–hydrogen bond. The hydrogen ion diffusion results in the interface state and mobility degradation [23]. While the BTI generates the electrical field perpendicular to the channel, the hot carrier injection (HCI) combines horizontal and perpendicular electric field to the channel. The HCI accompanied with the self-heating effect exhibits more degradation for FinFETs than what is expected [25]–[27]. However, the interface state generation and oxide trap can be passivated (recovered) by bond formation with hydrogen atoms [26], [28]. HCI is also a critical factor to shift V_t in compared with other reliability mechanisms [24]. The interplay of the superposed gate and drain voltages has well described the NBTI and HCI degradation of p-MOSFETs [29]. This study compared the impact of NBTI and HCI on these devices by finding the degradation level from electrical characteristics.

II. DEVICE FABRICATION AND MEASUREMENT

A. GATE STACKS OF MULTI-THRESHOLD VOLTAGE MOSFET

This study used 16 nm FinFET CMOS technology. The gate-last FinFETs were tri-gate with 20 fins. Figs. 2(a)–2(d) present the gate schematic of WFM stacks, metal barriers, and dielectrics. The high-k dielectric HfO_2 reduces the leakage current and the equivalent oxide thickness. However, HfO_2 generally exhibits a high density of interface state and fixed charges. An interfacial layer of SiO_2 was deposited before the deposition of HfO_2. TiN serves as an effective barrier as metal gate stacks [30]. The bottom metal barrier made of TiN on TaN can effectively improve the oxide trap density of high-k HfO_2 for metal stacks [12]. TaN was also used in this study for the metal barrier and etch stop layer. The metal stacks included TiN as the top and bottom metal barriers. Low-resistivity tungsten (W) was filled onto the top barrier metal (TiN).

The gate-last approach is suitable for WFM tuning because the gate-first approach is ineffective for WFM tuning. On the contrary, the gate-first approach suffers from subsequent high-temperature processes, thus varying the work function on the gate and leading to a threshold voltage shift due to oxygen diffusion [31]. The work function of aluminum is nearly 4.1 eV and suitable as an nWFM. The WFM used titanium aluminide (TiAl) and TiN to adjust V_t. The thickness of TiN was adopted to tune V_t. The added TiN layers converted n-type FinFETs into p-type FinFETs. According to literature, the addition of AlN in TiN can convert pMOSFET to nMOSFET (~4.59 eV) [30]. The composition of TiAl as nWFM can modulate WFM by combining TiN [9]. Figs. 2(a)–2(d) present the schematic of n-type low threshold voltage (nLVT), n-type standard threshold voltage (nSVT), p-type standard threshold voltage (pSVT), and p-type low threshold voltage (pLVT) FinFETs, respectively.

B. DEVICE MEASUREMENT AND RELIABILITY TEST

The B1500A semiconductor device parameter analyzer was used for electrical measurement. The transfer drain current

to gate voltage (I_D-V_G) was measured under a small (0.05 V) and large drain voltage (V_D). The gate leakage current (I_G-V_G) measured the gate-to-body current under different V_G. As the NBTI on p-MOSFETs is the most prominent effect for positive/ negative BTI on p-/ n- MOSFETs [32], [33], this research primarily studied NBTI on p-MOSFETs. The reliability test included NBTI and HCI on pLVT FinFETs. The HCI applied equal gate (V_G) and drain (V_D) potentials because the worst case arises in FinFETs at equal biases [34]. The NBTI stress was found to cause significant degradation with V_G greater than V_t of 2.2 V, or $V_G > (V_t\text{-}2.2)$ V. The current NBTI thus applied a stress voltage of $V_G = -2.5$ and -2.6 V. By contrast, HCI stress voltages were found to cause significant degradation with $V_D = V_G$ greater than V_t of 1.1 V, or $V_G > (V_t\text{-}1.1)$ V. The HCI thus used the stress voltages of -1.3 and -1.4 V. The electrical properties of the devices were measured on a logarithmic scale because the current degradation was on the logarithmic scale of time [5]. The lifetime of the devices was presumably a 10% variation of the electrical parameters, including maximum transconductance ($G_{M,MAX}$), subthreshold slope (S.S.), and V_t.

III. RESULTS AND DISCUSSION

A. ELEMENT ANALYSIS OF THE GATE STACKS MOS

All of the measured FinFETs had 20 fins. The element analysis focused on a pLVT FinFET (Fig. 3(a)). The fin height, width, and length were 42, 10, and 20 nm, respectively. The TEM micrograph of a fin (MSSCORPS Co., Ltd.) has an atomic-scale resolution for element analysis (Fig. 3(b)). Fig. 3(c) presents the element line scan obtained by energy-dispersive X-ray spectroscopy. The line scan corresponds to the micrograph in Fig. 3(b). The element ratio extended to 50 nm helped clarify the sequence of metal stacks. The element distribution was symmetrical and centered at 25 nm. The metal stacks showed that after tungsten (W), Ti increased at the onset of N because TiN served as the top metal barrier. TiAl (nWFM) followed the top metal barrier. The pWFM and bottom metal barrier (TiN) then appeared again. TaN emerged before the dielectrics (HfO_2 and SiO_2). The metal stack sequence agrees with the schematic in Fig. 2(d).

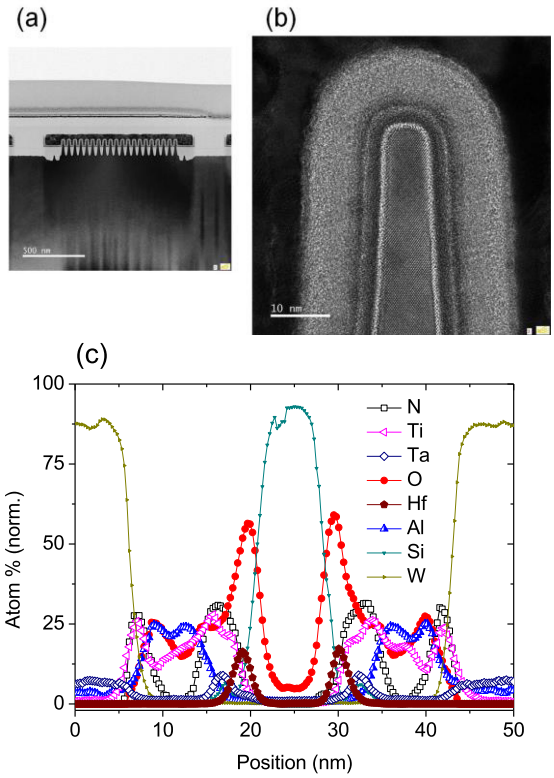

FIGURE 3. (a) Micrograph of the 20-fin pLVT FinFET in this research and (b) cross-sectional profile of the fin obtained with a transmission electron microscope used for the element analysis in (c), which indicates the element ratio for the location of the line scan on 50 nm width extent.

B. CHARACTERIZATION OF WFM STACKS

Figs. 4(a)–4(d) present the drain current (I_D) as a function of gate voltage (V_G) and the corresponding transconductance (G_m) with fin lengths of 16, 20, 36, and 72 nm for nLVT, nSVT, pSVT, and pLVT FinFETs, respectively. The plots indicate that the WFM stacks enabled the FinFETs to modulate $|V_t|$ and convert the properties from n- into p-type FinFETs. A small drain voltage ($|V_D|$) of 0.5 V was applied to drive the devices. All of the measuring devices had a fin width of 10 nm. The S.S. and transconductance (G_M) increased with the decrease in fin length, which agrees with SCE. The devices in Figs. 4(a) and 4(d)(nLVT and pLVT) exhibit a low $|V_t|$ in Figs. 4(b) and 4(c)(nSVT and pSVT). Fig. 5 summarizes V_t with different fin lengths. The result agrees well with V_t roll-off for the four types of devices.

The I_D-V_G plots of nLVT and nSVT FinFETs (Fig. 6(a)) and pSVT and pLVT FinFETs (Fig. 6(b)) indicate that the turn-on current (I_{ON}) increased by roughly one order of magnitude from $|V_D|$=0.05 V to $|V_D|$=1.2 V. However, the turn-off current (I_{OFF}) increased by approximately three orders of magnitude, resulting in a decrease in I_{ON}/I_{OFF} by two orders of magnitude. In addition, the gate-induced drain leakage (GIDL) became significant for $|V_D|$=1.2 V (dashed circle).

Body bias has been used to modulate threshold voltages on ultra-thin silicon-on-insulator and buried oxide FETs. A recent study has shown that body bias can also influence the electrical properties of bulk FinFETs [5]. The V_G offset swings with body bias (V_B) due to the properties of bulk FinFETs. Unlike silicon on insulator FinFETs, the gate offset is shiftable with body bias for bulk FinFETs. Figs. 7(a) and 7(b) show that the minimum gate current (I_G) shifted with body bias, indicating that the body bias generated an offset to the gate. We found that the I_G level of the p-type (pSVt and pLVt) generally exhibits a lower I_G than n-type (nSVt and nLVt), making the minimum I_G below the noise floor (Fig. 7(b)). The I_G difference should result from metal gate stacks because all the devices share the same substrate. The tunneling current in dielectric is directly responsible for the I_G difference [35]. The TiN layer may not only serve as WFM

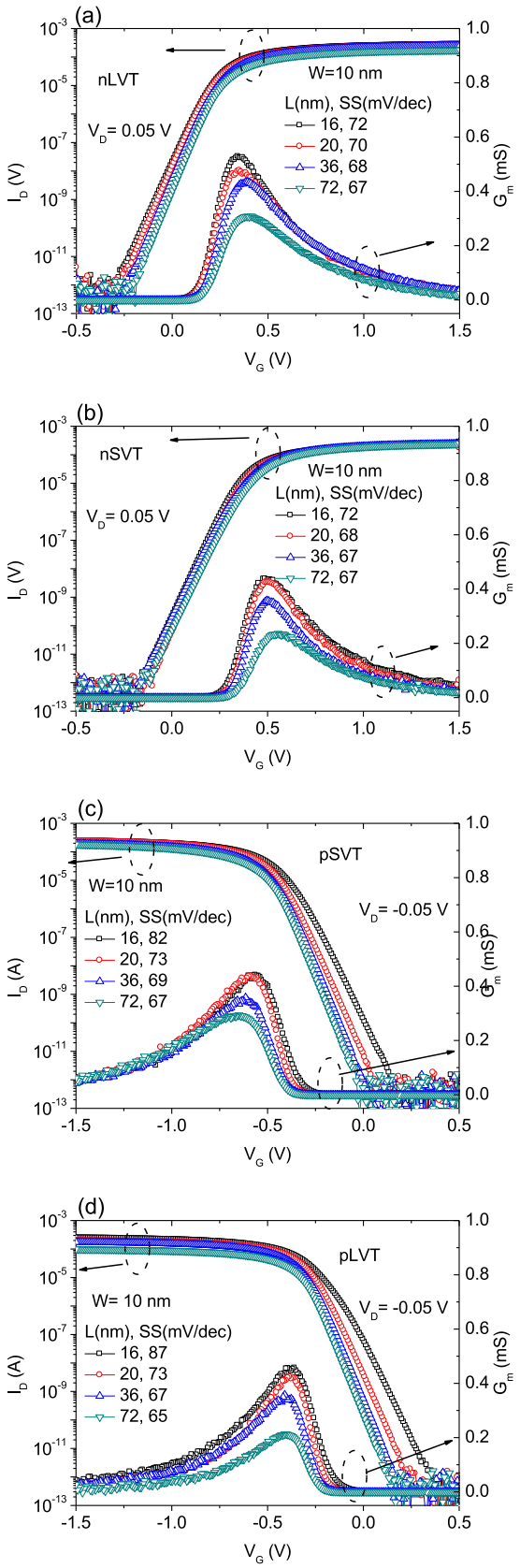

FIGURE 4. Measured I_D-V_G and G_M of (a) nLVT, (b) nSVT, (c) pSVT, and (d) pLVT FinFETs. The fin lengths are 16, 20, 36, and 72 nm. All of the fin widths are 10 nm.

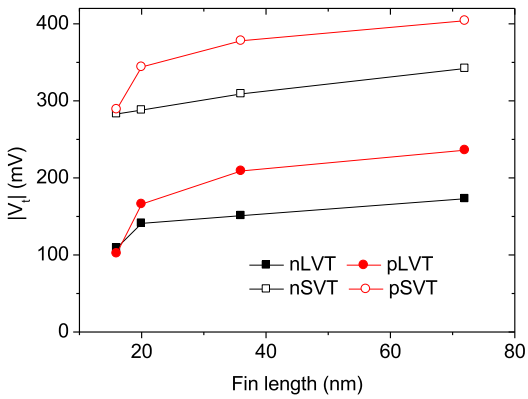

FIGURE 5. Threshold voltages ($|V_t|$) of nLVT, nSVT, pSVT, and pLVT FinFETs for fin lengths of 10, 20, 36, and 72 nm.

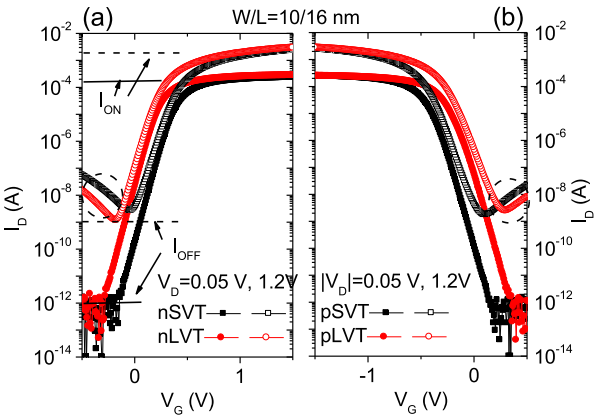

FIGURE 6. I_D-V_G plots of (a) nLVT and nSVT and (b) pSVT and pLVT FinFETs with drain voltage ($|V_D|$) of 0.05 (solid symbols) and 1.2 V (empty symbols).

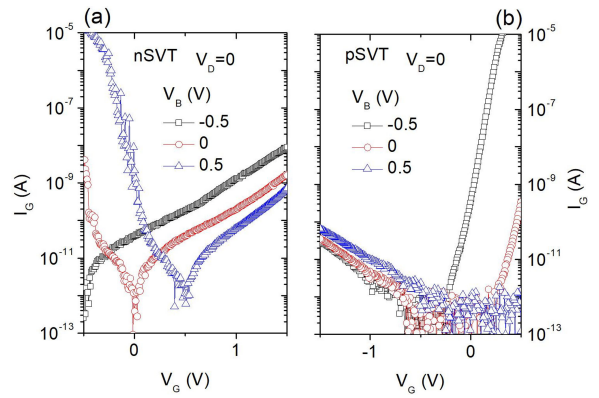

FIGURE 7. I_G-V_G plots of (a) nSVT and (b) pSVT FinFETs with body voltage (V_B) of −0.5, 0, and 0.5 V.

in this case but also a barrier against metal diffusion, such as Al [36]–[38]. However, the metal compounds could diffuse slightly. The element analysis in Fig. 3(c) shows that the signals of the barrier elements (empty marks: N, Ti, and Ta) and nWFM element (Ti and Al) may overlap with dielectrics (solid marks: Hf and O). Perhaps the gate of the p-type MOSFETs contains thicker metal nitride layers, thus presenting lower I_G leakage than the n-type MOSFETs. Figs. 8(a) and 8(b)

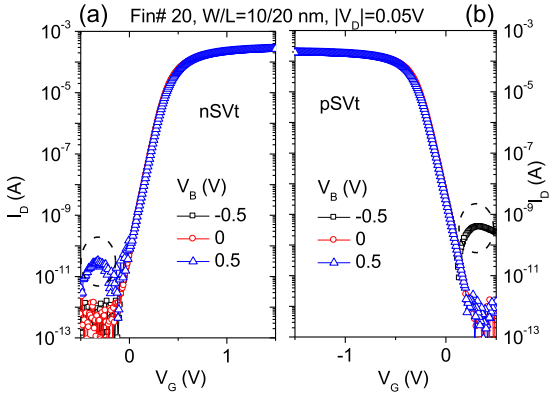

FIGURE 8. I_D-V_G plots of (a) nSVT and (b) pSVT FinFETs with body voltage (V_B) of −0.5, 0, and 0.5 V.

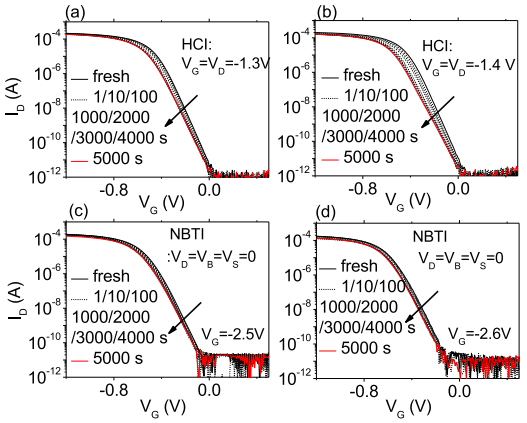

FIGURE 9. I_D-V_G curves of p-type FinFETs at (a) HCI with $V_G = V_D = -1.3$ V, (b) HCI with $V_G = V_D = -1.4$ V, (c) NBTI with $V_G = -2.5$ V, and (d) $V_G = -2.6$ V measured at fresh and stress times of 1, 10, 100, 1000, 2000, 3000, 4000, and 5000 s.

present the I_D-V_G plots of nSVT and pSVT, respectively, at a body bias (V_B) of –0.5, 0 (unbiased), and 0.5 V. The opposite body potential (V_B) against gate voltage (V_G) caused drain leakage after V_G turned the devices off. Notably, the I_D bulge was unlike conventional GIDL. The drain leakage reached the maximum at $|V_G|$ of about 0.33 V. The drain leakage of nLVT and pLVT devices is similar to those in Figs. 8(a) and 8(b)(not shown). This bulge emerged because a vertical electrical field was built in the bulk FinFETs when V_G and V_B had an opposite potential. The induced I_D leakage reached the peak when a maximum local electric field on the channel contributed the highest I_G.

C. HCI AND NBTI ON P-MOSFET

The aging reliability by HCI at $V_G = V_D$ was measured under fresh and stress times of 1, 10, 100, 1000, 2000, 3000, 4000, and 5000 s because the damage is related to logarithmic running time [5], [39]. The I_D-V_G curves of the p-type FinFETs at HCI of −1.3 and −1.4 V are presented in Figs. 9(a) and 9(b), respectively. The shift toward the left indicates an increase in $|V_t|$. S.S. also increased with stress time. The high-stress voltage (−1.4 V) led to a higher shift in S.S. than the low-stress

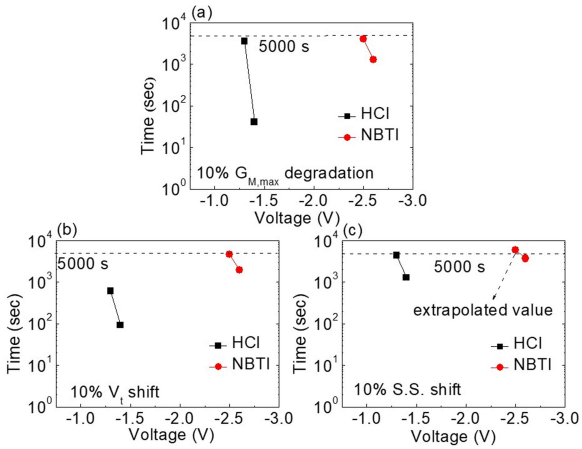

FIGURE 10. Lifetime is obtained from fresh FinFETs to (a) 10% degradation of the maximum values of transconductance ($G_{M,\,max}$), (b) 10% V_t shift, and (c) 10% S.S. shift by NBTI and HCI.

voltage (−1.3 V). The NBTI test also revealed that the gate stress voltages with −2.5 (Fig. 9(c)) and −2.6 V (Fig. 9(d)) represented the increase in $|V_t|$ and S.S., respectively.

We used 10% of the variation in the maximum values of transconductance ($G_{M,\,max}$), V_t shift, and S.S. shift to evaluate the lifetime of the FinFETs by NBTI and HCI, as presented in Figs. 10(a), 10(b), and 10(c), respectively. The negative slopes indicate that the stress time decreased with stress voltage to cause a 10% shift in electrical parameters. Additionally, HCI exhibited a steeper slope than NBTI. These results imply that less time was consumed to generate a 10% shift in $G_{M,\,max}$, V_t, and S.S. by HCI than by NBTI in these ranges. A higher impact and more profound trap generation were created by HCI than by NBTI stress. Every increment of 0.1 V by HCI also generated a more considerable effect than NBTI according to the plots.

IV. CONCLUSION

This study successfully used HK/MG technology and WFM stacks to achieve multi-V_t and n-/p-type FinFETs. The characterization and reliability of the devices satisfy the characteristics of conventional FinFETs. The I_G-V_G curve may differentiate the configuration of the gate stacks. However, further investigation on the gate current leakage mechanism to the gate stacks is required. Moreover, the gate-to-body electrical field exhibits the current leakage in bulk FinFETs in the off state. The results of this investigation show that WFM stack modulation provides platforms to n-/p-type MOSFETs and multi-V_t to achieve high-performance and low-power-consumption integrated circuit design.

ACKNOWLEDGMENT

The authors are grateful to the staff of United Microelectronics Corporation for their informative discussions and MSSCORPS Co., Ltd. for TEM and element analysis. The project is supported under contract number MOST 109-2221-E-390-001.

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